LMR-Patters-history=V1.12_Revision-History

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V1.12 07-25-2019

PTC-ACSES patterns corrected for output levels.

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V1.11 07-03-2019

Added following patterns.

ptc_acses_Base.bin

ptc_acses_Mobile.bin

ptc_acses_Fred.bin

dmr_ms_1031_5_pcnt_ber_cc01_172800_sps.txt

NOTE: The three ptc-acses patterns are single slot transmissions with a blank

(all zero) payload. These can be used to verify Bit Error Rate for receivers.

The Base pattern includes a beacon transmission. The Mobile does not.

ptc_acses_Fred (For Railroad Experimental Data) is a custom pattern that

Users can replace with a specific payload via Anritsu Customer Service

or Marketing, who have the tools to create this custom pattern.

dmr_ms_1031_5_pcnt_ber_cc01_172800_sps.txt is a mobile station transmission

of the 1031Hz pattern with one out of every 20 bits flipped, which creates

an audible distortion to the tone and measures a 5% BER.

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V1.10 04-10-2019

Added following pattern.

  dPMR_O.153.txt

NOTE This is a copy of the "nxdn_pn9_4800_172800_sps.txt" pattern that

already exists for NXDN. Support for this dPMR pattern was added in V3.10,

but due to miscommunication, the firmware wanted this filename, rather than

the dPMR filename. Rather than change the firmware, it's easier to add the

pattern to the USB drive. It will only affect dPMR option pattern loading.

NOTE V3.10 or later firmware is required to recognize dPMR_O.153.txt

NOTE While the pn9 sequence pattern works for both NXDN and dPMR, the 1031 Hz

pattern for NXDN will not work for dPMR, because these radios use different

voice codecs, so the same bit sequence does not result in the same audio

from the two radios.

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V1.09 01-04-2018

Added following pattern.

TETRA_T1_TCH_7p2_01_0000_00000_60.bin

NOTE: This is a 60-second pattern to support the Hytera vendor of Base Stations

for Base Station Receiver Sensitivity tests. This pattern has the same LMR Master

Systerm requirements as the other .bin patterns: 2 GB Sig Gen memory,

Sig gen version >= 1.05, DSP FPGA Ver >= 1.30, CPU FPGA Ver >= 2.28

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V1.08 04-07-2016

Added following patterns.

TETRA_T1_TCH_7p2_00_0000_00000_60.bin

TETRA_T1_TCH_7p2_01_0000_00000_01.bin

TETRA_T1_TCH_7p2_01_0310_00100_01.bin

TETRA_T1_TCH_7p2_07_0159_13787_60.bin

TETRA_T1_TCH_7p2_63_1023_16383_60.bin

NOTE: Above are Tetra - BS Sensitivity test patterns which need larger memory on S412E.

System requirment for above Tx patterns to be loaded involves 2 GB Sig Gen memory,

Sig gen version >= 1.05, DSP FPGA Ver >= 1.30, CPU FPGA Ver >= 2.28

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V1.07 02-24-2016

Added following patterns.

dmr_bs_1031_idle_cc00_172800_sps.txt

dmr_bs_1031_idle_cc02_172800_sps.txt

dmr_bs_1031_idle_cc03_172800_sps.txt

dmr_bs_1031_idle_cc04_172800_sps.txt

dmr_bs_1031_idle_cc05_172800_sps.txt

dmr_bs_1031_idle_cc06_172800_sps.txt

dmr_bs_1031_idle_cc07_172800_sps.txt

dmr_bs_1031_idle_cc08_172800_sps.txt

dmr_bs_1031_idle_cc09_172800_sps.txt

dmr_bs_1031_idle_cc10_172800_sps.txt

dmr_bs_1031_idle_cc11_172800_sps.txt

dmr_bs_1031_idle_cc12_172800_sps.txt

dmr_bs_1031_idle_cc13_172800_sps.txt

dmr_bs_1031_idle_cc14_172800_sps.txt

dmr_bs_1031_idle_cc15_172800_sps.txt

modified following pattern

dmr_bs_1031_idle_cc01_172800_sps.txt

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V1.06 3-6-2015

Added nxdn 1031 cal pattern with 5% BER for nxdn.

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V1.05 6-17-2014

Added LSM patterns for P25.

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V1.04 1-7-2014

Added TETRA patterns.

Added PTC PN9 patterns.

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V1.03 8-14-2012

Added P25p2 patterns.

Added 2 NXDN pn9 framed patterns.

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V1.02 10-31-2011

Added 4 NXDN DTS patterns.

Used in LMR Master S412E

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V1.01 10-12-2011

Added PTC patterns and DMR "ms_cmove" patterns.

Updated DMR "ms_1031" patterns.

Updated matlab scripts.

Used in LMR Master S412E

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V1.00 6-8-2011

Initial Release: Patterns for P25, NXDN, DMR

and Matlab Scripts for creating patterns

Used in LMR Master S412E

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