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TECHNICAL NOTE

Latest Information on Standardization of ITU-T Jitter Measuring Instruments Q5/SG4 Expert Meeting Report

ANRITSU CORPORATION

MBP-1SG040171-00

Latest Information on Standardization of ITU-T Jitter Measuring Instruments Q5/SG4 Expert Meeting Report

October 2004

Anritsu Corporation
IP Network Division

Good Morning (Afternoon). Today I would like to present my report on the ITU-T SG4/Q5 Expert Working Group held from September 27 to 30 this year.

Outline of ITU-T Q5/SG4 Expert Meeting Results (1/2)

Summary

The results of the Expert Meeting (2004.09.27–30) are summarized below:

(a) Revised draft O.172 (WD22)
(b) Confidential report to NPL (WD23)
(c) Review of Subjects (WD24)

Several items are still remaining in Appendices VII and VIII of Draft O.172 (Oct. 2004) but progress with obtaining consent at the next ITU-T general meeting (March 2005) is well in hand.

Working Group Reference : ITU-T members can obtain the full documentation from the following URL

http://ties.itu.int/u/tsg4/sg4/rapporteur-meetings/2004-09-South Queensferry/

The ITU-T SG4/Q5 Expert Meeting was held at Queensferry in Scotland. The results of the Group are summarized in the three items shown here. Item (a) indicates that the revised draft of O.172 reflecting the results of this review was changed to document number WD22. The main change is to the contents of the residual jitter verification methods in Appendix VII and Appendix VIII resulting from the May 2004 meeting. I will explain the details later. Item (b) deals with the writing of a confidential report (on remaining themes) to the National Physical Laboratory (NPL), which participated in the discussions as a third-party calibration organization, about jitter tester verification methods in Appendix VII and Appendix VIII. Item (c) deals with a review of items (Living List) that remain as investigation themes for the Expert Meeting. As a result of this meeting, the main themes were analyzed and it was decided to seek consent for Draft O.172 at the next general meeting of ITU-T expected to be held in March 2005. The reference materials used by the Expert Working Group can be downloaded using FTTP from this URL by people with a TIES account.

Outline of ITU-T Q5/SG4 Expert Meeting Results (2/2)

- **Main Discussion Themes**

(1) Review of Optical Standard Level

Review of optical standard level for residual jitter verification

(2) Review of Receiver Measurement Error (W)

Review of receiver error (STM-16, STM-64) and definition of STM-256 values

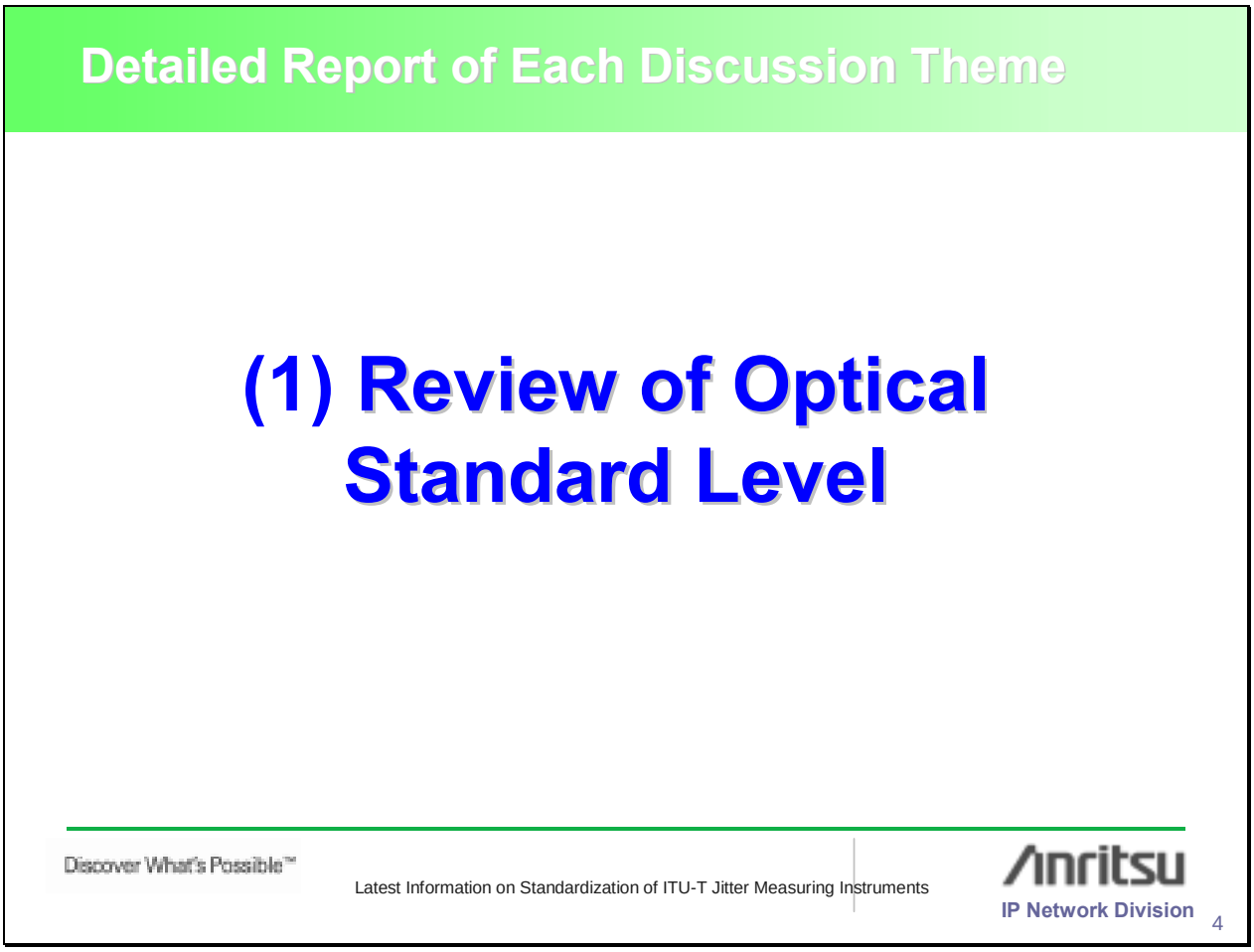
(3) Review of Appendix VII

Review of Appendix VII measurement method error verification and block diagram of method for eliminating pattern jitter

(4) Review of Appendix VIII

Examination of standards and measurement filters for Appendix VIII edge insertion method and edge insertion algorithm error verification themes decided at previous meeting

These four main themes were discussed at this meeting. Point 1 deals with a review of the optical standard level. Currently, the input level range for specifying jitter tester error is -10 to -12 dBm, but there was a proposal about the need to review each bit rate to match the Launch Power of the G-series. This was discussed. Point 2 deals with a review of the jitter tester receiver measurement error (W). The discussion covered updating of the currently specified values for STM-16 and 64 as well as specification of a value for STM-256. The proposal for STM-256 came from Anritsu. Based on this proposal, review of receiver error was discussed. Point 3 deals with review of the jitter tester verification methods described in Appendix VII and examined the error of the measurement methods. In addition, company A holds a patent on the pattern jitter remover block so there is an urgent need to find another block that can be used without payment of patent license fees. This meeting was able to come up with another simple block diagram so Anritsu proposed its use instead of the patented block. Point 4 deals with review of the other jitter tester verification method in Appendix VIII. There were three main items. First was re-examination of the edge insertion method as a subject for the May 2005 meeting. Second was examination of the standard method for clarifying the edge insertion method algorithm error. Third was examination of the specifications for the filter band when measuring the DUT signal using an oscilloscope. I am going to explain these items in more detail later.



First, I will explain the review of the optical standard level which was the first of the main discussion themes.

Detailed Report of Each Discussion Theme
(1) Review of Optical Standard Level

Introduction

O.172 specifies input of a signal with a level range from -10 to -12 dBm as the standard level for verifying tester error. This time, the situation was left unchanged for STM-16 and higher equipment minimum output power but it was agreed that a review should be held for compatibility with G-series Output Power specifications.

Discussion Result

The current specifications (-10 to -12 dBm) will be left unchanged but a note will be added saying, “It is also permissible to use a standard level that is compatible with the G-series Output Power.”

Currently, the optical input level specification for jitter tester error is -10 to -12 dBm. However, for standards higher than STM-16, since the minimum Output Power specified for the G-series is higher than this range, it is necessary to match the level with an external attenuator. This time, there was a proposal about the need to specify a range from the G-series Output Power to -12 dBm, so as to be able to get rid of the need for an external attenuator. As a result of discussion, since it would be impossible to come up with a specification covering the entire Output Power, it was decided that the standard would remain at the current level of -10 to -12 dBm. However, a note was added allowing use of a standard matching the G-series Output Power.

Detailed Report of Each Discussion Theme
(1) Review of Optical Standard Level

- **Reference: G.693 (December 2003)**

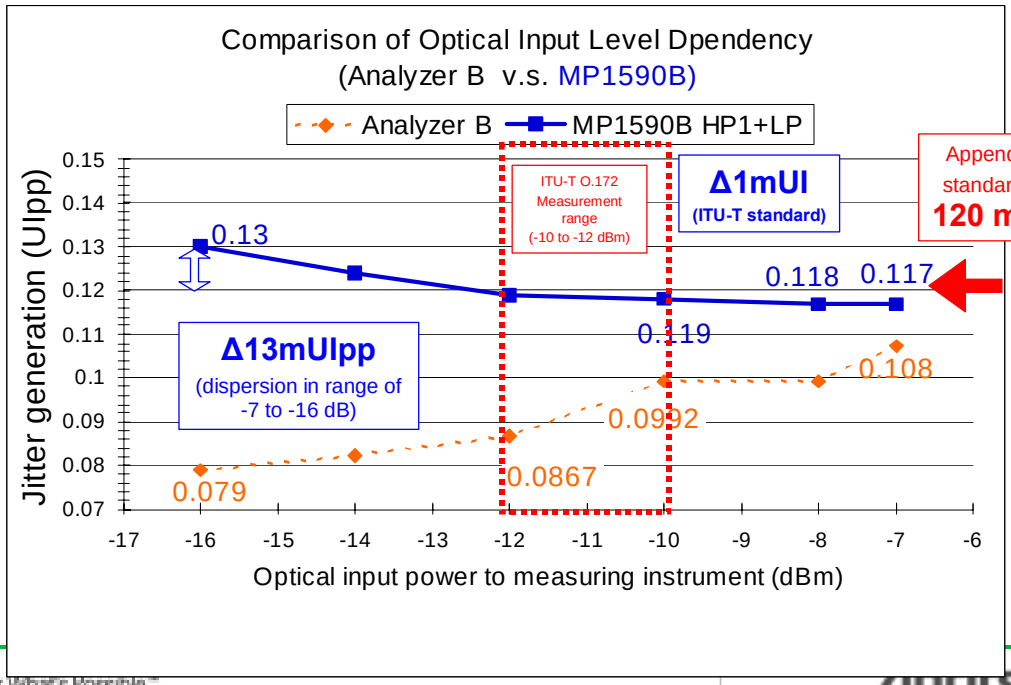
Table 4/G.693 – Optical interface parameters specified for applications with 2 km target distance

Application code	Unit	VSR2000-2R1	VSR2000-2L2 VSR2000-2L3 VSR2000-2L5	VSR2000-3R1[e)]	VSR2000-3R2[e)] VSR2000-3R3[e)] VSR2000-3R5[e)]	VSR2000-3M1	VSR2000-3M2 VSR2000-3M3 VSR2000-3M5	VSR2000-3H2 VSR2000-3H3 VSR2000-3H5
G.691 Application code		I-64.1	I-64.2r - -					
G.959.1 Application code		P1I1-2D1	P1I1-2D2r					
Target distance	km	2	2	2	2	2	2	2
Bit rate/line coding of optical signals	–	NRZ 10G	NRZ 10G	NRZ 40G	NRZ 40G	NRZ 40G	NRZ 40G	NRZ 40G
Fibre type	–	G.652	G.652 G.653 G.655	G.652	G.652 G.653 G.655	G.652	G.652 G.653 G.655	G.652 G.653 G.655
Transmitter at reference point MPI-S								
Source type		SLM	SLM	SLM	SLM	SLM	SLM	SLM
Operating wavelength range	nm	1290-1330	1530-1565	1290-1330	1530-1565	1290-1330	1530-1565	1530-1565
Maximum mean output power	dBm	–1	–1	+3	+3	+10	+3	+3
Minimum mean output power	dBm	–6	–5	0	0	+8	0	0
Receiver at reference point MPI-R								
Minimum sensitivity (BER of 1×10^{-12})	dBm	–11	–13	–5	–5	–5	–13	–17
Minimum overload	dBm	–1	–1	+3	+3	+2	0	0

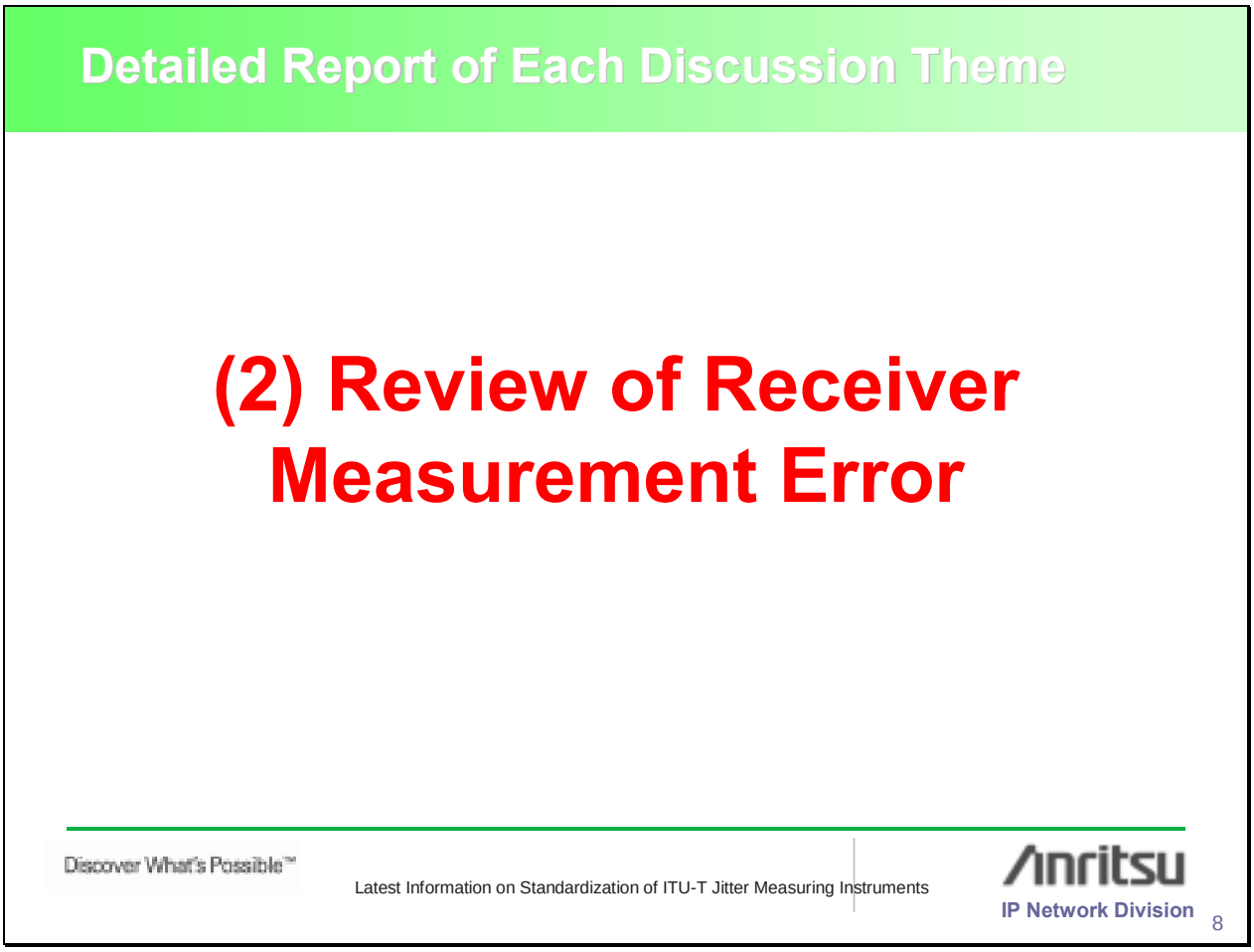
For reference, the circled parts in this slide show the specifications for STM-64 and STM-256 taken from the specifications for G.693 Optical interfaces for intra-office systems. In G.693, the maximum Output Power is specified as -1 dBm for VSR2000-2R1 applications. In these applications, due to this revision, it is possible to choose the error specification point in the range of -1 to -12 dBm. In the case of STM-256, since the maximum Output Power is +10 dBm, with applications other than VSR2000-3M1, it is possible to choose an error specification point in the +10 to -12 dBm range.

Detailed Report of Each Discussion Theme
(1) Review of Optical Standard Level

Comparison of optical input level dependency (STM-64/OC-192)



The data in this slide shows a comparison of the input level dependency of jitter measurement values when the level of a standard signal source with 120 mUIpp of jitter is varied, measured using the MP1590B and another maker's tester. The blue line shows the input level dependency of the jitter measurement with the MP1590B for STM-64/OC-192. Anritsu's MP1590 shows almost no change in the error even for standard levels of -10 dBm or more in line with the Note added this time. However, in the case of the other maker, although error can be suppressed in the range between -8 and -10 dBm, the error becomes very large outside this range. In addition, the appearance of a smaller than usual absolute value is a different phenomenon to level dependency.

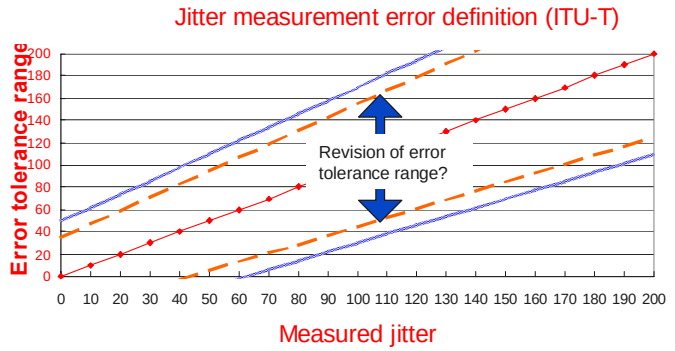


Next, I want to explain the details of the jitter tester receiver measurement error (W) in the second main discussion theme.

Detailed Report of Each Discussion Theme
(2) Review of Receiver Measurement Error

Introduction

O.172 defines receiver total measurement error with two parameters (R and W) as shown below. When performing jitter verification (especially jitter generation measurement) defined for the G-series, there have been requests for smaller jitter tester error. The two jitter tester verification methods described in Appendix VII and Appendix VIII have nearly been ratified so the strongly requested W value for STM-16 and STM-64 was re-examined. In addition, STM-256 equipment is starting to be appear in general use so there is an urgent need to standardize the definitions of the STM-256 R and W values which is now FFS.



O.172 Jitter Tester Receiver Error Definition

±R% of reading ± W UIpp

O.172 specifies two parameters - W and R - for the jitter tester total measurement error. The total error tolerance range is composed of the percentage error R% of the expected value and fixed error of W UIpp. In other words, as shown in this table, when the value on the horizontal axis is the true value, in the current O.172, the range between the blue lines is specified as the error tolerance range. In other words, since the percentage error R% ratio gets larger as the true value gets larger, the tolerance range gets wider. The Appendix VII and Appendix VIII jitter tester verification methods have almost been established at this meeting and there was a proposal that we should review the values for STM-16 and STM-64 to achieve the dotted orange line. In addition, since there are no error specifications for STM-256 transmission equipment already on the market, Anritsu proposed values for the STM-256 standard.

Detailed Report of Each Discussion Theme
(2) Review of Receiver Measurement Error

Discussion Results

As a result, it was decided to hold over any changes to the STM-16 and STM-64 residual jitter value until the next meeting because a member was opposed to the revision. However, for STM-256 and the Anritsu proposal, it was agreed to proceed with incorporation of the same value as the current STM-64 value as the next step in the standard verification.

As a result of the discussions, since a member was opposed to the revisions, it was decided to hold off on any review of STM-16 and STM-64 until the next general meeting in March 2005. In the interval until the next meeting, an effort will be made to persuade opposed members about the merit of the revision. However, with respect to STM-256, as a result of the Anritsu proposal, the STM-64 value was specified as the starting value. Moreover, similar to the STM-64 situation, it was agreed to add a note describing the target of reducing STM-256 error.

Detailed Report of Each Discussion Theme
(2) Review of Receiver Measurement Error

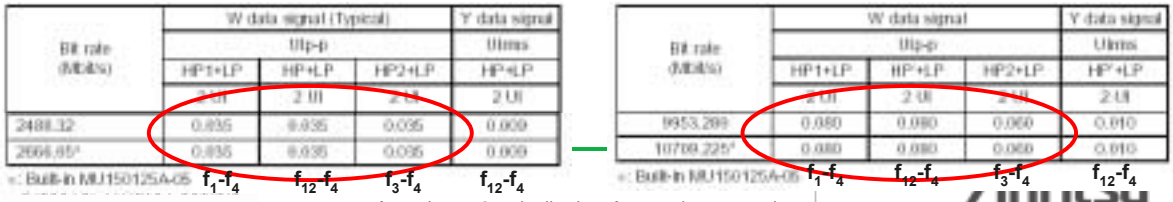
MP1590B Specification (Reference)

The MP1590A/B has been available as a commercial product since October 2003 and the revisions about accuracy proposed this time have been incorporated in the catalog (0.035 UIpp with HP1+LP). In addition, the following measurement accuracy of better than ±20m UIpp has been achieved using the High precision Jitter Analysis (Option 30).

Revised Contents Proposed This Time

Signal	Maximum peak-to-peak jitter error (UIpp) for given digital signals					
	Structured signal			Clock signal		
	f_1-f_4	f_{12}-f_4	f_3-f_4	f_1-f_4	f_{12}-f_4	f_3-f_4
STM-16	0.1	~~0.05~~0.035	~~0.05~~0.035	0.05	0.03	0.03
STM-64	~~0.15~~0.1	–	~~0.05~~0.035	0.05	–	0.03
STM-256	~~FFS~~0.150	–	~~FFS~~0.05	~~FFS~~0.05	–	~~FFS~~0.05

MP1590A/B Specifications (from Datasheet)



Latest Information on Standardization of ITU-T Jitter Measuring Instruments

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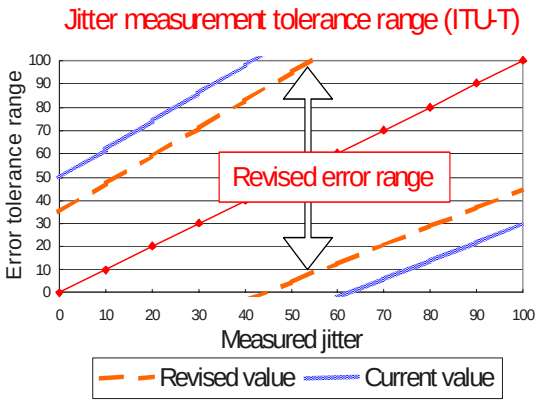
Following the launch of the Anritsu MP1590 in October 2003, the accuracy specification in the catalog for the standard unit has been revised in line with the measurement error revisions proposed at this meeting. When Option 30 (High Precision Jitter Analysis) is installed, it is possible to achieve a measurement accuracy of ±20 mUIpp with lower error. The middle part of this screen shows the revised values proposed at this meeting. For STM-16 and STM-64, we proposed revising the error tolerance from 50 mUIpp to 35 mUIpp at filter conditions f_3-f_4 (1M to 20M: STM-16; 4M to 80M: STM-64). In addition, the f_{12}-f_4 filter is the specification for the filter (12k to 20M : OC-48) in the Telcordia standard (GR-253). As a result, it was proposed to revise the 50 mUIpp error tolerance to 35 mUIpp. Furthermore, there was a proposal to revise the 150 mUIpp tolerance at f_1-f_4 (20k to 80MHz) in STM-64 to 100 mUIpp. With respect to STM-256, since we have yet to establish a verification method that takes sufficient account of the current verification method error, we are using the same error as the current STM-64 standard for the starting value. In the future, it was agreed to add a note about using the same target error value of 35 mUIpp (f_2-f_4 :16M to 320M) as the STM-64 standard. The values in the bottom tables are the values taken from the MP1590 catalog but they are all 35 mUIpp at both 2.5G and 10G under all filter conditions and there will be no impact even if the standard changes next year.

Detailed Report of Each Discussion Theme
(2) Review of Receiver Measurement Error

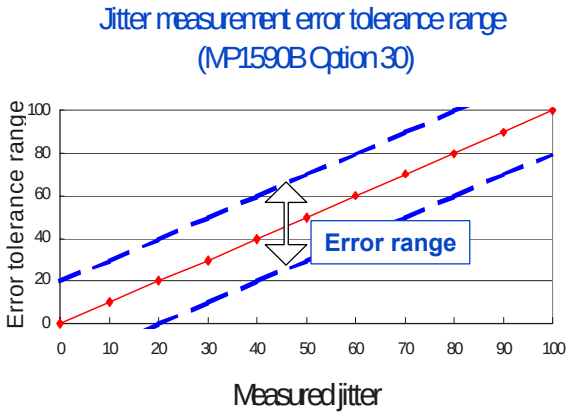
MP1590B Option30 Specification (Reference)

The following graphs compare the jitter error tolerance range for the ITU-T specification and Anritsu's Option 30

O.172 Error Specification



MP1590B Option 30 Values



This slide shows a comparison of the O.172 error tolerance range proposed at this meeting and the MP1590 (with Option 30). The blue lines in the graph on the left show the current O.172 error tolerance range and the red dotted lines show the value for the current revision. These error tolerance ranges are composed of a combination of the two parameters R% and W UIpp mentioned previously. As a result, the error tolerance range gets wider as the true value becomes larger (moving to the right). By contrast, the MP1590 Option 30 measurement error of ±20mUIpp including R% and W UIpp is guaranteed at values below 100 mUIpp. This makes it possible to achieve the traceability of Appendix VIII.

(3) Review of Appendix VII

Next, I will explain the review of Appendix VII (one jitter verification method) in the third main discussion theme.

Detailed Report of Each Discussion Theme
(3) Review of Appendix VII

Introduction

The following themes regarding the Appendix VII jitter tester evaluation methods were discussed.

(1) No method for verifying jitter at final output

- No proposal at this meeting and no discussion

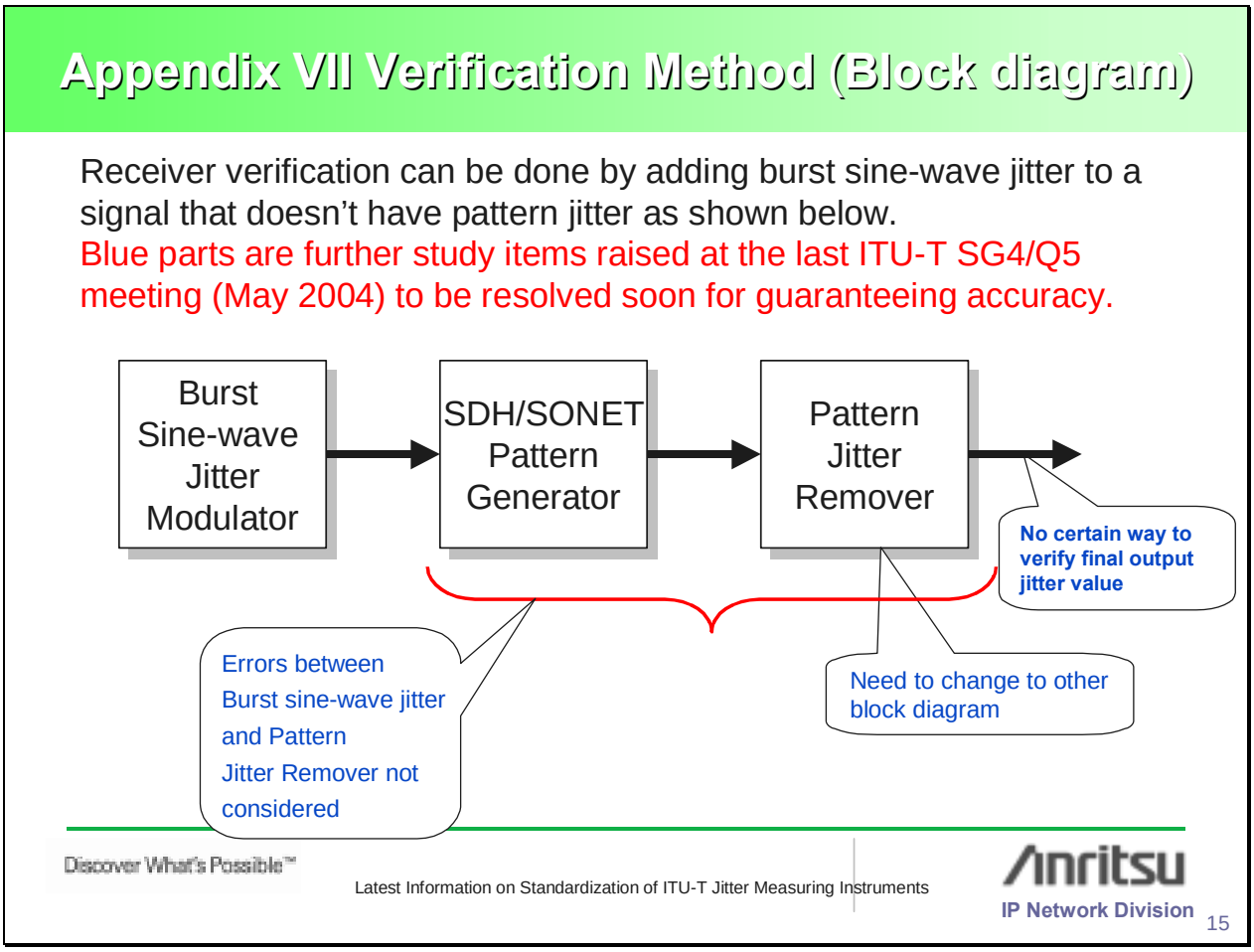
(2) Measurement error verification and evaluation pattern verification

- As current themes, since it is impossible to achieve an ideal signal generator (zero pattern jitter), the jitter amount with added burst sine-wave jitter changes according to the timing.
- Clarify types of evaluation pattern that are able to verify error

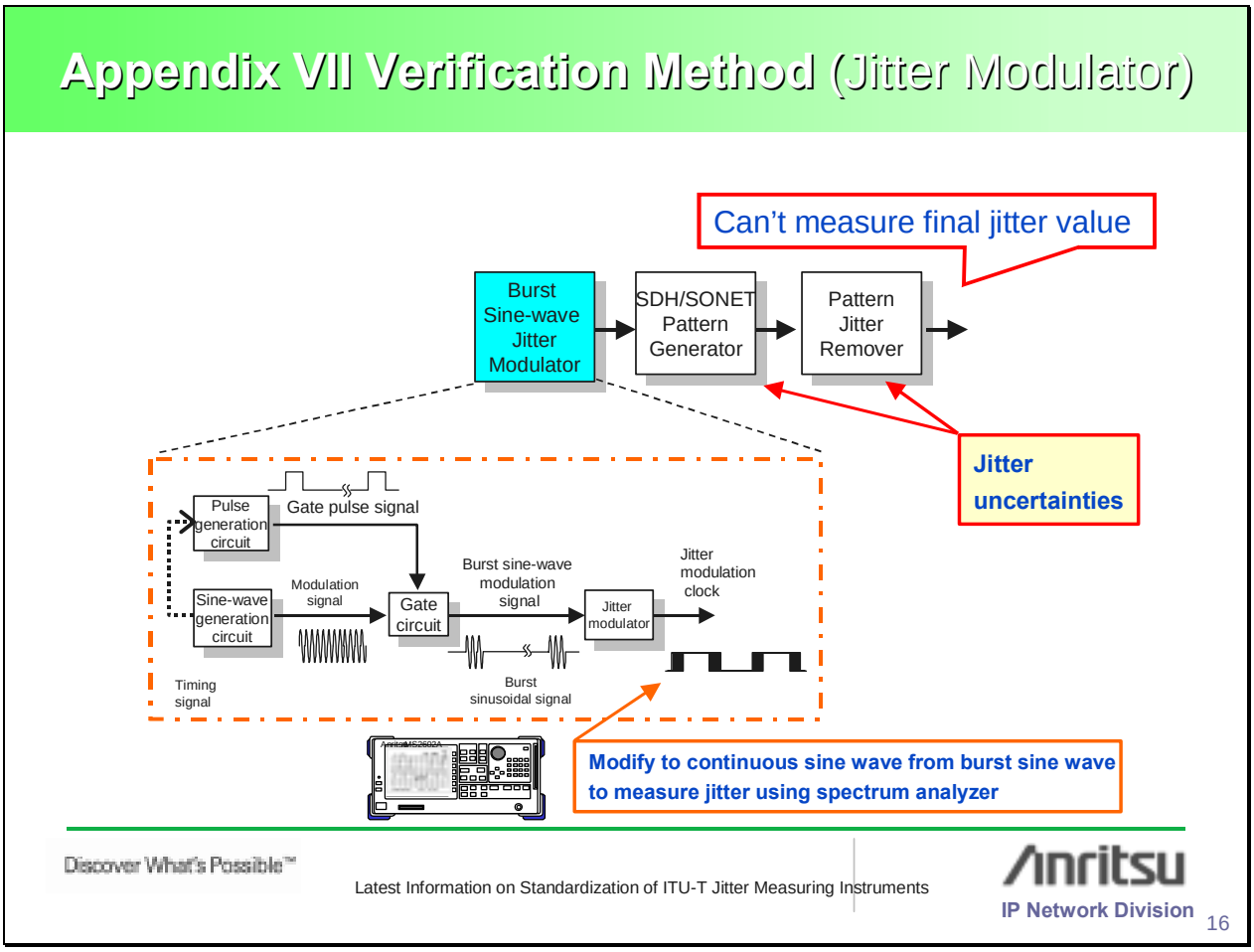
(3) Review of block diagram of circuit for eliminating pattern jitter

- Replace with simple block diagram that can achieve 10 mUIpp using the Appendix VIII verification method.

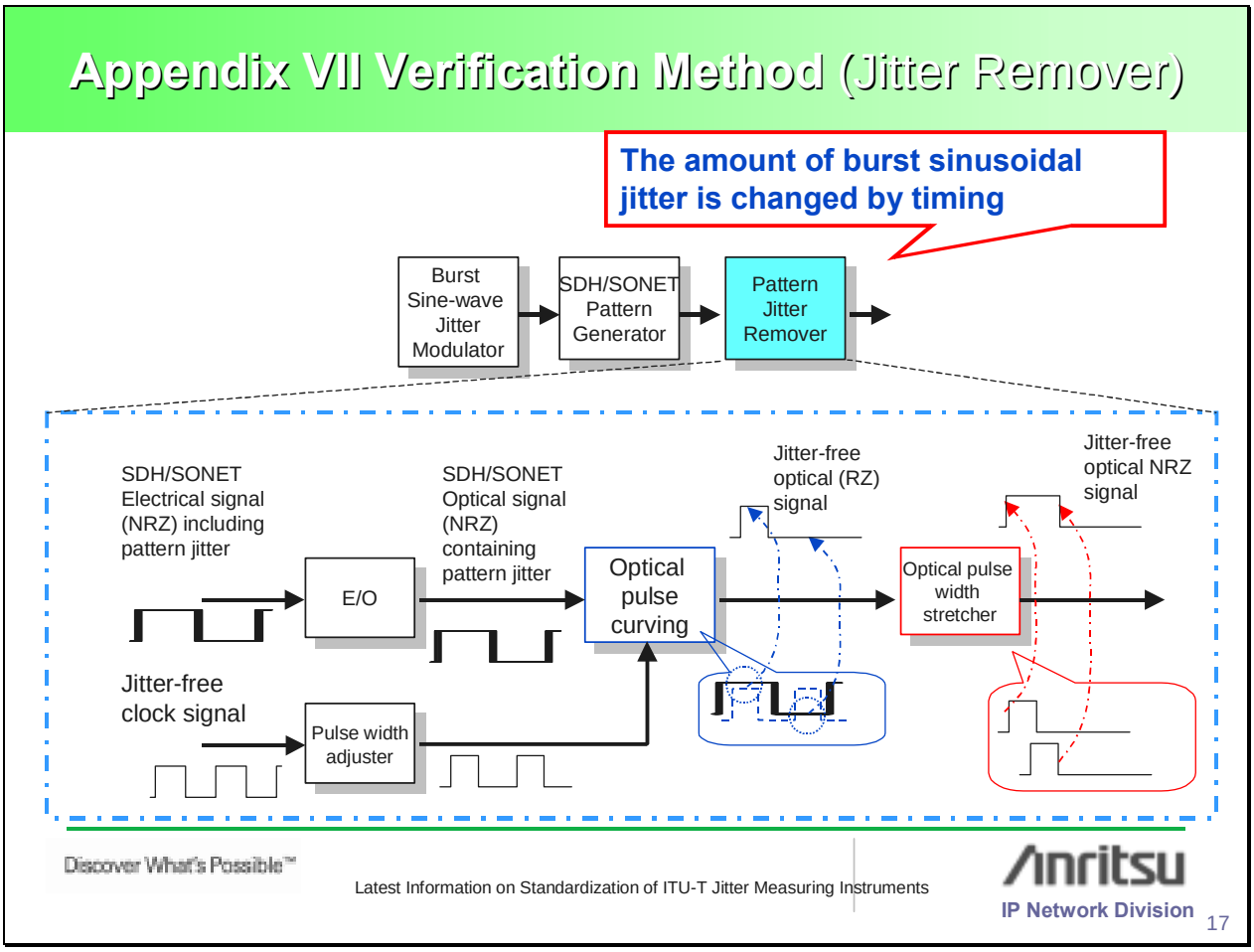
These three points concerning Appendix VII were discussed at this meeting as subjects raised at the ITU-T meeting in May 2004. With respect to Point 1, since there is no method for verifying the jitter of the final output of the signal source in Appendix VII, currently only the jitter of the clock level can be investigated. As a result, there is a need for a verification method (procedure) for the final output jitter. However, there was no discussion at this meeting on this theme because there was no proposal. With respect to point 2, there was discussion about measurement error. Appendix VII describes a method for adding burst sine-wave jitter to a signal from which jitter has been removed and measuring this burst jitter. However, since it is not possible to achieve an ideal data generator containing no pattern jitter, error of less than 10 mUIpp is permissible in O.172. When the burst sine-wave jitter is added, the maximum jitter of 10 mUIpp may fluctuate as a result of the pattern jitter and generation timing. This error was discussed at this meeting. In addition, there was also discussion about SDH/SONET patterns that can guarantee the jitter accuracy of Appendix VII. With respect to point 3, the pattern jitter remover block diagram was reviewed because company A holds a patent on the present block diagram. Currently, since we have been unable to confirm that the block can be used free of license payments to company A, there is a problem for all users of this verification method. At this meeting, Anritsu reported on a simple block diagram that can achieve the same performance and there was discussion about reviewing the block diagram.



To make the Appendix VII method a practical proposition, it is necessary to produce a reference signal using the three blocks shown here. The block on the left is a jitter modulator that can add jitter of about 100 mUIpp as a burst sinusoidal signal generated at a clock of 9.95328 GHz. The middle block generates an STM-64 (9.95328 Gbit/s) frame signal at a clock of 9.95328 GHz. To obtain the SDH frame signal frame synchronization, a Non Scramble Byte (A1, A2, J0/Z0) is defines at SOH 1ROW. Pattern jitter occurs at this point. In addition, jitter also occurs at the Payload. When a data signal including these jitters is evaluated by the receiver of a jitter tester, accurate jitter evaluation is impossible due to the presence of these jitters. As a consequence, the pattern jitter at the final block shown on the right is used to remove jitter generated in the SDH/SONET pattern, reducing errors due to pattern jitter. In this method, since there is no certain way to evaluate the amount of jitter added by the jitter modulated in the final output stage (output of pattern jitter remover), it is not possible to accurately determine the amount of jitter in the evaluation signal. Moreover, since company A has a patent on the block diagram for the pattern jitter remover described in the references, it is necessary to revise the block diagram to a different form so that all users can use the technology free-of-charge without patent licensing issues.



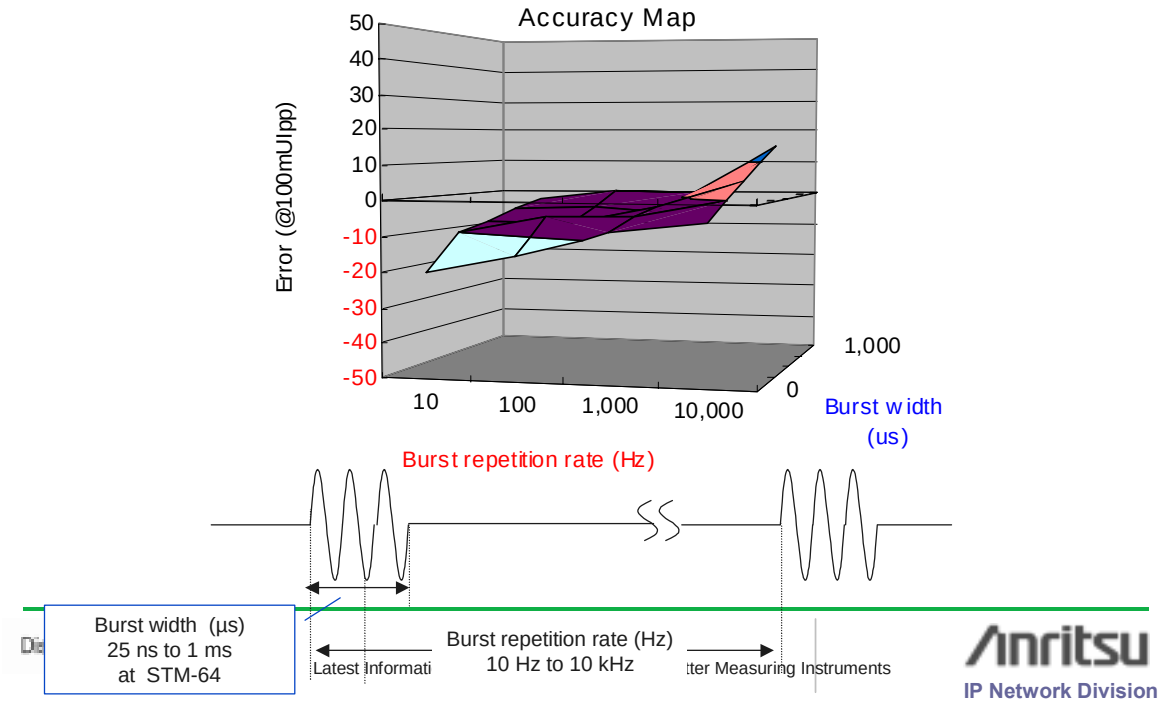
The Appendix VII method performs receiver evaluation with a signal to which jitter is added as a burst sinusoidal wave. However, it is not a method that permits accurate evaluation in the final-stage signal. The Appendix VII method is a method for evaluating whether or not it is possible to detect a fixed peak jitter amount (100 mUIpp) while changing the modulation signal burst repetition rate and burst width. However, Appendix VII provides a method for confirming the amount of added jitter by using a clock signal to which jitter has been added as a continuous sine wave (jitter modulator output) instead of a burst sine wave. In this case, the amount of jitter is found using a spectrum analyzer. In other words, it is possible the perform calibration of the jitter value with a modulation signal having different frequency components from the finally used modulation signal (burst sine wave), based on the supposition that it is the same as the peak jitter value. Moreover, since a signal with a known jitter value is passed through the pattern generator and pattern jitter remover, it is not necessary to take changes in jitter due to these blocks into consideration.



Since company A has a patent on this block diagram for the pattern jitter remover described in this slide, it is necessary to revise the block diagram to a different form so that all users can use the technology free-of-charge without patent licensing issues. The Appendix VII method requires a pattern jitter remover to remove pattern jitter of less than 10 mUIpp (1 ps at 10 G) that is a source of error. However, since it is not possible to achieve an ideal data generator containing no pattern jitter, error of less than 10 mUIpp is permissible in O.172. When the burst sine-wave jitter is added, the maximum jitter of 10 mUIpp may fluctuate as a result of the pattern jitter and generation timing.

Appendix VII Accuracy Map

The Appendix VII accuracy map is used to evaluate the burst sinusoidal modulation signal defined below.



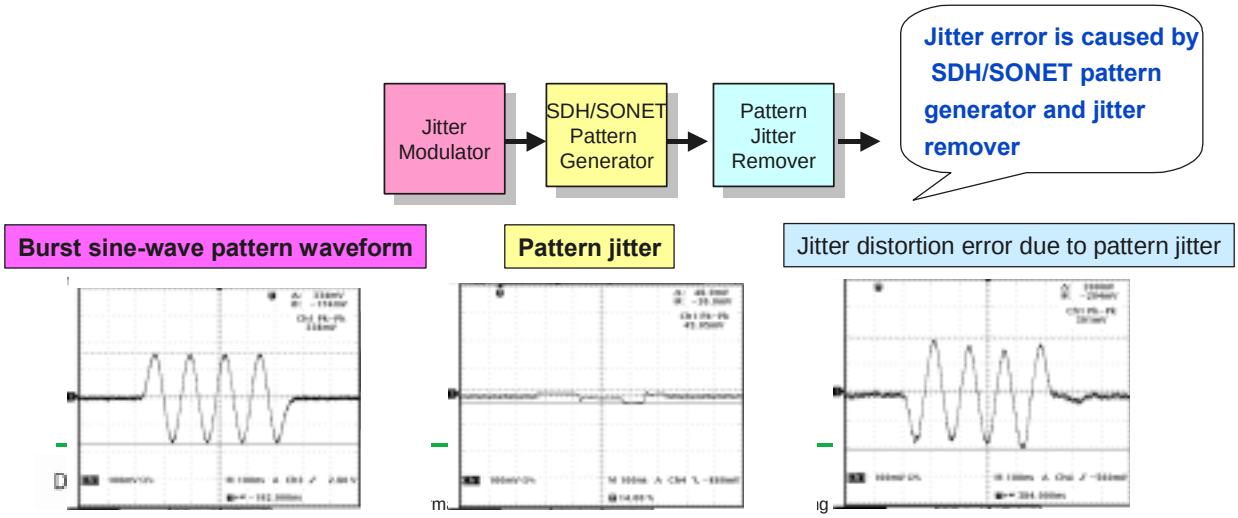
The Appendix VII method does offer a method for confirming whether or not a fixed peak jitter (100 mUIpp) can be detected at the receiver while varying the modulation signal burst repetition rate and burst width using the matrix shown here. However, this accuracy map evaluation has no meaning when it is not possible to confirm that the amount of jitter generated at the send side under any conditions is constant (100 mUIpp) at the final output.

Detailed Report of Each Discussion Theme
(3) Review of Appendix VII

Discussion Results (1/3)

(2) Measurement Error Verification and Evaluation Pattern Verification

In the Appendix VII verification method, as explained above, there is error due to the pattern jitter and superimposed timing; actual verification methods are a subject of future evaluation.



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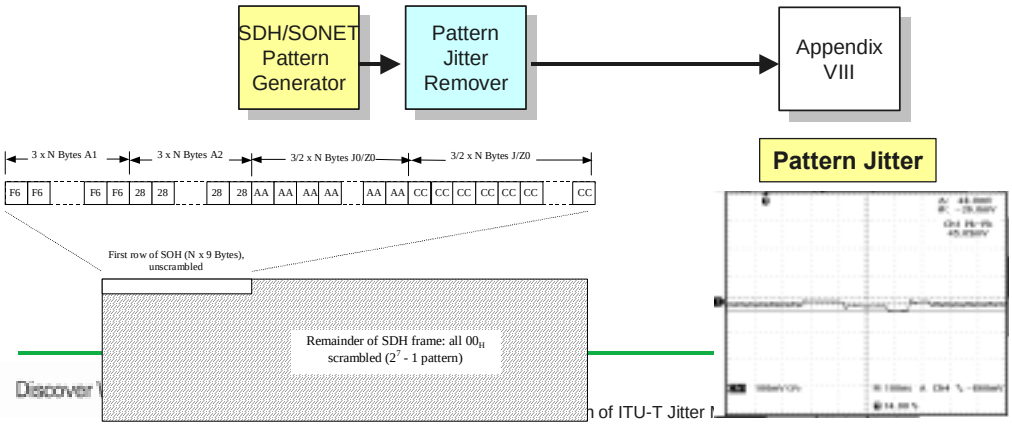
This slide covers the discussion of the first discussion item with respect to the variation in the burst sine-wave jitter cause by the residual pattern jitter. As already clarified above, there are continuing discussions on actual future verification methods. These three waveforms show how the jitter changes with an added burst sine wave. The graph on the left shows the modulation waveform when jitter is added to the clock by a burst sine wave. The middle graph shows the waveform when the pattern jitter is not completely removed by the pattern jitter remover and the right graph shows the signal with modulation-like distortion when the incompletely removed pattern jitter is superimposed periodically.

Detailed Report of Each Discussion Theme
(3) Review of Appendix VII

Discussion Results (2/3)

(2) Measurement Error Verification and Evaluation Pattern Verification

The pattern that can verify jitter specified in Appendix VII and the limits on the diagnostic pattern defined for use in Appendix VIII were explained.



This slide covers the evaluation pattern discussed in item 2. Appendix VII describes various possible evaluation patterns but it is necessary to use the verification method of Appendix VIII as a method to evaluate the pattern jitter remover characteristics. Since the Appendix VII method emphasizes Non Scramble jitter, evaluation is performed using a special diagnostic pattern. The diagnostic pattern is defined so as to set the ALL0+PRBS 7 Scramble pattern in the Scramble part. At the current time, the evaluation in Appendix VIII can only use this diagnostic pattern due to problems with measurement time and accuracy. Consequently, when evaluating jitter accuracy using Appendix VII, we added a note describing precautions about only using the diagnostic pattern defined in Appendix VIII.

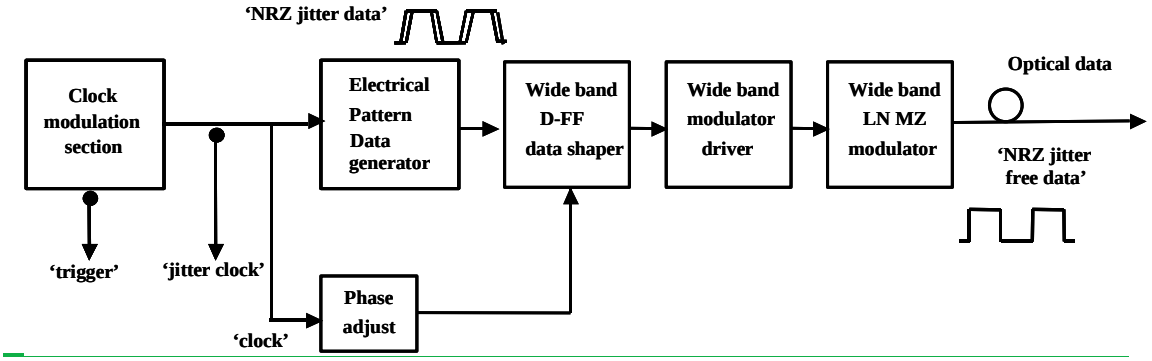
Detailed Report of Each Discussion Theme
(3) Review of Appendix VII

Discussion Results (3/3)

(3) Review of Block Diagram of Circuit for Removing Pattern Jitter

It was confirmed that the simple block proposed by Anritsu could achieve low pattern jitter so the following new block diagram was added.

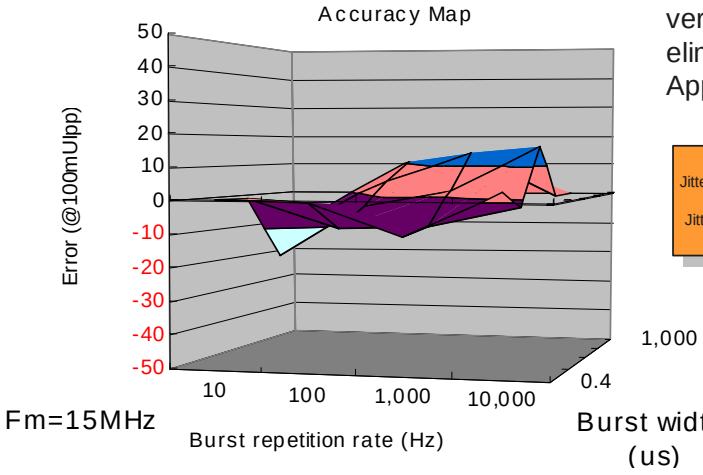
Figure VII.4 – Alternative Optical Data Generation Block Diagram



This slide covers the review of the circuit block diagram for removing pattern jitter as the third discussion theme. In addition to the current block diagram, the block diagram above proposed by Anritsu was added. To deal with the issue of the patent held by company A, company A and ITU-T will continue negotiations until the March 2005 meeting.

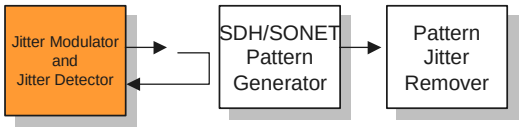
MP1590B Accuracy Map (Typical)

The MP1590B accuracy map was determined according to the standard method described in Draft ITU-T O.172 (September 2004).
The values for burst width and burst repetition rate are values specified in ITU-T O.172 Table VII.1.

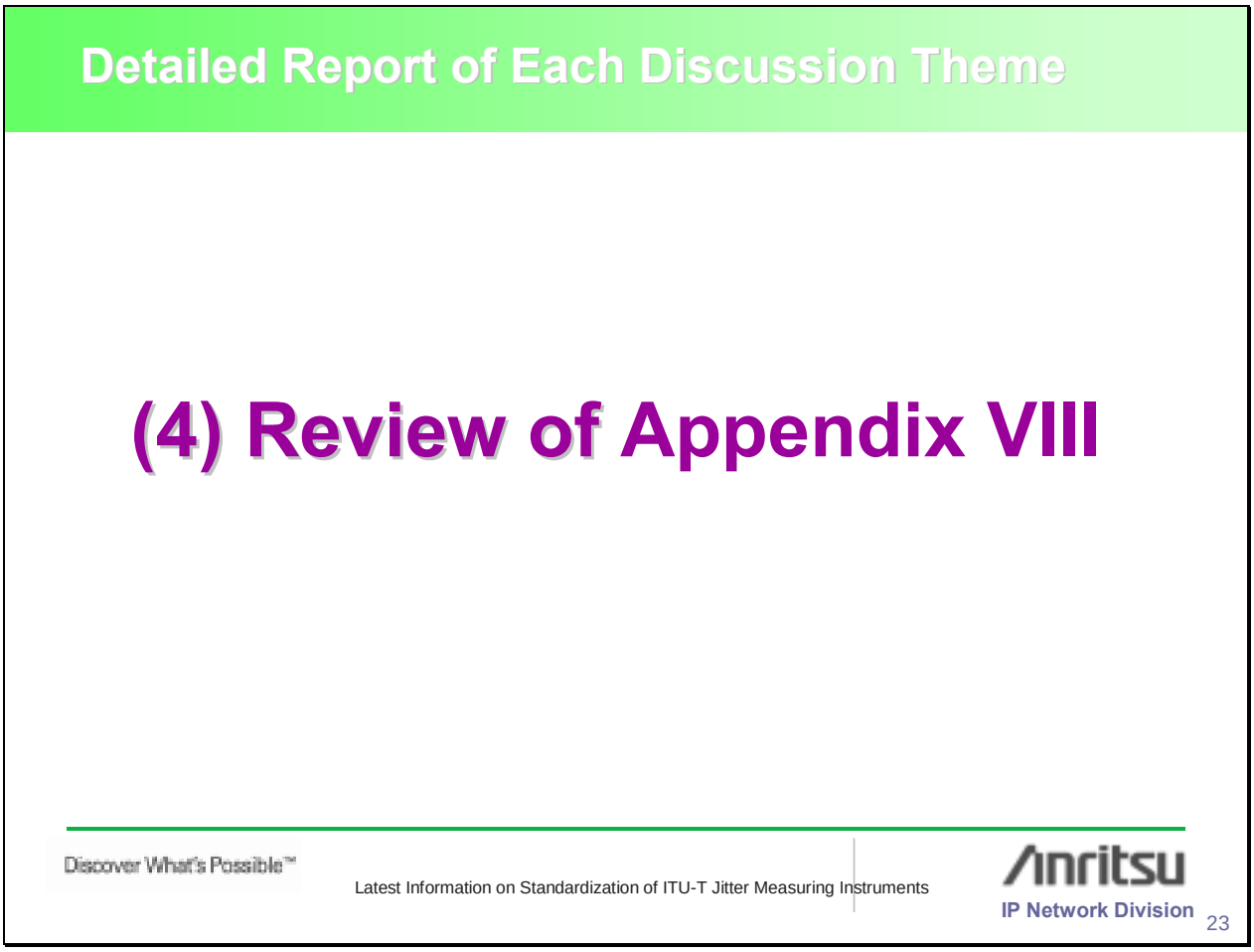


Fm=15MHz

We used the clock loop-back test for verification, since the method to eliminate pattern jitter referenced in Appendix VII has uncertainties.



This slide shows some typical measurement results when the MP1590B is evaluated using the evaluation system of Appendix VII. We can see that the randomness is excellent and within ±15 mUIpp. This evaluation was performed by looping back a calibrated clock signal to eliminate the above-described accuracy issues.



Finally, I want to explain the details of the review of Appendix VIII (one of jitter tester verification methods), which is the fourth main discussion theme.

Detailed Report of Each Discussion Theme
(4) Review of Appendix VIII

Introduction

The following themes were discussed for the jitter tester verification methods in Appendix VIII

(1) Re-verification of Edge Insertion Method

- A substitute method is required because the current HOLD method causes error especially when evaluating a signal including DCD (Duty Cycle Distortion).

(2) Edge Insertion Method Algorithm Error Verification Standard

- A standard is required for verifying the Edge Insertion algorithm error.

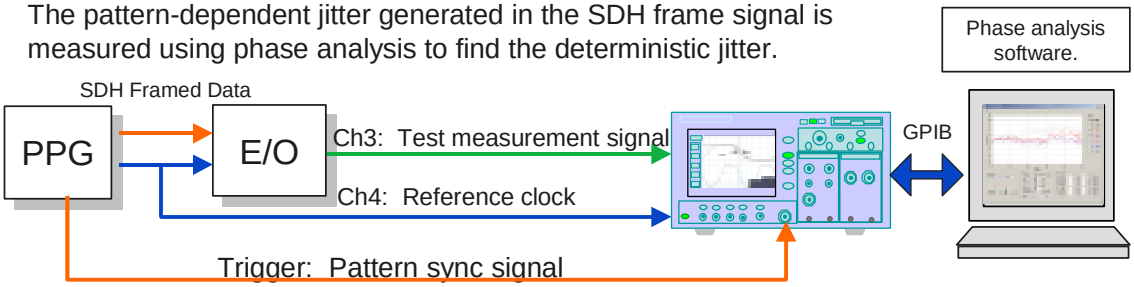
(3) Definition of Filter Band

- It is necessary to clearly define the measurement band at the oscilloscope side.

These three points were discussed at this meeting based on themes for Appendix VIII raised at the May 2004 ITU-T meeting. The first point is a re-examination of the Edge Insertion method used for correction when there is no edge. Currently, the Hold method is used in which the previous data is copied, but since error is caused when evaluating a signal including Duty Cycle Distortion (DCD), it is necessary to find a correction method that has smaller error. Point 2 discusses standards for evaluating error of the edge insertion algorithm. Since the Edge Insertion method is just a data correction method, there is error due to the algorithm and a standard must be defined to clarify the degree of this error. Point 3 covered discussions of a filter to be used when evaluating a DUT signal using an oscilloscope.

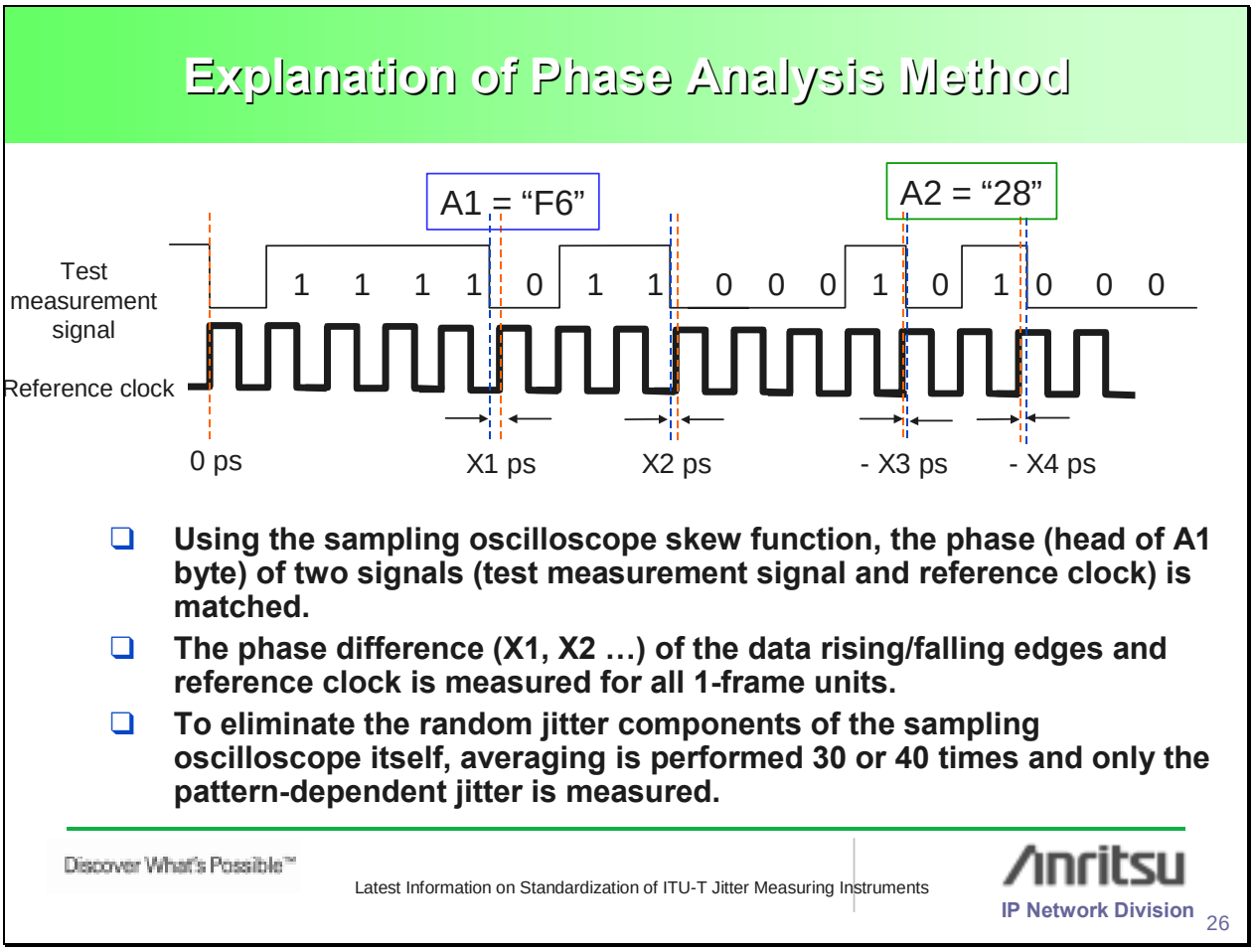
Appendix VIII Evaluation Method
Phase Analysis Method

The pattern-dependent jitter generated in the SDH frame signal is measured using phase analysis to find the deterministic jitter.



- **The phase difference of the edge of the jitter-free reference clock and test measurement signal is compared to measure the pattern jitter (phase measurement).**
- **The observed waveform is averaged to remove random jitter components.**
- **The filter (HP1 + LP or HP2 + LP) is calculated by digital signal processing after pattern jitter measurement.**

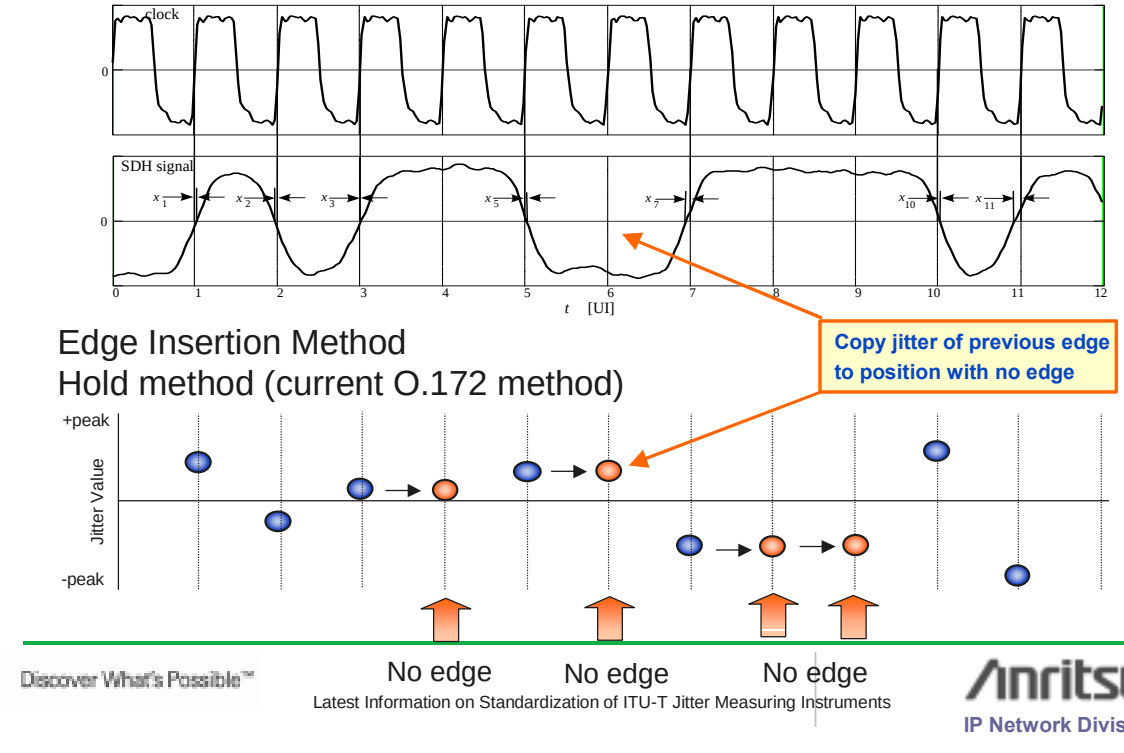
Now, I will explain the phase analysis technique (O.172 Appendix VIII verification method) for evaluating deterministic jitter such as pattern jitter.
This can be measured using general-purpose measuring instruments. First, an SDH frame signal is generated using a PPG. This signal is converted to an optical signal by an E/O converter and this optical signal is connected to a sampling oscilloscope. The clock for the reference signal is also connected simultaneously and monitored. These signals are synchronized by a pattern sync signal and monitored. Since the reference clock has no pattern jitter, the pattern jitter can be measured by measuring the phase difference of the rising and falling edge of the reference clock and data signal. To eliminate random jitter in this signal and the sampling oscilloscope itself, the signal is averaged using the averaging function and then evaluated. The jitter filtering required to evaluate jitter is performed by filter processing using DSP after the phase difference data has been completely measured.



Here is a slightly more concrete explanation. This diagram shows the test measurement signal data and reference clock. First, the skew function of the sampling oscilloscope is used to align the edge of the A1 byte of the non scramble byte. Next, the phase difference X1 ps between the data edge (here only the falling edge is monitored but actually both the rising and falling edges are monitored) and the reference clock is measured. The phase difference (X2, X3, …) between each edge and the reference clock is measured for every frame while the signal drifts. (It is also possible to measure the scramble byte part.) As explained before, the phase analysis technique separates out only deterministic jitter for evaluation so random jitter is removed by the averaging function. Since this measurement is a relative evaluation of the clock and data, sampling oscilloscope error can be ignored.

Detailed Report of Each Discussion Theme
(4) Review of Appendix VIII

Current Edge Insertion Method



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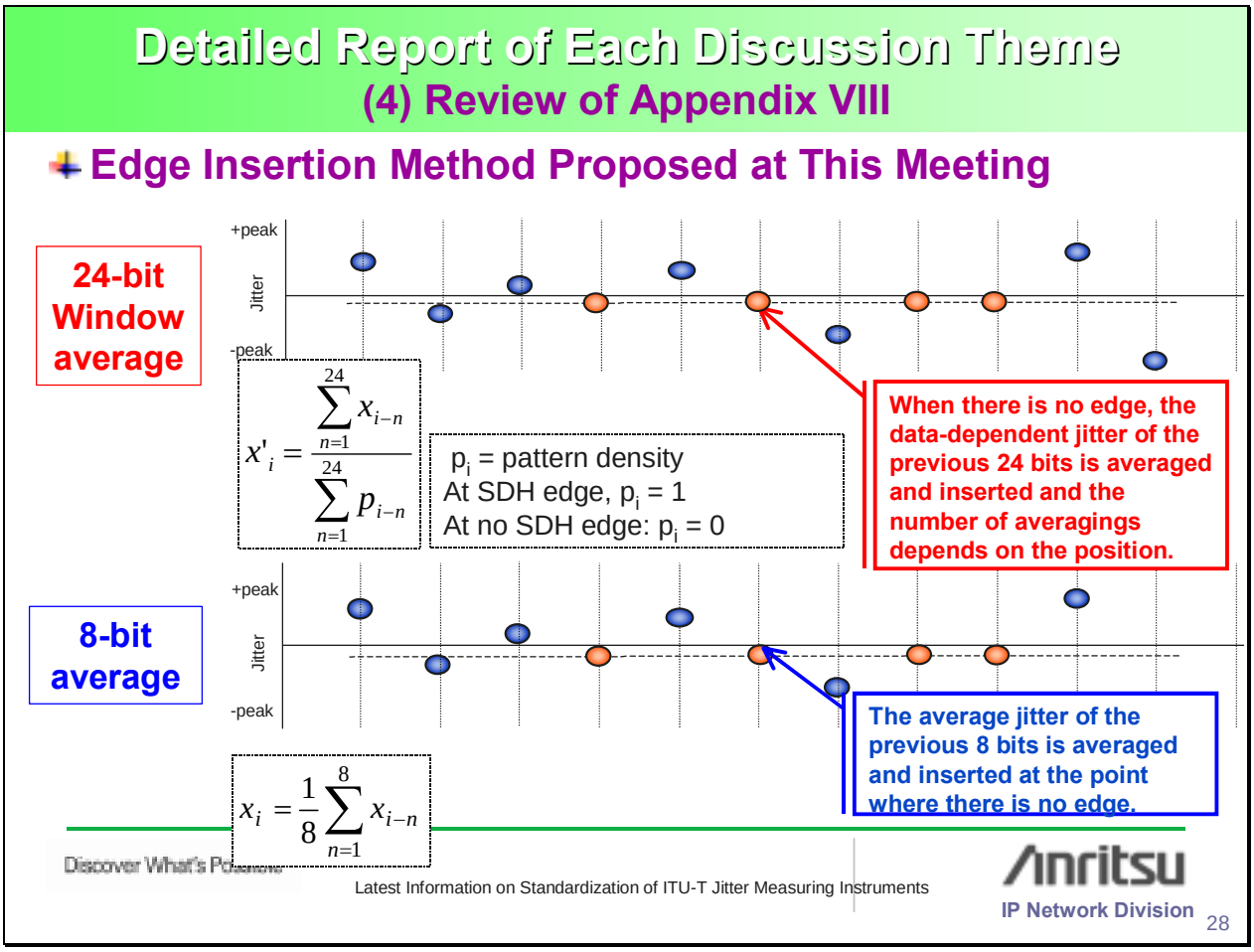
This slide explains the Edge Insertion method, which is a theme in Appendix VIII. The Appendix VIII verification method uses an oscilloscope for evaluating jitter in the data signal. The phase error between the edges of the data signal and reference clock signal is measured at each bit using a sampling oscilloscope to find the pattern jitter in the data signal using a measuring instrument other than a jitter tester. This figure explains the currently used Hold Edge Insertion Method. In this method, parts without a data edge are corrected so that there is a full set of edge data. The top part of the slide is a graph showing a comparison (blue) of the phase differences of each edge of the clock and data. In the Hold Edge Insertion method used so far, parts without an edge (orange) have the jitter at the previous edge copied to them. When this method is used to evaluate a signal with a lot of Duty Cycle Distortion (DCD), it causes a large error. This meeting examined other correction methods that could be substituted for the currently used Hold method.



These two Edge Insertion methods were proposed at this meeting. The 24-bit Window averaging method is a method for determining correction data that averages jitter data for the 24 bits of data prior to the point with no edge. In this method, the number of averagings changes with the pattern density data. The 24-bit Window width is chosen on the assumption that there is no part with no edge that exceeds 24 contiguous bits (possibility of no data for 8 contiguous bits). On the other hand, the 8-bit averaging method determines the correction data by averaging the jitter for the 8 bits prior to the part with no data edge. In this case, the averaging data count is always fixed at 8 bits.

Detailed Report of Each Discussion Theme
(4) Review of Appendix VIII

Discussion Results (1/3)

(1) Re-evaluation of Edge Insertion Methods

Although the error is small when evaluating a signal with low DCD (Duty Cycle Distortion) using the **HOLD method,** the error becomes large when the DCD is large. The following table compares the error using sample data for three types of edge insertion method. With the **8-bit averaging method**, there is no great difference in the error from using the **24-bit Window averaging method.** However, since 24-bit Window averaging produces a slightly smaller error, 24-bit Window averaging should be used.

Table 1 Insertion Error of Each Insertion Algorithm

Transmission signal (STM-64)	Jitter result of ideal CDR method [mUIpp]	Insertion error [%]		
		Hold	AVG8	AVG24 24-bit window
Example a	18	-14	-1	0
Example b	20	+22	0	0
Example c	19	+14	0	0
Example d	23	+21	-3	-4
Example e	60	+17	+1	-2
Example f	99	+16	-1	-1
Example g	120	+10	+7	0
Example h	7	+24	-16	-16
Example i	24	+7	-15	-4

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The Edge Insertion method discussed as an evaluation theme for the Appendix VIII verification method uses the 24-bit Window averaging method. However, whichever method is used, there is always error because these methods are data correction methods. As explained above, the measurement results include error due to the algorithm and we are investigating the error of algorithms for future verification methods. This table shows the results of error evaluations using several types of sampling data for the Hold method and the two Edge Insertion methods explained previously. Various types of sample data were evaluated including data with large and small jitter, large pattern jitter, and jitter with high randomness. In particular, evaluation was not performed to minimize DCD. Clearly, this evaluation cannot be said to be sufficient but this table shows the evaluation results but against the background of time constraints. The second column from the left is the peak jitter value calculated by a method that finds the correction value using the ideal CDR method explained later. The three proposed correction methods were compared based on this value. For the currently used Hold method, in a signal in which DCD was not controlled (optimized), the error sometimes ranged from -14% to +24%. However, for sample “h” with a maximum error rate of +24%, the reference jitter was 7 mUIpp, so the error was about 1.68 mUIpp. In a comparison using the same sample, there was very little difference between the error for the 8-bit and 24-bit methods, but when seen from the overall perspective, the 24-bit Window averaging method produces results with the smaller error so the 24-bit Window averaging method should be used.

Detailed Report of Each Discussion Theme
(4) Review of Appendix VIII

Discussion Results (2/3)

(2) Standards for Evaluation of Edge Insertion Method Algorithm Error

The Anritsu-patented Ideal CDR method was proposed as a basis for evaluating Edge Insertion algorithm error. There were no proposals from other members at the meeting, so it was decided to continue by adding the evaluation to the Living List.

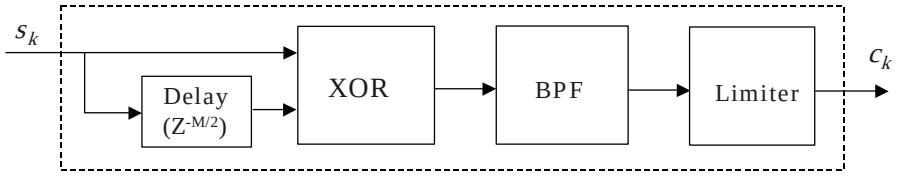


Figure 4 Example of Block Diagram of Clock Data Recovery

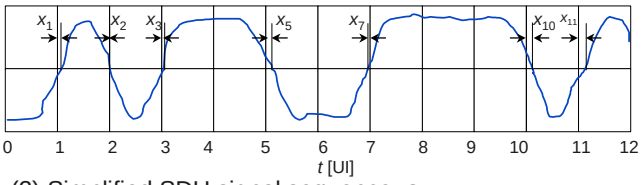
As a basis for clarifying Edge Insertion algorithm error raised as the second evaluation item for the Appendix VIII verification method, since there were no proposals from members other than Anritsu, it was agreed to add the evaluation to the Living List. This diagram shows the reference method proposed by Anritsu for Edge Insertion error comparison. The correction data calculated using the ideal CDR method is used to calculate jitter; since digital signal processing is used for all blocks, an ideal reference value with no error is found for the comparison.

Detailed Report of Each Discussion Theme
(4) Review of Appendix VIII

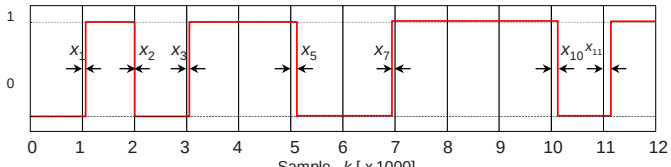
Ideal CDR Method (Reference)

As a basis for verifying the error of edge insertion algorithms, Anritsu introduced its following patented ideal CDR method, which was used as described below as the standard calibration method for edge insertion with no error when Anritsu evaluated Appendix VIII.

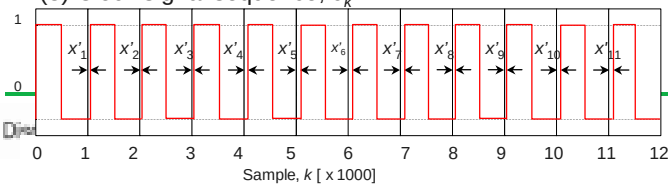
(1) SDH signal



(2) Simplified SDH signal sequence, s_k



(3) Clock signal sequence, c_k



[Evaluation Procedure]

1. Measure the pattern-dependent phase values, x_i, with a resolution of 1 mUI at the SDH signal edges, according to steps 1 through 3 in subclause VIII.2.1.
2. Make a simplified SDH signal sequence, s_k, by using x_i. Here, the amplitude value of s_k is 0 or 1, and the sampling interval of s_k is 1/1000 times the corresponding SDH bit rate. Assign x_i to the phase error value at the corresponding data edges of s_k.
3. Input the sequence s_k to the ideal clock data recovery (CDR) realised by the digital signal processing shown in Figure VIII.7. The clock signal sequence, c_k, is output from the CDR. Detect the phase error sequence, x'_i, at every rising edge of c_k.

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This slide explains the reference (ideal CDR method) patented by Anritsu that can be used to evaluate the error of the Edge Insertion methods. First, the jitter at each data edge is found using the procedure described in Appendix VIII as shown in the top part of the slide. Next, substitution is performed as shown in the middle part of the slide to create an ideal signal (zero at rising and falling edges) with the jitter found in (1). This signal is passed through the digital signal blocks described on the previous page to become an ideal CDR. The regenerated clock jitter appearing in this ideal CDR output is used as the correction data. This method is ideal but since it involves a large amount of computation time, it is unsuitable for real-time processing. As a result, this method cannot be used for actual measurement so it was not proposed as a basis for error evaluation. When performing Appendix VIII at Anritsu, all the evaluation methods including the currently used Hold method, the 24-bit Window averaging method used this time, and this ideal CDR method are all checked to determine the reference signal value.

Detailed Report of Each Discussion Theme
(4) Review of Appendix VIII

Discussion Results (3/3)

(3) Definition of Filter Band

To raise the measurement accuracy, it was decided to perform evaluation using band limiting with a 4th order Bessel filter (-3 dB band 0.75 x Bit Rate) at the oscilloscope input stage.
(See ANNEX B/G.957 and ANNEX A/G.691.)

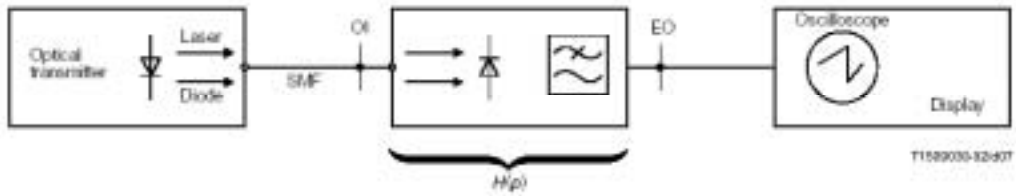


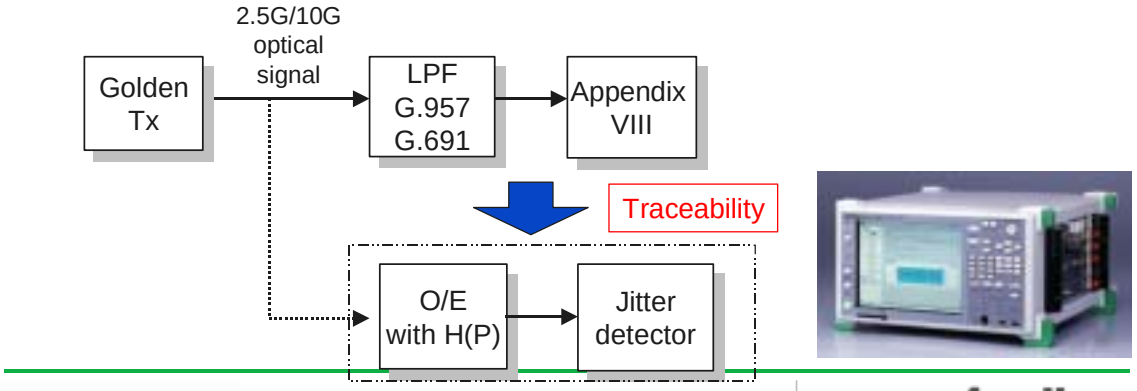
FIGURE B.1/G.957
Measurement set-up for transmitter eye diagram

As the third point in the Appendix VIII verification method, when inputting a signal to an oscilloscope, measurement is performed using a 4th order Bessel band-limiting filter as specified in G.957, and G.691.

Detailed Report of Each Discussion Theme
(4) Review of Appendix VIII

MP1590B Block Diagram (Reference)

- When using a signal from a 2.5G/10G direct modulator conforming to the Appendix VIII evaluation method of ITU-T O.172, it is important to perform evaluation with the same H(P) as at eye mask evaluation.
- To perform accurate traceability, the jitter tester must also have the H(P) characteristics.
- Since the MP1590B has traceability, the H(P) characteristics are incorporated in the tester, permitting high accuracy jitter measurement even when using the signal from a direct modulator.

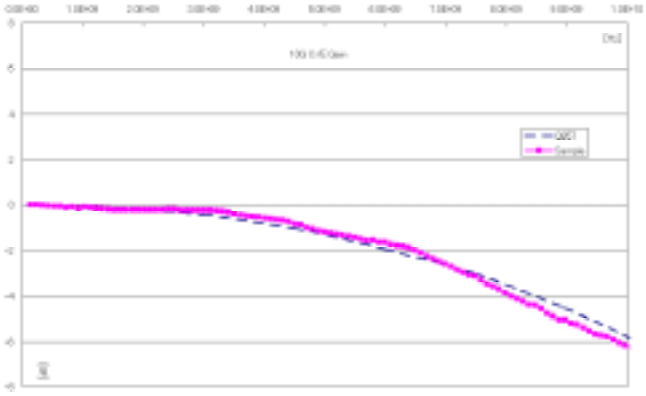


To determine the traceability of jitter using a 2.5G/10G direct modulator, a Bessel filter meeting the G.957 and G.691 specifications is inserted even when using the Appendix VIII evaluation method. The MP1590B is designed to provide traceability whatever the route. In other words, its input section also has the H(P) transfer function characteristics and the result of this meeting, officially confirmed the need for these characteristics.

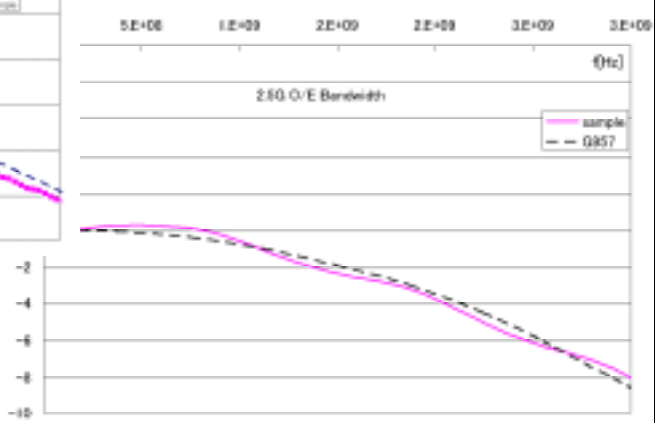
Detailed Report of Each Discussion Theme
(4) Review of Appendix VIII

MP1590B O/E Filter Characteristics (Reference)

[10 Gbit/s]



[2.5 Gbit/s]



The red line in this slide shows the characteristics of the filter at the O/E side of the MP1590. The dotted line shows the characteristics of the Bessel filter specified in G.957 and G.691. We can see that the filter characteristics match at every bit rate.

We plan to continue producing these types of materials about each ITU-T meeting to ensure that everybody has a clear understanding of the progress being made.
Thank you.

Anritsu

Specifications are subject to change without notice.

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