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TECHNICAL NOTE

# Newest Information and Further ITU-T O.172 Study Items

ANRITSU CORPORATION

MBP-1SG040142

# Newest Information and Further ITU-T O.172 Study Items

August 2004

IP Network Division

Anritsu Corporation



Good Morning (Afternoon). Today I am going to introduce some new topics related to standardization of the jitter testing presently being examined by the ITU-T SG4/Q5 group.

# ITU-T SG4/Q5 Meeting Results (1/2)

## Summary

Outcome of last meeting (2004.05.03–04)
(a) Revised draft O.172 (TD30-PLEN)
(b) Sending liaison to NIST (TD31-PLEN)
(c)Task reviews (TD35-PLEN)

Both Appendix VII and Appendix VIII on Draft O.172 are on the agenda for the next meeting.



The previous meeting of the SG4/Q5 group was held on May 3 and 4 this year in Geneva, Switzerland. These three topics were the outcome of that meeting.
Currently, with respect to Appendix VII and VIII related to examination of jitter testers under O.172, we have identified securing measurement precision and clarifying measurement uncertainties. These subjects have been classified as Under Study for discussion and examination by the next meeting. The latest version of Draft O.172 reflecting these contents has been assigned the revised document number TD30-PLEN.
With respect to item (b), a liaison statement letter has been drafted to request checking of the Appendix VII and VIII jitter tester verification methods by NIST as a third-party testing organization.
Item (c) covers the review of the Living List for future tasks.

## ITU-T SG4/Q5 Meeting Results (2/2)

- Next meeting

  To reach an agreement at the next SG4 meeting, an interim meeting will be held in the UK from 2004.09.27–30.

- Liaison

  The Anritsu proposal (D184) was agreed and SG4/Q5 decided to send a liaison to NIST as a third party to give advice about measurement accuracy in verification methods (Appendix VII, VIII). The same information will be sent unofficially to NPL in the UK and PTT in Germany.



The next general meeting of ITU-T SG4 is planned to be held in Geneva, Switzerland in March 2005. Prior to that, an interim meeting of experts will be held in the UK to clarify the current results which will then be presented to the next general meeting in 2005 for the purpose of obtaining official consent.

Anritsu proposed a jitter tester verification method under O.172 Appendix VII and VIII for checking by an impartial third party and, in addition to sending the results to NIST, unofficial checks by NPL in the UK and PTT in Germany have also been requested.

## Further Study Items for O.172 Appendix VII, VIII

The following points for guaranteeing accuracy were raised at the last ITU-T SG4/Q5 meeting to be resolved soon.

- **Appendix VII**

1. No certain way to verify final output jitter value
   → No known way to confirm standardized value at Accuracy Map, so unable to separate errors of receiver from those of transmitter
   → Jitter errors at data generator not considered at all (assuming ideal no-jitter circuit)
2. Can't measure exact pattern jitter value that is factor in measurement errors
3. Need to review circuit block diagram that can remove pattern jitter (One company informed last meeting that they hold patent for current method)

- **Appendix VIII**

1. Need to verify edge-insertion method accuracy



At the previous meeting in May this year, the contents of the Appendix VII and VIII jitter tester verification methods were introduced.
In the Appendix VII method, evaluation is performed by imposing a burst sinusoidal signal with 100 mUIpp jitter onto a data signal from which pattern jitter has been removed and these three issues were identified.

There is no certain way to verify the amount of jitter in the final output signal that is jitter modulated by the burst sine-wave modulation signal.

There is no way of accurately verifying the amount of jitter (less than 10 mUIpp) in the data signal from which pattern jitter has been removed.

Currently, since Company A has a patent on block diagram for the jitter-removal circuit described as a reference example in Appendix VII, it is clear that users will be prohibited from using the verification method, and as a result, it is necessary revise the block diagram so that all users will be able to use the method without patent licensing issues.
The Appendix VIII method has the same configuration as jitter generation measurement in which a sampling oscilloscope is used to separate the amount of jitter in the reference signal into DJ and RJ for evaluation. In this method, the jitter at the part of the NRZ signal with no edge is evaluated, requiring validation of the edge-insertion method in terms of the previously standardized Hold method (copying jitter of previous edge).

## Jitter Trend and Anritsu Approach (1)

# ITU-T O.172
# Appendix VII Update

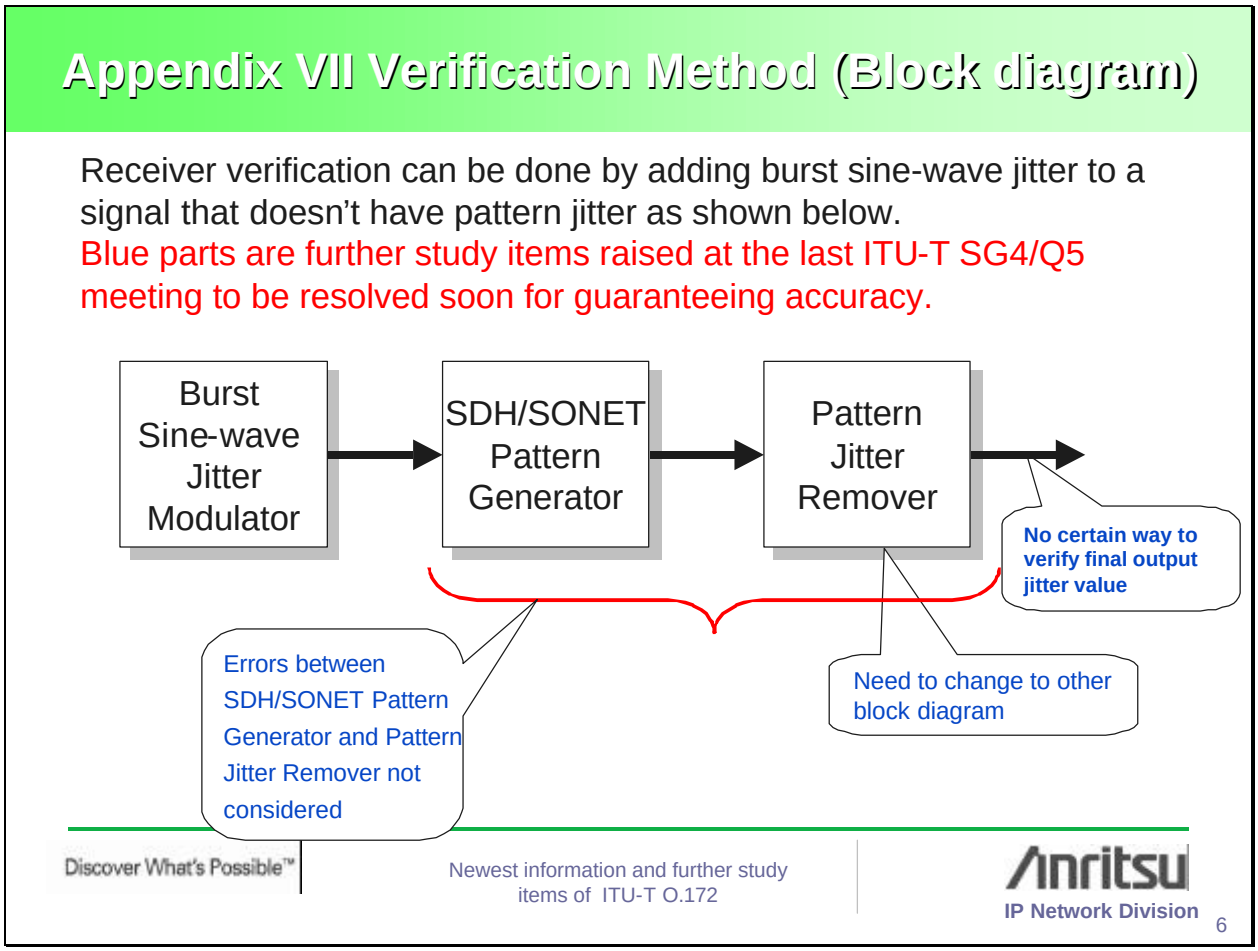
SG4 Meeting in May 2004

**Is Pattern Jitter Actually "Zero"?**

**How can you verify the jitter value of the final output?**

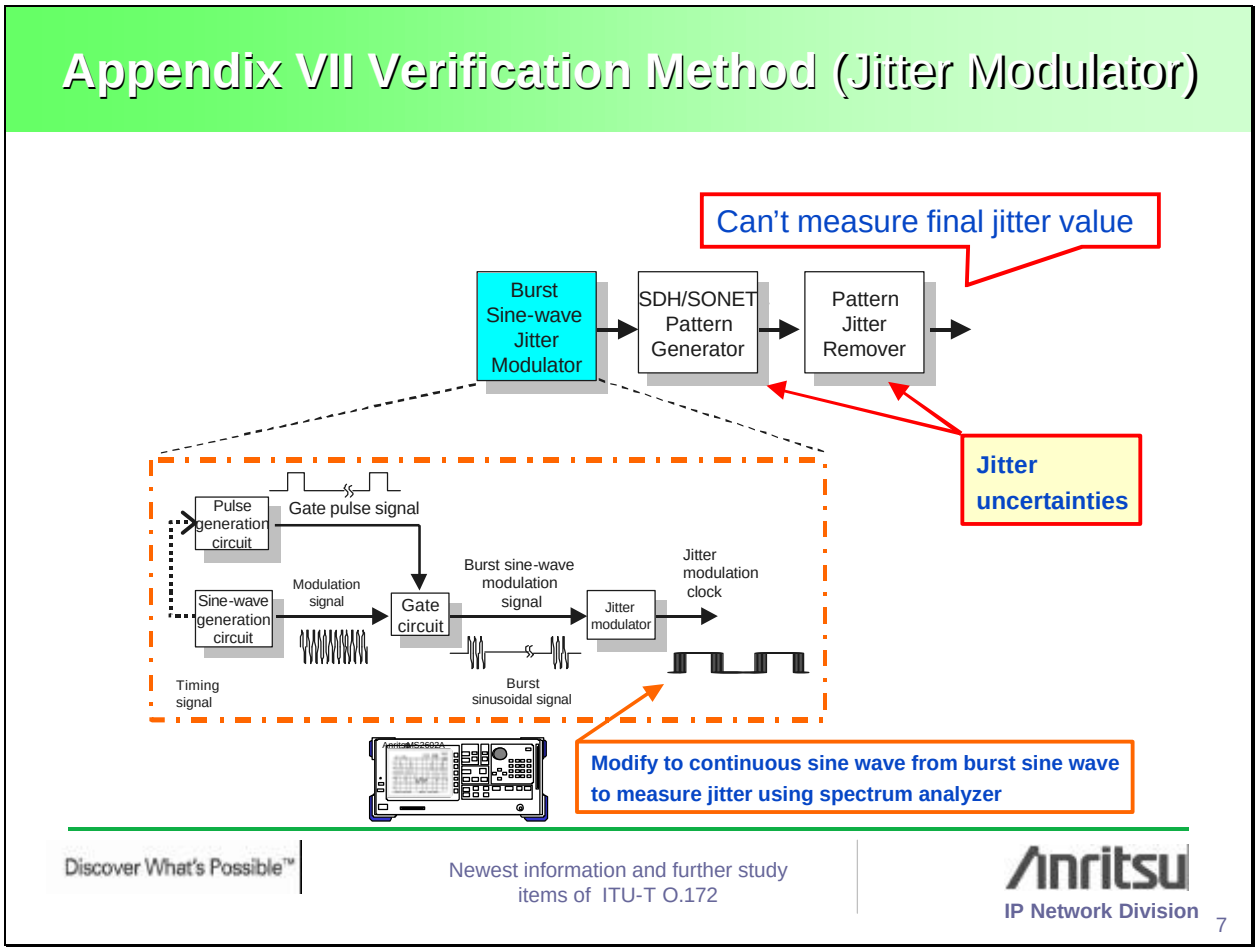


From here on, I am going to explain the issues of the current Appendix VII method using block diagrams and figures, etc.

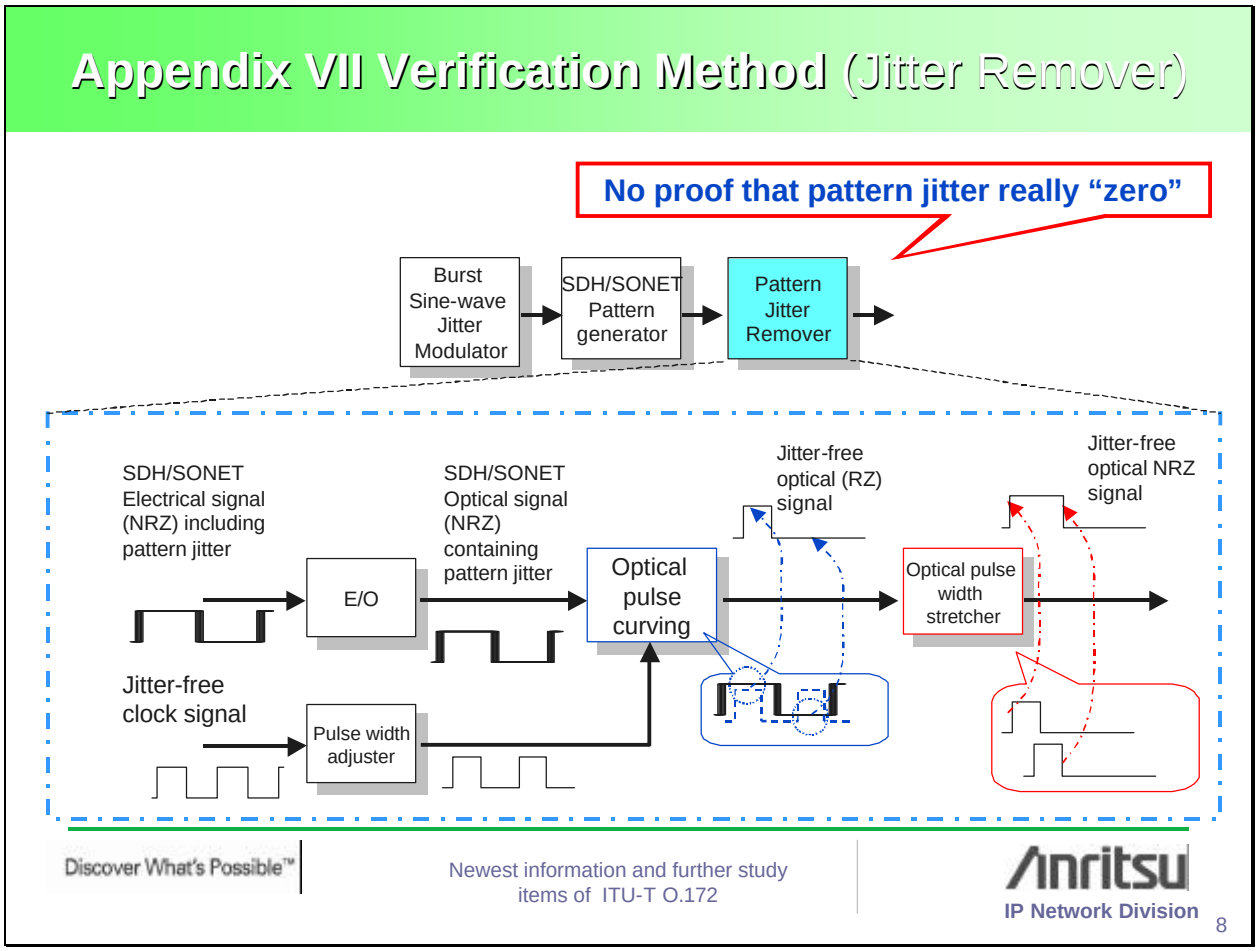



To make the Appendix VII method a practical proposition, it is necessary to produce a reference signal using the three blocks shown here. The block on the left is a jitter modulator that can add jitter of about 100 mUIpp as a burst sinusoidal signal generated at a clock of 9.95328 GHz. The middle block generates an STM-64 (9.95328 Gbit/s) frame signal at a clock of 9.95328 GHz. To obtain the SDH frame signal frame synchronization, a Non Scramble Byte (A1, A2, J0/Z0) is defines at SOH 1ROW. Pattern jitter occurs at this point. In addition, jitter also occurs at the Payload. When a data signal including these jitters is evaluated by the receiver of a jitter tester, accurate jitter evaluation is impossible due to the presence of these jitters. As a consequence, the pattern jitter at the final block shown on the right is used to remove jitter generated in the SDH/SONET pattern, reducing errors due to pattern jitter. However, when evaluating an actual signal, since jitter due to the evaluation-target pattern cannot be completely removed, there is little sense in setting a pattern even if it can be evaluated at various pattern settings (Payload PRBS31 +Scramble).

In this method, since there is no certain way to evaluate the amount of jitter added by the jitter modulated in the final output stage (output of pattern jitter remover), it is not possible to accurately determine the amount of jitter in the evaluation signal. Moreover, since company A has a patent on the block diagram for the pattern jitter remover described in the references, it is necessary to revise the block diagram to a different form so that all users can use the technology free-of-charge without patent licensing issues.



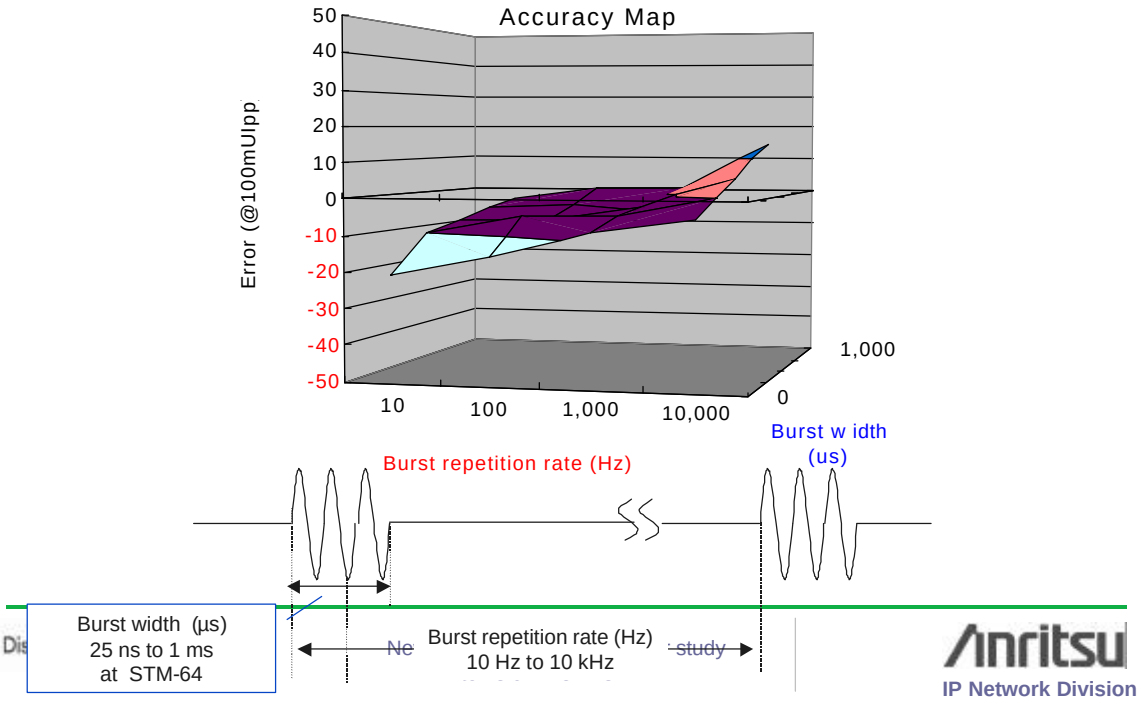

The Appendix VII method performs receiver evaluation with a signal to which jitter is added as a burst sinusoidal wave. However, it is not a method that permits accurate evaluation in the final-stage signal. The Appendix VII method is a method for evaluating whether or not it is possible to detect a fixed peak jitter amount (100 mUIpp) while changing the modulation signal burst repetition rate and burst width. However, Appendix VII provides a method for confirming the amount of added jitter by using a clock signal to which jitter has been added as a continuous sine wave (jitter modulator output) instead of a burst sine wave. In this case, the amount of jitter is found using a spectrum analyzer. In other words, it is possible the perform calibration of the jitter value with a modulation signal having different frequency components from the finally used modulation signal (burst sine wave), based on the supposition that it is the same as the peak jitter value. Moreover, since a signal with a known jitter value is passed through the pattern generator and pattern jitter remover, it is not necessary to take changes in jitter due to these blocks into consideration.




The Appendix VII method requires a pattern jitter remover to remove pattern jitter at 10 mUIpp (1 ps at 10 G) that is a source of error. Unfortunately, there is no method for directly checking jitter of less than 10 mUIpp in the jitter band specified by ITU-T (HP1 + LP).

# Appendix VII Accuracy Map

The Appendix VII accuracy map is used to evaluate the burst sinusoidal modulation signal defined below.




The Appendix VII method does offer a method for confirming whether or not a fixed peak jitter (100 mUIpp) can be detected at the receiver while varying the modulation signal burst repetition rate and burst width using the matrix shown here. However, this accuracy map evaluation has no meaning when it is not possible to confirm that the amount of jitter generated at the send side under any conditions is constant (100 mUIpp) at the final output.

## Jitter Trend and Anritsu Approach (2)

# ITU-T O.172

# Appendix VIII Update

# Verification of Edge-insertion Technique

Anritsu proposal for next ITU-T meeting in September 2004

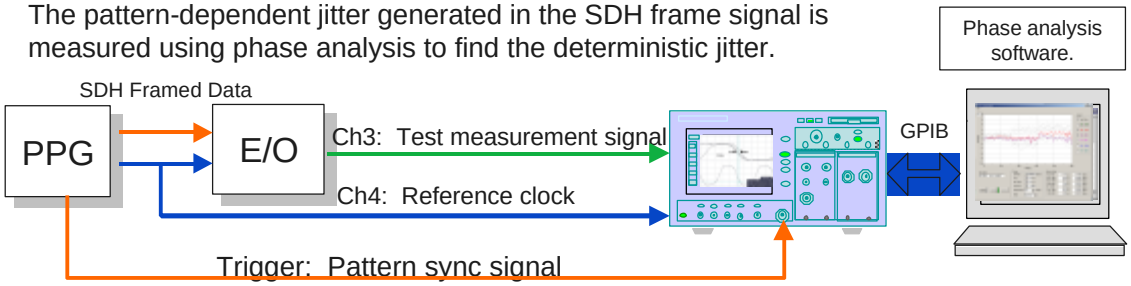
**How to consider jitter value of NRZ data column with no edge?**



From here on, I am going to explain some evaluation results produced by Anritsu following the previous meeting in May this year, regarding some issues about the current Appendix VII method, as well as some ideas supporting the current method that do not have accuracy problems. These ideas will be proposed to the next ITU-T meeting.

# Appendix VIII Evaluation Method
## Phase Analysis Method

The pattern-dependent jitter generated in the SDH frame signal is measured using phase analysis to find the deterministic jitter.

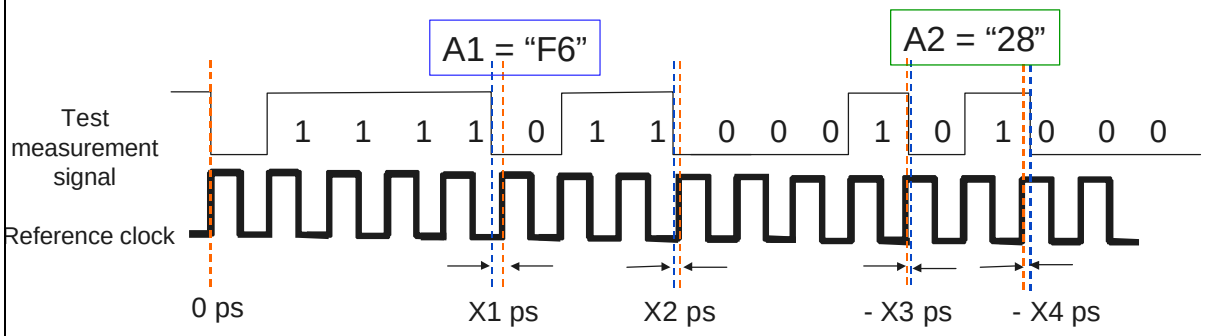



- **The phase difference of the edge of the jitter-free reference clock and test measurement signal is compared to measure the pattern jitter (phase measurement).**
- **The observed waveform is averaged to remove random jitter components.**
- **The filter (HP1 + LP or HP2 + LP) is calculated by digital signal processing after pattern jitter measurement.**



Now, I will explain the phase analysis technique (O.172 Appendix VIII verification method) for evaluating deterministic jitter such as pattern jitter.
This can be measured using general-purpose measuring instruments. First, an SDH frame signal is generated using a PPG. This signal is converted to an optical signal by an E/O converter and this optical signal is connected to a sampling oscilloscope. The clock for the reference signal is also connected simultaneously and monitored. These signals are synchronized by a pattern sync signal and monitored. Since the reference clock has no pattern jitter, the pattern jitter can be measured by measuring the phase difference of the rising and falling edge of the reference clock and data signal. To eliminate random jitter in this signal and the sampling oscilloscope itself, the signal is averaged using the averaging function and then evaluated. The jitter filtering required to evaluate jitter is performed by filter processing using DSP after the phase difference data has been completely measured.

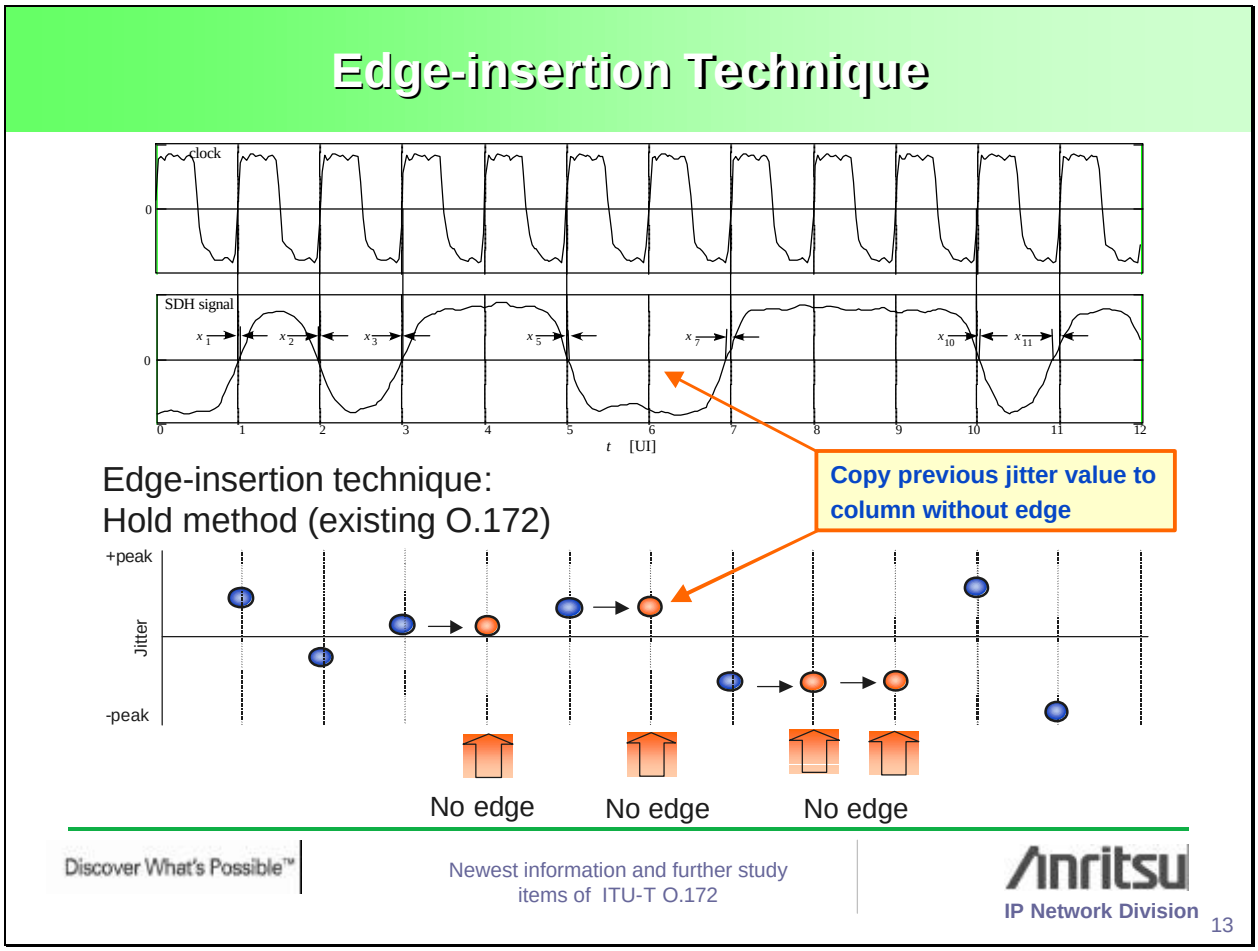
# Explanation of Phase Analysis Method




- **Using the sampling oscilloscope skew function, the phase (head of A1 byte) of two signals (test measurement signal and reference clock) is matched.**
- **The phase difference (X1, X2 …) of the data rising/falling edges and reference clock is measured for all 1-frame units.**
- **To eliminate the random jitter components of the sampling oscilloscope itself, averaging is performed 30 or 40 times and only the pattern-dependent jitter is measured.**

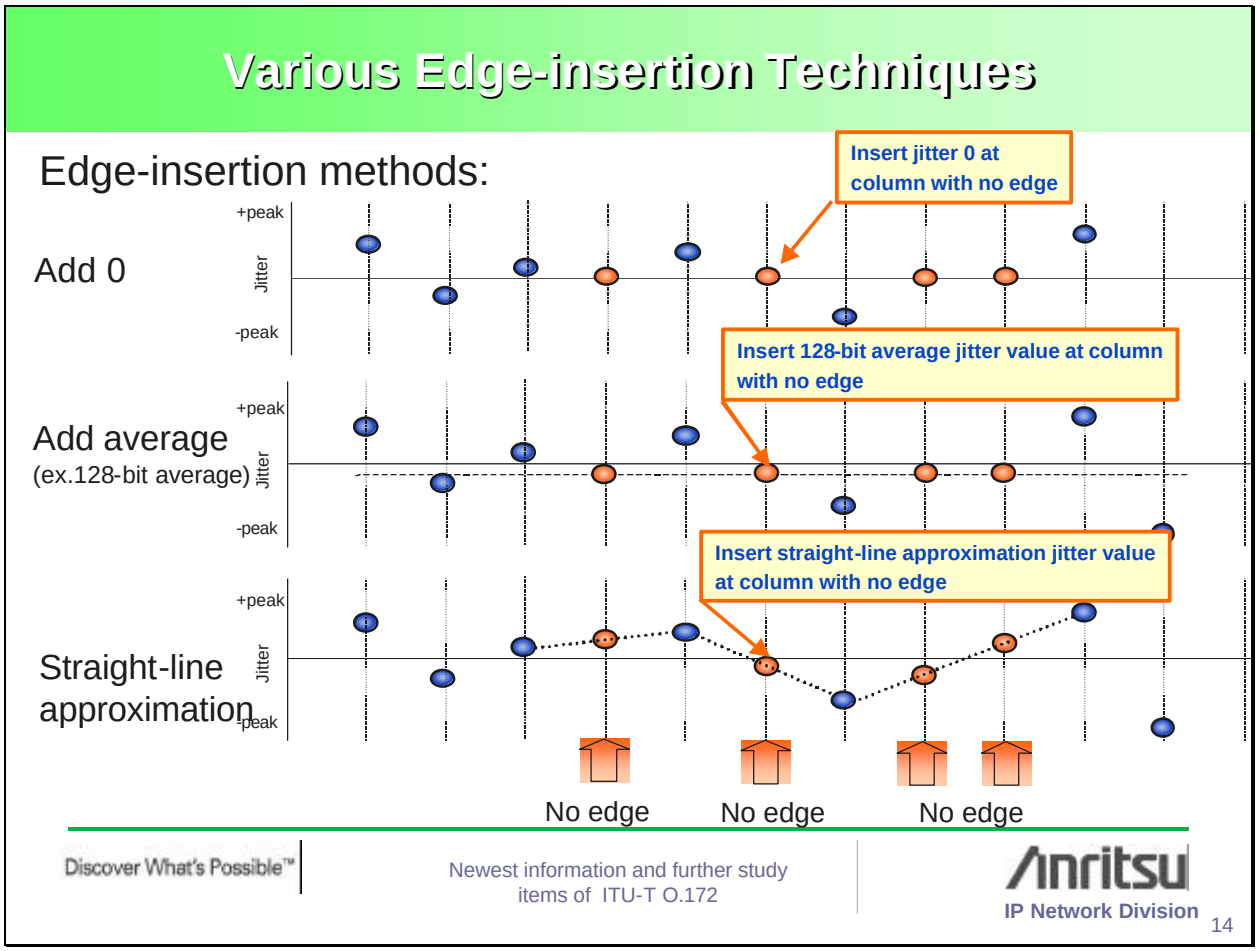


Here is a slightly more concrete explanation. This diagram shows the test measurement signal data and reference clock. First, the skew function of the sampling oscilloscope is used to align the edge of the A1 byte of the non scramble byte. Next, the phase difference X1 ps between the data edge (here only the falling edge is monitored but actually both the rising and falling edges are monitored) and the reference clock is measured. The phase difference (X2, X3, …) between each edge and the reference clock is measured for every frame while the signal drifts. (It is also possible to measure the scramble byte part.) As explained before, the phase analysis technique separates out only deterministic jitter for evaluation so random jitter is removed by the averaging function. Since this measurement is a relative evaluation of the clock and data, sampling oscilloscope error can be ignored.

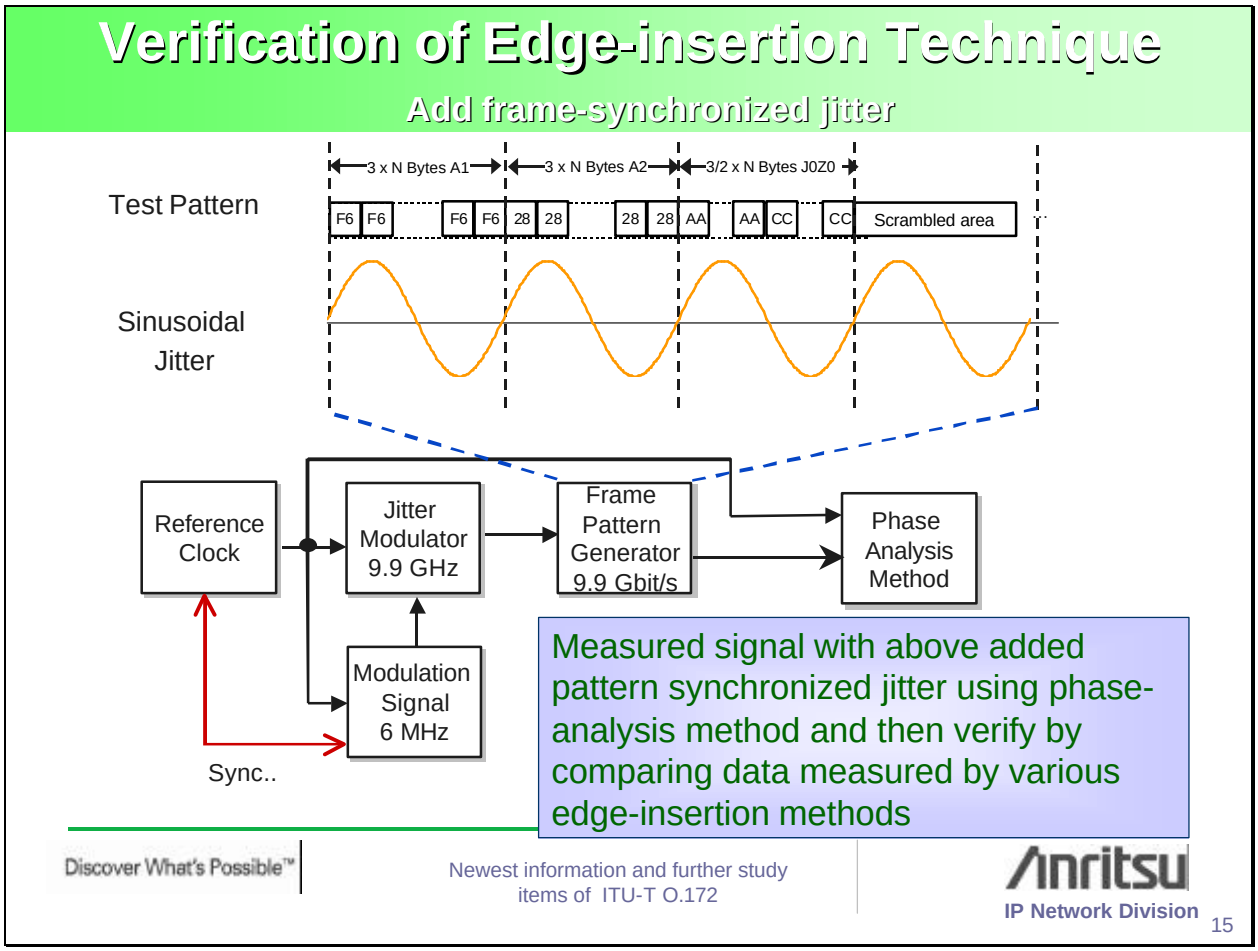



Appendix VIII describes use of a sampling oscilloscope to evaluate the amount of jitter in a data signal. The phase difference at the edge of the data signal and the reference clock signal is measured at each bit using a sampling oscilloscope to find the pattern jitter of the data signal without using a jitter tester as the measuring instrument. At the May 2004 meeting, the need for technical support for an interpolation method for NRZ data with no edge was identified but could not be evaluated due to time considerations. The following materials explain the various edge-insertion techniques that our company has investigated following the ITU-T meeting that do not present the accuracy problems of the current Hold method.

The figure in this slide shows a comparison of the phase difference (blue) of the edges of the clock and data signals, indicating the points (orange) where the jitter value of previous edge was copied because there was no edge so as specified in Appendix VIII.



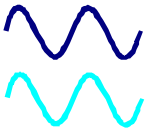

Another two other methods were proposed at the previous ITU-T meeting in addition to the Hold method described on the previous slide. The top part of this slide shows the Add 0 method in which a jitter value of 0 is added at parts where there is no edge. The middle part shows the Add average method in which the average jitter value for the previous 128 bits is added to the parts where there is no edge. However, neither of these two methods was proposed based on any evidence of real technical advantages. The bottom part of this slide shows the method examined by Anritsu; in this method, a straight line is approximated between the previous and succeeding edges and the interpolated value is inserted at the point where there is no edge. These four methods were simulated to examine the error inherent in each method.




To investigate the edge-insertion error, it is necessary to specify the theoretical value. As shown in this block diagram, evaluation was performed by simulating a signal to which jitter is added using a sinusoidal modulation waveform synchronized to the SDH frame. In other words, the block diagram shown here is not the block diagram used for the actual evaluation—it only shows a conceptual image of the evaluation system. First, an SDH frame pattern with no pattern jitter is generated by a simulator. Since the signal is produced by a simulator, all the jitter values are zero. A phase variation is produced by the synchronization of the modulation signal (sine wave or burst wave with this generated pattern. This makes it possible to find the phase error of each edge of a signal to which hypothetical phase variation has been added using a simulator in the same manner as Appendix VIII. In this case, we measured and compared the jitter value at the points with no edge in the previously described four methods.
As explained before, phase modulation is caused by the modulation signal synchronized to the pattern so we can determine the theoretical value of the jitter even at locations with no edge and this was used to evaluate the errors of each edge-insertion method.

# Verification of Edge-insertion Technique

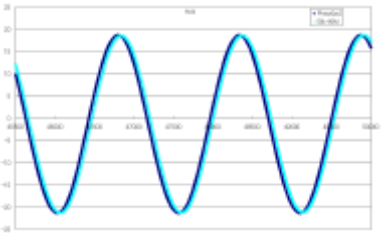
## Simulation Result—Sinusoidal Jitter



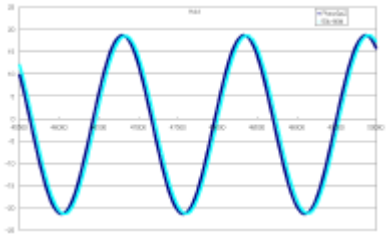
Ideal jitter

50 kHz–80 MHz filtered jitter with edge interpolation

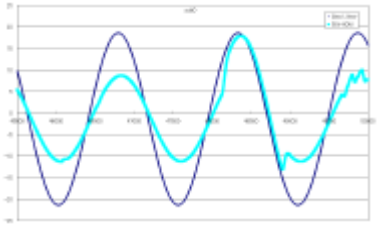
Straight-line approximation



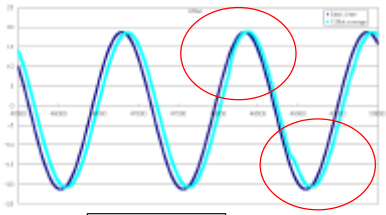
Hold

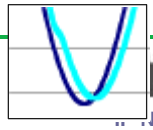


Add 0 ps



Add 128-bit average





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This slide shows the measured phase errors obtained by comparing the results obtained by the methods in Appendix VIII and the ideal results obtained by simulation. In this case, a sine wave was used as the modulation signal because the aim was to confirm the degree of distortion caused by each edge-insertion method. The dark blue line is the ideal jitter while the light blue line shows the results found for each of the interpolation methods.

As you can see, the Hold method specified in Appendix VIII and the new straight-line approximation method examined by Anritsu produce very similar results with almost the same values and little jitter. On the other hand, the Add 0 method produces unquestionable jitter. In addition, the Add 128 bit average method causes some jitter (and the same trend even with a different bit count).

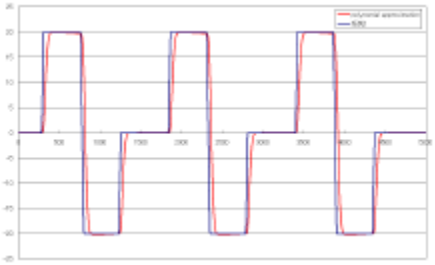
# Verification of Edge-insertion Technique

## Simulation Result—Pulse Jitter

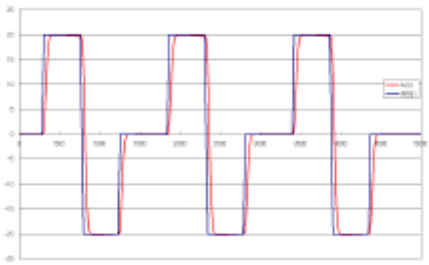
Ideal jitter

50 kHz–80 MHz filtered jitter with edge interpolation

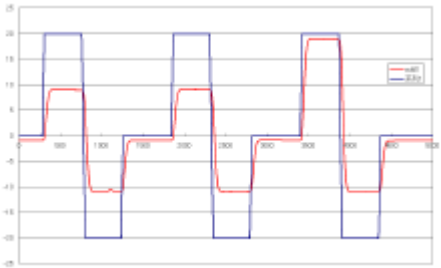
Straight-line approximation



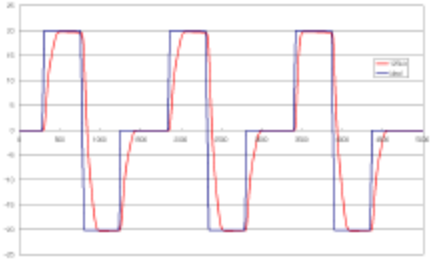
Hold



Add 0 ps



Add 128-bit average



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Instead of using a sine-wave modulation signal, the next slide compares the frame-pattern simulated pulse jitter. The dark blue line shows the ideal jitter and the red line shows the result for each interpolation method. The results of the Hold method specified in Appendix VIII and the new straight-line approximation method evaluated by Anritsu are very similar with practically no delay other than delay caused by the 80-MHz LPF and very similar jitter values. On the other hand, the Add 0 insertion method produces unquestionable jitter. In addition, the Add 128 bit average method causes large delay other than delay caused by the 80-MHz LPF and some jitter (and the same trend even with a different bit count).

# Verification of Edge-insertion Technique

## Edge Insertion—Simulation Summary

| Interpolation method | Pattern-dependent jitter waveform | | | |
|---|---|---|---|---|
| | Sine wave | | Rectangular wave | |
| | Peak-Peak Error [%] | RMS Error [%] | Peak-Peak Error [%] | RMS Error [%] |
| Hold | **-1** | 0 | **-2** | -1 |
| Null | -20 | -46 | -30 | -47 |
| 128-bit average | -4 | -4 | -1.8 | -6 |
| Straight-line approximation | **-0.1** | 0 | **-0.5** | -0.8 |

- The accuracy of the edge-insertion technique can be confirmed by inspecting the jitter imposed by a pattern-synchronized sine-wave modulation signal and a pulse-modulation signal.
- Clearly both the 0-ps and averaged-value approaches are inadequate for accurate measurement.
- The most accurate results are derived by using the Hold or Straight-line Approximation methods (small distortion).



This table summarizes the simulation results explained so far; for the Hold edge-insertion method specified in Appendix VIII, the difference between the ideal jitter value and the jitter value at sine-wave modulation was just -1% and was -2% at pulse wave modulation. On the other hand for the Add 0 method proposed at the previous meeting, the same errors were extremely large at -20% and -30%, respectively. For the Add 128-bit average method, the error was -4% at sine-wave modulation and -18% at pulse wave modulation.

From these results, it is clear that the currently recommended Hold edge-insertion method has no serious problems in terms of accuracy. However, it is also clear that the newly examined straight-line approximation method also produces even smaller errors than the Hold method.

## Summary of Further O.172 Study Items

### Further Study Items for Appendix VII

1. No certain way to verify final output jitter value
2. Can't measure exact pattern jitter value, which is one measurement error
3. Need to review circuit diagram that can remove pattern jitter
   - ✓ **Many uncertainties**
   - ✓ **Appndix VII is a method effective in jitter evaluation of the clock interface which removed the indefinite element.**

### Further Study Items for Appendix VIII

1. Accuracy of Edge Insertion
   - ✓ **Current Hold and/or Straight-line Approximation method reasonable and correct way to measure pattern jitter accurately**

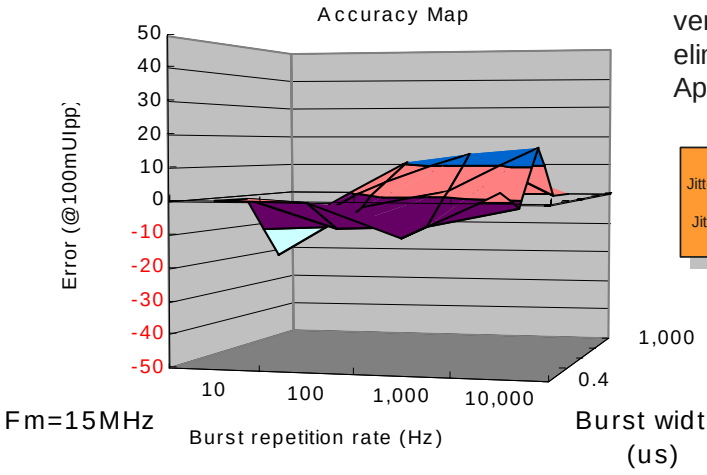
Pattern jitter is the most dominant type of jitter.
The most important item for a jitter analyzer is how to measure pattern jitter exactly.



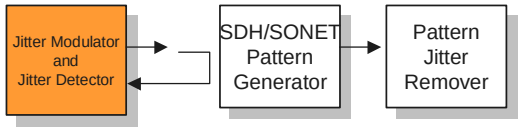
This slide summarizes all the issues discussed so far.
For the Appendix VII method:
First, the fatal problem is that since there is no certain way to versify the jitter value in the final output, there is no way to obtain the traceability needed for assuring accuracy.
Second, since it is not possible to verify the existence or degree of pattern jitter (10 mUIpp), accuracy will always be limited by addition of this error.
Third, Appendix VII is a method effective in jitter evaluation of the clock interface which removed the indefinite element.
For the Appendix VIII method:
First, our simulation results confirm that the current Hold method has no problems with accuracy.
Second, at evaluation of an actual signal, the most important consideration is to use a method that is able to accurately evaluate the pattern jitter, which is the most serious jitter included in the signal.

# MP1590A/B Accuracy Map (Typical)

The MP1590A/B accuracy map was determined according to the standard method described in Draft ITU-T O.172 (May 2004).
The values for burst width and burst repetition rate are values specified in ITU-T O.172 Table VII.1.




We used the clock loop-back test for verification, since the method to eliminate pattern jitter referenced in Appendix VII has uncertainties.

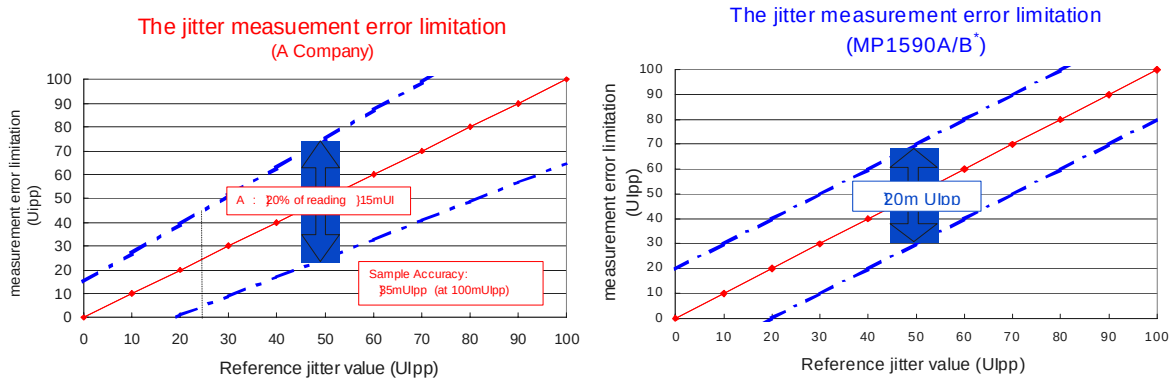





This slide shows some typical measurement results when the MP1590A/B is evaluated using the evaluation system of Appendix VII. We can see that the randomness is excellent and within ±15 mUIpp. This evaluation was performed by looping back a calibrated clock signal to eliminate the above-described accuracy issues.

# The definition of jitter measurement accuracy

- **In case of ITU-T O.172 and A company (lower left)**
  The total jitter measurement accuracy of ITU-T O.172 and A company is specified by variable error (R%) and fixed error (W UIpp).
  *Accuracy <= ± R% of reading ± W UIpp*
- **In case of MP1590A/B* (Lower right)**
  The total jitter measurement accuracy of MP1590A/B* is only specified by fixed error (W UIpp) which was Traced by ITU-T O.172 Appendix VIII jitter verification method. (* with Option 30 High-Precision Jitter Analysis)
  *Accuracy <= ± 20mUIpp*

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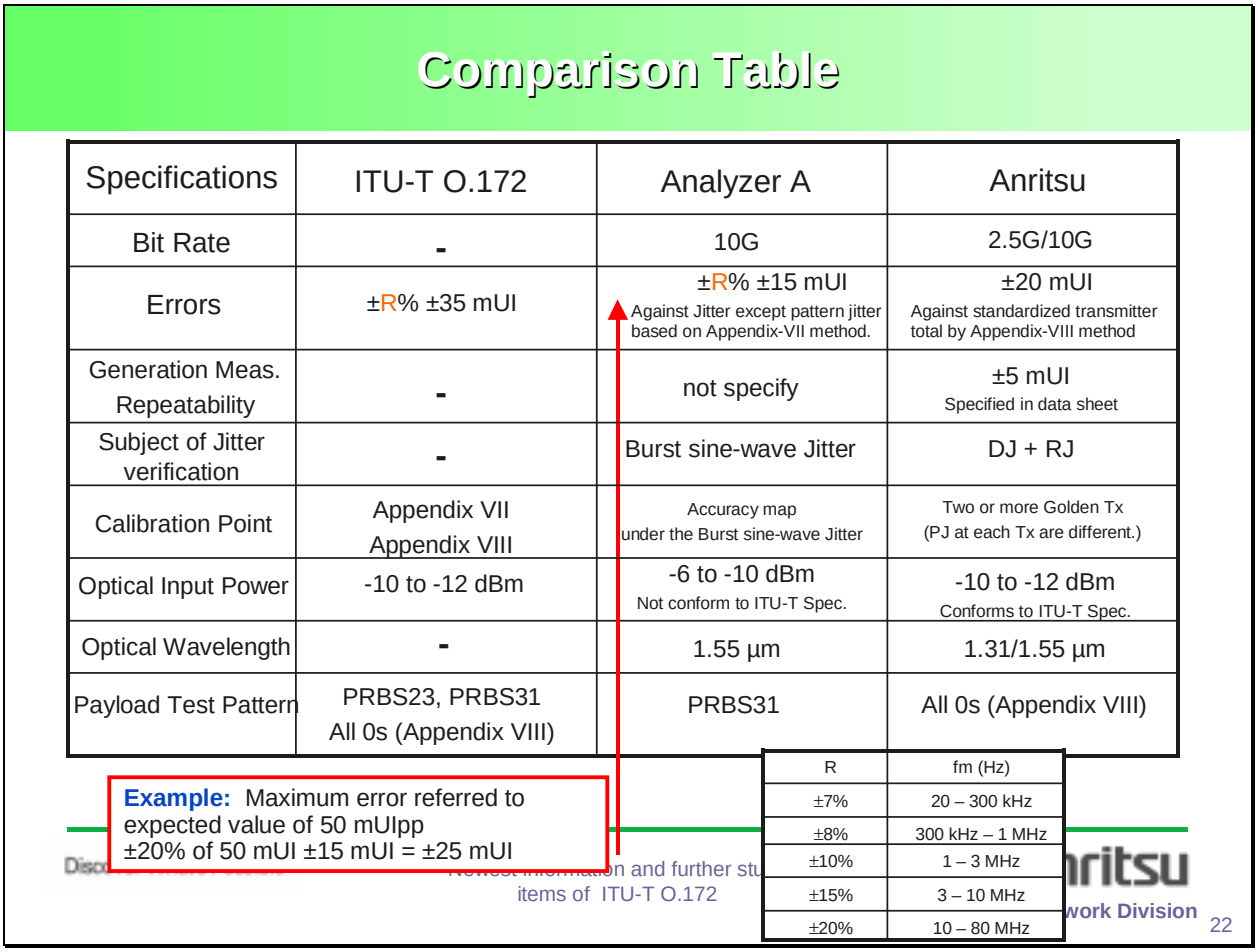
This slide explains some definition of jitter measurement accuracy. In case of ITU-T O.172 and A company, the total jitter measurement accuracy of ITU-T O.172 and A company is specified by variable error (R%) and fixed error (W UIpp) as following formula.

In case of ITU-T O.172 and A company, the total jitter measurement accuracy is specified by variable error (R%) and fixed error (W UIpp) as following formula.

Accuracy <= ± R% of reading ± W UIpp

Blue line on the figure show the maximum error . In case of ITU-T O.172 , the maximum measurement error is ± 55mUIpp to reference jitter value 100mUIpp. In case of A Company, the maximum measurement error ± 35mUIpp to reference jitter value 100mUIpp.

The total jitter measurement accuracy of MP1590A/B* is only specified by fixed error (± 20mUIpp) which was traced by ITU-T O.172 Appendix VIII jitter verification method. You can see to compare two figures which is better.



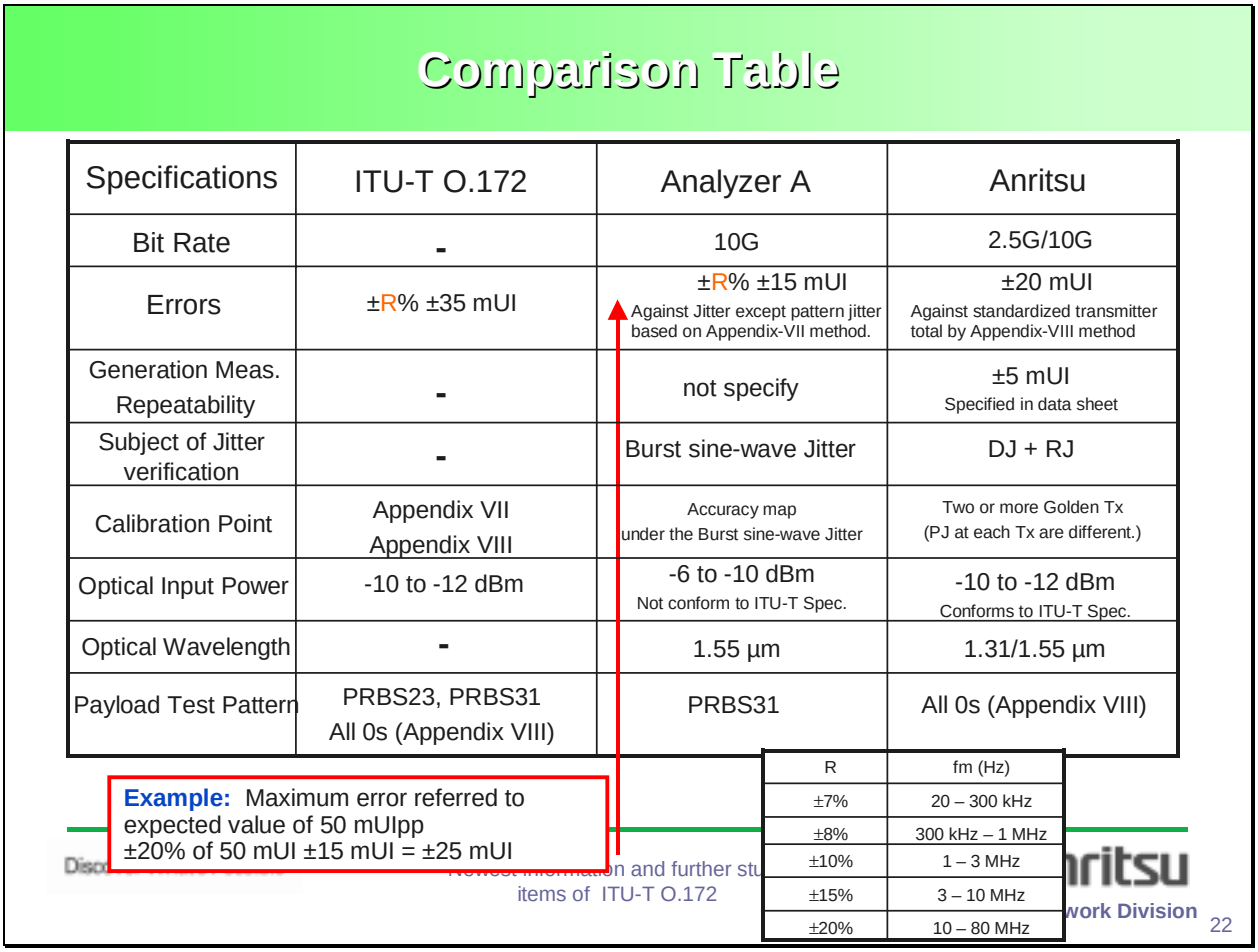

Lastly, this table compares the measurement accuracy specified by ITU-T O.172 and that provided by Anritsu's MP1590A/B and another analyzer.

First, the MP1590A/B supports both bit rates of 2.5 and 10G but the other analyzer only supports 10 G. This is important for assuring traceability even for the many direct modulators operating at 2.5 G. (By following Appendix VIII, Anritsu can assure traceability for direct modulators.)

Second, although error is defined, with the Anritsu equipment we are able to assure an error of ±20 mUIpp referenced to a transmitter standardized by the Appendix VIII method. By comparison, the other analyzer assures an accuracy of ±15 mUIpp based on the uncertain traceability of Appendix VII. As shown below, since this includes the ITU-T O.172 modulation frequency error, the true error specification is actually ±R% (up to 20%) ±15 mUI. Moreover, Anritsu are able to assure an repeatability error of ±5mUIpp. The other analyzer does not have such specification.

Third, the MP1590A/B are able to assure as total jitter value which include DJ (Deterministic Jitter) and RJ (Random Jitter). Moreover, MP1590A/B is calibrated by some different transmitters standardized by the Appendix VIII method. The another analyzer only assure burst sinusoidal jitter value.

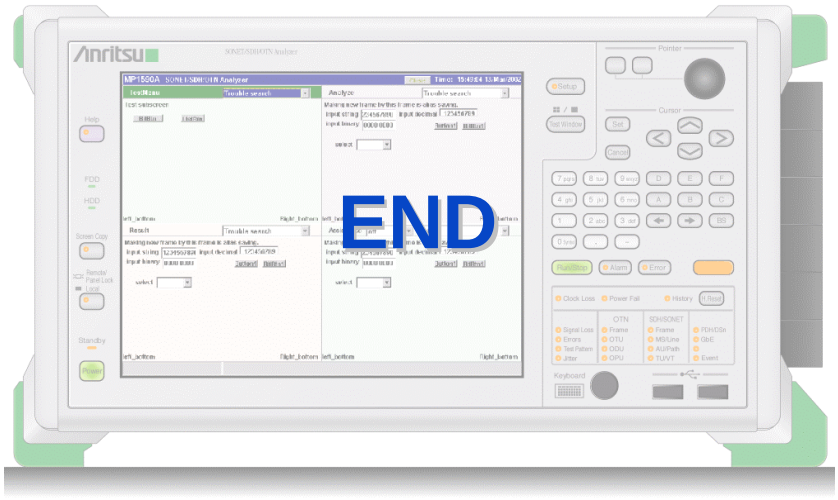
(more)




Fourth, the optical level for assuring accuracy specified by ITU-T O.172 should cover a range of -10 to -12 dBm for all optical interfaces recommended by ITU-T G series Anritsu's MP1590A/B completely satisfies this specification. Additionally, there is hardly any level dependence even outside this level range. The other analyzer does not conform to the range specified by 0.172 and does not conform to the optical interfaces recommended by ITU-T G series.

Fifth, the MP1590A/B supports both wavelengths of 1.31 and 1.55 µm while the other analyzer only supports 1.55 µm.

sixth, for the payload test pattern, Anritsu's MP1590A/B supports the pattern specified by Appendix VII/A.1 of ITU-T O.172, whereas the other analyzer supports PRBS2$^{31}$-1. As explained in the notes on Slide 9, although company A's specification is based on Appendix VII A, since evaluation is performed with a signal from which pattern-dependent jitter has been completely removed and to which burst sine-wave jitter has been added, the guaranteed generation pattern has no meaning.






To offer a more complete understanding of the issues we have discussed here today, we are planning to publish more of these types of reference materials after the next ITU-T meeting.

Thank you.

Newest Information and Further ITU-T O.172 Study Items TECHNICAL NOTE

Anritsu

Specifications are subject to change without notice.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