MX368031A
Device Test Signal
Generation Software
Operation Manual
(For MU368030A)

Third Edition

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Measurement Solutions
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About This Manual

This Operation Manual explains the outline, measurement examples, remote control and other aspects of MX368031A Device Test Signal Generation Software. This software is designed to be installed in the MU368030A Universal Modulation Unit mounted on the MG3680 Series Digital Modulation Signal Generator.

[ ] represents a panel key.

The MG3680 Series Digital Modulation Signal Generator Main Unit Operation Manual and the MU368030A Universal Modulation Unit Operation Manual are available as separate volumes.

Use it in conjunction with this Operation Manual.
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Section 1  Overview

This section describes the outline and product configuration of MX368031A Device Test Signal Generation Software product and standard accessories.

1.1  Product Overview ....................................................... 1-2
1.2  Product Configuration ................................................... 1-3
1.1 Product Overview

The MX368031A Device Test Signal Generation Software (hereinafter, referred to as this software) is system software to be installed in the MU368030A Universal Modulation Unit.

To use this software, a Universal Modulation Unit must be mounted on the MG3680 Series Digital Modulation Signal Generator.

By installing this software and selecting a Device Test Signal, you can generate modulation signals applicable to various communication systems, such as cdma2000 and GSM, without using an external baseband signal source.
1.2 Product Configuration

Standard configuration of the MX368031A is given in the table below. After unpacking, check that all items listed are included. If any items are missing or damaged, please contact Anritsu or one of our agencies.

<table>
<thead>
<tr>
<th>Items</th>
<th>Model name/type</th>
<th>Product name</th>
<th>Quantity</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main unit</td>
<td>MX368031A</td>
<td>Device Test Signal Generation Software</td>
<td>1</td>
<td>Supplied for Compact Flash or ATA Flash card.</td>
</tr>
<tr>
<td>Accessories</td>
<td></td>
<td>PC card adapter</td>
<td>1</td>
<td>Supplied only for Compact Flash card</td>
</tr>
<tr>
<td></td>
<td>W1794AE</td>
<td>Operation Manual</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>
Section 2  Operation Outline

This section describes basic screen contents and how to input auxiliary signals when mounting the MU368030A Universal Modulation Unit installed with this software onto the MG3680 Series.

2.1 Screen Transitions ..................................................... 2-2
2.2 Setting Modulation Parameters ..................................... 2-3
2.3 Inputting External Trigger Signal .................................... 2-5
2.4 Re-installing data of the Universal Modulation Unit .... 2-5
2.1 Screen Transitions

The screens are transited as shown below:

- Press main function key “Digital Mod.”

*Digital modulation setup screen*

- Press main function key “Config.”

*Environment setup screen*
2.2 Setting Modulation Parameters

Pressing \[ \text{Digital Mod} \] causes the indicator LED to go on and the Main screen to appear. Basic parameters related to digital modulation can be set on this screen. This section describes settings for the Main screen.

1. **Baseband**
   Select On/Off for the operation of the Baseband Signal Generator Unit.

2. **I/Q Mod.**
   Select the I/Q signal source for orthogonal modulation. Select “Int” to use the internal signal source for the I/Q signal (using this software) or “Ext” to use the external input.

   Initial value: Int

3. **Pulse Mod.**
   Set the modulation signal on the pulse modulator.

   - Int: Selects the control signal generated by this software.
   - Ext: Uses the external input signal for pulse modulation regardless of modulation settings.
   - Off: No pulse modulation

4. **System**
   Set the system software. Select “DTSG” to start this software.

5. **Pattern**
   Select the Device Test Signal.

   The Device Test Signal is a modulation signal available on this software that is suitable for evaluating devices used in mobile communication system’s base stations or terminals. For Device Test Signals available, refer to “Device Test Signals list” in Section 3.1.
Section 2  Operation Outline

   Int: Outputs an RF signal in synchronization with the internal trigger signal.
   Ext: Outputs an RF signal in synchronization with the trigger signal input to the Start TRIG connector. “Ext” can only be selected when a Device Test Signal applicable to “cdma2000 system Reverse” has been selected. Refer to “Device Test Signals list” in Section 3.1.

[7] Trigger Delay
   It sets the output signal delay for the trigger signal input to the Start TRIG connector. For details, refer to Section 3.2.

[8] Reference Clock
   Int: Generates the reference clock inside MG3681A.
   Ext (TTL): Inputs the reference clock externally (using the Ref. Clock connector). At this time, set this connector to TTL mode.
   Ext (AC): Same as Ext except that the Ref. Clock connector mode should be set to AC (5Vp-p).
2.3 Inputting External Trigger Signal

You can synchronize the signal input from Start TRIG at digital signal input connector No. 2 on the front panel of the main unit with the RF output timing. For details, refer to Section 3.2.

2.4 Re-installing data of the Universal Modulation Unit

It is available to re-install data of the Universal Modulation Unit. First, insert the attached memory card, which has MX368031A saved, into the PC-card slot on the rear panel of the MG3680 series. Then, press [F5] (Wave Data Update) in the Digital Modulation Parameter Setting Screen. Selecting “yes” in the Selecting window starts downloading. It takes approximately six minutes to complete. Do not turn the power off while downloading is in progress.
This section explains the modulation signals applicable to various systems and synchronization with the external trigger input.

3.1 Modulation Signal Details

3.1.1 EDGE System (GSM_EDGE)

3.1.2 GSM System (GSM_GMSK)

3.1.3 PDC System (Pi/4DQPSK_PDC)

3.1.4 IS-136 system (Pi/4DQPSK_IS-136)

3.1.5 PHS system (Pi/4DQPSK_PHS)

3.1.6 cdma2000 system

3.2 External Trigger
### 3.1 Modulation Signal Details

A list of Device Test Signals is given below.

**Table 3-1  Device Test Signals list**

<table>
<thead>
<tr>
<th>No.</th>
<th>Device Test Signals</th>
<th>Applicable systems</th>
<th>Frame-coding</th>
<th>Symbol data</th>
<th>Synchronization with external trigger</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>GSM_EDG</td>
<td>EDGE</td>
<td>Absent</td>
<td>PN9 continuous</td>
<td>Disabled</td>
</tr>
<tr>
<td>1</td>
<td>GSM_GMSK</td>
<td>GSM</td>
<td>Absent</td>
<td>PN9 continuous</td>
<td>Disabled</td>
</tr>
<tr>
<td>2</td>
<td>Pi/4DQPSK_PDC</td>
<td>PDC</td>
<td>Absent</td>
<td>PN9 continuous</td>
<td>Disabled</td>
</tr>
<tr>
<td>3</td>
<td>Pi/4DQPSK_IS-136</td>
<td>IS-136</td>
<td>Absent</td>
<td>PN9 continuous</td>
<td>Disabled</td>
</tr>
<tr>
<td>4</td>
<td>Pi/4DQPSK_PHS</td>
<td>PHS</td>
<td>Absent</td>
<td>PN9 continuous</td>
<td>Disabled</td>
</tr>
<tr>
<td>5</td>
<td>1xRTTrc1_FWD</td>
<td>cdmaOne/2000 1xRTT Reverse</td>
<td>Present</td>
<td>FCH 9.6kbps</td>
<td>Enabled</td>
</tr>
<tr>
<td>6</td>
<td>1xRTTrc3(1)_RVS</td>
<td>cdma2000 1xRTT RC3 Reverse</td>
<td>Present</td>
<td>PICH FCH 9.6kbps</td>
<td>Enabled</td>
</tr>
<tr>
<td>7</td>
<td>1xRTTrc3(2)_RVS</td>
<td>cdma2000 1xRTT RC3 Reverse</td>
<td>Present</td>
<td>PICH FCH 9.6kbps SCH 9.6kbps</td>
<td>Enabled</td>
</tr>
<tr>
<td>8</td>
<td>1xRTTrc3(3)_RVS</td>
<td>cdma2000 1xRTT RC3 Reverse</td>
<td>Present</td>
<td>PICH DCCH 9.6kbps</td>
<td>Enabled</td>
</tr>
<tr>
<td>9</td>
<td>1xRTTrc1-2_FWD</td>
<td>cdmaOne/2000 1xRTT RC1-2 Forward</td>
<td>Spreading only</td>
<td>PICH, SyncCH, PagingCH FCH 19.2kps x 6</td>
<td>Disabled</td>
</tr>
<tr>
<td>10</td>
<td>1xRTTrc3-5_FWD</td>
<td>cdma2000 1xRTT RC3-5 Forward</td>
<td>Spreading only</td>
<td>PICH, SyncCH, PagingCH FCH 38.4kps x 6</td>
<td>Disabled</td>
</tr>
<tr>
<td>11</td>
<td>1xEV-DO_FWD</td>
<td>cdma2000 1xEV-DO Forward 16QAM</td>
<td>Spreading only</td>
<td>Traffic Channel</td>
<td>Disabled</td>
</tr>
<tr>
<td>12</td>
<td>1xEV-DO_RVS</td>
<td>cdma2000 1xEV-DO Reverse</td>
<td>Spreading only</td>
<td>Traffic Channel</td>
<td>Disabled</td>
</tr>
</tbody>
</table>
3.13 Modulation Signal Details

3.1.1 EDGE System (GSM_EDGE)
When this Device Test Signal is selected, the PN9-stage pseudo-random pattern 511-bit circulating data is modulated to $3\pi/8$ offset 8PSK with a Gaussian linear filter and output. The PN9-stage pseudo-random pattern used as data has continuity. The symbol rate is 273.833... ksps.

3.1.2 GSM System (GSM_GMSK)
When this Device Test Signal is selected, the PN9-stage pseudo-random pattern 511-bit circulating data is GMSK-modulated and output. The PN9-stage pseudo-random pattern used as data has continuity. The symbol rate is 273.833... ksps.

3.1.3 PDC System (Pi/4DQPSK_PDC)
When this Device Test Signal is selected, the PN9-stage pseudo-random pattern 511-bit circulating data is modulated to $\pi/4$ DQPSK with a Root Nyquist filter ($\alpha=0.5$) and output. The PN9-stage pseudo-random pattern used as data has continuity. The symbol rate is 21 ksps.

3.1.4 IS-136 system (Pi/4DQPSK_IS-136)
When this Device Test Signal is selected, the PN9-stage pseudo-random pattern 511-bit circulating data is modulated to $\pi/4$ DQPSK with a Root Nyquist filter ($\alpha=0.35$) and output. The PN9-stage pseudo-random pattern used as data has continuity. The symbol rate is 24.3 ksps.

3.1.5 PHS system (Pi/4DQPSK_PHS)
When this Device Test Signal is selected, the PN9-stage pseudo-random pattern 511-bit circulating data is modulated to $\pi/4$ DQPSK with a Root Nyquist filter ($\alpha=0.5$) and output. The PN9-stage pseudo-random pattern used as data has continuity. The symbol rate is 192 ksps.
Section 3  Details of Functions

3.1.6  cdma2000 system

3.1.6.1  1xRTT Reverse RC1 (1xRTTrc1_RVS)

When this Device Test Signal is selected, R-FCH of 1xRTT Reverse RC1 is output. Frame-coding and IQ modulation are carried out according to 3GPP2 C.S0002-0-2. The output signal parameter is given below.

<table>
<thead>
<tr>
<th></th>
<th>Data Rate</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>R-FCH</td>
<td>9.6 kbps</td>
<td>PN9fix</td>
</tr>
</tbody>
</table>

Frame-coding shown in the functional block diagram given below is carried out for the signals output by selecting this Device Test Signal. Frame-coding is carried out for four continuous frames (taking 20 ms to output one frame) and a 4-frame length waveform pattern obtained by frame-coding is repeatedly output. Because the length of the three cycles of I/Q channel PN sequence used for short-code spreading equal the 4-frame length, the short code keeps continuity during outputting the signal. Therefore, this output signal can be used for modulation accuracy measurement or Frame Error Rate (FER) measurement using CRC. No spreading is made using long code.
3.1 Modulation Signal Details

Add Frame Quality Indicator → Add 8 Encoder Tail bits → Convolutional Encoder R=1/3, K=9 → Block Interleaver (576 Symbols)

64-ary Orthogonal Modulator → Signal Point Mapping → Baseband Filter

I Channel PN Sequence → 1/2 PN Chip Delay → Signal Point Mapping → Baseband Filter

Q Channel PN Sequence

Fig. 3-1  Device Test Signal–Block diagram of 1xRTTrc1_RVS

* As shown in the following figure, the PN9 generator is initialized every four frames and the same 4-frame length data is repeatedly output. Therefore, PN9fix keeps continuity within these four frames but not with other sets of four frames.

<table>
<thead>
<tr>
<th>PN9fix</th>
<th>frame 4</th>
<th>frame 1</th>
<th>frame 2</th>
<th>frame 3</th>
<th>frame 4</th>
<th>frame 1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

Short Code cycle (26.66...ms)

Range keeping PN9fix continuities 4 frame (80 ms)

Fig. 3-2  PN9fix data and short code
3.1.6.2 1xRTT Reverse RC3 (1xRTTrc3(1)_RVS)

When this Device Test Signal is selected, 1xRTT Reverse RC3 multiple signal is output. Frame-coding and IQ modulation are carried out according to 3GPP2 C.S0002-0-2. The multiplexed channels are PICH and R-FCH. The parameters for multiplexed channels are given below.

<table>
<thead>
<tr>
<th></th>
<th>Walsh Code</th>
<th>Code Power</th>
<th>Data Rate</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>R-PICH</td>
<td>0</td>
<td>−5.278 dB</td>
<td>N/A</td>
<td>All “0”</td>
</tr>
<tr>
<td>R-FCH</td>
<td>4</td>
<td>−1.528 dB</td>
<td>9.6 kbps</td>
<td>PN9fix*</td>
</tr>
</tbody>
</table>

R-PICH (Reverse Pilot Channel),
R-FCH (Reverse Fundamental Channel)

Frame-coding shown in the functional block diagram given below is carried out for signals output by selecting this Device Test Signal. Frame-coding is carried out for four continuous frames (taking 20 ms to output one frame) and a 4-frame length waveform pattern obtained by frame-coding is repeatedly output. Because the length of the three cycles of I/Q channel PN sequence used for short-code spreading equal the 4-frame length, the short code keeps continuity during outputting the signal. Therefore, this output signal can be used for modulation accuracy measurement or Frame Error Rate (FER) measurement using CRC. No spreading is made using long code.
3.1 Modulation Signal Details

172 bits / 20 ms

Fig. 3-3 Device Test Signal–Block diagram of 1xRTTrc3(1)_RVS (Part1/2)

Fig. 3-4 Device Test Signal–Block diagram of 1xRTTrc3(1)_RVS (Part2/2)

Note:

Binary signal “0” is replaced with 1 and “1” with –1.

* Because the PN9 generator is initialized every four frames, the same 4-frame length data is repeatedly output. Therefore, the PN9 keeps continuity within these four frames but not with other sets of four frames. See Figure “PN9fix data and short code” in Section 3.1.6.1.
3.1.6.3 1xRTT Reverse RC3 (1xRTTrc3(2)_RVS)

When this Device Test Signal is selected, 1xRTT Reverse RC3 multiple signal is output. Frame-coding and IQ modulation are carried out according to 3GPP2 C.S0002-0-2. The multiplexed channels are R-PICH, R-FCH, and R-SCH. The parameters for multiplexed channels are given below.

<table>
<thead>
<tr>
<th></th>
<th>Walsh Code</th>
<th>Code Power</th>
<th>Data Rate</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>R-PICH</td>
<td>0</td>
<td>−7.5912 dB</td>
<td>N/A</td>
<td>All “0”</td>
</tr>
<tr>
<td>R-FCH</td>
<td>4</td>
<td>−3.8412 dB</td>
<td>9.6 kbps</td>
<td>PN9fix</td>
</tr>
<tr>
<td>R-SCH</td>
<td>2</td>
<td>−3.8412 dB</td>
<td>9.6 kbps</td>
<td>PN9fix</td>
</tr>
</tbody>
</table>

Frame-coding shown in the functional block diagram given below is carried out for signals output by selecting this Device Test Signal. Frame-coding is carried out for four continuous frames (taking 20 ms to output one frame) and a 4-frame length waveform pattern obtained by frame-coding is repeatedly output. Because the length of the three cycles of I/Q channel PN sequence used for short-code spreading equal the 4-frame length, the short code keeps continuity during outputting the signal. Therefore, this output signal can be used for modulation accuracy measurement or Frame Error Rate (FER) measurement using CRC. No spreading is made using long code.
3.1 Modulation Signal Details

Fig. 3-5  Device Test Signal–Block diagram of 1xRTTrc3(2)_RVS (Part1/2)

Fig. 3-6  Device Test Signal–Block diagram of 1xRTTrc3(2)_RVS (Part2/2)

Note:
Binary signal “0” is replaced with 1 and “1” with –1.

* Because the PN9 generator is initialized every four frames, the same 4-frame length data is repeatedly output. Therefore, the PN9 keeps continuity within these four frames but not with other sets of four frames. See Figure “PN9fix data and short code” in Section 3.1.6.1.
Section 3  Details of Functions

3.1.6.4  1xRTT Reverse RC3 (1xRTTrc3(3)_RVS)

When this Device Test Signal is selected, 1xRTT Reverse RC3 multiple signal is output. Frame-coding and IQ modulation are carried out according to 3GPP2 C.S0002-0-2. The multiplexed channels are R-PICH and R-DCCH. The parameters for multiplexed channels are given below.

<table>
<thead>
<tr>
<th></th>
<th>Walsh Code</th>
<th>Code Power</th>
<th>Data Rate</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>R-PICH</td>
<td>0</td>
<td>-5.278 dB</td>
<td>N/A</td>
<td>All “0”</td>
</tr>
<tr>
<td>R-DCCH</td>
<td>8</td>
<td>-1.528 dB</td>
<td>9.6 kbps</td>
<td>PN9fix*</td>
</tr>
</tbody>
</table>

R-PICH (Reverse Pilot Channel), R-DCCH (Reverse Dedicated Channel)

Frame-coding shown in the functional block diagram given below is carried out for signals output by selecting this Device Test Signal. Frame-coding is carried out for four continuous frames (taking 20 ms to output one frame) and a 4-frame length waveform pattern obtained by frame-coding is repeatedly output. Because the length of the three cycles of I/Q channel PN sequence used for short-code spreading equal the 4-frame length, the short code keeps continuity during outputting the signal. Therefore, this output signal can be used for modulation accuracy measurement or Frame Error Rate (FER) measurement using CRC. No spreading is made using long code.
3.1 Modulation Signal Details

Add Frame Quality Indicator
Add 8 Encoder Tail bits
Convolutional Encoder R=1/4, K=9
Symbol Repetition (2x Factor)
Block Interleaver (1536 Symbols)

Reverse Dedicated Control Channel Bits (PN9fix*)
172 bits/ 20 ms

Add Frame Quality Indicator
Add 8 Encoder Tail bits
Convolutional Encoder R=1/4, K=9
Symbol Repetition (2x Factor)
Block Interleaver (1536 Symbols)

Reverse Traffic Channel Bits (PN9fix*)
172 bits/ 20 ms

Fig. 3-7 Device Test Signal–Block diagram of 1xRTTrc3(3)_RVS (Part1/2)

Reverse Pilot Channel
All “1”

Relative Gain

Reverse Dedicated Control Channel
Walsh Cover (++++++++--------)

Relative Gain

Reverse Fundamental Channel
Walsh Cover (++++-----+++++---)

Decimator by Factor of 2

Baseband Filter

I

Q

Note:
Binary signal “0” is replaced with 1 and “1” with –1.

Fig. 3-8 Device Test Signal–Block diagram of 1xRTTrc3(3)_RVS (Part2/2)

* Because the PN9 generator is initialized every four frames and the same 4-frame length data is repeatedly output. Therefore, the PN9 keeps continuity within these four frames but not with other sets of four frames. See Figure “PN9fix data and short code” in Section 3.1.6.1.
3.1.6.5 1xRTT Forward RC1 (1xRTTrc1-2_FWD)

When this Device Test Signal is selected, 1xRTT Forward RC1 multiple signal is output according to 3GPP2 C.S0002-0-2. The multiplexed channels are F-PICH, F-SyncCH, PagingCH, and F-FCHx6 (data sequences obtained by spreading six symbol data sequences with Walsh code 8, 9, ..., and 13). The parameters for multiplexed channels are given below.

<table>
<thead>
<tr>
<th></th>
<th>Walsh Code</th>
<th>Code Power</th>
<th>Symbol Rate</th>
<th>Symbol Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>F-PICH</td>
<td>0</td>
<td>−7.0 dB</td>
<td>N/A</td>
<td>All “0”</td>
</tr>
<tr>
<td>F-SyncCH</td>
<td>32</td>
<td>−13.3 dB</td>
<td>4.8 ksps</td>
<td>PN9fix*</td>
</tr>
<tr>
<td>PagingCH</td>
<td>1</td>
<td>−7.3 dB</td>
<td>19.2 ksps</td>
<td>PN9fix*</td>
</tr>
<tr>
<td>F-FCH x 6</td>
<td>8 to 13</td>
<td>−10.3 dB</td>
<td>19.2 kbps</td>
<td>PN9fix*</td>
</tr>
</tbody>
</table>

F-PICH (Forward Pilot Channel), F-SyncCH (Forward Sync Channel), PagingCH (Paging Channel), F-FCH (Forward Fundamental Channel)

Processing shown in the following functional block diagram is carried out for the signals output by selecting this Device Test Signal. This functional block diagram shows functional blocks for individual channels and symbol data for each channel is added after being processed as shown in this functional block diagram. This processing is carried out for four continuous frames (taking 20 ms to output one frame) and a 4-frame length waveform pattern obtained as a result of this processing is repeatedly output. Because the length of the three cycles of I/Q channel PN sequence used for short-code spreading equal the 4-frame length, the short code keeps continuity during outputting the signal. Therefore, this output signal can be used for modulation accuracy measurement. Scrambling with long code and PCB Mux are not carried out.
**3.1 Modulation Signal Details**

![Diagram of modulation signal details]

**Note:**

Binary signal “0” is replaced with 1 and “1” with –1.

Fig. 3-9  Device Test Signal–Block diagram of 1xRTTrc1-2_FWD

* Because the PN9 generator is initialized every four frames and the same 4-frame length data is repeatedly output. Therefore, the PN9 keeps continuity within these four frames but not with other sets of four frames. See Figure “PN9fix data and short code” in Section 3.1.6.1.
### 3.1.6.6 1xRTT Forward RC3 (1xRTTrc3-5_FWD)

When this Device Test Signal is selected, 1xRTT Forward RC3 multiple signal is output according to 3GPP2 C.S0002-0-2. The multiplexed channels are F-PICH, F-SyncCH, PagingCH, and F-FCHx6 (six data sequences obtained by spreading six symbol data sequences with Walsh code 8, 9, ..., and 13). The parameters for multiplexed channels are given below.

<table>
<thead>
<tr>
<th></th>
<th>Walsh Code</th>
<th>Code Power</th>
<th>Symbol Rate</th>
<th>Symbol Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>F-PICH</td>
<td>0</td>
<td>–7.0 dB</td>
<td>N/A</td>
<td>All “0”</td>
</tr>
<tr>
<td>F-SyncCH</td>
<td>32</td>
<td>–13.3 dB</td>
<td>4.8 kbps</td>
<td>PN9fix*</td>
</tr>
<tr>
<td>PagingCH</td>
<td>1</td>
<td>–7.3 dB</td>
<td>19.2 kbps</td>
<td>PN9fix*</td>
</tr>
<tr>
<td>F-FCH x 6</td>
<td>8 to 13</td>
<td>10.3 dB</td>
<td>38.4 kbps</td>
<td>PN9fix*</td>
</tr>
</tbody>
</table>

F-PICH (Forward Pilot Channel), F-SyncCH (Forward Sync Channel), PagingCH (Paging Channel), F-FCH (Forward Fundamental Channel)

Processing shown in the functional block diagram given below is carried out for the signals output by selecting this Device Test Signal. This functional block diagram shows functional blocks for individual channels and symbol data for each channel is added after being processed as shown in this functional block diagram. This processing is carried out for four continuous frames (taking 20 ms to output one frame) and a 4-frame length waveform pattern obtained as a result of this processing is repeatedly output. Because the length of the three cycles of I/Q channel PN sequence used for short-code spreading equal the 4-frame length, the short code keeps continuity during outputting the signal. Therefore, this output signal can be used for modulation accuracy measurement. Scrambling with long code and PCB Mux are not carried out.
Note: Binary signal “0” is replaced with 1 and “1” with –1.

* Because the PN9 generator is initialized every four frames and the same 4-frame length data is repeatedly output. Therefore, the PN9 keeps continuity within these four frames but not with other sets of four frames. See Figure “PN9fix data and short code” in Section 3.1.6.1.
3.1.6.7 1xEV-DO Forward (1xEV-DO_FWD)

When this Device Test Signal is selected, 1xEV-DO Forward multiple signal is output according to 3GPP2 C.S0024. The multiplexed channels are given in the table below. For F-TCH, no channel coding is carried out; PN15fix* data is directly modulated with 16 QAM.

<table>
<thead>
<tr>
<th>MAC index</th>
<th>Power</th>
<th>Data</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preamble</td>
<td>5</td>
<td>0.0 dB</td>
<td>All “0”</td>
</tr>
<tr>
<td>Pilot Channel</td>
<td>N/A</td>
<td>0.0 dB</td>
<td>All “0”</td>
</tr>
<tr>
<td>MAC Channel RPC</td>
<td>5</td>
<td>−3.0 dB</td>
<td>All “0”</td>
</tr>
<tr>
<td>RA</td>
<td>N/A</td>
<td>−3.0 dB</td>
<td>All “0”</td>
</tr>
<tr>
<td>Traffic Channel</td>
<td>N/A</td>
<td>0.0 dB</td>
<td>PN15fix* 16 QAM</td>
</tr>
</tbody>
</table>

The block diagrams for IQ mapping and time division multiplex (TDM) follow.
### 3.1 Modulation Signal Details

<table>
<thead>
<tr>
<th></th>
<th>Preamble</th>
<th>Data</th>
<th>MAC</th>
<th>Pilot</th>
<th>MAC</th>
<th>Data</th>
<th>MAC</th>
<th>Pilot</th>
<th>MAC</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>64 chip</td>
<td>336 chip</td>
<td>64 chip</td>
<td>96 chip</td>
<td>64 chip</td>
<td>800 chip</td>
<td>64 chip</td>
<td>96 chip</td>
<td>64 chip</td>
<td>400 chip</td>
</tr>
</tbody>
</table>

1 slot = 1.67 ms

* Because the PN15 generator is initialized every three frames, the same 3-frame length data is repeatedly output. Therefore, the PN15 keeps continuity within these three frames but not with other sets of three frames.
3.1.6.8 1xEV-DO Reverse (1xEV-DO_RVS)

When this Device Test Signal is selected, 1xEV-DO Reverse multiple signal is output according to 3GPP2 C.S0024. The multiplexed channels are given in the table below.

<table>
<thead>
<tr>
<th>Channel</th>
<th>Walsh Code</th>
<th>Power</th>
<th>Data</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pilot Channel</td>
<td>0</td>
<td>-18.68 dB</td>
<td>All “0”</td>
<td></td>
</tr>
<tr>
<td>RRI Channel</td>
<td>0</td>
<td>-18.68 dB</td>
<td>RRI Symbol = “101”</td>
<td></td>
</tr>
<tr>
<td>DRC Channel</td>
<td>0 (8-ary Walsh Func.) &amp; 8</td>
<td>-18.68 dB</td>
<td>DRC Value = “0x01”</td>
<td></td>
</tr>
<tr>
<td>ACK Channel</td>
<td>4</td>
<td>-18.68 dB</td>
<td>All “0”</td>
<td></td>
</tr>
<tr>
<td>Reverse Data Channel</td>
<td>2</td>
<td>-0.18 dB</td>
<td>PN9fix*</td>
<td>8192 Symbol/slot</td>
</tr>
</tbody>
</table>

Processing shown in the functional block diagram given below is carried out for signals output by selecting this Device Test Signal. For reverse data channels, no channel coding is carried out; PN9fix* data is directly spreaded. The DRC and ACK channels are active at all time slots. This processing is carried out for three continuous frames (taking 26.66... ms to output one frame) and a 3-frame length waveform pattern obtained as a result of this processing is repeatedly output.

As the long code mask, 0x3FFFFFFF is used for MI and 0x00000000001 for MQ.

Fig. 3-14  Device Test Signal–Block diagram of 1xEV-DO_RVS (Part 1/2)
3.1 Modulation Signal Details

Fig. 3-15 Device Test Signal–Block diagram of 1xEV-DO_RVS (Part2/2)

* Because the PN9 generator is initialized every three frames, the same 3-frame length data is repeatedly output. Therefore, the PN9 keeps continuity within these three frames but not with other sets of three frames.
3.2 External Trigger

The figure given below shows the RF signal output timing for inputting a trigger signal to the Start TRIG input (front panel) for synchronizing with other devices. This external trigger operation can be set only when a Device Test Signal applicable to cdma2000 1xRTT Reverse has been selected. The RF signal is output with a delay of 9/8 chip (1 chip = 1/1228.8 ms) plus trigger delay set value from the trigger rise edge. Because the RF output timing includes an error of ±2/16 chip, the actual delay from Start TRIG input is as shown in the expression given below.

\[
\text{(Delay from Start TRIG input)} = 9/8 \text{ chip} + (\text{Trigger Delay}) \pm (\text{Delay error})
\]

START TRIG input is TTL.

![Fig. 3-16 External trigger operation](image-url)
Section 4  Measurement

This section explains transmission amplifier evaluation measurement, as an example of measurement when mounting the MU368030A Universal Modulation Unit installed with the MX368031A Device Test Signal Generation Software onto the MG3681A Digital Modulation Signal Generator.

4.1 Evaluation Measurement of the Transmission Amplifier's Adjacent Channel Leakage Power Ratio ................. 4-2
4.1 Evaluation Measurement of the Transmission Amplifier's Adjacent Channel Leakage Power Ratio

This section explains evaluation measurement of the Adjacent Channel Leakage Power Ratio on the Transmission Amplifier.

**Setup**

![Diagram showing the setup for measurement.

**Measurement procedure**

1. Set the MG3681A frequency to the one used for the test.
2. Set the MG3681A output level to one suitable for the DUT and Impedance-matching coupling circuit.
3. Set the Device Test Signal to be measured in the MG3681A Pattern.
4. Use a spectrum analyzer to evaluate the adjacent channel leakage power ratio.
Section 5  Remote Control

This section provides a list of GPIB device messages categorized by function and also describes in detail these device messages arranged in alphabetical order, when the MU368030A Universal Modulation Unit installed with the MX368031A Device Test Signal Generation Software is mounted in the MG3681A Digital Modulation Signal Generator.

For further description of remote control, refer to Section 4 “Remote Control” in the MG3681A Main Unit Operation Manual.

5.1  List of Device Messages Categorized by Function .... 5-2
5.2  Details of Device Messages in Alphabetical Order .... 5-4
5.1 List of Device Messages Categorized by Function

Command and query messages
The header portion of the command message is a reserved word represented by capital alphanumeric characters. The end of a query message header contains an interrogation mark (?). In the argument part of command and query messages, multiple arguments can be separated with a separator (\(\cdot\)). Arguments are described below.

[1]  Capitals : Reserved word
[2]  Numerals : Reserved word
[3]  Small letters in argument part:
  \(f\) (Frequency) : Numeric data (NR1, NR2, NR3)
  Suffix code : GHZ, GZ, MHz, MZ, kHz, KZ, HZ
  When the unit is omitted, HZ is assumed.
  \(l\) (level) (relative value) : Numeric data (NR1, NR2, NR3 format)
  Suffix code : dB
  When the unit is omitted, dB is assumed.
  \(n\) (integer without unit) : Numeric data (NR1 format)
  \(r\) (real number without unit) : Numeric data (NR2 format)
  \(h\) (hexadecimal number without unit) : Numeric data (hexadecimal number)
  \(s\) (character string) : Alphanumeric characters enclosed in double quotation marks (" ") or single quotation marks (’‘).
# List of Device Messages Categorized by Function

Device messages list

## <Common>

<table>
<thead>
<tr>
<th>Items</th>
<th>Command messages</th>
<th>Query messages</th>
<th>Response messages</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Control items</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I/Q Source Internal</td>
<td>MODE INT</td>
<td>MODE?</td>
<td>MODE INT</td>
</tr>
<tr>
<td></td>
<td>IQSRC INT</td>
<td>IQSRC?</td>
<td>IQSRC INT</td>
</tr>
<tr>
<td>I/Q Source External</td>
<td>MODE EXT</td>
<td>MODE?</td>
<td>MODE EXT</td>
</tr>
<tr>
<td></td>
<td>IQSRC EXT</td>
<td>IQSRC?</td>
<td>IQSRC EXT</td>
</tr>
<tr>
<td>I/Q Source OFF</td>
<td>MODE OFF</td>
<td>MODE?</td>
<td>MODE OFF</td>
</tr>
<tr>
<td></td>
<td>IQSRC OFF</td>
<td>IQSRC?</td>
<td>IQSRC OFF</td>
</tr>
<tr>
<td>System DTSG</td>
<td>SYS DTSG</td>
<td>SYS?</td>
<td>SYS DTSG</td>
</tr>
<tr>
<td>Baseband ON</td>
<td>BASEBAND ON</td>
<td>BASEBAND?</td>
<td>BASEBAND ON</td>
</tr>
<tr>
<td>Baseband OFF</td>
<td>BASEBAND OFF</td>
<td>BASEBAND?</td>
<td>BASEBAND OFF</td>
</tr>
<tr>
<td>PM ON</td>
<td>PMO ON</td>
<td>PMO?</td>
<td>PMO ON</td>
</tr>
<tr>
<td>PM OFF</td>
<td>PMO OFF</td>
<td>PMO?</td>
<td>PMO OFF</td>
</tr>
</tbody>
</table>

## <Modulation>

<table>
<thead>
<tr>
<th>Items</th>
<th>Command messages</th>
<th>Query messages</th>
<th>Response messages</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Control items</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pattern</td>
<td>PAT n</td>
<td>PAT?</td>
<td>PAT n</td>
</tr>
<tr>
<td></td>
<td>n : 0 to 15</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reference Clock Source</td>
<td>REFCLK INT</td>
<td>REFCLK?</td>
<td>REFCLK INT</td>
</tr>
<tr>
<td>Reference Clock Source</td>
<td>REFCLK EXT</td>
<td>REFCLK?</td>
<td>REFCLK EXT</td>
</tr>
<tr>
<td>Reference Clock Source</td>
<td>REFCLK EXT2</td>
<td>REFCLK?</td>
<td>REFCLK EXT2</td>
</tr>
<tr>
<td>Start Trigger Delay</td>
<td>STDLY n</td>
<td>STDLY?</td>
<td>STDLY n</td>
</tr>
<tr>
<td></td>
<td>n : 0 to 16777215</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Start Trigger Source</td>
<td>STGS INT</td>
<td>STGS?</td>
<td>STGS INT</td>
</tr>
<tr>
<td>Start Trigger Source</td>
<td>STGS EXT</td>
<td>STGS?</td>
<td>STGS EXT</td>
</tr>
</tbody>
</table>
5.2 Details of Device Messages in Alphabetical Order

<Examples>

FREQ

<table>
<thead>
<tr>
<th>Function</th>
<th>Sets the frequency.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Command message</td>
<td>FREQ a</td>
</tr>
<tr>
<td>Value of a</td>
<td>–2.99975 to 3 GHZ</td>
</tr>
<tr>
<td></td>
<td>–2999.75 to 3000 MHZ</td>
</tr>
<tr>
<td></td>
<td>–2999750 to 3000000 KHZ</td>
</tr>
<tr>
<td></td>
<td>–2999750000.00 to 3000000000 HZ</td>
</tr>
<tr>
<td>Query message</td>
<td>FREQ?</td>
</tr>
<tr>
<td>Response message</td>
<td>FREQ a</td>
</tr>
<tr>
<td>Example</td>
<td>FREQ 123MHZ</td>
</tr>
</tbody>
</table>
### BASEBAND

**Baseband (On/Off)**

**Function**
Sets baseband On/Off.

**Command message**
BASEBAND a

**Value of a**
- **ON** : Baseband On
- **OFF** : Baseband Off

**Query message**
BASEBAND?

**Response message**
BASEBAND a

**Example**
BASEBAND ON
I

IQSRC

I/Q Source

Function

Selects the modulation source for digital modulation.

Command message

IQSRC a

Value of a

INT : Internal (internal modulation unit)

EXT : External (external input)

OFF : I/Q modulation stop (only pulse modulation enabled)

Query message

IQSRC?

Response message

IQSRC a

Example

IQSRC INT
PAT

Pattern

Function
Selects the Device Test Signal.

Command message
PAT n

Value of n
0 to 15

Query message
PAT?

Response message
PAT n,s

Restrictions
For test signals associated with the value of “n,” see “Device Test Signals list ” in Section 3.1. Note that there may be some cases where there are fewer signals.

Example
PAT 2

PMO

Pulse-Modulation

Function
Sets On/Off and Internal/External of pulse modulation.

Command message
PMO a

Value of a
INT : Internal (generates with modulation unit)
EXT : External (uses external device)
OFF : Off (signals always exist)

Query message
PMO?

Response message
PMO a

Example
PMO ON
REFCLK

Reference Clock Source

**Function**
Selects the baseband reference timing (external or internal).

**Command message**
REFCLK a

**Value of a**
- INT : Internal selection
- EXT : External (TTL) selection
- EXT2 : External 2 (AC: 5Vp-p) selection

**Query message**
REFCLK?

**Response message**
REFCLK a

**Example**
REFCLK INT
**STDLY**

Start Trigger delay amount

**Function**
Sets the RF signal output timing.

**Command message**
STDLY n

**Value of n**
0 to 16777215

**Query message**
STDLY?

**Response message**
STDLY n

**Restrictions**
Only waveform data (such as 1xRTT Reverse) also allowing selection of external trigger can be set.

**Example**
STDLY 10

---

**STGS**

Start Trigger Source

**Function**
Sets On/Off and Internal/External of pulse modulation.

**Command message**
STGS a

**Value of a**
INT : Internal (generates with modulation unit)
EXT : External (uses external device)
OFF : Off (signals always exist)

**Query message**
STGS?

**Response message**
STGS a

**Restrictions**
Only waveform data (such as 1xRTT Reverse) also allowing selection of external trigger can be set.

**Example**
STGS INT
SYS

System

**Function**
Sets the digital modulation system.

**Command message**
SYS a

**Value of a**
- **NONE**: Digital modulation system not mounted.
- **DTSG**: Device Test Signal Generation Software

**Query message**
SYS?

**Response message**
SYS a

**Example**
SYS DTSG
Section 6  Performance Test

This section describes the performance test when MX368031A Device Test Signal Generation Software is installed on the MU368030A Universal Modulation Unit, which is mounted on the MG3681A Digital Modulation Signal Generator. In order to implement the performance test as preventive maintenance, information such as required measuring instrument, setup procedure, and test procedures are included.

6.1 Performance Test
   6.1.1 About the performance test
   6.1.2 Instruments required for the performance test

6.2 Modulation Accuracy of RF Output

6.3 Waveform Quality of RF Output

6.4 Output Level Accuracy
6.1 Performance Test

6.1.1 About the performance test

The performance test explained here is implemented as part of preventive maintenance against performance deterioration of the instrument. You are advised to implement a performance test whenever necessary, for examples, upon acceptance inspection, regular inspection, and post-repair performance confirmation. If you find an item, which does not meet specifications during a performance test, please contact Anritsu Corporation or one of our dealers.

The performance test consists of the following items:

- Modulation accuracy of RF output
- Waveform quality of RF output
- Output level accuracy

Be sure to implement periodically the performance test for items considered important as preventive maintenance. We recommend that the performance inspection is executed regularly once or twice a year.

In addition, it is recommended that the results are summarized using the Appendix C “Performance Test Record.”

---

**CAUTION**

Unless otherwise specified, be sure to warm up the device to be tested and the measuring instruments for at least 30 minutes or over until they become stable, before implementing the performance test. To ensure the maximum measurement accuracy, we recommend that you observe the above as well as keeping the room temperature, limiting AC power voltage fluctuations to a minimum, and making sure that there are no problems with noise, vibration, dust, humidity or other environmental factors.
### 6.1.2 Instruments required for the performance test

A list of instruments required for the performance test is shown below.

<table>
<thead>
<tr>
<th>Test Item</th>
<th>Recommended Instrument</th>
<th>Anritsu Model Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>Modulation accuracy of RF output</td>
<td>Transmitter Tester (with GSM, π/4DQPSK analysis software)</td>
<td>MS8608A +MX860802A +MX860805A</td>
</tr>
<tr>
<td>Waveform quality of RF output</td>
<td>Transmitter Tester (with cdma analysis software)</td>
<td>MS8608A +MX860803A</td>
</tr>
<tr>
<td>Output level accuracy</td>
<td>Power meter</td>
<td>ML4803A</td>
</tr>
<tr>
<td></td>
<td>Power sensor</td>
<td>MA4601A</td>
</tr>
</tbody>
</table>
6.2 Modulation Accuracy of RF Output

Test specifications

- EVM \( \leq 1.8\% \text{ (rms)} \)
- PDC, PHS: \( \leq 2.0\% \text{ (rms)} \)
- EDGE: \( \leq 2.5\% \text{ (rms)} \)
- phase error
  - GSM: \( \leq 1^\circ\text{(rms)} \leq 3^\circ\text{(peak)} \)

Conditions

- RF output level: +5 dBm
- Carrier frequency: 100 to 2100 Hz
- Level continuous mode: Off

Test procedures

1. Set the modulation parameter of MG3681A as shown below:
   - Preset: –
   - Baseband: On
   - I/Q Mod: Int
   - Digital Modulation: On
   - System: DTSG
   - Pattern: Device Test Signal to be measured

2. Set the frequency of MG3681A for the test frequency.
3. Set +5dBm for the output level of MG3681A
4. Set MS8608A for the setting of the modulation accuracy measurement. (Refer to the operation manual of MS8608A for details of the setting.)
5. Measure the modulation accuracy of RF modulation signal using MS8608A.
6.3 Waveform Quality of RF Output

Test specifications
CDMA2000: \( p \geq 0.997 \)

Conditions
- RF output level: – 3 dBm
- Carrier frequency: 100 to 2300 MHz
- Level continuous mode: Off

Test procedure

1. Set the modulation parameter of MG3681A as shown below:
   - Preset: –
   - Baseband: On
   - I/Q Mod: Int
   - Digital Modulation: On
   - System: DTSG
   - Pattern: Device Test Signal to be measured

2. Set the frequency of MG3681A for the test frequency.

3. Set -3 dBm for the output level of MG3681A.

4. Set the MS8608A for the setting of the waveform quality measurement. (Refer to the operation manual of MS8608A for details of the setting.)

5. Measure the waveform quality of RF output signal by using MS8608A.
6.4 Output Level Accuracy

Test specifications

Difference between the output levels in the CW mode and the followings.

- PDC/PHS/IS-136: ±1.0 dB
- GSM/EDGE: ±1.0 dB
- CDMA2000 “RC1RVS/RC3RVS(1)“: ±1.0 dB
- CDMA 2000 (others): ±1.2 dB

Conditions

- RF output level
  - PDC/PHS/IS-136: ≤ +5 dBm
  - GSM/EDGE: ≤ +5 dBm
  - CDMA2000 “RC1RVS/RC3RVS(1)“: ≤ −3 dBm
  - CDMA2000 (Others): ≤ −3 dBm

- Carrier frequency: 10 to 3000 MHz
- Level continuous mode: Off
6.4 Output Level Accuracy

Test procedure

MG3681A
+ MU368030A (Universal Modulation Unit)
+ MX368031A (Device Test Signal Generation Software)

[1] Set the modulation parameter of MG3681A as shown below:

- Preset : –
- Baseband : On
- I/Q Mod : Int
- Digital Modulation : On
- System : DTSG
- Pattern : Device Test Signal to be measured


[3] Execute the zero calibration and sensor sensitivity calibration of power meter

[4] Set the output level of MG3681A as desired. (Measurable low-level in the above system depends on the sensitivity of the power meter.)

[5] Set the calibration factor of power meter.

[6] Set the Digital Modulation of MG3681A to OFF, and measure the output level of MG3681A when CW is set.

[7] Set the Digital Modulation of MG3681A to ON, and measure the output level of MG3681A when modulation is in progress.

[8] Confirm whether the difference between the measured values obtained from step 6 and 7 is within the specifications.
<table>
<thead>
<tr>
<th>Appendix</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Appendix A</td>
<td>Specifications</td>
<td>A-1</td>
</tr>
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<td>Appendix B</td>
<td>List of Initial Value</td>
<td>B-1</td>
</tr>
<tr>
<td>Appendix C</td>
<td>Performance Test Record</td>
<td>C-1</td>
</tr>
</tbody>
</table>
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When installed in MU368030A mounted on MG3680 series

<table>
<thead>
<tr>
<th>Item</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Corresponding System</strong></td>
<td>EDGE, GSM, PDC, PHS, IS-136 CDMA2000 (RC1 RVS, RC3 RVS, RC1-2 FWD, RC3-5 FWD, 1xEV-DO FWD, 1xEV-DO RVS)</td>
</tr>
<tr>
<td><strong>Baseband Filter</strong></td>
<td>EDGE : Gauss Liner GSM : Gauss BbT=0.3 PDC, PHS : Root Nyquist α =0.5 IS-136 : Root Nyquist α=0.35 CDMA2000 RC1 RVS, RC3 RVS, 1xEV-DO RVS : IS-95spec CDMA2000 RC1-2 FWD, RC3-5 FWD, 1xEV-DO FWD : IS-95spec+EQ</td>
</tr>
<tr>
<td><strong>Modulation Data</strong></td>
<td>EDGE, GSM, PDC, PHS, IS-136 : PN9 continuous CDMA2000 : Depends on each channel configuration</td>
</tr>
<tr>
<td><strong>Corresponding Channel Configuration</strong></td>
<td>CDMA2000 RVS RC1</td>
</tr>
<tr>
<td></td>
<td>CDMA2000 RVS RC3(1)</td>
</tr>
</tbody>
</table>
### Appendix A Specifications

<table>
<thead>
<tr>
<th>Item</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Corresponding Channel Configuration</strong></td>
<td></td>
</tr>
</tbody>
</table>
| **CDMA2000 RVS RC3(3)** | Corresponding specifications 3GPP2 C.S0002-02  
Channel configuration  
• Pilot Channel: Code Power – 5.278 dB  
• Dedicated Control Channel: Data Rate=9600 bps, Walsh Cover 8, Code Power – 1.528 dB  
Long Code Mask = 0  
Does not comply with MAC Layer. |
| **CDMA2000 FWD RC1-2** | Corresponding specifications 3GPP2 C.S0002-02  
Channel configurations  
• Pilot Channel: 5.278 dB  
• Sync Channel: BPSK, Symbol Rate=4.8 kbps, Walsh Cover 32, Code Power – 13.3 dB  
• Paging Channel: BPSK, Symbol Rate=19.2 kbps, Walsh Cover 1, Code Power – 7.3 dB  
• Traffic Channel: BPSK, Symbol Rate=19.2 kbps, Walsh Cover 8-13, Code Power – 10.3 dB  
Long Code Mask = 0  
Does not comply with TPC MUX.  
Does not comply with Channel Coding |
| **CDMA2000 FWD RC3-5** | Corresponding specifications 3GPP2 C.S0002-02  
Channel configuration  
• Pilot Channel: 7.0 dB  
• Sync Channel: BPSK, Symbol Rate=4.8 kbps, Walsh Cover 32, Code Power – 13.3 dB  
• Paging Channel: BPSK, Symbol Rate=19.2 kbps, Walsh Cover 1, Code Power – 7.3 dB  
• Traffic Channel: QPSK, Symbol Rate=38.4 kbps, Walsh Cover 8-13, Code Power – 10.3 dB  
Long Code Mask = 0  
Does not comply with TPC MUX.  
Does not comply with Channel Coding |
| **1xEV-DO FWD** | Corresponding specifications 3GPP2 C.S0024 Version 2.0  
Channel configuration:  
• Priamble: MACindex=5  
• Pilot Channel:  
• MAC Channel:  
  • RPC bit: All"0", MAC index=5, Power = – 3 dB  
  • RA bit: All"0", Power = – 3 dB  
• Traffic Channel: 16QAM, 1536 symbol / slot (Data is PN15)  
Does not comply with Channel Coding, and modulates 6144-bit / slot of PN15 directly by 16QAM modulation.  
Time-Division Multiplexing: 1-Slot Case |
### Appendix A Specifications

<table>
<thead>
<tr>
<th>Item</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Corresponding Channel Configuration</strong></td>
<td></td>
</tr>
<tr>
<td>1xEV-DO RVS</td>
<td></td>
</tr>
<tr>
<td>Corresponding specifications</td>
<td>3GPP2 C.S0024 Version 2.0</td>
</tr>
<tr>
<td>Channel configuration</td>
<td></td>
</tr>
<tr>
<td>• Pilot Channel</td>
<td>:Code Power = – 18.68 dB</td>
</tr>
<tr>
<td>• MAC Channel</td>
<td>:RRI Symbol “101”, Code Power = – 18.68 dB</td>
</tr>
<tr>
<td></td>
<td>DRC Symbols “01(h)”, All slots are Active, Code Power = – 18.68 dB</td>
</tr>
<tr>
<td></td>
<td>DRC Cover Symbols “0”</td>
</tr>
<tr>
<td>• ACK Channel</td>
<td>:All”0” All slots are Active, Code Power = – 18.68 dB</td>
</tr>
<tr>
<td>• Data Channel</td>
<td>:Symbol Rate=307.2 kbps, Code Power = – 0.18 dB</td>
</tr>
<tr>
<td></td>
<td>Does not comply with Channel Coding</td>
</tr>
<tr>
<td></td>
<td>Long Code Mask :MI=3FFFFFFF(h), MQ=0000000001(h)</td>
</tr>
<tr>
<td><strong>Carrier Frequency Range</strong></td>
<td>10 to 3000 MHz</td>
</tr>
<tr>
<td><strong>Output Level Accuracy</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td>For output level when CW is set:</td>
</tr>
<tr>
<td></td>
<td>• PDC, PHS, IS-136 : ± 1.0 dB (at ≤ +5 dBm)</td>
</tr>
<tr>
<td></td>
<td>• GSM, EDGE : ± 1.0 dB (at ≤ +5 dBm)</td>
</tr>
<tr>
<td></td>
<td>• CDMA2000 RC1 RVS, RC3 RVS(1) : ± 1.0 dB (at ≤ − 3 dBm)</td>
</tr>
<tr>
<td></td>
<td>• CDMA2000 RC3 RVS(2,3) RC1-2 FWD, RC3-5 FWD, 1xEV-DO : ± 1.2 dB (at ≤ − 3 dBm)</td>
</tr>
<tr>
<td><strong>Modulation Accuracy</strong></td>
<td>When +5 dBm is output in the range from 100 to 2100 MHz</td>
</tr>
<tr>
<td></td>
<td>• PDC, PHS : 1.8%(rms)</td>
</tr>
<tr>
<td></td>
<td>• IS-136 : 2.0%(rms)</td>
</tr>
<tr>
<td></td>
<td>• EDGE : 2.5%(rms)</td>
</tr>
<tr>
<td></td>
<td>Phase Error</td>
</tr>
<tr>
<td></td>
<td>• GSM : 1°(rms), 3° (peak) (at 18 to 35°C)</td>
</tr>
<tr>
<td><strong>Waveform Quality</strong></td>
<td>When –3 dBm is output in the range from 100 to 2300 MHz, and from 18 to 35°C. CDMA2000(1xEV-DO excluded.) : ρ ≥ 0.997</td>
</tr>
</tbody>
</table>
## Specifications

<table>
<thead>
<tr>
<th>Item</th>
<th>RF output level: +5 dBm, detection mode: at POSITIVE PEAK</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>• PDC (PLL MODE: NORMAL, 100 to 1600 MHz, RBW 1 kHz, VBW 3 kHz)</td>
</tr>
<tr>
<td></td>
<td>≤ – 63 dBC (50 kHz offset, 21 kHz BW)</td>
</tr>
<tr>
<td></td>
<td>≤ – 67 dBC (100 kHz offset, 21 kHz BW)</td>
</tr>
<tr>
<td></td>
<td>• PHS (PLL MODE: NARROW, 100 to 1000 MHz, 1750 to 2500 MHz, RBW 3 kHz, VBW 10 kHz)</td>
</tr>
<tr>
<td></td>
<td>≤ – 66 dBC (600 kHz offset, 192 kHz BW)</td>
</tr>
<tr>
<td></td>
<td>≤ – 69 dBC (900 kHz offset, 192 kHz BW)</td>
</tr>
<tr>
<td></td>
<td>• IS-136 (PLL MODE: NORMAL, 100 to 2100 MHz, RBW 1 kHz, VBW 3 kHz)</td>
</tr>
<tr>
<td></td>
<td>≤ – 42 dBC (30 kHz offset, 24.3 kHz BW)</td>
</tr>
<tr>
<td></td>
<td>≤ – 64 dBC (60 kHz offset, 24.3 kHz BW)</td>
</tr>
<tr>
<td></td>
<td>≤ – 64 dBC (90 kHz offset, 24.3 kHz BW)</td>
</tr>
<tr>
<td></td>
<td>• GSM (PLL MODE: NARROW, 100 to 3000 MHz, RBW 3 kHz, VBW 10 kHz)</td>
</tr>
<tr>
<td></td>
<td>≤ – 35 dBC (200 kHz offset, 30 kHz BW)</td>
</tr>
<tr>
<td></td>
<td>≤ – 66 dBC (400 kHz offset, 30 kHz BW)</td>
</tr>
<tr>
<td></td>
<td>• EDGE (PLL MODE: NARROW, 100 to 3000 MHz, RBW 3 kHz, VBW 10 kHz)</td>
</tr>
<tr>
<td></td>
<td>≤ – 38 dBC (200 kHz offset, 30 kHz BW)</td>
</tr>
<tr>
<td></td>
<td>≤ – 67 dBC (400 kHz offset, 30 kHz BW)</td>
</tr>
</tbody>
</table>

Note that performance deterioration of MG3681A caused by Spurious is excluded.

<table>
<thead>
<tr>
<th>Leakage Power Adjacent Channel</th>
<th>In the range from 100 to 2300 MHz, ratio of total power to power within 30 kHz band at –3 dBm output. When PLL MODE: NORMAL is set</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>• CDMA2000 RC1-2 FWD</td>
</tr>
<tr>
<td></td>
<td>≤ – 62 dBC (885 kHz ≤ offset &lt; 1.98 MHz)</td>
</tr>
<tr>
<td></td>
<td>≤ – 67 dBC (1.98 MHz ≤ offset &lt; 2.5 MHz)</td>
</tr>
<tr>
<td></td>
<td>≤ – 77 dBC (2.5 MHz ≤ offset &lt; 5.0 MHz)</td>
</tr>
<tr>
<td></td>
<td>• CDMA2000, others</td>
</tr>
<tr>
<td></td>
<td>≤ – 65 dBC (885 kHz ≤ offset &lt; 1.98 MHz)</td>
</tr>
<tr>
<td></td>
<td>≤ – 70 dBC (1.98 MHz ≤ offset &lt; 2.5 MHz)</td>
</tr>
<tr>
<td></td>
<td>≤ – 77 dBC (2.5 MHz ≤ offset &lt; 5.0 MHz)</td>
</tr>
</tbody>
</table>

Note that performance deterioration of MG3681A caused by Spurious is excluded.
## Specifications

<table>
<thead>
<tr>
<th>Item</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>IQ Output Level</strong></td>
<td></td>
</tr>
<tr>
<td>PDC, PHS, IS-136</td>
<td>359 mV(rms)</td>
</tr>
<tr>
<td>GSM</td>
<td>357 mV(rms)</td>
</tr>
<tr>
<td>EDGE</td>
<td>287 mV(rms)</td>
</tr>
<tr>
<td>CDMA2000 RC1RVS</td>
<td>287 mV(rms)</td>
</tr>
<tr>
<td>CDMA2000 RC3RVS</td>
<td>203 mV(rms)</td>
</tr>
<tr>
<td>CDMA2000 FWD</td>
<td>101 mV(rms)</td>
</tr>
<tr>
<td>1xEV-DO</td>
<td>101 mV(rms)</td>
</tr>
<tr>
<td><strong>IQ Output Level</strong></td>
<td>± 5% (OPT-11 not mounted)</td>
</tr>
<tr>
<td></td>
<td>± 10% (OPT-11 mounted)</td>
</tr>
<tr>
<td><strong>Setting range of Level Continuos Mode</strong></td>
<td>+10 to – 10 dB</td>
</tr>
<tr>
<td><strong>Symbol Rate</strong></td>
<td></td>
</tr>
<tr>
<td>PDC</td>
<td>21 kbps</td>
</tr>
<tr>
<td>PHS</td>
<td>192 kbps</td>
</tr>
<tr>
<td>IS-136</td>
<td>12.15 kbps</td>
</tr>
<tr>
<td>GSM</td>
<td>270.833 kbps</td>
</tr>
<tr>
<td>EDGE</td>
<td>270.833 kbps</td>
</tr>
<tr>
<td><strong>Chip Rate</strong></td>
<td>CDMA2000</td>
</tr>
<tr>
<td></td>
<td>1.2288 Mcps</td>
</tr>
<tr>
<td><strong>Transmission Speed Accuracy</strong></td>
<td>Depends on reference signal accuracy of MG 3680 series (Excluded in external synchronization)</td>
</tr>
<tr>
<td>Backup Area of Firmware Used</td>
<td>CPU:137.3 kByte, FPGA:49.5 kByte</td>
</tr>
</tbody>
</table>
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## Appendix B  List of Initial Value

<table>
<thead>
<tr>
<th>Setting</th>
<th>Initial Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital Modulation Main Screen</td>
<td></td>
</tr>
<tr>
<td>Pattern</td>
<td>0:GSM_EDGE</td>
</tr>
<tr>
<td>Trigger Source</td>
<td>Int</td>
</tr>
<tr>
<td>Trigger Delay</td>
<td>0/48sps (0.0000sps)</td>
</tr>
<tr>
<td>Reference Clock</td>
<td>Int</td>
</tr>
</tbody>
</table>
Appendix C  Performance Test Record

Tested at: ___________________________  Report No.  __________

______________________________  Date  __________

______________________________  Tested by  __________

Product Name  MG3681A Digital Modulation SG
+MU368030A  Universal Modulation Unit
+MX368031A  Device Test Signal Generator Software

Serial No.  __________  Ambient temperature  __________°C
AC Power frequency  _____ Hz  Relative Humidity  _____ %

Remarks:
________________________________________________________________________
________________________________________________________________________
________________________________________________________________________

Modulation Accuracy (Section 6.2)

* EVM

<table>
<thead>
<tr>
<th>Device Test Signal</th>
<th>Setting Output Level</th>
<th>Result</th>
<th>Specifications Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MHz</td>
<td>MHz</td>
<td>MHz</td>
</tr>
<tr>
<td>PDC</td>
<td>+5 dBm</td>
<td>MHz</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.8%</td>
</tr>
<tr>
<td>PHS</td>
<td>+5 dBm</td>
<td>MHz</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1.8%</td>
</tr>
<tr>
<td>IS-136</td>
<td>+5 dBm</td>
<td>MHz</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.0%</td>
</tr>
<tr>
<td>EDGE</td>
<td>+5 dBm</td>
<td>MHz</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.5%</td>
</tr>
</tbody>
</table>

* Phase Error

<table>
<thead>
<tr>
<th>Device Test Signal</th>
<th>Setting Output Level</th>
<th>Result</th>
<th>Specifications Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MHz</td>
<td>MHz</td>
<td>MHz</td>
</tr>
<tr>
<td>GSM</td>
<td>+5 dBm</td>
<td>MHz</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1° (rms)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3° (peak)</td>
</tr>
</tbody>
</table>
### Waveform (Section 6.3)

<table>
<thead>
<tr>
<th>Device Test Signal</th>
<th>Setting Output Level</th>
<th>MHz</th>
<th>MHz</th>
<th>MHz</th>
<th>MHz</th>
<th>MHz</th>
<th>Specifications Minimum</th>
</tr>
</thead>
<tbody>
<tr>
<td>RC1 RVS</td>
<td>− 3 dBm</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.997</td>
</tr>
<tr>
<td>RC3 RVS(1)</td>
<td>− 3 dBm</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.997</td>
</tr>
<tr>
<td>RC3 RVS(2)</td>
<td>− 3 dBm</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.997</td>
</tr>
<tr>
<td>RC3 RVS(3)</td>
<td>− 3 dBm</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.997</td>
</tr>
<tr>
<td>RC1-2 FWD</td>
<td>− 3 dBm</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.997</td>
</tr>
<tr>
<td>RC3-5 FWD</td>
<td>− 3 dBm</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.997</td>
</tr>
</tbody>
</table>

### Output Level Accuracy (Section 6.4)

<table>
<thead>
<tr>
<th>Device Test Signal</th>
<th>Setting Output Level</th>
<th>MHz</th>
<th>MHz</th>
<th>MHz</th>
<th>MHz</th>
<th>MHz</th>
<th>Specifications Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>PDC</td>
<td>dBm</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>± 1.0 dB</td>
</tr>
<tr>
<td>PHS</td>
<td>dBm</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>± 1.0 dB</td>
</tr>
<tr>
<td>IS-136</td>
<td>dBm</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>± 1.0 dB</td>
</tr>
<tr>
<td>GSM</td>
<td>dBm</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>± 1.0 dB</td>
</tr>
<tr>
<td>EDGE</td>
<td>dBm</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>± 1.0 dB</td>
</tr>
<tr>
<td>RC1 RVS</td>
<td>dBm</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>± 1.0 dB</td>
</tr>
<tr>
<td>RC3 RVS(1)</td>
<td>dBm</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>± 1.0 dB</td>
</tr>
<tr>
<td>RC3 RVS(2)</td>
<td>dBm</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>± 1.2 dB</td>
</tr>
<tr>
<td>RC3 RVS(3)</td>
<td>dBm</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>± 1.2 dB</td>
</tr>
<tr>
<td>RC1-2 FWD</td>
<td>dBm</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>± 1.2 dB</td>
</tr>
<tr>
<td>RC3-5 FWD</td>
<td>dBm</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>± 1.2 dB</td>
</tr>
<tr>
<td>1xEV-DO FWD</td>
<td>dBm</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>± 1.2 dB</td>
</tr>
<tr>
<td>1xEV-DO RVS</td>
<td>dBm</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>± 1.2 dB</td>
</tr>
</tbody>
</table>
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