Physical Layer Measurement for Next-Generation 5G/IoT Wired Communications

Next-generation wired communications standard are being actively discussed to support the anticipated explosion in data traffic volumes with growing use of various applications, such 5G mobile broadband, the Internet of Things (IoT), M2M (Machine to Machine) communications, Cloud Computing, etc. This paper outlines some high-speed standards for next-generation communications and describes some physical-layer measurement techniques, targeting the era of 5G and IoT.

1 - Introduction

Development of 5G mobile communications technology is progressing, targeting commercial rollout in 2020[1,2,3,12,13]. Moreover, the 2020 Tokyo Summer Olympics seem likely to mark the start of ultra-HD 4K and 8K video streaming services[1,2,3,12]. As well as Cloud Computing, attention is increasingly focusing on new applications and businesses, such as the Internet of Things (IoT) and Machine to Machine (M2M), linking people and things via wireless communications[1,2,3,12,13]. Against this background of increasing demand for ever-faster data communications speeds, this paper introduces the next generation of high-speed wired communications standards and describes physical-layer measurement techniques targeting 5G/IoT.

2 - Need for 5G/IoT Generation Wired Networks

The volume of mobile data traffic is forecast to increase 1000-fold between 2010 and 2020. Moreover, peak data rates in wireless sections will reach 10 Gbit/s[1,2,3]. Consequently, there is an urgent need for new next generation communications standards supporting these data demands.

2.1 5G Mobile Fronthaul

The Cloud-Radio Access Network (C-RAN) technology looks promising for the 5G[1,2,3,12,13]. The Common Public Radio Interface (CPRI) standard[4] recommends a wired connection between the centralized Base Band Units (BBU) and the Remote Radio Head (RRH). Currently, the CPRI standard specifies bit rates up to 12.16512 Gbit/s, but the advent of 5G will demand speeds of at least 100 Gbit/s per cell[2], and it is assumed that the technical barrier to increasing bit rates will be reached sometime soon. Consequently, a Radio over Ethernet (RoE) technology[7] is under study, which encapsulates and transports the CPRI, etc. on Ethernet, which has 100 Gbit/s speed in practical use and 400 Gbit/s under standardization[6]. The RoE technology itself has problems with frame jitter, synchronization between base stations, frequency and time synchronization[7]. As a consequence, joint use of RoE, Synchronous Ethernet (SyncE), and IEEE1588v2 Precision Time Protocol (PTP) is being investigated[7] and a new Next Generation Fronthaul Interface (NGFI) standard is being discussed as a replacement for CPRI[10,11].

2.2 5G Mobile Backhaul

Since 5G is implemented on general-purpose servers in data centers to virtualize the functions of hardware, such as the BBU, in software, Software Defined Network (SDN) and Network Function Virtualization (NFV) technologies are being investigated[2,3,12,13]. The centralized BBU in the data center requires a communications bandwidth of 10 Gbit/s per unit and 5G mobile backhaul requires a maximum capacity of 1 Tbit/s[2]. Achieving these requirements means using the optical fiber efficiently. As well as using the conventional Wavelength Division Multiplexing (WDM) and Passive Optical Network (PON)[2,3,8,10,11,12] technologies, there is increasing need for new next-generation, high-speed wired standards, such as 400 Gbit/s Ethernet. Additionally, 5G requires a highly reliable mobile backhaul. Consequently, the mainstream focus is on carrier-grade Ethernet supporting functions such as link monitoring, remote fault detection, automatic re-routing, etc., using Operation Administration and Maintenance (OAM) technologies[2,3,12,13].

2.3 Data Centers

Data center traffic is increasing year-on-year and volumes are expected to increase by about three fold between 2014 and 2019[14]. In addition to facilitating Cloud Computing services, new applications such as IoT and M2M will appear alongside 5G. Processing of these “big data” and other applications will require parallel processing by multiple servers to achieve efficiency. In most cases, Ethernet is used for server-to-server communications, but InfiniBand is commonly used for High Performance Computing (HPC) applications and enterprise server level interconnects[15]. InfiniBand is a fast and low-latency standard optimized for HPC by using Remote Direct Memory Access (RDMA) to lower CPU and memory access loads. It is mostly used now for 10 Gbit/s and 40 Gbit/s but is expected to become mainstream for future 100 Gbit/s and 400 Gbit/s services[2].

3 - Faster Wired Communications

The era of 5G and IoT is seeing increasing need for faster bit rates, such as 100 Gbit/s and 400 Gbit/s, and this section outlines the physical-layer standards forming the basis for increasing the speed of Ethernet and InfiniBand communications standards.

The Institute of Electrical and Electronics Engineers, Inc. (IEEE) has standardized gigabit class Ethernet as 1, 10, 40, and 100 Gbit/s[6,17,18]. However, work is underway on 25 Gbit/s and 50 Gbit/s standards to supplement the above bit rates for use as low-cost interconnects in data centers[19]. Additionally, new 200 Gbit/s and 400 Gbit/s speeds are being examined as new standards[20]. The Non Return to Zero (NRZ) and 4 level Pulse Amplitude Modulation (PAM4) technologies used for the 400 GbE (Gigabit Ethernet) standard under investigation have both been broadly certified[25]. Table 1 lists the 400 GbE standards.

400GbE Standards								
Standard	Optical IF					Electrical IF (CDAUI-n)		
	Distance	Fiber	Number of lane	Baudrate	Format	Number of lane	Baudrate	Format
400GBASE - SR16	100 m	MMF	16 ch (MPO-16)	25G	NRZ	CDAUI-16	25G	NRZ
400GBASE - DR4?	500 m	SMF	4 ch (PSM4)	50G	PAM4	CDAUI-8	25G	PAM4
400GBASE - FR8	2 km	SMF	8 λ WDM	25G	PAM4	CDAUI-8	25G	PAM4
400GBASE - LR8	10 km	SMF	8 λ WDM	25G	PAM4	CDAUI-8	25G	PAM4

Table 1: 400 GbE Standards

Since the PAM4 format supports higher bit rates at lower modulation speeds, it helps suppress problems with degraded signal waveforms at higher speeds. On the other hand, due to the multi-level modulation, it has the disadvantage of having a worse signal-to-noise ratio than NRZ at the same baud rate due to the smaller Eye opening amplitude. To compensate for this, bit error correction using Forward Error Correction (FEC) is being investigated. The plan is to rollout 400 GbE in late 2017. Figure 1 shows an example of a PAM4 waveform.

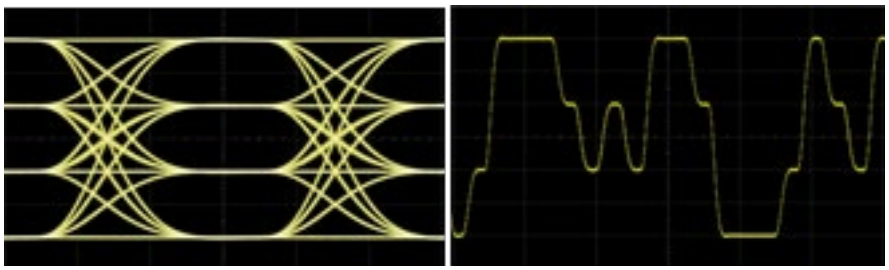


Figure 1: PAM4 Waveform

The InfiniBand physical layer bit rates are standardized by the InfiniBand Trade Association (IBTA) at 2.5, 5, 10, 14, and 25 Gbit/s per link[21]. Additionally, rates of 50 and 100 Gbit/s are being planned as next-generation standards[22]. Further, with InfiniBand, the number of links can be in parallel such as 1, 4, and 12 lanes to achieve large increases in the effective communications speed[21]. The 50 Gbit/s speed now in planning seems likely to use NRZ. Currently, no decision has been made on the signal to used for 100 Gbit/s. It is possible to achieve a maximum of 600 Gbit/s using 12 links, each of 50 Gbit/s. Table 2 lists the InfiniBand standard bit rates.

InfiniBand Standard Data Rates		
InfiniBand Standard	Bit Rate	Link Number
FDR (Fourteen Data Rate)	14 Gbit/s	1, 4, 12
EDR (Enhanced Data Rate)	25 Gbit/s	1, 4, 12
HDR (High Data Rate)	50 Gbit/s	1, 4, 12
NDR (Next Data Rate)	100 Gbit/s	1, 4, 12

Table 2: InfiniBand Standard Bit Rates

3.1 CEI Standard

The physical layer of Ethernet, InfiniBand and many other high-speed communications is based on the Common Electrical I/O (CEI) standard defined by the Optical Internet-working Forum (OIF)[23]. CEI defines the physical layer standard up to 28 Gbit/s while speeds up to 56 Gbit/s are defined in CEI-56G[24]. The NRZ technology is standardized for CEI-28G but the next-generation CEI-56G standard is still considering whether to adopt NRZ or PAM4[26]. To assure interoperability at the physical layer, CEI defines various Signal Integrity (SI) requirements; Table 3 lists the CEI-56G SI specifications.

CEI-56G Signal Integrity Specifications

Standard	Interface	Distance	Coding	Symbol Rate Class	Target BER	Tx Jitter Components	Rx Jitter Tolerance
CEI-56G-USR	Die to Die	0 - 10 mm	NRZ	56G	1E-15	TJ,RJ,BUJ,Even Odd Jitter	-
CEI-56G-XSR	Chip to Optical Engine	0 - 50 mm	NRZ	56G	1E-15	TJ,RJ,BUJ,Even Odd Jitter	-
		0 - 50 mm	PAM4	28G	1E-15	TJ,RJ,BUJ,Even Odd Jitter	-
CEI-56G-VSR	Chip to Pluggable Module	0 - 150 mm	NRZ	56G	1E-15	TJ,RJ,BUJ,Even Odd Jitter	TSJ, UUGJ, UBHPJ
		0 - 100 mm	PAM4	28G	1E-6	TJ,RJ,BUJ,Even Odd Jitter	TSJ, UUGJ, UBHPJ
CEI-56G-MR	Chip to Chip Back plane,	0 - 500 mm	PAM4	28G	1E-6	-	SJ
CEI-56G-LR	Cupper cable	0 - 1000 mm	TBD	TBD	TBD	-	-

Table 3: CEI-56G Signal Integrity Specifications

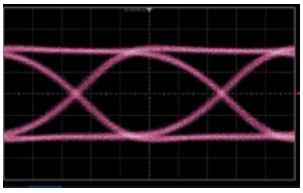
As shown in Table 3, the Jitter characteristics are a key part in assuring interoperability and SI. The minimum differential signal quality assured at the transmitter side is specified by the Eye Mask. Random Jitter (RJ) is caused by Gaussian-distributed thermal noise; Bounded Uncorrelated Jitter (BUJ) is caused by inter-signal crosstalk; Half Period Jitter is caused by degraded data signal duty; and Total Jitter (TJ) is the sum of all these Jitters. The quality of the error free differential signal received at the receiver side is also specified by the Eye Mask. Moreover, as well as RJ, BUJ, and HPJ, the jitter tolerance at the receiver side is also specified by Sinusoidal Jitter (SJ) simulating periodic jitter caused by switching power supplies, etc., Data Dependent Jitter (DDJ) and Inter-Symbol Interference (ISI), jitter which are caused by all forms of bit transition and transmission path losses. The transmission path loss characteristics between the transmitter and receiver are also specified to assure the quality of the differential data signal. The loss specification is to suppress the occurrence of DDJ and ISI. The conformance of the system inter-operability and SI to the CEI standards can be confirmed by these measurements and evaluations.

4 - Best 64 Gbit/s BER Measurement Solution

The Anritsu Signal Quality Analyzer MP1800A series is a Bit Error Rate Tester (BERT) supporting bit rates of 100 Mbit/s to 64.2 Gbit/s. It has 6 slots for installing measurement modules. In addition to the typical 32.1 Gbit/s Pulse Pattern Generator (PPG) and Error Detector (ED) modules, a synthesizer and Jitter modulation source can also be installed. The PPG module can generate Emphasis and PAM4 waveforms when used in combination with an external converter. Additionally, an external expansion 64 Gbit/s Multiplexer (MUX) and Demultiplexer (DEMUX) box is available to implement 64 Gbit/s BERT measurements. Anritsu was the first to release a 64 Gbit/s BERT systems meeting the Jitter Tolerance measurement requirements of the CEI standards. It supports all the RJ, SJ, BUJ, and HPJ Jitter Tolerance measurement requirements as well as measurement of both the NRZ and PAM4 technologies.

4.1 32G/64Gbit/s NRZ Measurement Function

The MP1800A series supports BER measurements using a PPG with high waveform quality and MUX. Figure 2 shows the 56 Gbit/s NRZ waveform output from the 64 Gbit/s MUX. Figure 3 shows the 28 Gbit/s NRZ waveform output from the 32 Gbit/s PPG.



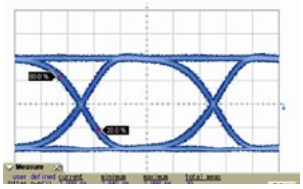


Figure 2: 56 Gbit/s NRZ Waveform *Figure 3: 28 Gbit/s NRZ Waveform*

As well as having a maximum amplitude of 3.5 Vp-p and wide variable range of 0.5 Vp-p, the 64 Gbit/s MUX also has a very small intrinsic RJ at 56 Gbit/s of only 200 fs rms (typ.), as well as an excellent Tr/Tf of 8 ps (20% to 80% typ.). The 32 Gbit/s PPG achieves an intrinsic RJ of 275 fs rms at 25 Gbit/s. Since all the RJ specifications are well within the CEI standard for RJ of 413 fs rms (0.15UIp-p @ 25 Gbit/s, converted from BER = 1E-12), the Jitter Tolerance of the DUT receiver can be measured with very high accuracy using the RJ modulation function. Additionally, the 64 Gbit/s DEMUX input has a high sensitivity of 25 mVp-p (typ.) at 56 Gbit/s. This is useful for receiving signals that have been attenuated by transmission path loss. These superior characteristics have been achieved by fabricating our own hybrid module with a high-speed Monolithic Microwave IC (MMIC) using an Indium Phosphide (InP) Heterojunction Bipolar Transistor (HBT) process. The fmax and ft for the InP HBT process are 479 GHz and 233 GHz, respectively.

Figure 4 shows the InP HBT MMIC and the hybrid module external appearance.

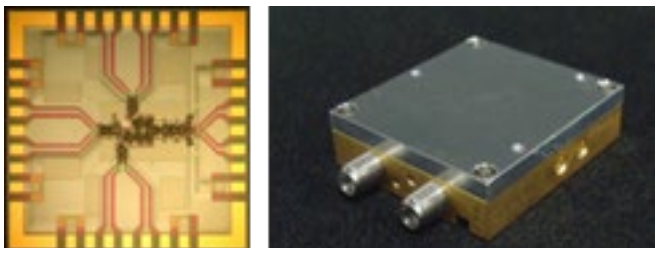
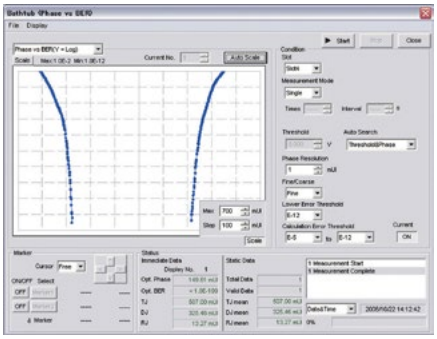


Figure 4: InP HBT MMIC and Hybrid Module Appearance

The MP1800A series supports many automatic measurement applications. Figure 5 shows the Bathtub Jitter measurement screen. This measurement estimates the TJ, RJ, and DJ based on BER measurement results for variations in the phase of the sampling clock. Since the time for measuring the Jitter at BER = 1E-15 specified by CEI is extremely long, the measurement time is shortened by estimating the Jitter at BER = 1E-15 based on a lower-rate BER.

Figure 6 shows the Eye Diagram measurement screen. This is drawn as a contour describing the relationship between the sampling clock phase and amplitude threshold at the same BER. This measurement can be used to observe changes in the Eye opening with BER and to evaluate waveform quality overall.



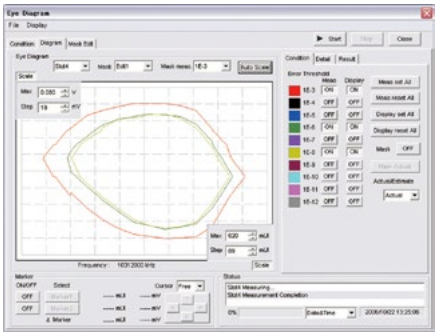


Figure 5: Bathtub Jitter Measurement Screen *Figure 6: Eye Diagram Measurement Screen*

4.2 32/56 Gbaud PAM4 Measurement Function

The MP1800A 32 Gbit/s BERT supporting PAM4 BER measurements up to 32 Gbaud. The MP1800A 64 Gbit/s BERT can generate PAM4 signal waveforms up to 56 Gbaud and supports BER measurements up to 43 Gbaud. Figure 7 shows the MP1800A 56 Gbaud PAM4 measurement setup.

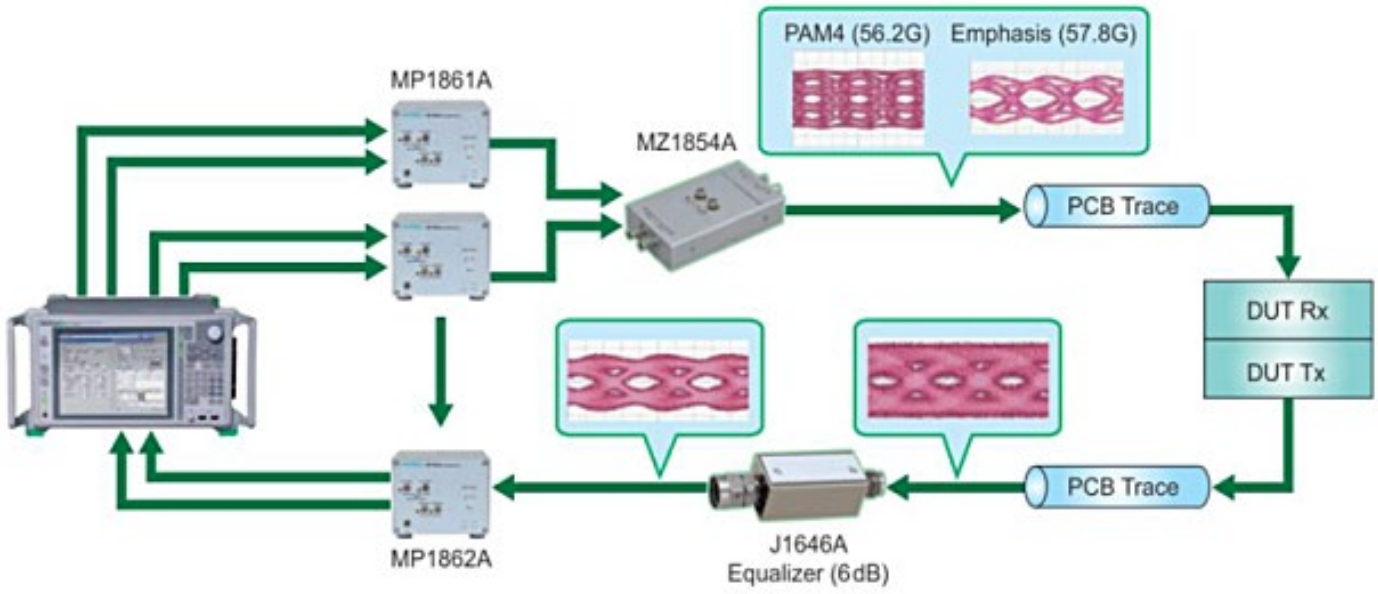


Figure 7: MP1800A 56 Gbaud PAM4 Measurement Setup (BER measures each EYE)

The MP1800A PAM4 Tx signal is generated by combining two output from either MUX or PPG by external data-combiner. Figure 8 shows a 56 Gbaud PAM4 waveform and Figure 9 shows a 28 Gbaud PAM4 waveform. A key good feature is the completely symmetrical Eye opening shape at the top and bottom and the matching crossover point positions.

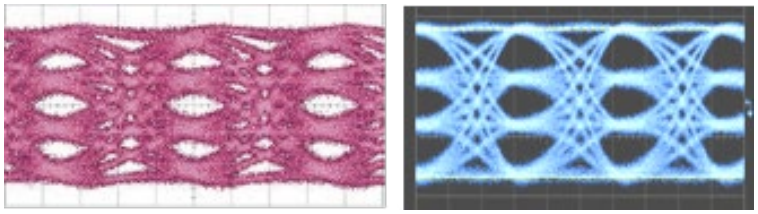


Figure 8: 56 Gbaud PAM4 Waveform *Figure 9: 28 Gbaud PAM4 Waveform*

The BER of PAM4 waveforms is measured via a passive equalizer for correcting the transmission path loss. The BER is measured for one Eye opening out of the three Eye openings. In case the PAM4 waveform is synthesized from a Pseudo Random Binary Sequence (PRBS) pattern, BER measurement is simple because the center Eye opening is the PRBS pattern itself. The BER of the top and bottom Eye openings is measured using a provided dedicated PAM4 PRBS data pattern. However, since the top and bottom Eye openings are substantially 50% valid for BER measurement, the Bit Mask function is used to remove invalid bits from the BER measurement target. The BER is calculated finally for the entire PAM4 waveform by summing the BER for each Eye opening.

4.3 Jitter Tolerance Measurement Function

Jitter Tolerance is a key index for evaluating the performance of the receiver system using Clock Data Recovery (CDR). Figure 10 shows the MP1800A series 64 Gbit/s BERT SJ maximum modulation.

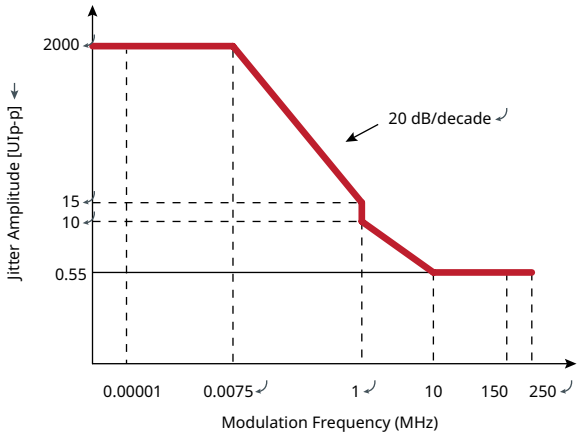


Figure 10: MP1800A Series 64 Gbit/s BERT SJ Max. Modulation

The CEI standard specifies an SJ of 17UI at a modulation frequency of 10 Hz. The MP1800A can add SJ of up to 2000UI. At 80 MHz it can add SJ of 0.55UI compared to the CEI specification of 0.05UI. In other words, since it can add much more SJ than specified by the CEI standard, it can measure the DUT performance and margins. Using the MP1800A series, not only can CEI-specified SJ be added, but also Jitter Tolerance can be measured while RJ and BUJ are being impressed; RJ is equivalent to Unbounded Gaussian Jitter in the CEI standard, and BUJ is equivalent to Uncorrelated High Probability Jitter. As explained previously, the MP1800A RJ is much smaller than the CEI specification, supporting high-accuracy Jitter Tolerance measurement of the DUT receiver section while RJ is added. Since BUJ mimics crosstalk between data signals in the transmission path, BUJ is generated by band limited PRBS31 pattern from 1/10 to 1/3 of the bit rate which is using a first-order low pass filter with a cutoff frequency from 1/20 to 1/10 of the bit rate. The measurement screen (Figure 11) uses an easy-to-understand signal flow path for impressing various Jitter types at various configurations and the Jitter modulation amount, frequency, filter characteristics, etc., can be set for each Jitter type.

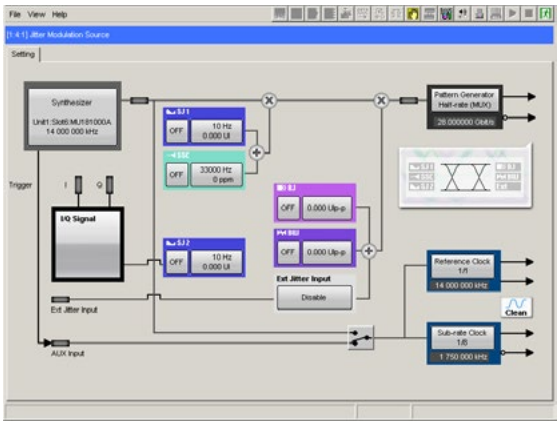


Figure 11: Jitter Measurement Screen

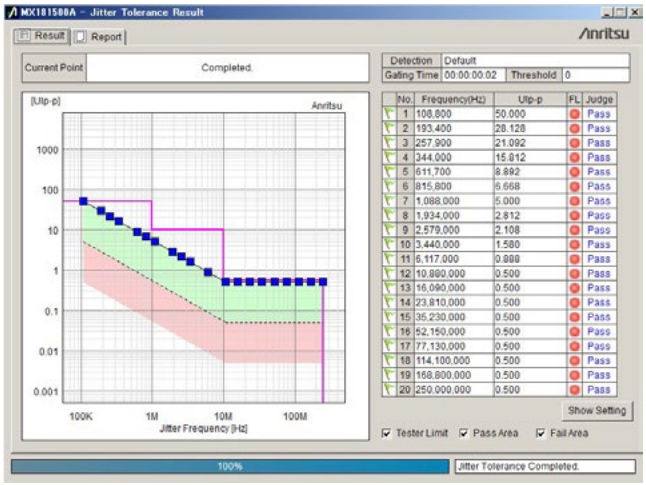


Figure 12: Jitter Tolerance Measurement Application Software

Figure 12 shows the Jitter Tolerance measurement application software screen. Using this software automates the Jitter Tolerance measurement procedure to increase the efficiency of performance evaluation tests.

As shown in Figure 12, the Jitter Tolerance measurement results are presented as graphs so the user can perform evaluations while confirming the results. Generally, in receiver systems using CDR, the CDR loop bandwidth is designed to be 1/1667 and below of the bit rate but an excessively narrow loop band degrades the Jitter Tolerance and cannot meet the Jitter Tolerance standard. Additionally, if the recovered Clock Jitter is large, Jitter occurring out of the loop band frequency causes bit errors. Jitter Tolerance measurements can be used to verify whether or not the receiver system satisfies the recommendations of the CEI standard.

5 - Measurement Challenges in Next-Generation Interconnects

The frequency-dependent nature of the channel linking transmitter and receiver on one hand, and the quest for ever increasing transceiver data rates (and thus increased harmonic content, e.g. ≥ 56 Gbps NRZ) on the other require careful design and characterization of the channel constituents. These are mainly substrates, packages, interposers, connectors, and printed-circuit boards (PCB) whose electrical performance is dominated by the frequency-dependent characteristics of the dielectric/semiconductor materials, vias, and transmission-line interconnects. Such characteristics include insertion loss, crosstalk, dispersion, clock and data skew, characteristic impedance, radiation, and parasitics, and have traditionally been measured by means of time-domain reflectometry (TDR) and time-domain vec-tor network analysis (TD-VNA). While such measurement techniques have been used extensively in the characterization of interconnects, their applicability in higher-data rate situations where harmonics of the clock exceed ~70 GHz is severely limited by a number of factors summarized below as follows:

1. Limited analog bandwidth of current TDR receivers. This in turn limits the bandwidth of TD-VNA measurements.
2. Limited dynamic range of scattering-parameter measurements. This is a direct result of
   a. The higher noise floor in a TD-VNA where the open-receiver architecture is in direct contrast with the highly tuned receivers in a frequency-domain VNA (FD-VNA).
   b. The decaying power spectrum of the harmonics in a step or pulse stimulus.
3. The temperature dependence (compromised stability over time), and limited directivity of the resistive directional bridge used to separate incident and reflected waves. These result in larger measurement uncertainty when compared with an FD-VNA.

Consequences of the above mentioned limitations include the following:

1. Difficulty/inability to assess coupling between lossy pairs of interconnects as a result of the limited dynamic range.
2. Difficulty/inability to resolve discontinuities and to generate broadband channel models needed in the analysis of transmitter-receiver chains as a result of the limited bandwidth.
3. High scattering-parameter uncertainty, with an impact on the generation of causal equivalent-circuit models.

6 - Broadband VNAs for Next-Generation Interconnects

The channel measurement challenges discussed in Section 5 can be alleviated by use of broadband, high-dynamic-range vector network analysis. By way of example, the 5th harmonic of a 56 Gbps NRZ clock falls within the frequency range of a 145 GHz FD-VNA. To this end, we recently introduced the world's first miniature commercial NLTL-based reflectometers and showed that these can be used to extend the frequency range of a microwave VNA to 145 GHz [27-29]. Essential ingredients in this process are monolithic NLTL samplers used to extend the VNA receivers from 30 GHz to 145 GHz, NLTL harmonic generators used to extend the CW source from 54 GHz to 145 GHz, high-directivity directional couplers, and a 0.8-mm coaxial port connector. The miniature 145 GHz reflectometer is shown in figure 13 along with a previous version limited to 110 GHz [27-28]. The integrated reflectometers and microwave VNA are shown in Fig. 14. In addition to their miniature size, these reflectometers provide highly attractive features such as short/long term thermal stability due to the vanishing thermal gradient across the modules, high amplitude and phase stability, and raw directivity to mention a few. Most importantly, placing the sampling directional bridge closest to the DUT provides long term amplitude and phase stability. It is these features in particular that lend themselves well to signal-integrity and device measurements whether these are performed on a probe station at the chip, interposer, package, or PCB level, or as part of a test fixture.

Figure 13. a) to 110 GHz with a 1-mm coaxial connector b) to 145 GHz with a 0.8 mm connector

Miniature broadband frequency extensions for a microwave FD-VNA

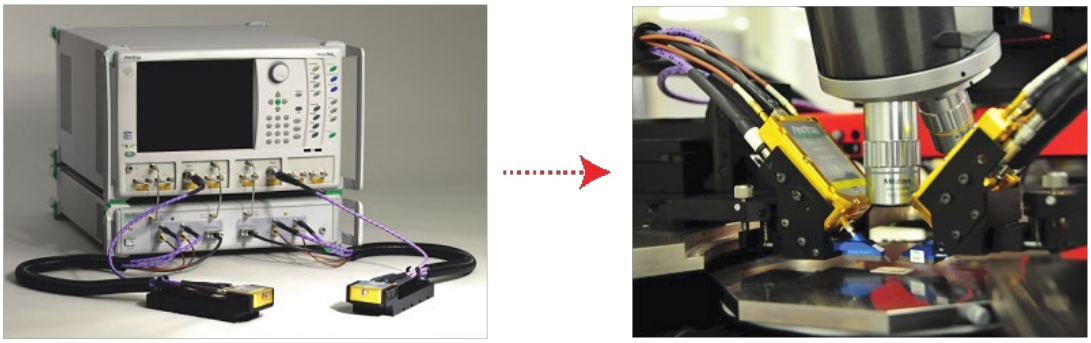


Figure 14. Miniature broadband frequency extensions integrated with a microwave FD-VNA. The resulting system has an extended bandwidth of (a) 70 kHz to 110 GHz and (b) 70 kHz to 145 GHz shown in a setup for on-wafer measurements. Both FD-VNA and frequency extensions are based on Anritsu NLTL technology.

Measurement possibilities brought about by the 70 kHz to 145 GHz VNA are illustrated in Fig. 15. Prime among them are enhanced spatial resolution, skew, and crosstalk.

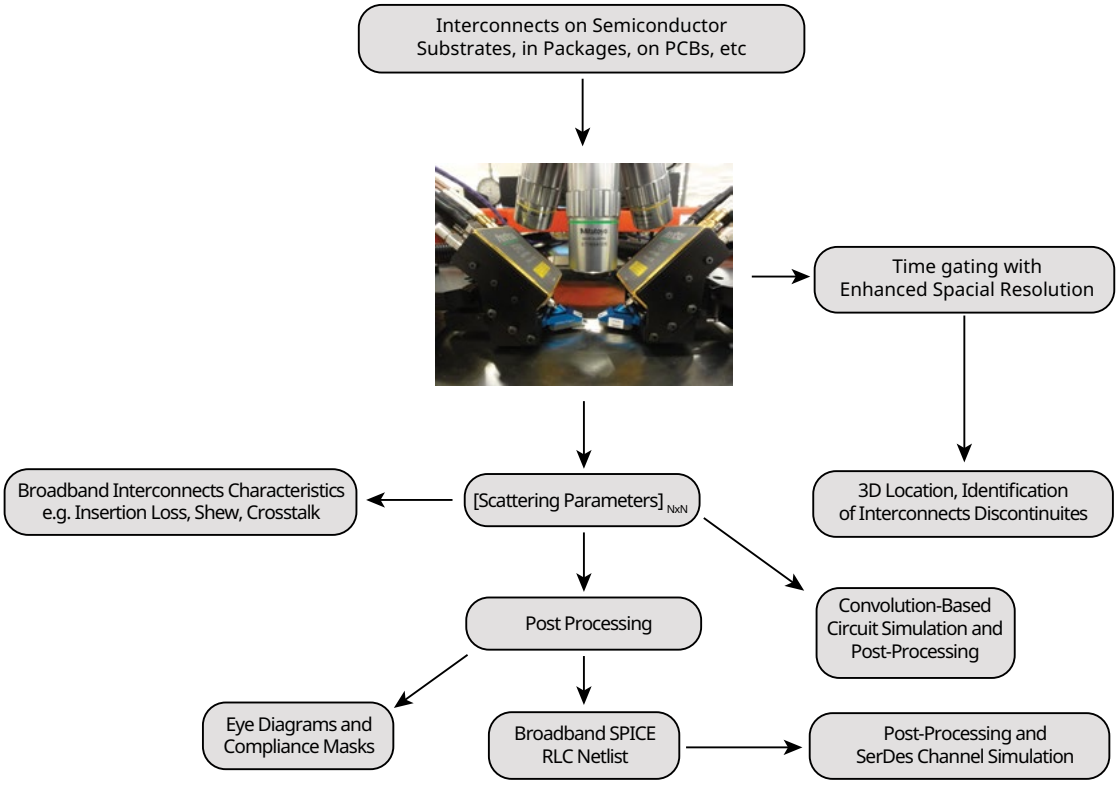


Figure 15. Interconnect measurement possibilities with a broadband high-dynamic-range (i.e. > 110 dB @ 110 GHz) VNA.

7 - Summary

Next-generation high-speed wired communication standards expected to support huge data traffic in the 5G/IoT era, and CEI standards referred by multiple next generation physical layer standards are introduced. And Signal Integrity and its measurement technologies are also summarized that will secure next-generation physical layer interoperability.

Anritsu will continue to contribute to the development of wired communication by providing measuring instruments for its physical layer that is growing in terms of higher speed and greater sophistication.

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9 - Authors

Kazuhiro Yamane
1st Product Development Dept. R&D Div. Measurement Business Group

Takanari Minami
1st Product Development Dept. R&D Div. Measurement Business Group

Wataru Aoba
Project Team 1
Product Marketing Dept. Marketing Div. Measurement Business Group

Shuichi Matsuda
1st Product Delvelopment Dept. R&D Div. Measurement Business Group

Taketo Saito
1st Product Delvelopment Dept. R&D Div. Measurement Business Group

Tatsuya Iwai
1st Product Delvelopment Dept. R&D Div. Measurement Business Group

Karam Noujein
Technology Fellow & Director Network Infrastructure Business Unit (NIBU) - Americas