Development of EA Modulator Driver for 40GbE using InP DHBTs

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[Summary] The 40GBASE-FR is one of the Ethernet physical layer specifications of 40GbE standards supporting serial optical communications over 2 km single-mode fiber at data rate of 40 Gbit/s. In the transmitter module of optical transceivers compliant with the above specifications, EA modulator is widely used as Electro-optical (E/O) converter. EA driver is used to drive above EA modulator for E/O conversion, and is required to operate over 40 Gbit/s with an output amplitude of 2.5 Vpp. This paper reports development of a 40GbE EA driver IC using high-speed IC process technology based on InP DHBT with high-speed operation and high breakdown voltage characteristics. We designed EA driver IC using a distributed amplifier and the new differential transmission line layout topology— called intersected differential transmission line layout — is adopted for signal lines of the distributed amplifier to improve output waveform quality. We confirmed that the developed IC provides clear output waveform with an output amplitude of 2.55 Vpp (1.35 W power consumption) and RMS jitter of 560 fs at a bit rate of 44.6 Gbit/s. Additionally, we also confirmed the developed IC's excellent temperature characteristics with a small variation of output amplitude over a temperature range from –5° to +80°C.

1 Introduction

Metro networks and data centers are explosive increasing in network traffic due to the spread of smartphones and the increase in cloud computing services. To handle these growing network traffic, 100/40 Gbit/s Ethernet (100/40GbE) technologies, which have larger communication capacity than the previous 10GbE technology, had been investigated, and then 100/40GbE standards were standardized in 2010.

40GBASE-FR is one of the Ethernet physical layer specifications of 100/40GbE standards, and supports serial optical communications over 2 km single-mode fiber at data rates of 40 Gbit/s band. Figure 1 shows an example of the block diagram for the transmitter module of an optical transceiver compliant with the 40GBASE-FR.

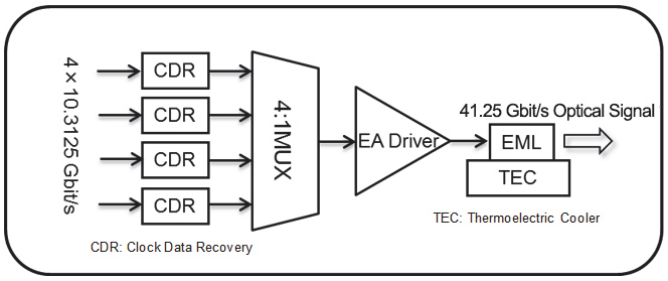

Figure 1 Block Diagram of Transmitter Module

As shown in this diagram, Electro absorption modulator integrated laser (EML) is used for electro- optical conversion and EA modulator of the EML is driven by EA driver amplifying the 40 Gbit/s band electrical signal output from the 4:1 multiplexer (4:1 MUX). Up until now, Anritsu has implemented a high-speed IC process technology based on InP DHBT (Double Hetero-junction Bipolar Transistor)[1), 2)] with a high- speed operation and a high breakdown voltage characteristics (current gain cut-off frequency f_T = 230 GHz, breakdown voltage BV_{CEO}= 6 V). The high-speed ICs using this technology are provided as key devices in Anritsu measurement equipment[3)]. Our InP DHBT characteristics of a operation speed and a breakdown voltage are adequate to implement the 40GbE EA driver IC required for a high-speed operation and a large output amplitude. Therefore, we developed the 40GbE EA driver IC using our IC process.

This paper describes target specifications and basic structure of the circuit for the developed 40GbE EA driver IC and introduces some of the design concepts for achieving a low-jitter, clear output waveform. Additionally, we investigate that the intersected differential transmission line layout which we devised can minimize differential skew in differential transmission line by simulation analysis and report the evaluation results for the output waveform of the 40GbE EA driver IC using our technology.

2 Setting of Target Specifications

It is important to set the target specifications for EA driver IC taking into consideration standard trends and performance differentiation. The key target specifications are summarized below.

(1) Max. Operation Bit Rate: 40GBASE-FR must be able to support the OTN (Optical Transport Network) recommended OTU3 having data rate of 43.0 Gbit/s. Additionally, the OTN standardization also have been discussing OTU3e having data rate of 44.6 Gbit/s.

(2) Output Amplitude: Assuring excellent transmission characteristics for 40 Gbit/s band optical signals requires an extinction ratio of more than 10 dB for the EA modulator output optical signal. To obtain this extinction ratio generally requires drive voltage of more than 2.5 Vpp for the EA modulator.

(3) Power Consumption: Since 40GbE optical transceivers widely use the CFP (Centum gigabit Form Factor Pluggable), this development also assumes installation into the CFP transceiver too. Small size and low power are required for the components installed in small transceivers like the CFP. Therefore, the EA driver IC is required a target power consumption of less than 1.6 W.

(4) RMS (Root Mean Square) Jitter: Low jitter characteristics are required for the optical output waveform of the optical transceiver to satisfy the mask margin requirements and generally a value of less than 1000 fs is required. In developing the EA driver IC we set a target value of less than 850 fs to assure a sufficient mask margin and plan for product differentiation.

(5) Operating Temperature: The optical transceiver requires an operating temperature range from 0° to 70°C. We set the operating temperature range from –5° to +80°C considering internal temperature rise, where the EA driver IC is installed in the optical transceiver.

Table 1 summarizes the EA driver IC target specifications based on the above points.

Table 1 Target Specifications for EA Driver IC

Item	Target Value
Max. Operation Bit Rate	44.6 Gbit/s
Output Amplitude	2.5 Vpp min.
Power Consumption	1.6 W max.
RMS Jitter	850 fs max.
Operating Temperature	–5° to 80°C

3 Design

3.1 Design Concept

Figure 2 shows the block diagram of the designed EA driver IC. The IC is composed of a three stages differential amplifiers that are the input buffer, the pre-buffer and the booster amplifier. The input buffer receives a differential signal output from the 4:1 MUX and the booster amplifier output single-ended signal driving the EA modulator. The input buffer and the pre-buffer operate as limiting amplifiers keeping the internal voltage swing constant while the booster amplifier boost the signal to 2.5 Vpp. Since the designing the booster amplifier is a key point to amplify a high-bit-rate signal exceeding 40 Gbit/s to 2.5 Vpp while keeping low jitter characteristics, first, we describe the design procedure for a general booster amplifier in this section, and then clarify the problems of a conventional technology in section 3.2 followed by a new proposal for the intersected differential transmission line layout solving these problems in section 3.3.

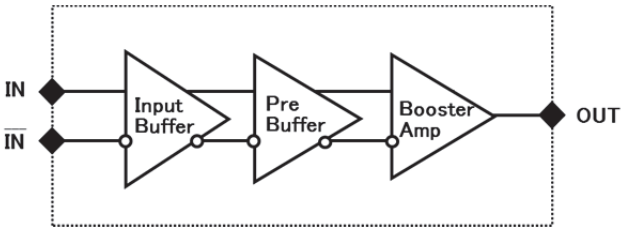

Figure 2 Block Diagram of EA Driver IC

Generally, booster amplifiers using a distributed amplifier circuit are favored for large output amplitude and high-speed operation. The details of the basic principles of the distributed amplifier circuits are explained in the appendix. Figure 3 shows the layout configuration for a conventional booster amplifier including transmission lines (represented by rectangles), and a conventional technology is explained using this diagram. This booster amplifier is an example of a distributed amplifier circuit composed of four differential-amplifier-unit cells. The output terminals of each differential-amplifier-unit cell is connected in parallel by the transmission line TLo1, TLo2 wired alternately and forming the artificial transmission line TLo. Additionally, the differential input terminals of each differential-amplifier-unit cell is connected in parallel by the alternately wired transmission lines TLi1, and TLi2, and TLi1b, and TLi2b, forming the artificial transmission line TLi. TLo is a single-ended artificial transmission line and the $V_{OUT}(+)$

signal from the output terminal (right terminal) is output to the EA modulator. TLi is composed of two lines forming a differential artificial transmission line; the $V_{IN}(+)/V_{IN}(–)$ differential signal is input at the start terminal (left terminal). In the following description, each of the two lines forming TLi are called the $V_{IN}(+)$ signal line and $V_{IN}(–)$ signal line.

In designing the differential-amplifier-unit cells for the above-described booster amplifier, it is important to optimize the output current and DHBT emitter size and the number of unit cells considering the required bandwidth and output amplitude. On the other hand, in designing the artificial transmission lines TLi and TLo, it is important to understand points (1) to (3) below for optimizing the characteristic impedance and length of transmission lines.

(1) The characteristic impedance of the artificial transmission line TLo must be matched to the 50 Ω input impedance of the EA modulator.

(2) In order to lower power consumption of the pre-buffer, it is important to set the pre-buffer load resistance value which is matched to the characteristic impedance (Odd mode impedance) of the artificial transmission line TLi to the highest possible. Moreover, the reason for the lowering power consumption is that increasing the load resistance value allow of reducing the pre-buffer output current without decreasing the output voltage swing of pre-buffer.

(3) The electrical lengths between each differential-amplifier-unit cell of the TLi and TLo artificial transmission lines must be equal so that the output signals of each differential-amplifier-unit cell are combined with same phase.

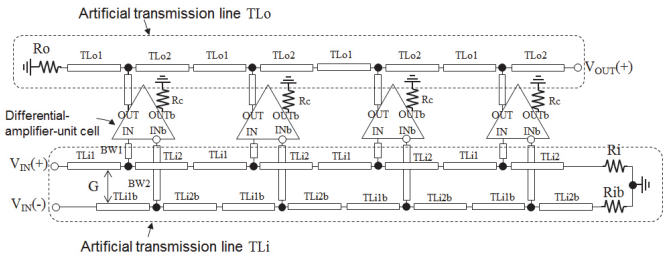

Figure 3 Schematic Layout Configuration of Conventional Booster Amplifier

3.2 Problems with Conventional Booster Amplifier

The conventional artificial transmission line TLi shown in Figure 3 is arranged with $V_{IN}(+)$ signal line and $V_{IN}(–)$ signal line separated by the distance G. Using this layout, the branch line BW1 between the $V_{IN}(+)$ signal line and the IN terminal of the differential-amplifier-unit cell is not the same as the branch line length BW2 between the $V_{IN}(–)$ signal line and the INb terminal of the differential-amplifier-unit cell. In particular since the length of branch line BW2 is longer than the distance G, there is a large impact on the transmission characteristics. For example, when the TLi artificial transmission line is designed with an characteristic impedance of 70 Ω, the minimum gap G is at least several tens of micrometers when Anritsu fabricates an IC by forming the transmission line on InP substrate, and the length of the branch line BW2 cannot be ignored in comparison to the wavelength of the operating frequency. When considering the input impedance of the differential-amplifier-unit cell is sufficiently high, like BW2, the length of the branch line acts as a capacitance due to the open stub characteristics and has an adverse effect on the transmission characteristics, causing jitter deterioration in the output waveform. This jitter deterioration can be reduced by narrowing the gap G but at the same time narrowing the gap G increases the electromagnetic coupling between both lines which reduces the characteristic impedance and causes design problems outlined in item (2) of section 3.1. As a result, it is difficult to achieve both low power consumption and low jitter characteristics with suiting the target specifications.

3.3 Intersected Differential Transmission Line Layout

To satisfy the target specifications, we propose the new differential transmission line layout topology— called intersected differential transmission line layout —shown in Figure 4. In this design, the TLi1 transmission lines are arranged at 45° angle extending across the length and connected via branch lines BW1 to the IN terminals of the unit cells, while the TLi2 transmission lines are folded back at a right angle to the TLi1. Similarly, the TLib transmission lines are also arranged at 45° extending across the length and connected via branch lines BW2 to the INb terminals of the unit cells while the TLi2b transmission lines are folded back at a right angle to the TLi1b. Moreover TLi1b and TLi2 intersect each other at a right angle with an insulating layer interposed therebetween at the central positions between IN and INb terminals of the unit cells, Similarly to these lines, TLi1 and TLi2b intersect each other at the central positions

between each unit cell. Using this layout, since the length of the branch lines BW1 and BW2 can be equal and short, the impact of the branch lines on the transmission characteristics can be reduced. As a result, the TLi' artificial transmission line characteristic impedance can be increased without jitter deterioration. In comparison to the conventional transmission line shown in Figure 3, at first glance, the characteristic impedance design for the proposal layout transmission line seems difficult but since the gap G between the two lines is constant from the start terminal to the end terminal connected to the termination resistors Ri and Rib, the design procedure is the same as the conventional transmission line. Additionally, although an intersection of two signal lines complicate characteristic impedance design for a differential transmission line, the proposal layout can be easy to design characteristic impedance. Because, when the two signal lines intersect each other at a right angle as in this layout, there is no mutual inductances between the two lines and only the capacitance which is fabricated in the intersection portions of two signal lines may be considered as a factor causing impedance disturbance. Moreover, since Anritsu's IC process use low-dielectric-constant BenzoCycloButene (BCB) as the insulation layer interposed between the two lines, the effect of the capacitances of the intersection portions is sufficiently low to be negligible.

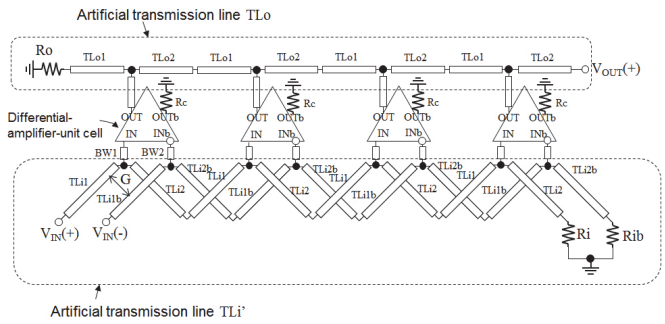

Figure 4 Distributed Amplifier Circuit using Intersected Differential Transmission line Layout

4 Simulation Analysis

To confirm that the proposed intersected differential transmission line layout has better performance than the conventional transmission line, we performed simulation analysis of a differential artificial transmission line with characteristic impedance of 70 Ω. Figures 5a and 5b show the input return loss and the transmission phase characteristics, respectively, for the conventional artificial transmission line TLi. The analysis frequencies were from DC to 65 GHz (about three times the fundamental frequency for a 44.6 Gbit/s signal). As can be seen from Figure 5a, the return loss is increased to –10 dB at 65 GHz in V_{IN}(–) signal line, which was worse than the V_{IN}(+) signal line. This is due to the fact that the excessive capacitances caused by the open stub characteristics of the longer branch lines BW2 added to the V_{IN}(–) signal line. In addition, as can be seen from Figure 5b, V_{IN}(–) signal line has phase delay (differential skew) of 30° at 65 GHz compared to the V_{IN}(+) signal line due to above excessive capacitances. These results suggest that the differential skew and return loss degradation in the TLi artificial transmission line induce the electrical lengths mismatch to the TLo, unnecessary signal distortions and electromagnetic noise, causing jitter deterioration in the output waveform.

Figures 6a and 6b show the input return loss and the transmission phase characteristics, respectively, for an artificial transmission line TLi' using the proposal layout. Since the lengths of the branch lines BW1 and BW2 are the same and short, the input return loss is a low value of –17 dB or less up to 65 GHz and we can see that there is no differential skew between the two lines. These results confirmed that this design will reduce jitter in the output waveform.

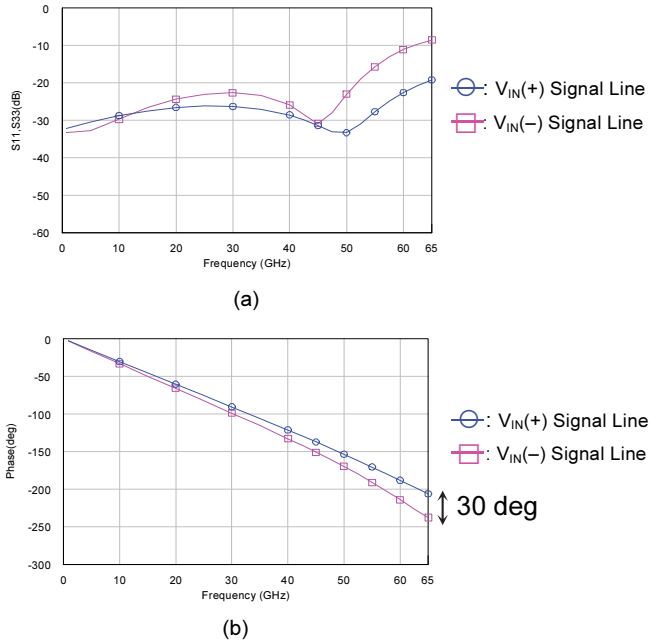

Figure 5 (a) Input Return Loss and (b) Transmission Phase Characteristics of Conventional Differential Artificial Transmission Line TLi

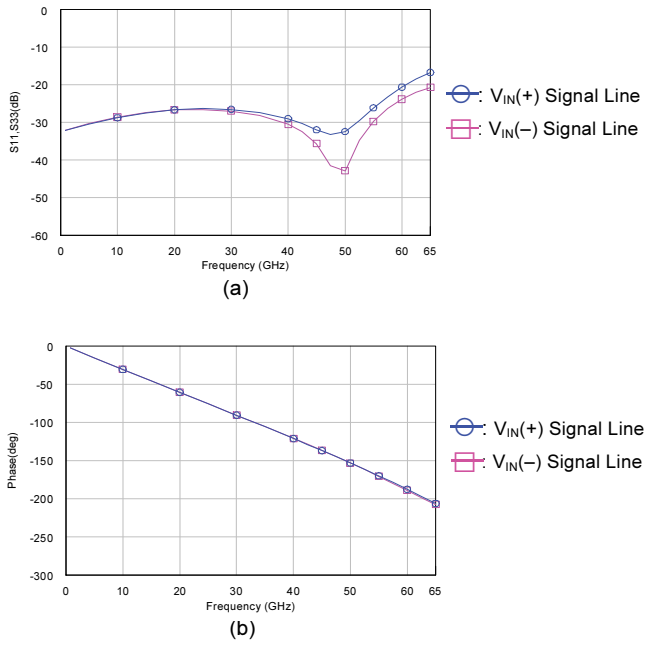

Figure 6 (a) Input Return Loss and (b) Transmission Phase Characteristics of Differential Artificial Transmission Line TLi' using Intersected Differential Transmission Line Layout

5 Fabrication and Evaluation

We designed and fabricated an EA driver IC with a chip size of 1.5 mm × 2 mm based on the simulation analysis described above. Evaluation was carried out using RF probes. Figure 7 shows the output return loss (S22) of the fabricated EA driver IC. The solid line shows the measured data and the dashed line shows the simulation result. This solid line indicates the return loss of the artificial transmission line TLo terminated with the resistor Ro shown in Figure 4. These results confirmed that the measured output return loss is low value of –15 dB or less up to 50 GHz. It was evident from measured data of low output return loss that the designing of the artificial transmission line TLo was optimized desirably. In addition, the measured data is in a good coincidence with the simulation result. Thus, we confirmed that the analytical method used in this work is valid.

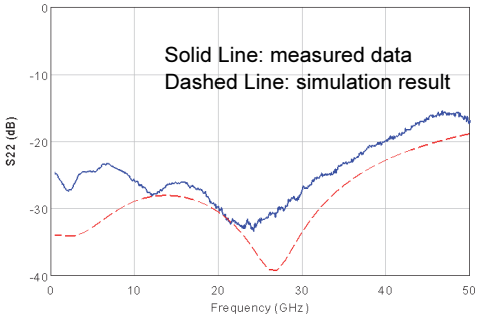

Figure 7 Output Return Loss of EA Driver IC

Figure 8 shows the measured output waveform of the fabricated EA driver IC. Table 2 lists the measurement conditions. We measured output waveform in a single-ended input condition because the developed EA driver IC can normally operate under the single-ended input condition owing to the limiting effect of the input buffer and the pre-buffer.

Table 2 Measurement Conditions

Bit Rate	44.6 Gbit/s (PRBS 2^{31}–1)
Input Amplitude	0.4 Vpp (single-ended input signal)
Power Supply Voltage and Current	–5.2 V, 260 mA

From the figures 8, we confirmed that the output amplitude was over 2.5 Vpp at 44.6 Gbit/s and the RMS jitter was 560 fs. Additionally, the power consumption calculated from the power supply voltage and current values shown in Table 2 is determined to be about 1.35 W. These results confirmed that the EA driver IC using proposed intersected differential transmission line layout satisfied the target specifications. Furthermore, the rise and fall times (20% - 80%) were small at only 8.2 ps and 6.5 ps, respectively, providing an sufficiently wide EYE opening for driving the EA modulator at 44.6 Gbit/s.

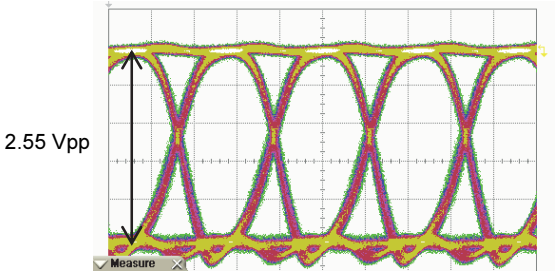

Figure 8 44.6 Gbit/s Output Waveform Measured with RF Probes (Vertical: 0.5 V/div, Horizontal: 10 ps/div)

We also evaluated the temperature characteristics of the fabricated EA driver IC. The IC was assembled into a metal case module with two coaxial connectors for input and output single-ended signals. We measured the 44.6 Gbit/s output waveforms of the module at various temperatures. Figure 9 shows the output amplitude and RMS jitter measured at each temperature in this test. This figure shows that the variation of the output amplitude over a temperature range from –5° to +80°C is ±25 mVpp. The suppression of output amplitude variation over a wide temperature range was ow-

ing to adopting a current mirror circuit for constant current sources in the differential-amplifier-unit cells. Moreover, although not shown by the graph, the fluctuation of the cross point is just ±0.5% over the specified temperature range, which was the sufficiently practical characteristic for a 40GbE EA driver IC. Although the RMS jitter tended to be larger at lower temperatures, it was still a sufficiently small value of 630 fs at –5°C. Based on these results, we confirmed that the fabricated IC provide excellent waveform characteristics without any obvious change in output waveform with over the target temperature range from –5° to +80°C.

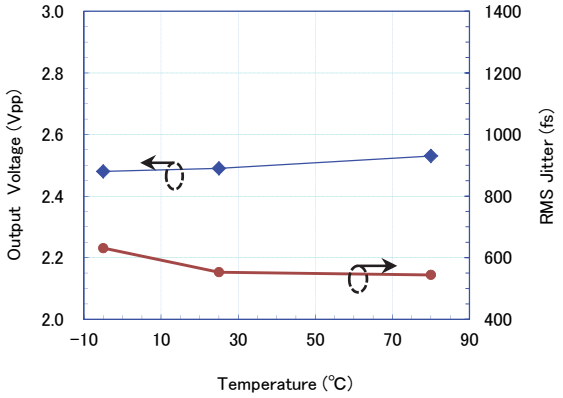

Figure 9 Variation of Output Amplitude and RMS Jitter with Temperature

6 Conclusions

We developed the 40GbE EA driver IC using high-speed IC process technology based on InP DHBT with high-speed operation and high breakdown voltage characteristics. We designed EA driver IC adopting the new intersected differential transmission line layout for the signal lines of the distributed amplifier to improve output waveform quality. We confirmed that the fabricated IC provides clear output waveform with an output amplitude of 2.55 Vpp (1.35 W power consumption) and RMS jitter of 560 fs at a bit rate of 44.6 Gbit/s. Moreover, The output waveform did not show any obvious change over the temperature range from –5° to +80°C. The evaluation results demonstrated that this developed IC is applicable as an EA driver IC for 40GbE optical transceiver modules.

After passing reliability tests, this IC has been released as the AG4P18C and is being used in optical communications systems. Future work is focused on using this technology to develop an EA driver IC supporting ultra-high-speed 100 and 400GbE communications.

References

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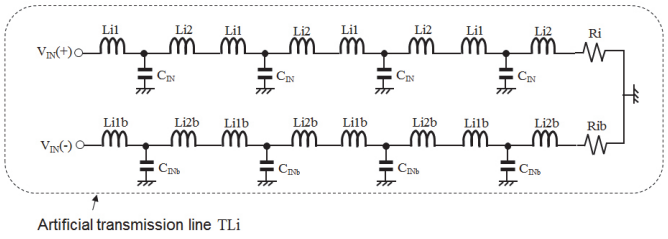
Appendix

1. Basic Principles of Distributed Amplifier Circuit

The distributed amplifier circuit consists of multiple amplifier-unit cells that are arranged in parallel at predetermined intervals. The input and output terminals of each amplifier-unit cell are connected in parallel by transmission lines with high characteristics impedances. In this structure, input and output capacitances of amplifier-unit cells and inductances of transmission lines construct artificial transmission lines having a high cut-off frequency. Using the circuit in Figure 3 of the main text as an example, Appendix Figure 1 is the equivalent circuit of the differential artificial transmission line TLi terminated with the resistor Ri and Rib. Li1, Li2, Li1b, and Li2b are lumped-element inductances of the transmission lines TLi1, TLi2, TLi1b, and TLi2b respectively, and C_{IN} and C_{INb} are capacitances of the IN and INb terminals of each differential-amplifier-unit cell. This ladder structure of these inductances and capacitances construct the artificial transmission line TLi. The TLi transmission line have a high cut-off frequency because the inductances of the transmission lines neutralize the effect in which the capacitances of IN and INb terminals limit bandwidth of a transmission line. On the other hand, the artificial transmission line TLo having a high cut-off frequency, not shown by the equivalent cir-

cuit, is constructed by the lumped-element inductances for the transmission lines TLo1 and TLo2, and the capacitances of the OUT terminals of each differential-amplifier-unit cell. Since the characteristic impedance (Odd mode impedance) of the differential artificial transmission line TLi and the value of the resistors Ri and Rib match to the output impedance of the $V_{IN}(+)/V_{IN}(-)$ signal source (pre-buffer load resistance value), the $V_{IN}(+)/V_{IN}(-)$ differential signal is transmitted to each differential-amplifier-unit cell in wideband with low return loss characteristics. Each differential-amplifier-unit cell amplify the $V_{IN}(+)/V_{IN}(-)$ differential signal and output the amplified signal from the OUT terminal. The signals output from the OUT terminals are combined with same phase to be large amplitude signal $V_{OUT}(+)$ on the artificial transmission line TLo, and the $V_{OUT}(+)$ signal is output to the electric load (EA modulator). Since the characteristic impedance of the artificial transmission line TLo and the value of the termination resistor Ro match to the input impedance of the electric load, the $V_{OUT}(+)$ signal is transmitted to electric load in wideband with low return loss characteristics. Thus, the distributed amplifier circuit can provide both large output amplitude and wideband operation due to the above principles.



Appendix Figure 1 Equivalent Circuit of Differential Artificial Transmission Line TLi

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