Application Note

Anritsu

FEC Evaluation Using BERT

MP1800A Series
Signal Quality Analyzer

1. Outline of RS-FEC and Evaluation

The IEEE802.3bj standard specifies transmission methods using Reed Solomon FEC (RS-FEC). In this standard, 100GBase-CR4/KR4 uses RS (528, 514) and 100GBase-KP4 uses RS (544, 514).

RS-FEC is defined as follows using RS (n, k) and t, where:

k: Data to be encoded

n: Number of Symbols including redundant bits for error correction (also called Block)

t: Number of error-correctable Symbols

$$t = (n-k)/2$$

In the above-described RS-FEC, both t Symbols can be error corrected and 2t Symbols can be error detected.

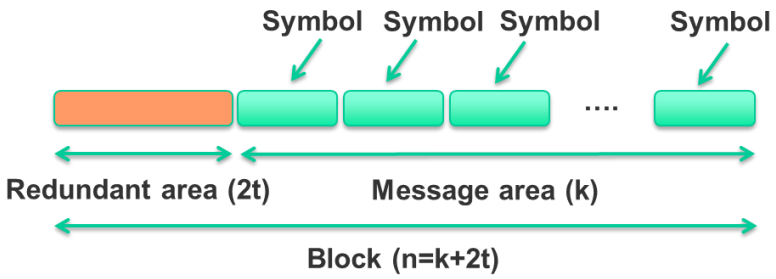

Figure 1.1 RS (n, k) FEC Composition

With RS-FEC, units composed of multiple bits, each called a Symbol, are encoded. Consequently, both error correction and error detection are performed in Symbol units, not bit units. Irrespective of whether there is one or many errors within one Symbol, it is counted as one Symbol error (Figure 1.2)

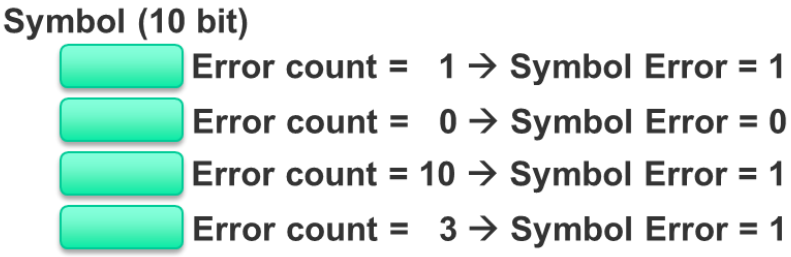

Figure 1.2 Error Bit Number vs. Symbol Error Number

As a result, the key evaluation parameters for RS-FEC are the number of Symbol Errors in one block and how the errors are distributed.

Generally, with RS-FEC, each Symbol is 8 bits long, but IEEE802.3bj specifies a Symbol length of 10 bits. In RS (528, 514) used by 100GBase-CR4/KR4, since 140 redundant bits are appended to the Message area of 5140 bits (20 x 257 bits), one block is 5280 bits long. In addition, with RS (528, 514), up to 7 Symbol Errors can be corrected and up to 14 Symbol Errors can be detected.

Since each Symbol is 10 bits long, the theoretical maximum number of bits that can be corrected in one block is 7 x Symbol (10 bits) or 70 bits, but if the errors are distributed across 8 or more Symbols, not all errors can be corrected even when there are less than 70. Similarly, the theoretical maximum number of detectable errors is 140 bits in 14 Symbols but if the errors are distributed across 15 or more Symbols, not all errors can be detected.

Since 100GBase-KP4 uses RS (544, 514) FEC and 300 redundant bits are appended to the Message area of 5140 bits (20 x 257 bits), up to 15 Symbol Errors can be corrected and up to 30 can be detected.

The next section describes how to use the Capture function of the Error Detector in the MP1800A Signal Quality Analyzer (SQA) to evaluate RS-FEC with these characteristics.

2. Setting MP1800A Signal Quality Analyzer

The MP1800A SQA Error Detector has a Capture function for saving data received using various triggers to internal memory. Using the Capture function supports confirmation of the degree of DUT error correction. This section explains how the MP1800A generates a normal PRBS and how the received PRBS error data is output for evaluation as a Capture file that the customer can use to confirm the degree of error correction from the error data in the file.

Table 2.1 Capture Function Specifications

Capture Function	
Memory Blocks	1, 2, 4, 8, 16, 32, 64, 128
Memory size	8 Mbits / n (n: Memory blocks)
Trigger	Error, Manual, External input, Match pattern

The Capture function establishes synchronization using the Error Detector and performs BER measurement. The procedure for setting the Capture function is explained below.

Refer to Figure 2.1. First, choose the Capture tab at the Error Detector screen.

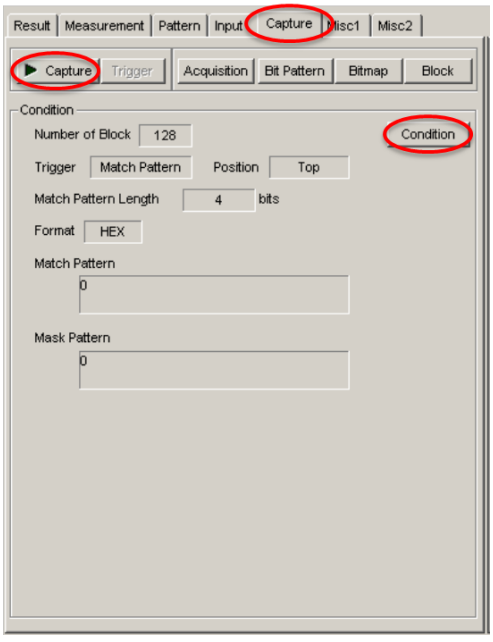

Figure 2.1 Capture Display

Next, press the Condition button to fetch the Condition Setting screen shown in Figure 2.2 and set the Capture conditions. At this screen, set Number of Block to 128, and Trigger to Error Detect, and then press OK. This setting can save up to 128 receive patterns each of 65536 bits to memory whenever an error occurs.

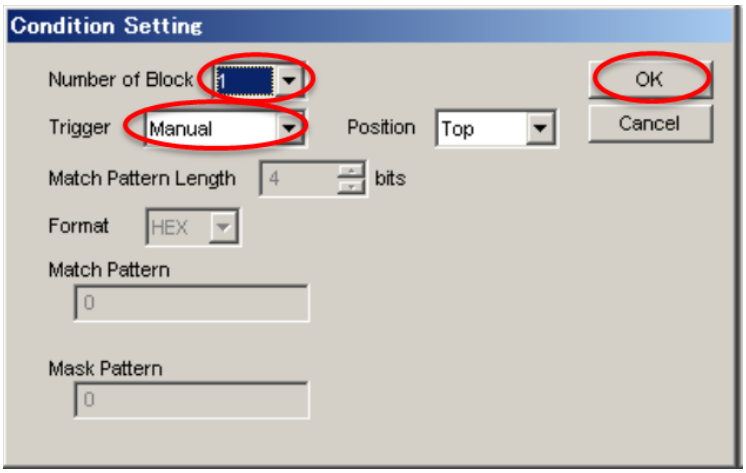

Figure 2.2 Condition Setting Screen

Since the IEEE802.3bj RS-FEC standard specifies either 5440 or 5280 bits per Block, it is possible to save 10 or more RS-FEC Blocks in one Capture Block (65536 bits). Selecting the smallest possible value at Number of Block (Figure 2.2) with a large Capture Memory Size increases the number of RS-FEC Blocks that can be captured at one time.

After completing the Capture settings, press the Capture button (Figure 2.1) to capture the data received each time an error occurs. Capture stops either when all the blocks specified at Number of Block have been captured or when the Capture button is pressed again.

The following explains the procedure for reading the captured data. The Acquisition button shown in Figure 2.3 is enabled either when all the Blocks specified as described in Figure 2.2 have been captured, or when the Capture button is pressed again after error generation.

Figure 2.3 Enabled Acquisition Button

The Capture Acquisition screen (Figure 2.4) is displayed when the Acquisition button is pressed. This screen is used to display which of the captured Block data in memory to display on-screen.

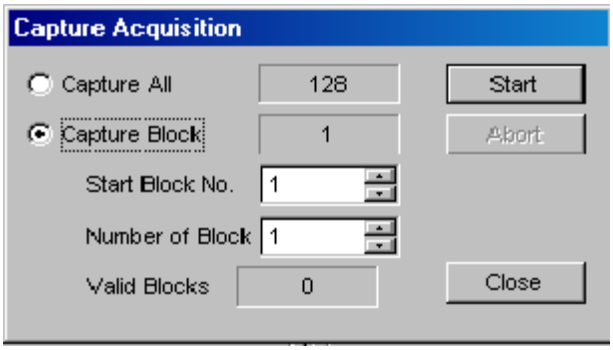

Figure 2.4 Capture Acquisition Screen

Select Capture All to view all captured Blocks. To confirm only some Blocks, select Capture Block and specify Start Block No. as well as Number of Block (from Start Block No.) and press the Start button to start capture to the screen.

There are three methods for displaying captured data: Bit Pattern, Bitmap, and Block. Whichever method is used, both Insertion Errors (bits that should be 0 are incorrectly 1) and Omission Errors (bits that should be 1 are incorrectly 0) can be checked. Bit Pattern displays the captured data in either binary or hexadecimal format. Bitmap does not display 0 or 1 data, but instead displays color-coded information about errors to provide an intuitive grasp of the overall distribution of errors. Block displays multiple blocks in parallel and is used for understanding specific bit sequences in which similar errors occur or not.

Analyses using the Bitmap and Bit Pattern formats are useful for FEC analysis. First, the Bitmap display is used to show whether errors occur either in bursts or randomly to clarify the overall trend in the error distribution. Next, the Bit Pattern display is used to clarify the type of distribution when errors are viewed in Symbol units.

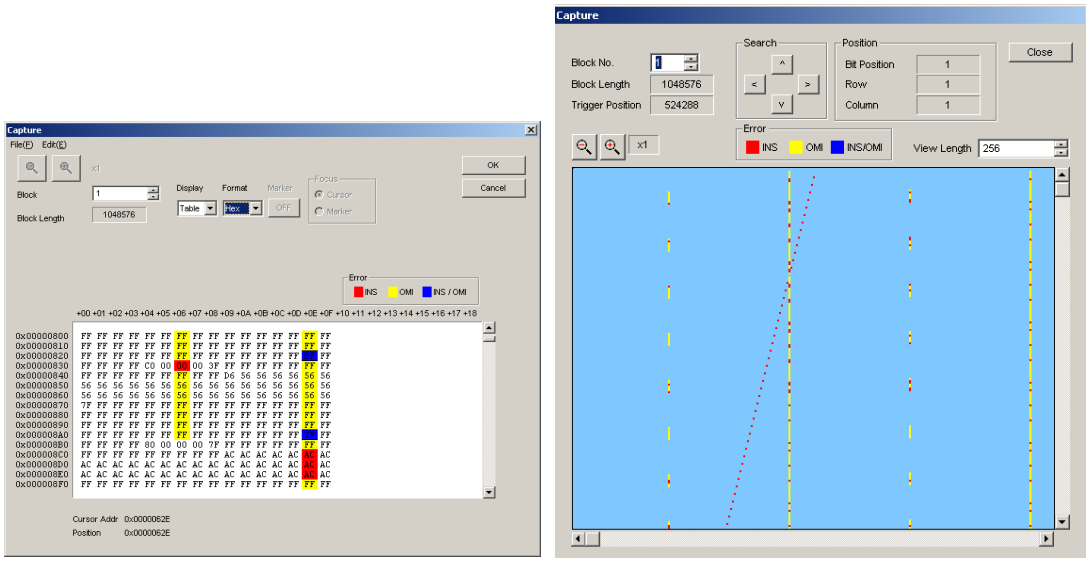

Figure 2.5 Bit Pattern Screen and Bitmap Screen

3. Understanding Error Counts

The captured data can be saved either as binary text (BIN Text Pattern) or hexadecimal text (HEX Text Pattern).

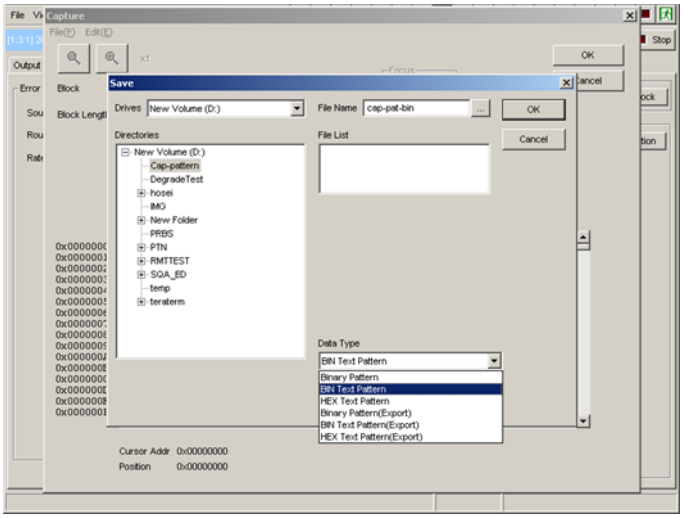

Figure 3.1 Saving Capture Data

Selecting BIN Text Pattern at Data Type of the File Menu shown above and saving the captured data creates the following three files when cap-pat-bin is specified as the file name for example:

cap-pat-bin.txt: Describes capture conditions and pattern data
cap-pat-bin 000.dtt: Saves Reference Pattern for captured receive pattern
cap-pat-bin 001.dtt: Saves position of errors for captured receive pattern

Parts with errors are indicated by “1” and parts without errors are indicated by “0”.

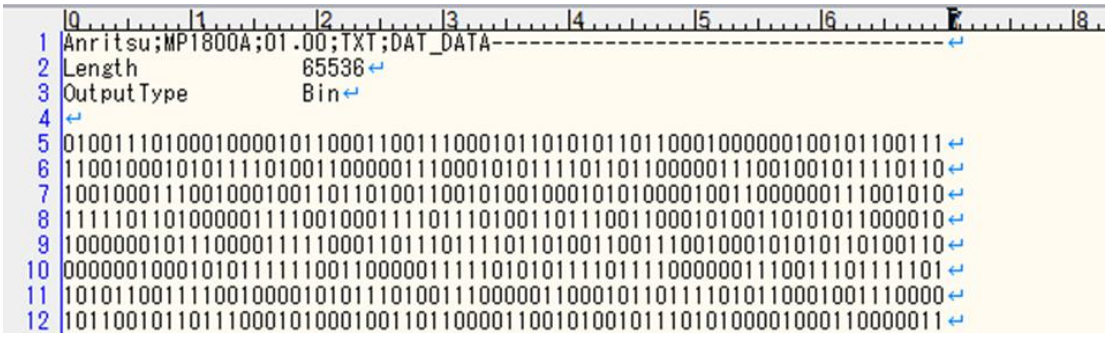

*Figure 3.2 Reference Pattern (***000.dtt)*

Figure 3.2 shows an example of a PRBS pattern.

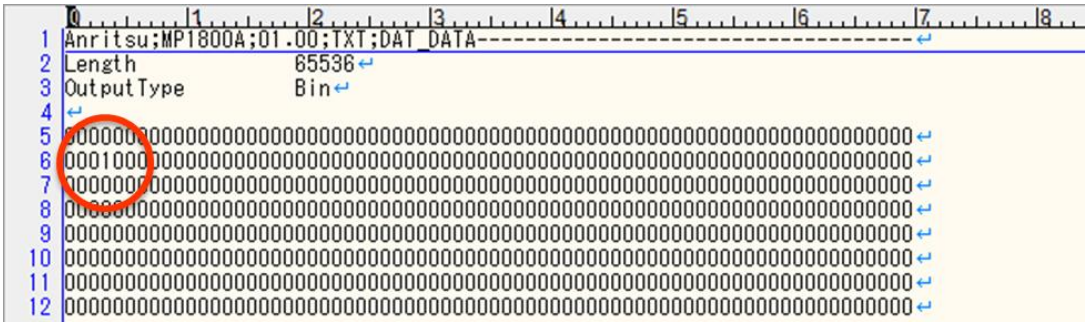

*Figure 3.3 Error bit information (***001.dtt)*

In the example of Figure 3.3, the location with 1 circled in red indicates an error. It is possible to clarify how many Symbols an error runs across while at the same time clarifying the overall number of errors by counting the number of “1” values in the ***001.dtt file including this error information.

Reference:

- IEEE 802.3bj™/D3.1, 13th February 2014
- Error Correction Code and Its Applications, Ohmsha, ISBN-13: 978-4274034862

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● **United States**
Anritsu Company
1155 East Collins Blvd., Suite 100, Richardson,
TX 75081, U.S.A.
Toll Free: 1-800-267-4878
Phone: +1-972-644-1777
Fax: +1-972-671-1877

● **Canada**
Anritsu Electronics Ltd.
700 Silver Seven Road, Suite 120, Kanata,
Ontario K2V 1C3, Canada
Phone: +1-613-591-2003
Fax: +1-613-591-1006

● **Brazil**
Anritsu Eletrônica Ltda.
Praça Amadeu Amaral, 27 - 1 Andar
01327-010 - Bela Vista - São Paulo - SP - Brazil
Phone: +55-11-3283-2511
Fax: +55-11-3288-6940

● **Mexico**
Anritsu Company, S.A. de C.V.
Av. Ejército Nacional No. 579 Piso 9, Col. Granada
11520 México, D.F., México
Phone: +52-55-1101-2370
Fax: +52-55-5254-3147

● **United Kingdom**
Anritsu EMEA Ltd.
200 Capability Green, Luton, Bedfordshire, LU1 3LU, U.K.
Phone: +44-1582-433200
Fax: +44-1582-731303

● **France**
Anritsu S.A.
12 avenue du Québec, Bâtiment Iris 1- Silic 612,
91140 VILLEBON SUR YVETTE, France
Phone: +33-1-60-92-15-50
Fax: +33-1-64-46-10-65

● **Germany**
Anritsu GmbH
Nemetschek Haus, Konrad-Zuse-Platz 1
81829 München, Germany
Phone: +49-89-442308-0
Fax: +49-89-442308-55

● **Italy**
Anritsu S.r.l.
Via Elio Vittorini 129, 00144 Roma, Italy
Phone: +39-6-509-9711
Fax: +39-6-502-2425

● **Sweden**
Anritsu AB
Kistagången 20B, 164 40 KISTA, Sweden
Phone: +46-8-534-707-00
Fax: +46-8-534-707-30

● **Finland**
Anritsu AB
Teknobulevardi 3-5, FI-01530 VANTAA, Finland
Phone: +358-20-741-8100
Fax: +358-20-741-8111

● **Denmark**
Anritsu A/S
Kay Fiskers Plads 9, 2300 Copenhagen S, Denmark
Phone: +45-7211-2200
Fax: +45-7211-2210

● **Russia**
Anritsu EMEA Ltd.
Representation Office in Russia
Tverskaya str. 16/2, bld. 1, 7th floor.
Russia, 125009, Moscow
Phone: +7-495-363-1694
Fax: +7-495-935-8962

● **United Arab Emirates**
Anritsu EMEA Ltd.
Dubai Liaison Office
P O Box 500413 - Dubai Internet City
Al Thuraya Building, Tower 1, Suit 701, 7th Floor
Dubai, United Arab Emirates
Phone: +971-4-3670352
Fax: +971-4-3688460

● **India**
Anritsu India Private Limited
2nd & 3rd Floor, #837/1, Binnamangla 1st Stage,
Indiranagar, 100ft Road, Bangalore - 560038, India
Phone: +91-80-4058-1300
Fax: +91-80-4058-1301

● **Singapore**
Anritsu Pte. Ltd.
11 Chang Charn Road, #04-01, Shriro House
Singapore 159640
Phone: +65-6282-2400
Fax: +65-6282-2533

● **P.R. China (Shanghai)**
Anritsu (China) Co., Ltd.
Room 2701-2705, Tower A,
New Caohejing International Business Center
No. 391 Gui Ping Road Shanghai, 200233, P.R. China
Phone: +86-21-6237-0898
Fax: +86-21-6237-0899

● **P.R. China (Hong Kong)**
Anritsu Company Ltd.
Unit 1006-7, 10/F., Greenfield Tower, Concordia Plaza,
No. 1 Science Museum Road, Tsim Sha Tsui East,
Kowloon, Hong Kong, P.R. China
Phone: +852-2301-4980
Fax: +852-2301-3545

● **Japan**
Anritsu Corporation
8-5, Tamura-cho, Atsugi-shi, Kanagawa, 243-0016 Japan
Phone: +81-46-296-1221
Fax: +81-46-296-1238

● **Korea**
Anritsu Corporation, Ltd.
5FL, 235 Pangyoyeok-ro, Bundang-gu, Seongnam-si,
Gyeonggi-do, 463-400 Korea
Phone: +82-31-696-7750
Fax: +82-31-696-7751

● **Australia**
Anritsu Pty. Ltd.
Unit 21/270 Ferntree Gully Road, Notting Hill,
Victoria 3168, Australia
Phone: +61-3-9558-8177
Fax: +61-3-9558-8255

● **Taiwan**
Anritsu Company Inc.
7F, No. 316, Sec. 1, NeiHu Rd., Taipei 114, Taiwan
Phone: +886-2-8751-1816
Fax: +886-2-8751-1817

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