

# MP8931A

Bit Error Rate Tester

1 kHz to 155 MHz





The MP8931A Bit Error Rate Tester has digital broadcast interfaces (DVB-ASI, DVB-SPI) in addition to the general bit-error-rate test function. It is suitable for quality evaluation at device production/construction and for maintenance after installation.

## Features

- Clock frequency: 1 kHz to 155 MHz
- Pseudo-random (PN9/15/23) and ALL0/1, 1010 fixed pattern measurement
- MP8931A includes conventional NRZ I/F (TTL-Clock/Data/Enable) as standard equipment, as well as DVB-ASI\*<sup>1</sup> and DVB-SPI\*<sup>2</sup>, both of which are for digital broadcasting
- Selectable error rate measurement part in an DVB I/F data packet is possible
- Error insertion
- GPIB/RS-232C I/F
- Small design (Thin case)

\*1: DVB-ASI: Digital Video Broadcasting - Asynchronous Serial Interface

\*2: DVB-SPI: Digital Video Broadcasting - Synchronous Parallel Interface

# MP8931A

## Bit Error Rate Tester

1 kHz to 155 MHz

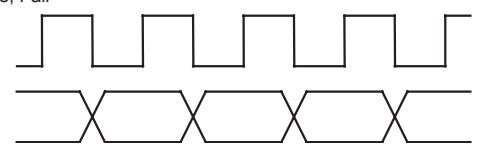
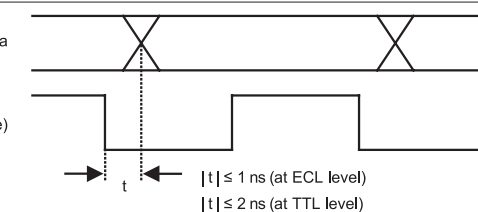
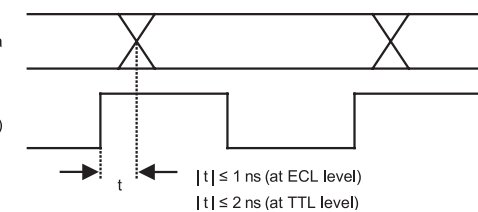


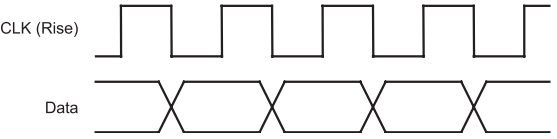
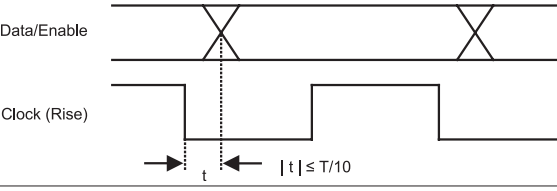
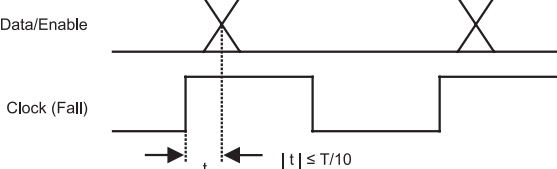
# Specifications

## (1) Common Items

Item	Specifications
Measurement Interface	NRZ, DVB-SPI, DVB-ASI
Remote Control Interface	GPIO, RS-232C
Internal Clock Frequency Setting	Setting range: 1 kHz to 155 MHz, Resolution: 1 Hz, Accuracy: $\pm 10$ ppm
Transmission/Measurement Pattern	Pseudo-random code: PN9, PN9_REV, PN15, PN15_REV, PN23, PN23_REV, ALL"0", ALL"1", "1010" Synchronization establish condition: <ul style="list-style-type: none"> <li>• NRZ: 50 bits +N bits (N: Number of stages, "0" when fixed), when normal</li> <li>• DVB-SPI, SVB-ASI: <math>8 \times (8 + N)</math> bits, when normal</li> </ul> Synchronization loss condition: when 6 error bits of 64 bits detected
Error Addition	Manual, Continuous ( $10^{-2}$ , $10^{-3}$ , $10^{-4}$ , $10^{-5}$ , $10^{-6}$ , $10^{-7}$ )
Measurement Time/Number of Bits	Measurement time (000h00m01s00 to 999h59m59s90) Number of measurement bits ( $10^3$ to $10^{15}$ ) Repeat
AutoSync	On, Off
Burst	Disable, Enable
Status Indicator LED	Counting, Sync Loss, Signal Loss, Errors
Screen Display	[1] Switch between "Error rate" and "Number of errors/total count" [2] Over Flow display [3] Error display [4] Passed (elapsed) time/left (remaining) time display [5] Current/Last display
Display Screen Control	Screen display Off: None or 1, 5, 10, 20, 30, 40, 50, 60 min Brightness adjustment: 25, 50, 75, 100%
Auto Save of Setting Data	Saves the set parameters just before power-off and sets them automatically at the next power-on
Power Supply	Voltage: 85 to 250 V (ac) Frequency: 47.5 Hz to 63 Hz
Power Consumption	$\leq 50$ VA
Operating Temperature/Humidity	0° to 50°C, $\leq 80\%$ (Non condensing)
Dimensions	426 (W) $\times$ 88 (H) $\times$ 451 (D) mm, excluding protrusions
Mass	$\leq 7$ kg

## (2) NRZ Interface

Item		Specifications	
Common (I/O)	Connector	BNC (75 Ω)	
	Signal Type	Data/Clock	
Output Signal	Common to Data/Clock	Level	<ECL> High: $-0.9 \pm 0.2$ V, Low: $-1.7 \pm 0.2$ V <TTL> High: $+2.5 \pm 0.3$ V, Low: $0 \pm 0.3$ V
		Termination Voltage Conditions	ECL: $-2$ V, TTL: GND
		Termination	Fixed to 75 Ω
		Polarity Switching	Data: Positive, Negative Clock: Rise, Fall 
		Enable/Disable	Enable/Disable (fixed to Low) setting
	Data	Bit Rate	1 kHz to 155 MHz, Resolution: 1 Hz
		Waveform	NRZ
		Tr/Tf (20 to 80%)	ECL: $\leq 1$ ns, TTL: $\leq 1.5$ ns
	Clock	Frequency	1 kHz to 155 MHz, Resolution: 1 Hz Accuracy: $\pm 10$ ppm
		Duty	50% $\pm 10\%$
Tr/Tf (20 to 80%)		ECL: $\leq 1$ ns, TTL: $\leq 1.5$ ns	
Output Phase			
			

Item		Specifications		
Input Signal	Signal Type	Data/Clock/Enable		
	Common to Data/Clock Enable	Level	<ECL> High: 0 to -1.0 V, Low: -1.5 V to -2.5 V <TTL> High: +1.8 V to +5.0 V, Low: 0 to +1.0 V <Variable> Shown below	
		Termination Voltage Conditions	ECL: -2 V, TTL: GND Variable: -2.5 V to +3.3 V (user-defined) Resolution: 0.1 V	
		Threshold Voltage Conditions	ECL: -1.3 V, TTL: +1.4 V Variable: -2 V to +3 V (user-defined) Resolution: 0.1 V	
		Termination	75 Ω/1 MΩ	
	Polarity Switching	Data: Positive, Negative Clock: Rise, Fall Enable: Positive, Negative, Off  		
	Data/Enable	Waveform	NRZ	
	Clock	Frequency	1 kHz to 155 MHz, Accuracy: ±100 ppm	
		Duty	50 ±10%	
		Pulse Width	≥3 ns	
		Input Phase	Data/Enable	
			Clock (Fall)	

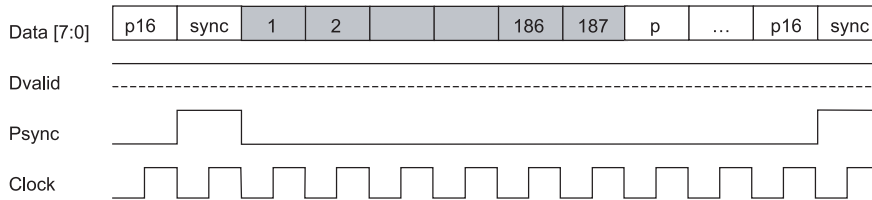
### (3) DVB-SPI interface

Item		Specifications																																																													
Common (I/O)	Connector	D_Sub 25 (Female) Table: Pin Contact Assignment <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Pin</th> <th>Signal</th> <th>Pin</th> <th>Signal</th> <th>Pin</th> <th>Signal</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>Clock A</td> <td>10</td> <td>Data 0 A</td> <td>18</td> <td>Data 5 B</td> </tr> <tr> <td>2</td> <td>System GND</td> <td>11</td> <td>DVALID A</td> <td>19</td> <td>Data 4 B</td> </tr> <tr> <td>3</td> <td>Data 7 A (MSB)</td> <td>12</td> <td>PSYNC A</td> <td>20</td> <td>Data 3 B</td> </tr> <tr> <td>4</td> <td>Data 6 A</td> <td>13</td> <td>Cable shield</td> <td>21</td> <td>Data 2 B</td> </tr> <tr> <td>5</td> <td>Data 5 A</td> <td>14</td> <td>Clock B</td> <td>22</td> <td>Data 1 B</td> </tr> <tr> <td>6</td> <td>Data 4 A</td> <td>15</td> <td>System GND</td> <td>23</td> <td>Data 0 B</td> </tr> <tr> <td>7</td> <td>Data 3 A</td> <td>16</td> <td>Data 7 B (MSB)</td> <td>24</td> <td>DVALID B</td> </tr> <tr> <td>8</td> <td>Data 2 A</td> <td>17</td> <td>Data 6 B</td> <td>25</td> <td>PSYNC B</td> </tr> <tr> <td>9</td> <td>Data 1 A</td> <td></td> <td></td> <td></td> <td></td> </tr> </tbody> </table> Logical conversion 1: Voltage of A is higher than that of B 0: Voltage of A is lower than that of B		Pin	Signal	Pin	Signal	Pin	Signal	1	Clock A	10	Data 0 A	18	Data 5 B	2	System GND	11	DVALID A	19	Data 4 B	3	Data 7 A (MSB)	12	PSYNC A	20	Data 3 B	4	Data 6 A	13	Cable shield	21	Data 2 B	5	Data 5 A	14	Clock B	22	Data 1 B	6	Data 4 A	15	System GND	23	Data 0 B	7	Data 3 A	16	Data 7 B (MSB)	24	DVALID B	8	Data 2 A	17	Data 6 B	25	PSYNC B	9	Data 1 A				
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9	Data 1 A																																																														
Termination	100 Ω																																																														
Signal Type	Data [7:0], Clock, Dvalid, Psync																																																														
Packet Type	[1] 204: (1) +187 + (16) packets [2] 188: (1) +187 packets [3] 204: (1+3) +184 + (16) packets [4] 188: (1+3) +184 packets [5] 204: (1) + 203 packets [6] 204: (1+3) + 200 packets																																																														
Output Signal	Common to Clock, Data DVALID, PSYNC	Level (LVDS)	Offset Voltage: 1.125 V to 1.35 V Differential Output Voltage: 247 mV to 454 mV																																																												
		Tr/Tf (20 to 80%)	≤T/7																																																												
		Enable/Disable	Enable/Disable (fixed to Low) setting																																																												
	Data	Data Out of PN Range	"Sync": 47 h (fixed) "16 Valid extra bytes", "PID": ALL1 (fixed)																																																												
	DVALID	Level	Fixed to "High"																																																												
	Clock (Byte clock)	Frequency	10 kHz to 13.5 MHz, Resolution: 1 Hz																																																												
		Duty	50 ±10%																																																												
	Output Phase	<p style="text-align: center;"> <math> t  \leq T/10</math>  <math>T = 1/f</math> </p>																																																													
Input Signal	Common to Clock, Data DVALID, PSYNC	Level (LVDS)	0.1 Vp-p to 2.0 Vp-p																																																												
		Data	Data Out of PN Range	Data are not compared for "Sync," "16 Valid extra bytes" or "PID"																																																											
		Frequency	10 kHz to 13.5 MHz																																																												
	Clock (Byte clock)	Duty	50 ±10%																																																												
		Input Phase	<p style="text-align: center;">                     Clock Period: <math>T = 1/f</math>                      Data Hold Time: <math>td = T/2 \pm T/10</math> </p>																																																												
Monitor Output	Enable/Disable (high-impedance) setting																																																														

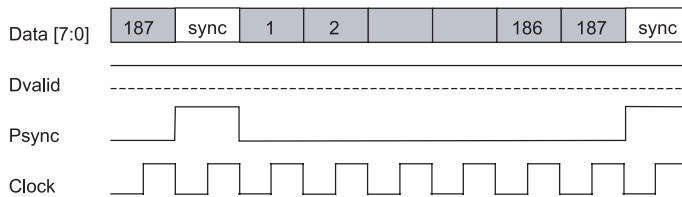
\*: An external clock (byte clock) can be used when this interface is selected.

## Timing

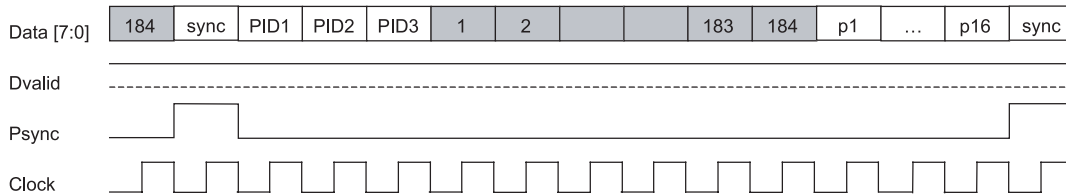
[1] When 187 bytes of 204-byte packet are measurement target:  $(1) + 187 + (16)$



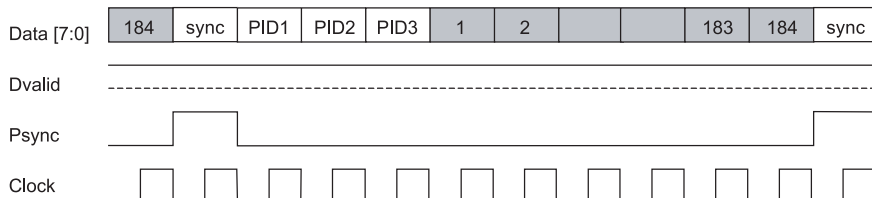
[2] When 187 bytes of 188-byte packet are measurement target:  $(1) + 187$



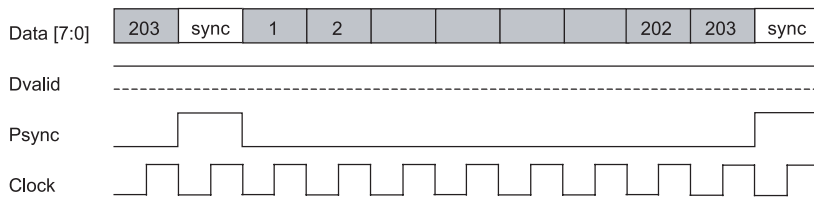
[3] When 184 bytes of 204-byte packet are measurement target:  $(1+3) + 184 + (16)$



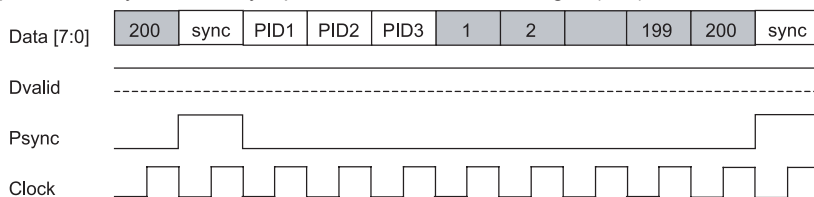
[4] When 184 bytes of 188-byte packet are measurement target:  $(1+3) + 184$



[5] When 203 bytes of 204-byte packet are measurement target:  $(1) + 203$



[6] When 200 bytes of 204-byte packet are measurement target:  $(1+3) + 200$



#### (4) DVB-ASI Interface

Item		Specifications
Common (I/O)	Connector	BNC (75 Ω)
	Termination	75 Ω
	Frequency	270 MHz (Internal clock)
	Packet Type	[1] 204: (1) + 187 + (16) packets [2] 188: (1) + 187 packets [3] 204: (1+3) + 184 + (16) packets [4] 188: (1+3) + 184 packets [5] 204: (1) + 203 packets [6] 204: (1+3) + 200 packets
Output	Level	800 mVp-p ±10%
	Tr/Tf (20 to 80%)	≤1.2 ns
	Line Rate	270 Mbaud ±100 ppm
	Data Out of PN Range	"Sync": 47 h (fixed) "16 Valid extra bytes," "PID": ALL1 (fixed)
	Output Mode	Packet mode
	Data Rate	1 MHz to 27 MHz, Resolution: 1 MHz When set to 27 MHz: Two "Stuffing Data" are inserted between packets
Input	Enable/Disable	Enable/Disable (fixed to Low) setting
	Level	Min. Sensitivity: 200 mV Max. Input Voltage: 880 mV
	Impedance	75 Ω
	Parity Check (except "Sync")	Data is not compared for "16 Valid extra bytes" and "PID"
	Frame Sync Establishment Conditions	"Sync" (47 h) detection, successively for three frames
Monitor Output	Frame Sync Loss Conditions	None (ignored)
	Monitor Output	Enable/Disable (High impedance) setting

#### (5) External Clock Input

Item	Specifications
Level	<ECL> High: 0 to -1.0 V, Low: -1.5 V to -2.5 V <TTL> High: +1.8 V to +5.0 V, Low: 0 to +1.0 V
Terminal Voltage Conditions	ECL: -2 V, TTL: GND
Threshold Voltage Conditions	ECL: -1.3 V, TTL: +1.4 V
Termination	75 Ω/1 MΩ
Frequency	ECL: 1 kHz to 155 MHz, TTL: 1 kHz to 100 MHz Accuracy: ±100 ppm
Duty	50 ±10%
Pulse Width	≥3 ns



# Ordering information

Please specify the model/order number, name and quantity when ordering.

The names listed in the chart below are Order Names. The actual name of the item may differ from the Order Name.

Model/Order No	Name
MP8931A	<b>Main frame</b> Bit Error Rate Tester
	<b>Standard accessories</b>
F0012	Power Cord: 1 pc
W2249AE	Fuse, 3.15 A: 1 pc
	MP8931A Operation Manual: 1 copy
	<b>Optional parts</b>
B0329A	Front Cover for 1MW 2U (Protective Cover)
J1011	D-Sub 25 Cable
J0026A	Coaxial Cord, 1 m
J0007	408JE-104, GPIB Cable (1 m)
J0008	GPIB Cable, 2 m (408JE-102)
J1256A	RS-232C Cable (1.5 m)

## Anritsu Corporation

5-1-1 Onna, Atsugi-shi, Kanagawa, 243-8555 Japan  
Phone: +81-46-223-1111  
Fax: +81-46-296-1238

## ● U.S.A.

### Anritsu Company

1155 East Collins Blvd., Suite 100, Richardson,  
TX 75081, U.S.A.  
Toll Free: 1-800-267-4878  
Phone: +1-972-644-1777  
Fax: +1-972-671-1877

## ● Canada

### Anritsu Electronics Ltd.

700 Silver Seven Road, Suite 120, Kanata,  
Ontario K2V 1C3, Canada  
Phone: +1-613-591-2003  
Fax: +1-613-591-1006

## ● Brazil

### Anritsu Eletrônica Ltda.

Praça Amadeu Amaral, 27 - 1 Andar  
01327-010 - Bela Vista - São Paulo - SP - Brasil  
Phone: +55-11-3283-2511  
Fax: +55-11-3288-6940

## ● Mexico

### Anritsu Company, S.A. de C.V.

Av. Ejército Nacional No. 579 Piso 9, Col. Granada  
11520 México, D.F., México  
Phone: +52-55-1101-2370  
Fax: +52-55-5254-3147

## ● U.K.

### Anritsu EMEA Ltd.

200 Capability Green, Luton, Bedfordshire, LU1 3LU, U.K.  
Phone: +44-1582-433200  
Fax: +44-1582-731303

## ● France

### Anritsu S.A.

12 avenue du Québec, Bâtiment Iris 1- Silic 612,  
91140 VILLEBON SUR YVETTE, France  
Phone: +33-1-60-92-15-50  
Fax: +33-1-64-46-10-65

## ● Germany

### Anritsu GmbH

Nemetschek Haus, Konrad-Zuse-Platz 1  
81829 München, Germany  
Phone: +49-89-442308-0  
Fax: +49-89-442308-55

## ● Italy

### Anritsu S.r.l.

Via Elio Vittorini 129, 00144 Roma, Italy  
Phone: +39-6-509-9711  
Fax: +39-6-502-2425

## ● Sweden

### Anritsu AB

Borgafjordsgatan 13, 164 40 KISTA, Sweden  
Phone: +46-8-534-707-00  
Fax: +46-8-534-707-30

## ● Finland

### Anritsu AB

Teknobulevardi 3-5, FI-01530 VANTAA, Finland  
Phone: +358-20-741-8100  
Fax: +358-20-741-8111

## ● Denmark

### Anritsu A/S (Service Assurance)

### Anritsu AB (Test & Measurement)

Kirkebjerg Allé 90, DK-2605 Brøndby, Denmark  
Phone: +45-7211-2200  
Fax: +45-7211-2210

## ● Russia

### Anritsu EMEA Ltd.

### Representation Office in Russia

Tverskaya str. 16/2, bld. 1, 7th floor.  
Russia, 125009, Moscow  
Phone: +7-495-363-1694  
Fax: +7-495-935-8962

## ● United Arab Emirates

### Anritsu EMEA Ltd.

### Dubai Liaison Office

P O Box 500413 - Dubai Internet City  
Al Thuraya Building, Tower 1, Suit 701, 7th Floor  
Dubai, United Arab Emirates  
Phone: +971-4-3670352  
Fax: +971-4-3688460

## ● Singapore

### Anritsu Pte. Ltd.

60 Alexandra Terrace, #02-08, The Comtech (Lobby A)  
Singapore 118502  
Phone: +65-6282-2400  
Fax: +65-6282-2533

## ● India

### Anritsu Pte. Ltd.

### India Branch Office

3rd Floor, Shri Lakshminarayan Niwas, #2726, 80 ft Road,  
HAL 3rd Stage, Bangalore - 560 075, India  
Phone: +91-80-4058-1300  
Fax: +91-80-4058-1301

## ● P.R. China (Hong Kong)

### Anritsu Company Ltd.

Units 4 & 5, 28th Floor, Greenfield Tower, Concordia Plaza,  
No. 1 Science Museum Road, Tsim Sha Tsui East,  
Kowloon, Hong Kong  
Phone: +852-2301-4980  
Fax: +852-2301-3545

## ● P.R. China (Beijing)

### Anritsu Company Ltd.

### Beijing Representative Office

Room 2008, Beijing Fortune Building,  
No. 5, Dong-San-Huan Bei Road,  
Chao-Yang District, Beijing 100004, P.R. China  
Phone: +86-10-6590-9230  
Fax: +86-10-6590-9235

## ● Korea

### Anritsu Corporation, Ltd.

8F Hyunjuk Building, 832-41, Yeoksam Dong,  
Kangnam-ku, Seoul, 135-080, Korea  
Phone: +82-2-553-6603  
Fax: +82-2-553-6604

## ● Australia

### Anritsu Pty. Ltd.

Unit 21/270 Ferntree Gully Road, Notting Hill,  
Victoria 3168, Australia  
Phone: +61-3-9558-8177  
Fax: +61-3-9558-8255

## ● Taiwan

### Anritsu Company Inc.

7F, No. 316, Sec. 1, Neihu Rd., Taipei 114, Taiwan  
Phone: +886-2-8751-1816  
Fax: +886-2-8751-1817

Please Contact: