# Clock Recovery Options for 32-Gbit/s High-Sensitivity ED

MU18304xB-022 2.4 to 28.1 Gbit/s
MU18304xB-023 25.5 to 32.1 Gbit/s

MP1800A Series Signal Quality Analyzer

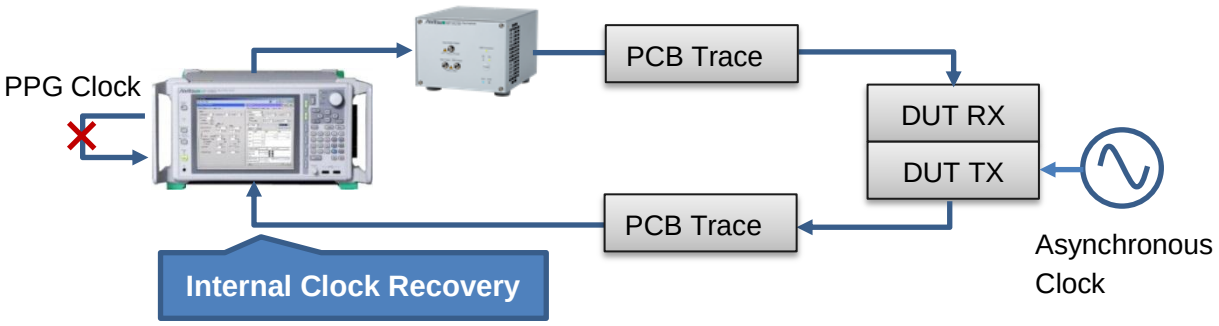
The rapid growth of cloud computing services has seen explosive increases in data center traffic, resulting in investigation of new high-speed communications standards, such as 100GBASE-SR4, 100GBASE-KR4, etc., to increase internal processing speeds of server and network equipment as well as communications speeds between equipment. Physical layer devices, such as SERDES, sometimes have different Tx and Rx Clock systems and Clock Recovery is required at the Error Detector for jitter tolerance tests. Additionally, since transmission using Multi-Mode Fiber (MMF) causes generation of jitter and wander components in the Rx module, Clock Recovery at the Error Detector is similarly required.
The Anritsu MU183040B/MU183041B High-Sensitivity ED is a plug-in module for the MP1800A Signal Quality Analyzer, supporting multichannel BER measurements up to 32.1 Gbit/s.
Installing this Clock Recovery option supports stress jitter tolerance tests of PHY devices with different Tx and Rx clocks, BER measurements of AOC devices, and simultaneous multichannel measurements, offering even more accurate and ideal signal integrity analyses.

## Applications

- ✓ High-Speed Backplanes and Cables: 100GbE (100GBASE-KR4, CR4)
- ✓ SERDES, CDR: CEI-25G, CEI-28G-VSR
- ✓ AOC (Active Optical Cables): InfiniBand™ FDR (14G), EDR (26G)
- ✓ Optical Transceiver Modules: CFP/CFP2/CFP4, QSFP/QSFP28, CXP for 16G/32G Fibre Channel, 100GbE (100GBASE-SR4, LR4, ER4), OTU4 (28Gx4)

## Features

- ✓ Built-in Clock Recovery: TRx Asynchronous SERDES Jitter Tolerance Tests
- ✓ Variable Clock Recovery Loop Bandwidth: Bit-rate/1667, Bit-rate/2578, 1MHz to 17 MHz*3
- ✓ High-Sensitivity ED: 10 mV (typical, Single-end, EYE Height)



## ■ Specifications
### MU183040B High-Sensitivity ED, MU183041B 4ch High-Sensitivity ED

| Items | Specifications |
|---|---|
| Operating Bit-Rate | 2.4 Gbit/s to 28.1 Gbit/s<br>MU183040B/41B-001: Extendible, 2.4 Gbit/s to 32.1 Gbit/s |
| Data Input | Differential, K-connector, 50Ω<br>MU183040B-010: 1ch<br>MU183040B-020: 2ch<br>MU183041B: 4ch |
| Input Amplitude | 0.05 Vp-p to 1.0 Vp-p |
| Sensitivity | EYE Height: 10 mVp-p (typical at 28.1 Gbit/s, single-end, at equivalent to BER 1E-9 with 70 GHz bandwidth sampling scope)<br>EYE Amplitude: 15 mVp-p (typical at 28.1 Gbit/s, single-end),<br>≤25 mVp-p (at 28.1 Gbit/s, single-end) |
| **Clock Recovery** NEW | **Clock Recovery from CH-1 Data input, internal distribution to each channel*1** |
| **Operating Bit-Rate** | **MU183040B/41B-022: 2.4 to 28.1 Gbit/s**<br>**MU183040B/41B-023: 25.5 to 32.1 Gbit/s*2** |
| **Loop Band Width Setting** | **MU183040B/41B-022: Bit-rate/1667, Bit-rate/2578,**<br>**Variable 3 to 17 MHz*3 (1-MHz steps)**<br>**MU183040B/41B-023: Bit-rate/1667, Bit-rate/2578** |
| External Clock Input | Single-end, 1ch, SMA connector, 50Ω |
| Frequency | Half-rate operation (1.2 GHz to 16.05 GHz) |
| Amplitude | 0.3 Vp-p to 1.0 Vp-p (–6.5 to +4.0 dBm) |
| Clock Delay Range | –1000 m to +1000 mUI/2-mUI steps |
| Pattern Detection | |
| PRBS | $2^n$-1 (n = 7, 9, 10, 11, 15, 20, 23, 31), Logic POS/NEG |
| Programmable DATA | Length 2 to 268,435,456 bits/ch, 1-bit steps |
| Aux Output | SMA Connector, 50Ω<br>Divided Clock (1/4 to 1/512), Pattern Sync., Recovered Clock (1/4 to 1/512) |
| Analysis Functions | Auto Adjust (4ch simultaneous, <1 s search)<br>Auto Search, Bathtub Jitter, EYE Diagram, EYE Margin |

*1: MU183041B-023 recovers Clock from CH-1 Data input and distributes to CH-1 and CH-2. Also recovers Clock from CH-3 Data input and distributes to CH-3 and CH-4.

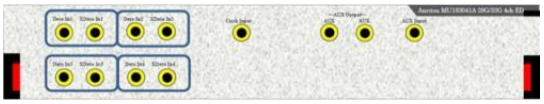
*2: MU183040B/41B-001 must be installed.

*3: Upper setting band depends on bit-rate; 17 MHz at 28.1 Gbit/s

## ■ Ordering Information

| Model | Name |
|---|---|
| MU183040B | 28G/32G bit/s High-Sensitivity ED |
| MU183040B-001 | 32G bit/s Extension |
| MU183040B-010 | 1ch ED |
| MU183040B-020 | 2ch ED |
| **MU183040B-022** NEW | **2.4 to 28.1 Gbit/s Clock Recovery** |
| **MU183040B-023** NEW | **25.5 to 32.1 Gbit/s Clock Recovery** |
| MU183041B | 28G/32G bit/s 4ch High-Sensitivity ED |
| MU183041B-001 | 32G bit/s Extension |
| **MU183041B-022** NEW | **2.4 to 28.1 Gbit/s Clock Recovery** |
| **MU183041B-023** NEW | **25.5 to 32.1 Gbit/s Clock Recovery** |

MU183040B (1ch or 2ch)



MU183041B (4ch)

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