



## 125 M to 12.5 Gbit/s BERT

MP2100A/MP2101A-090 PPG/ED Bit Rate Extension for PPG/ED

### Features

- **Wide bit-rate band with PPG/ED supporting various applications**

<Applications>

- ✓ CPRI (x1, x2, x4, x5, x8, x10) , OBSAI (RP3, RP3 x2, RP3 x4)
- ✓ Infiniband (x1, x2, x4)
- ✓ XAUI (3.125G)
- ✓ USB 3.0
- ✓ PCIe (1.0, 2.0, 3.0)
- ✓ SATA (1.5G, 3G, 6G), SAS
- ✓ GbE, 2 GbE, 10 GbE (WAN, LAN, OTU1e, OTU2e)
- ✓ FC, 2GFC, 3GFC, 4GFC, 8GFC, 10GFC, 10GFC FEC
- ✓ OC-3/STM-1, OC-12/STM-4, OC-24, OC-48/STM-16, OC-192/STM-64, OC-192/STM-64 FEC (G.975)
- ✓ OTU-1, OTU-2

<Bit rates>

- ✓ 8 to 12.5 Gbit/s
- ✓ 4 to 6.25 Gbit/s
- ✓ 2 to 3.125 Gbit/s
- ✓ 1 to 1.5625 Gbit/s
- ✓ 500 to 781.25 Mbit/s
- ✓ 250 to 390.625 Mbit/s
- ✓ 125 to 195.312 Mbit/s

- **Internal clock data recovery (CDR) and asynchronous data recovery<sup>(\*)</sup>**

The error detector (ED) uses internal CDR for bit rates at 4G to 6.25G and 8G to 12.5G. The ED sync. clock output (recovered clock output) can be used as the EYE/Pulse Scope trigger clock.

Asynchronous data recovery is used for BER testing at bit rates below 3.125G. Asynchronous data recovery samples incoming data signals using an over-clock and supports wideband BER measurements at low cost.

(\*1) Patent pending



# Specifications

## PPG

Item	Specifications	
	With MP2100A/MP2101A-090	Without MP2100A/MP2101A-090
Bit Rate	Variable bit-rate range (1-Kbit/s steps) 8 to 12.5 Gbit/s  1/N bit-rate operation range N = 2: 4 to 6.25 Gbit/s N = 4: 2 to 3.125 Gbit/s N = 8: 1 to 1.5625 Gbit/s N = 16: 500 to 781.25 Mbit/s N = 32: 250 to 390.625 Mbit/s N = 64: 125 to 195.312 Mbit/s	Variable bit-rate range (1-Kbit/s steps) 8.5 to 11.32 Gbit/s  1/N bit-rate operation range N = 2: 4.25G to 5.66Gbit/s N = 4: 2.125G to 2.83Gbit/s N = 8: 1.0625G to 1.415Gbit/s N = 16: 531.25M to 701.5Mbit/s N = 32: 265.625M to 353.75Mbit/s N = 64: 132.813M to 176.875Mbit/s

## ED

Item	Specifications	
	With MP2100A/MP2101A-090	Without MP2100A/MP2101A-090
Bit Rate	Variable bit-rate range (1-Kbit/s steps) 8 to 12.5 Gbit/s  1/N bit-rate operation range <sup>(*)2</sup> N = 2: 4 to 6.25Gbit/s N = 4: 2 to 3.125 Gbit/s N = 8: 1 to 1.5625 Gbit/s N = 16: 500 to 781.25 Mbit/s N = 32: 250 to 390.625 Mbit/s N = 64: 125 to 195.312 Mbit/s	Variable bit-rate range (1-Kbit/s steps) 8.5 to 11.32 Gbit/s 4.25G to 5.66Gbit/s
Electrical Data Input Amplitude	0.1 to 0.8 V (p-p) <sup>(*)3</sup> , AC coupling : 8.0 to 11.32 Gbit/s and 1/N bit rate above  0.25 to 0.8 V (p-p) <sup>(*)4</sup> , AC coupling: 11.320001 to 12.5 Gbit/s and 1/N bit rate above	0.1 to 0.8 V (p-p) <sup>(*)3</sup> , AC coupling: 8.5 to 11.32 Gbit/s and 1/N bit rate above

Items not specified here are specified in the standard MP210xA data sheet.  
 These preliminary contents and specifications may be changed without prior notice.

(\*)2 When N is 4 or higher, asynchronous data recovery is used for the ED. In this case, the ED sync. clock cannot be used.

(\*)3 10.3125G, single-ended 0.1 Vp-p, loopback, PRBS31, mark ratio 1/2, 20° to 30°C, BER <1E-12

(\*)4 12.288G, single-ended 0.25 Vp-p, loopback, PRBS31, mark ratio 1/2, 20° to 30°C, BER <1E-12

## Ordering Information

Please specify the model/order number, name and quantity when ordering.  
 Note that the model name may be different from the list.

### MP2100A BERTWave

Model/Order No.	Name
Main Frame	
MP2100A	BERTwave
Option	
MP2100A -001	Dual Electrical Receiver
MP2100A-005	Extended PPG/ED Channel
MP2100A -007	1ch Electrical BERT and Optical/Single-ended Electrical Scope
MP2100A -030	GPIO
MP2100A -050	XFP Slot
MP2100A -051	SFP + Slot
MP2100A -055	Clock Recovery for Eye/Pulse Scope
MP2100A-061 to 86	Filter and Filter Bank
MP2102A-062	2 High Bit Rate Filter Bank
MP2102A-063	3 to 4 High Bit Rate Filter Bank
MP2100A-090	Bit Rate Extension for PPG/ED
MP2100A -091	ED High Sensitivity

### MP2101A BERTWave PE

Model/Order No.	Name
Main Frame	
MP2101A	BERTWave PE
Option	
MP2101A -011	1CH PPG/ED
MP2101A -012	2CH PPG/ED
MP2101A-050	XFP Slot
MP2101A-051	SFP+ Slot
MP2100A -090	Bit Rate Extension for PPG/ED
MP2101A -091	ED High Sensitivity