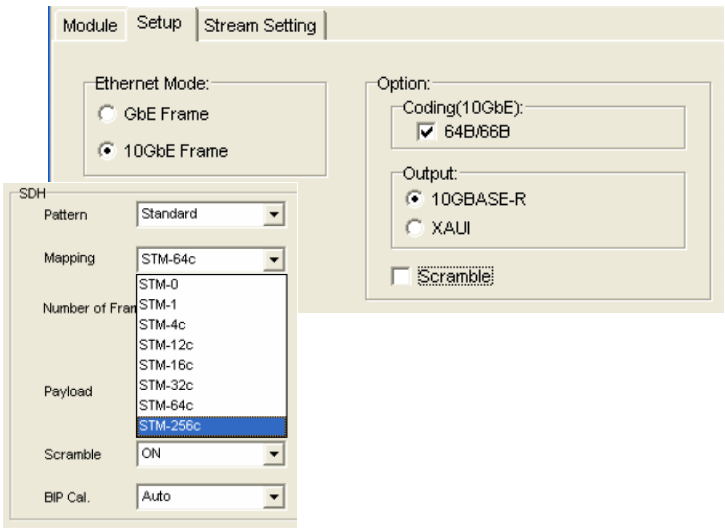
Leaflet

BERTWave

Anritsu

MX180001A SONET/SDH Pattern Editor
MX180003A GbE/10GbE Pattern Editor

MP2100A BERTWave Series



Supports MP2100A pattern editing software

The MP2100A Programmable Pattern File is compatible with the MP1800A. A Programmable Pattern File created using **Pattern Editor** can be read by the MP2100A/MP2101A to perform BER measurements using SDH/SONET and GbE/10GbE frame patterns. Note: There are some restrictions; see the reverse side for more details.

Key Features

The MP2100A/MP2101A uses an embedded Windows OS. **Pattern Editor runs on the BERTWave without an external PC** because it is a Windows application.

■ MX1800001A

The MX180001A SDH/SONET Pattern Editing Software can be installed in either an external PC or in the MP1800A and MP2100A/MP2101A to generate SONET/SDH standard-compliant frame patterns.

- Generates ITU-T G.707/Bellcore standard-compliant SDH/SONET patterns for STM-0~STM-256c, STS-1~STS-768c
- Generates maximum 428 frames with STM-64c/STS-192c (Due to hardware limits, the upper limit for the MP2100A/MP2101A is 1.3 Mbit per frame.)
- Full editing of all parts in 1-bit units
- B1/B2/B3 Calculation function
- Alarm and BIP Error addition function
- Scramble ON/OFF function
- Full editing function
- Text to internal data format conversion function

■ MX180003A

The MX180003A GbE/10GbE Pattern Editing Software can be installed in either an external PC or in the MP1800A and MP2100/MP2101A to generate GbE/10GbE frame patterns.

- Generates 1000BASE-X/10GBASE-R-compliant frame patterns
- 8B/10B, 64B/66B coding ON/OFF
- Scramble ON/OFF
- Full editing of four frame types
- GAP editing, including ISG, IFG and IBG
- FCS Error addition
- Bit Error addition to data field
- Dedicated MAC frame editing and data field area editing

Specifications and Operating Environment

Note: There are restrictions on MP2100A/MP2101A operation.

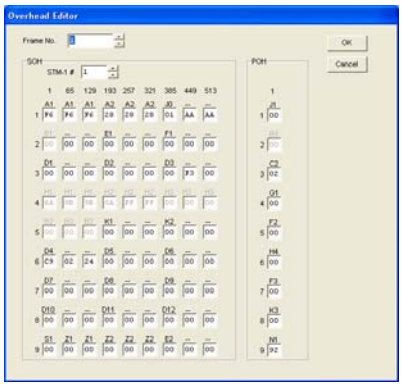
■ MX1800001A

Hardware

Item	Specification
PC	IBM-PC/AT or 100% compatible PC
CPU	300 MHz or faster Pentium®
OS	MS-Windows XP (English/Japanese)
Memory	512 MB (recommended minimum)
Monitor	Resolution: 800 x 600 pixels or better Colors: 256 or more
Hard Disk	Free space: 2 GB or more
Remote Interface	Ethernet

Specifications

Item	Specification
CH Combination	Independent, 2CH Combined, 4CH Combined
Pattern	No Frame, SDH, SONET
Logic	POG/NEG
Pattern Length	Independent 1 ~ 134217728 bits 2CH Combined 2 ~ 268435456 bits 4CH Combined 4 ~ 536870912 bits
Pattern Data	Free Format, ALL0, ALL1 PRBS2^n–1 (n = 7, 9, 11, 15, 20, 20z, 23, 31)
CID 0/1 Length	0/1 continuous bit length setting at ITU-T G.958-compliant CID Pattern *1 ~ (9*90*8-3*8)*N/Step1 (N = Mapping)
Scramble	ON/OFF



Overhead Editor Screen

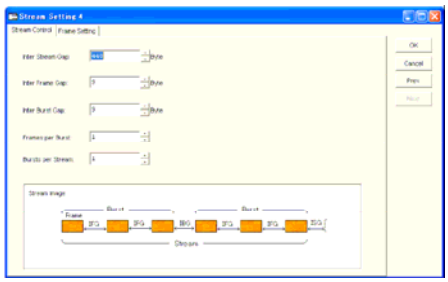
■ MX180003A

Hardware

Item	Specification
PC	IBM-PC/AT or 100% compatible PC, MP1800A (MP1800A-002 LAN option is required for direct pattern transfer from MX180003A to MP1800A)
CPU	800 MHz or faster Pentium®III
OS	MS-Windows XP® (English/Japanese)
Memory	512 MB (minimum)
Monitor	Resolution: 800 x 600 pixels or better Colors: 256 or more
Hard Disk	Free space: 2 GB or more
Remote Interface	10 Base-T, 100 Base-Tx Ethernet

Specifications

Item	Specification	
Coding	8B/10B (GbE), 64B/66B (10GbE) ON/OFF	
Scramble	ON/OFF	
Stream Setting	1 to 4 (Independent)	
Inter Stream Gap	8 to 2048 bytes	Step1 byte
Inter Frame Gap	1024 bytes	Step1 byte
Inter Burst Gap	9 to 1024 bytes	Step1 byte
Frames per Burst	1 to 1024 frames	Step1 frame
Frames per Stream	1 to 1024 frames	Step1 frame
Preamble	1 to 255 bytes	Step1 byte
Destination Address	Static, Increment, Decrement, Random	
Source Address	Static, Increment, Decrement, Random	
Data Field	1 to 255 bytes ALL1, ALL0, Programmable, 1/0 Alternate, PRBS2^n-1 (n = 7, 9, 11, 15, 20, 23, 31)	Step1 byte
Error Insertion	FCS Error, Bit Error Rate Error Start Frame: First frame to last frame Error Stop Frame: Error Start frame to last frame	



Stream Control Screen

Restrictions

- The maximum bit length that can be read by the MP2100A/MP2101A is 1.3 Mbit. Data parts exceeding this length are ignored.
- Since the MP2100A/MP2101A PPG Data output and ED Data input are AC coupled, supported patterns are restricted to patterns that are ½ of the Mark ratio.
- The MP2100A/MP2101A do not support the CH Combination and CH Synchronization functions.
- The MP2100A/MP2101A do not support direct pattern transfer over Ethernet from the MX180001A/MX180003A to hardware.
- The MP2100A/MP2101A can read the created Programmable Pattern File from the PPG or EDC by copying to the specified folder.
- Remote control by external equipment is not supported.

Consult us for other details not described here.

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No. MP210xA-Pattern_Editor-Leaflet-E-L-1-(1.00) 公知 Printed in Japan 2011-5 MG