G0430A PCIe5 Re-Driver Set Operation Manual

Third Edition

For safety and warning information, please read this manual before attempting to use the equipment. Keep this manual with the equipment.

ANRITSU CORPORATION

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G0430A PCIe5 Re-Driver Set Operation Manual

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For Safety -

Static Sensitive	Always take the following anti-static measures to prevent the internal circuit from being damaged when using this equipment.			
	 Wear a wrist strap connected to the ground terminal of this equipment. Connect the ground wires of this equipment, external measuring instruments and DUT before connecting a coaxial cable. Eliminate static electricity charged between the cores and outer conductors of an external device and the coaxial cable, before connecting this equipment and the external device. 			
Use in a Residential	This equipment is designed for an industrial environment.			
Environment	In a residential environment, this equipment may cause radio interference in which case the user may be required to take adequate measures.			
Use in Corrosive Atmospheres	Exposure to corrosive gases such as hydrogen sulfide, sulfurous acid, and hydrogen chloride will cause faults and failures.			
	Note that some organic solvents release corrosive gases.			

Anritsu Warranty

Anritsu Corporation provides the following warranty against stoppages arising due to manufacturing error, and against problems with operation occurring even though the procedures outlined in the operation manual were followed.

The equipment is warranted for one year from delivery and will be replaced free of charge only once under warranty.

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The hardware and software warranties are not valid under any of the following conditions:

- The fault is due to mishandling, misuse, or unauthorized modification or repair of the equipment by the customer.
- The fault is due to severe usage clearly exceeding normal usage.
- The fault is due to improper or insufficient maintenance by the customer.
- The fault is due to natural disaster, including fire, wind or flood, earthquake, lightning strike, or volcanic ash, etc.
- The fault is due to damage caused by acts of destruction, including civil disturbance, riot, or war, etc.
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- The fault is due to use of non-specified peripheral or applied equipment or parts, or consumables, etc.
- The fault is due to use of a non-specified power supply or in a non-specified installation location.
- The fault is due to use in unusual environments^(Note).
- The fault is due to activities or ingress of living organisms, such as insects, spiders, fungus, pollen, or seeds.

In addition, this warranty is valid only for the original equipment purchaser. It is not transferable if the equipment is resold.

Anritsu Corporation shall assume no liability for damage or financial loss of the customer due to the use of or a failure to use this equipment, unless the damage or loss is caused due to Anritsu Corporation's intentional or gross negligence.

Note:

For the purpose of this Warranty, "unusual environments" means use:

- In places of direct sunlight
- In dusty places
- In liquids, such as water, oil, or organic solvents, and medical fluids, or places where these liquids may adhere

- In salty air or in place chemically active gases (sulfur dioxide, hydrogen sulfide, chlorine, ammonia, nitrogen dioxide, or hydrogen chloride etc.) are present
- In places where high-intensity static electric charges or electromagnetic fields are present
- In places where abnormal power voltages (high or low) or instantaneous power failures occur
- In places where condensation occurs
- In the presence of lubricating oil mists
- In places at an altitude of more than 2,000 m
- In the presence of frequent vibration or mechanical shock, such as in cars, ships, or airplanes

Anritsu Corporation Contact

In the event of this equipment malfunctions, please contact a sales office listed in Anritsu Service and Sales office. Contact information can be found on the last page of the printed version of this manual, and is available in a separate file on the PDF version.

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China RoHS

产品中有害物质的名称及含量

部件名称		有害物质						
	铅	汞	镉	六价铬	多溴联苯	多溴二苯醚		
	(Pb)	(Hg)	(Cd)	[Cr(VI)]	(PBB)	(PBDE)		
印刷线路板 (PCA)	×	0	×	×	0	0		
机壳、支架 (Chassis)	×	0	×	×	0	0		
电缆、风扇、连接 器等 (Appended goods)	×	0	×	×	0	0		
本表格依据 SJ/T 11364 的规定编制。								

O: 表示该有害物质在该部件所有均质材料中的含量均在 GB/T 26572 规定的限量要求以下。

×: 表示该有害物质至少在该部件的某一均质材料中的含量超出 GB/T 26572 规定的限量 要求。

环保使用期限

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About This Manual

This operation manual explains the configuration, connection, and operation of the G0430A PCIe5 Re-Driver Set.

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Appendix A Channel Control Values of

Preset Files.....A-1

Chapter 1 Configuration of PCIe5 Re-Driver Set

The G0430A PCIe5 Re-Driver Set (hereafter G0430A) is an equalizer for 32 Gbaud NRZ signal. With G0430A for channel loss compensation, the MP1900A Signal Quality Analyzer-R can perform tests according to the PCIe 5.0 standard.

The G0430A consists of a printed circuit board, cables, software, adapters, screws, and posts.

Refer to the following table for the G0430A configuration.

No.	Name	Q'ty	Remarks
1	MAEQ-39904B EVM board	1	Linear Equalizer EVM board
2	Mini USB cable	1	Cable
3	USB flash drive	1	The following files are stored.
			• GUI software for EVM board
			Operation manual
			• Preset files
			• Test report
4	2.92mm Carlisle cable	2	Cable
5	K220B	2	Precision Adapter DC to 40 GHz, 50 Ω
6	DC cable	1	A pair of black and red cords
Ø	GND Connection Cable	1	Cable
8	ASB-316.5E	7	Posts
9	3NPS6Ni+SW+WBS	7	Screws
10	+3.3V label	1	

Table 1-1 G0430A Configuration

To use G0430A, the following required components should be prepared by the customer.

Table 1-2 Required Components

Model	Name	Q'ty	Remarks
J1728A	Electrical Length Specified Coaxial Cable (0.4m, K Connector)	2	J1728A or equivalent
N/A	DC Power Supply	1	Single power supply * (+3.3 V, 0.3 A)

*: LeCroy T3PS16081P has been confirmed to work with G0430A.

Chapter 2 Connection Procedure

2.1 Installation

Support MAEQ-39904B EVM board with screws and posts.



Place the MAEQ-39904B EVM board on a horizontal and level surface. Stick the +3.3V label near the red terminal.



Figure 2.1-2 Label Position

2.2 Setup

Never feed a voltage of more than +3.3 V for MAEQ-39904B EVM boad. Doing so may cause damage to it.

- 1. Turn on the MP1900A. Check that the DUT is turned OFF.
- 2. Set the DC power supply as below.

DC voltage: +3.3 V Current Limit: 0.3 A Output: OFF

3. Connect the cables (refer to Figure 2.2-1).

GND Connection cable (⑦):

Connect MP1900A and the MAEQ-39904B EVM board.

2.92mm Carlisle cable (④):

Attach to the MAEQ-39904B EVM board.

Mini USB cable (2):

Connect MP1900A or PC and the MAEQ-39904B EVM board.

K220B (⑤):

Connect MAEQ-39904B Ch1 output to Ch2 input with two K220Bs.

Note:

Unused channels (Ch0 and Ch3) do not need to be terminated.

- 4. Connect the DC power supply to MAEQ-39904B EVM board with the DC cable ([©]).
- 5. Connect the DUT, MAEQ-39904B EVM board, and the ED of MP1900A referring Figure 2.2-1 "Cable Connection".
- Turn on the output of DC power supply. Typical current is 260 mA.
- 7. Turn on the DUT.

When powering down, perform the procedure in reverse.

Chapter 2 Connection Procedure



Refer to the following figure for connecting each part.

Figure 2.2-1 Cable Connection



Figure 2.2-2 Connection Diagram

Chapter 3 Software Operation

3.1 Preparation

Prepare the G0430A for operation according to the following steps.

1. Install the GUI software on the host PC or MP1900A.

The GUI software is stored on the USB flash drive.

Folder name: \EVM Kit Zip File\EVM Setup vx.x.x

(x.x.x represents the software version)

Executable file: setup.exe

2. Verify jumpers are present in the positions shown in Figure 3.1-1 and Table 3.1-1.



Figure 3.1-1 EVM Jumper Settings

Table 3.1-1 EVM Jumper Settings

Board	Jumper	Setting	Description
Main Board (Green)	JP1	ON	3.3 V to AVCC
Controller (Blue)	JP1, JP2, JP8, JP3, JP4	1-2, ON	Micro-controller programming setup
	JP6	OFF	Do not use.

- 3. Connect the device under the test (hereafter, DUT) outputs to the MAEQ-39904B Ch1 inputs with the Carlisle connector cables.
- 4. Connect between the MAEQ-39904B Ch2 outputs and the MP1900A ED inputs by using 2.92mm Carlisle connector cables.

- Make sure the necessary hardware connections for the G0430A are in place, and launch the User Control software by going to Start > All Programs > MACOM Technology Solutions.
- Make sure the software is active, click Connect. The device will be recognized and displayed in the upper-right corner of the window.

When the **Bad COM Port Settings** dialog box is displayed, open Device Manager, expand **Ports (COM & LPT)**, and check the number displayed after USB Serial Device.



Figure 3.1-2 Port Number Indication of EVM board

Change the Port setting for software from **Auto** to the USB Serial Device number (for example, **COM5**).

Also, check that I²C Display is set to 7-Bit.



Figure 3.1-3 Connection Settings

7. On the right side of the **Channel Control** tab, click **Reset with No OTP Download** to reset the device.

The **Channel Control** tab helps you control the settings for each of the four channels individually.

The high frequency boost can be controlled by using the slide bar or by inputting a decimal number between 1 to 127 (①in Figure 3.1-4). Channel control also allows control over the settings like, low frequency boost, bias control, and disabling the channel (② and ③ in Figure 3.1-4).

On the individual channel tab, each of the four channels can be configured differently.



Figure 3.1-4 Channel Control tab

3.2 How to Optimize Return Path

For Receiver LEQ Test with PCIe Gen5 (32GT/s), it is important to optimize Return Path (DUT Tx to BERT ED). The procedure is shown below.

Requirements for using the G0430A

When testing the System, connect the G0430A between DUT Tx and ED. Refer to Chapter 2 "Connection Procedure" for how to set up the G0430A. Though the G0430A is not required for AIC Test, it is the same as the method of optimizing Return Path for System / AIC test.



Output amplitude of G0430A may become 1.8 Vp-p (differential) max. On the other hand, range of input amplitude of ED is 1.0 Vp-p (differential) or lower. Make sure not to exceed 1.0 Vp-p (differential) for output amplitude of G0430A.

When you connect between G0430A and ED directly with low transmission loss such as without ISI board, output of amplitude will become 1.0 Vp-p (differential) in condition that gain of G0430A is maximum and input amplitude of G0430A is 80 mVp-p (differential).

Insert the attenuator between G0430A and ED when the output amplitude of G0430A exceeds 1.0 Vp-p (differential). Check the amplitude of output waveform by using an oscilloscope whose bandwidth is 50 GHz or higher.

Preparation of preset files

To optimize the Return Path, you are required to prepare preset files for MAEQ-39904B.

1. Copy the zip file from the USB flash drive to the PC or MP1900A.

\Macom_MAEQ-39904_EQ_Preset.zip

2. Extract the zip file, and then make sure that the following 21 files are in the directory you specify.

MAEQ-39904_EQ_P0.txt MAEQ-39904_EQ_P1.txt

:

 $\begin{array}{l} MAEQ\text{-}39904_EQ_P19.txt\\ MAEQ\text{-}39904_EQ_P20.txt \end{array}$

3. Click the **Channel Control** tab, click **Load File** shown in Figure 3.2-1, and select a preset file.

State Connect	📑 Load File 🚽 Save State 🔹 Start Macro 🔋 Edit Script 🛛 🗹 Direct Write	МЛСОМ.
Device Settings OTP Channel Control	Monitors Memory Map Log	Connected To: MAEQ-39904B0
	chard Chard Chard	COM1 / I ² C 0x30
ch1_eq_hf:	2 v	Reset with OTP0 Download Reset with OTP1 Download

Figure 3.2-1 Loading a Preset File

Chapter 3 Software Operation

Optimization procedure

- Refer to the "Receiver Link Equalization Test" section in MX183000A High-Speed Serial Data Test Software Operation Manual and set up the test configuration according to the figure below.
- 2. Start MX183000A, set Specification to **5.0(32.0 GT/s)**, and then turn off all the stresses below.
 - SJ
 - RJ
 - DM
 - CM

IX183000A - PCIe Link Training		×		
e Setup Help		Operate MP1900A		
uipment Setup Link Training Run Test Gra	aph Report Electrical Idle			
Decification DUT .0(32.0 GT/s) V Root Complex (Syste	m) V	Link Start Measurement		
LTSSM State	Received	Matrix Scan	Jitter	
Linkup Speed	Use Preset PPG Final Preset	LEQ Test Setting	SJ1 Frequency 100000000 ‡	Hz
8b10b Received Transmitted SKP Count	PPG Final Cursor Pre-Cursor Cursor Post-Cursor		Amplitude 0.112	Ulp-p
Symbol Err		BER Measurement	SJ2	
Current RD Err	Full Swing, Low Frequency	LTSSM Log	SJ2 Mode SJ2 via MU181000 V	
Symbol Lock	Request Eq.		Frequency 10	Hz
		Loopback Method	Amplitude 0.000 🛊	Ulp-p
28b130b Received Transmitted	Recovery.EQ	Config No EQ.	0.00	ps p-p
(P Count	Phase0	Test Pattern	BUI 🗌	
S1/TS2 Symbol14-15 DC Balance	Phase1	Compliance ~	PRBS PRBS7 V	
vnc Header Err	Phase2	MCP ~	Bitrate 12.500000	Gbit/s
S1 OS Parity Err	Phase3	Timeout	Amplitude 0.000 🖨	Ulp-p
lock Lock		Option	0.00	a-a sa [
IEOS Counter		option		

Figure 3.2-2 Configuration of MX183000A Link Training

- 3. In the MX183000A main screen, select the **Setting** check box for LEQ Test, and follow the steps below:
 - 3a. Set PPG Starting Preset to P5.
 - 3b. Set DUT Initial Preset (Preset Hint Tx) to P9.
 - 3c. Set DUT Target Preset (Change Preset) to P9.
 - 3d. Click Apply.
 - 3e. Click **Option**, and then on the **PPG / ED** tab of the **Option** dialog box, set CTLE Gain to 0.0 dB.

MX183000A - PCIe Link Training		×	7
File Setup Help		Operate MP1900A	
Equipment Setup Link Training Run Test Gra	aph Report Electrical Idle		X
Specification DUT 5.0(32.0 GT/s) V Root Complex (System	m) 🗸 🗌 More results	Link Start	Ink EQ [PPG/ED] Trigger
LTSSM State Linkup Speed	Received Use Preset PPG Final Preset	Matrix Scan	7/s P1:-3.5, 0.0 CILE Gain [dB] PCle5 0.0 Auto
LEQ Test Rx LEQ Apply Rx LEQ Initial TX LEQ Tx LEQ Response	PPG Final Cursor Pre-Cursor Cursor Pest-Cursor	Configure BER Measurement	Preset
Loopback Through: Recovery Link EQ: Preset Saved Cursor	Full Swing, Low Frequency Link, Lane Number Request Eq	LTSSM Log	
Lane: U/8 Test Pattero: MCP (Modified Compliance Pattero)	RecoveryEQ	Recovery Full EQ.	
PPG Starting Preset: PS DUT Initial Preset (Preset Hint Tk): P9 DUT Target Preset (Change Preset): P9	PCIe 3 PCIe 4 PCIe 5 Phase0 Rhase1 Phase2 Phase3	Test Pattern Compliance V MCP V Timeout Option	Close

Figure 3.2-3 LEQ Test Setting of MX183000A Link Training

- 4. Turn the G0430A on, load channel control parameters shown in Table A-1 from a preset file named MAEQ-39904_EQ_P0.txt first as shown in Figure 3.2-1, and then click **Link Start**.
- 5. Click Link Start.

LITIK Start

6. Establish Loopback.

LTSSM State	
Linkup Speed	

- 6a. If Linkup Speed is not 32.0 Gbps and the LTSSM State is not Loopback.Active.Lead, increase the preset file number of the redriver, for example at intervals of four, EQ_P0 -> EQ_P4 -> ... -> EQ_P20. Each time the preset file number set to the redriver changes, make sure that the LTSSM is in the Loopback state displayed.
- 6b. If Loopback cannot be established despite the preset file number is set to EQ_P20, set the Preset values in steps 3b and

3c to P8, set the preset file number of the re-driver to EQ_P0, and then retry to check the Loopback state according to step 6a.

- 6c. If Loopback cannot be established even with Preset P8, redo step 6b with the Preset values set to P7, P6, ... P0.
- 6d. When Loopback is established according to steps 6a to 6c, check the Preset values of MX183000A and the preset file number of the re-driver.
- 6e. If Loopback cannot be established up to step 6d, remove ISI from the measuring system and retry steps 6a to 6d.
- * If Loopback cannot be established by the steps above, the measurement environment may be incorrect (cable connection error, etc.) or there may be a problem with the DUT, so review the measurement environment again.
- 7. BER optimization

Perform Link Training with the Preset values and the preset file number of the re-driver specified in step 6 to measure BER.

- 7a. Optimize EQ to find the setting that gives the optimal BER.
- 7b. Set the EQ confirmed in step 6.
- 7c. Run Auto Search.

Click Operate MP1900A to switch over to MP1900A GUI.

Operate MP1900A

Click the Auto Search button.



Set as below and click **Start**:

Mode:Fine(NRZ)Item:Threshold & PhaseCTLE Auto Adjust:OFF

Auto Search								
Advanced	OFF							?
Mode Fin	ne(NRZ)	– (The second	E Auto Adjust	→ St	art St	op	Close]
Item Th	reshold&Pha	se 💌	OFF		Set	ALL	Reset ALL]
Slot	ON/OFF	Data Threshold	XData Threshold	Clock Delay (mUI)	Clock Delay (ps)	CTLE (dB)		
Slot6-1 ED	ON							
Slot6-2 ED	OFF							

- 7d. Wait until Auto Search is completed, and then check BER.
- 7e. Increase the preset file number of the re-driver by 1 or 2 at a time, and then check the BER again. Repeat this step until the optimum BER is searched. If an error-free condition is achieved with multiple preset file numbers, use the preset file with the middle number of a series of preset file numbers as the optimum setting.
- 7f. Click the Auto Search button in step 7c again.
- 8. Confirm the setting parameters for optimization. These parameters for optimization are determined according to the procedure above (steps 1-7), as shown below:
 - Preset setting confirmed in step 6.
 DUT Initial Preset (Preset Hint Tx)
 DUT Target Preset (Change Preset)



• Threshold, Phase, and G0430A settings confirmed in step 7.

Slot	ON/OFF	Data Threshold	XData Threshold	Clock Delay (mUI)	Clock Delay (ps)	CTLE (dB)						
Slot6-1 ED	ON	2 mV	-2 mV	200 mUI	16.00 ps							
Device Settings OTP Channel Control Monitors Memory Map Log												
		Chan 0	Chan 1	Chan 2	Chan 3							
ch1_eq_hf:					0 28 h							
CH1 EF Bias Control: 2 ~												
ch1_eq_	lf:		3.0dB @2GHz	~	✓ eq_hq_cal_en (All Channels)							
ch1_bias_ctrl:		Bias current of 2X or 1.36 m/		nA ~	en_los_ch_1							
los_thr_ch_1:		LOS threshold of 72 mVppd		d ~	✓ mask_eq_los_ch <u>1</u>							
ch1_leq_ib_ptat_ef_cal:		EF calibration current of 8X / 8 or 339 uA		r 339 uA 🛛 👻	mask <u>a</u> larm_cn_1							
ch1_cal_	din:	Offset cali	bration voltage = 0.2	2 mV 🗸								

			×		
PCIe 5.0	CTLE Gain [dB] Preset Auto BER Measurement PCle5 ✓ №0[⊕] P7 : -6.0, 3.5 ✓	DM L Frequency Amplitude	- 2.10 ÷ GHz 4 ÷ mVp-p		
Pass/Fail	MX183000A - PCle Link Training	×			
Cycle Gating Time Switch To	File Setup Heip Equipment Setup Link Training Run Test Graph Report Electrical Idle Specification DUT Sol(32.0 GT/s) Root Complex (System) Image: More results	PCIe: Link Start PCIe:	L 230 ↔ mUI 2 266 ↔ mUI 8 234 ↔ mUI		
Manual BER Test Total BER Total Error Count Total Bits Current BER Sync Loss	LISSM State Received Linkup Speed Use Preset LEQ Test ReLEQ Apply PPG Final Preset PPG Final Cursor PreCursor	Matrix Scan PClev LEQ Test Setting Rx LEQ Configure	200 € mUI Reset		
	Rx LEQ Initial TX LEQ Tx LEQ Response Loopback Through: Recovery Full Swing, Low Frequency Link, Lane Number Image: 0/8	BER Measurement LTSSM Log Loopback Method	ta 2, Aggressor)		
	Test Pattern: MCP (Modified Compliance Pattern) Recovery EQ Con PPG Starting Preset: Prie 3 PCle 4 PCle 5 PT Phase0 PCle 3 PCle 4 PCle 5 DUT Initial Preset (Preset Hint Tay): Phase2 Phase2 Phase2	nfig No EQ v Test Pattern Compliance v MCP v Timeout	Clock Delay		
	Preset setting	Option			

Now, the Return Path is successfully optimized.

Figure 3.2-4 Setting Example of Optimization of Return Path

Appendix A Recommended Channel Control Values

The following table shows recommened combinations of values for Figure 3.1-4 Channel Control tab.

Set No.	ch1_eq_hf	CH1 EQ Bias Control	ch1_eq_lf (dB)	ch2_eq_hf	CH2 EQ Bias Control	ch2_eq_lf (dB)
0	28	2	3.0	$7\mathrm{F}$	3	3.0
1	20	2	3.0	$7\mathrm{F}$	3	3.0
2	18	2	3.0	$7\mathrm{F}$	3	3.0
3	10	1	3.0	$7\mathrm{F}$	3	3.0
4	8	1	3.0	$7\mathrm{F}$	3	3.0
5	1	1	3.0	$7\mathrm{F}$	3	3.0
6	1	1	3.0	78	3	3.0
7	1	1	3.0	70	3	3.0
8	1	1	3.0	68	3	3.0
9	1	1	3.0	60	3	3.0
10	1	1	3.0	58	3	3.0
11	1	1	3.0	50	2	3.0
12	1	1	3.0	48	2	3.0
13	1	1	3.0	40	2	3.0
14	1	1	3.0	38	2	3.0
15	1	1	3.0	30	2	3.0
16	1	1	3.0	28	2	3.0
17	1	1	3.0	$\overline{20}$	2	3.0
18	1	1	3.0	18	2	3.0
19	1	1	3.0	10	1	3.0
20	1	1	3.0	1	1	3.0

Table A-1 Recommended Channel Control Values