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Anritsu - GRL

PCIe 3.0 CEM Rx Test Application

Release Note

Fifth Edition

This software is released for PCIe CEM Rx Test.

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1. Released Software

Keysight				
Edition	GRL CEM Rx Test Application	Anritsu MX190000A	Anritsu MX183000A	Scope
05	V1.0.49	V4.03.12	V4.03.15	DSAZ634A V06.40.00714
	V1.0.49	V4.02.10	V4.02.10	DSAZ634A V06.40.00714
	V1.0.49	V4.01.32	V4.00.08	DSAZ634A V06.40.00714
04	V1.0.22	V3.01.10	V3.07.12	DSAZ634A V06.20.01101
03	V1.0.22	V3.00.05	V3.06.16	DSAZ634A V06.20.01101
02	V1.0.22	V2.05.08	V3.05.00	DSAZ634A V06.20.01101
01	V1.0.11	V2.05.08	V3.05.00	DSAZ634A V06.20.01101

Tektronix

Edition	GRL CEM Rx Test Application	Anritsu MX190000A	Anritsu MX183000A	Scope
05	V1.0.49	V4.03.12	V4.03.15	DPO73304DX
				10.8.3 Build 3
	V1.0.49	V4.02.10	V4.02.10	DPO73304DX
				10.8.3 Build 3
	V1.0.49	V4.01.32	V4.00.08	DPO73304DX
				10.8.3 Build 3
04	V1.0.22	V3.01.10	V3.07.12	DPO73304DX
				10.8.3 Build 3
03	V1.0.22	V3.00.05	V3.06.16	DPO73304DX
				10.8.3 Build 3
02	V1.0.22	V2.05.08	V3.05.00	DPO73304DX
				10.8.3 Build 3
01	V1.0.11	V2.05.08	V3.05.00	DPO73304DX
				10.8.3 Build 3

2. Peripheral Devices

The peripheral devices of the application are shown in the table.

Model	Name	
MP1900A	Signal Quality Analyzer-R	
MU181000B	12.5GHz 4port Synthesizer (Option02 is required.)	
MU181500B	Jitter Modulation Source	
MU195020A	21G/32G bit/s SI PPG	
MU195040A	21G/32G bit/s SI ED	
MU195050A	Noise Generator	

For the installation position of the mainframe, refer to the Anritsu website (https://www.anritsu.com).

3. Added Functions

Edition	Function	Description
05	Auto Scale	 This function turns off the Auto Scale function for Scope to shorten the time required for Initial Tx EQ and Tx LEQ response time test. When the function is set to True, input the amplitude of the Data output of the DUT in the Vertical Range (scale of the vertical axis of Scope) with a value equivalent to Differential Input. The recommended value for Vertical Range is 0.5 Vpp because the Power Divider practically attenuates the data output of the DUT by 6 dB. This software may fail in waveform decoding if the amplitude is too small for the scale or beyond the scale.
	Auto DUT Reset	 Scale. This function resets the DUT automatically during Compliance Test. To use this function, follow the steps below: a. In the Auto DUT Reset box, select Internal Power Cycle or Internal Power Reset. b. Set up Anritsu Z2025A PCIe CBB Controller according to the Z2025A Installation Guide. c. In the Prompt Before Link EQ Training box, select False. Application Options License Windows Help Power Cycle Off Time(s): 3 Power Cycle Off Time: Sets the time to turn off the CBB power. Power Reset Off Time: Sets the time to send the Power Reset signal to the DUT. Post Reset Wait Time(s): Post Reset Wait Time(s)
	Link Training Wait Time	Sets the time to wait after turning on Reset or Cycle before Link Training is started. This function sets the time to wait after Link Training is ready to start before it is started.
	Link Training CTLE Gain	Select a CTLE value option to set for SI ED. If the DUT Tx Insertion Loss is large, adjust the value.
	Log Link Training	This function saves an LTSSM Log file to the following directory of MP1900A every time Link Training is performed. "C:¥PCIE_LTSSM_LOG"

4. Bug Fixes

Edition	Item	修正内容
05	Tx LEQ Response time test and Rx LEQ test failed occasionally.	Tx LEQ Response time test and Rx LEQ test failed occasionally.
01	Sometimes, Preset calibration fails with Tektronix scope.	Calibration fails when attempting to execute Preset calibration. Bug occurs in GRL software version 1.00.11 and Tektronix scope software version 10.8.3.

5. Remaining Known Bugs

None

6. Usage Notes

The precautions for using each version are described below.

6.1 How to shorten measurement time

- BER and Margin Test

Decrease Margin Test Measurement Time and Margin Test Max Steps.

Conf	igurations	
	Compliance BER Measurement Time(s): 63 Maximum Compliance Error:	
	Margin Test Measurement Time(s): Margin Test Max Steps: 5	
	Margin Test Step Size(%): 20 Maximum Margin Test Error: 1	
	Loopback Mode: Recovery	-

Set Retrain When Sj Frequency Changed to False.

	Margin lest Measurement lime(s):	5
	Margin Test Max Steps:	5
	Margin Test Step Size(%):	20
	Maximum Margin Test Error:	1
	Loopback Mode: Reco	very 👻
	Retrain When Sj Frequency Change	ed: False 🗸
	MarginSearchLivePlot:	True 🔹
•		

6.2 Note on Link EQ Response time test

Perform a test with **Tx EQ Response time** (**Preset**) first and then perform it with **Tx EQ Response Time** (**Cursor**).

When starting the test with **Tx EQ Response Time (Preset**), the cursor values corresponding to Preset are notified from a DUT, and they are saved in MP1900A. These values are required for

testing with Tx EQ Response Time (Cursor).

Select Tests	Options License Windows Help $ \begin{array}{ccccccccccccccccccccccccccccccccccc$?	
	✓ DM Calibration ✓ Preset EQ Optimization ✓ Preset EQ Optimization ✓ Final ISI Calibration ✓ Final Eye Calibration ✓ Final Eye Calibration ✓ Final Eye Calibration ✓ Tx Link EQ Tests ✓ Tx Link EQ Tests ✓ Tx EQ Response Time Tests (Preset) ✓ Tx EQ Response Time Tests (Cursor) ✓ Rx Tests ✓ Tx Compliance Test ✓ ✓ Sj Margin Search Test	E v		3

To skip the test with **Tx EQ Response time (Preset)**:

Perform link training follow the below steps to acquire cursor values from a DUT. When replace the DUT to test **Tx EQ Response time (Cursor)**, the steps are required again.

- a. Launch MX183000A with PCIe Link Training application.
- b. Initialize the PCIe Link Training application.
- c. Set Specification to 3.0(8.0 GT/s).
- d. Click on LEQ Test Setting check box.

Equipment Setup Link Training Run Test Graph Report Electrical Idle Specification DUT More results Link Start (3.0/3.1(8.0 GT/s)) Endpoint (AIC) More results Link Start USSM State Predeved Preset Preset Unkup Speed Preset PPG Final Preset EEQ. Test SkP Count PPG Final Cursor Port-Cursor Dopback through Current RD Err Link, Lane Number LITSSM Log Loopback through SkP Count Phase0 (Root) Phase1 Test Pattern DCBalance Phase3 Mre Mre Phase3 ALL Mre Option	J MX183000A - PCIe Link Training File Setup Help		Operate MP1900A
Linkup Speed Use Preset Bb10b Received Transmitted PPG Final Preset Symbol Err PPG Final Oursor Current RD Err Full Swing, Low Frequency Symbol Lock Linku, Lane Number 128b130b Received Symbol Lock Transmitted Phase0 (Boot) PCle 3 PCie al Preset Test Pattern Compliance Phase1 Phase3 MCP Block Lock ALL	Specification	srapn keport	
128b130b Received Transmitted SKP Count	Bb10b Received Transmitted SKP Count	Use Preset PPG Final Preset PPG Final Cursor Post-Cursor Post-Cursor Post-Cursor Final Cursor Post-Cursor Post-Cur	ER Measurement LTSSM Log
	Received Transmitted SKP Count DCBalance Sync Header Err Parity Err	Phase0 (Root) Phase1 Phase2 Phase3	Compliance

e. Select **Rx LEQ** tab and click on **Apply** button.

MX183000A - PCIe Link Training		X
File Setup Help		Operate MP1900A
Equipment Setup Link Training Run Test Gra	aph Report Elect	trical Idle
Specification DUT 3.0/3.1(8.0 GT/s) Endpoint (AIC) 	More results	Link Start
LTSSM State	Received Use Preset PPG Final Preset	LEQ Test 📝 Setting Rx LEQ
LEQ Test Rx LEQ Apply Rx LEQ IIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII	PPG Final Cursor Pre-Cursor Cursor Post-Cursor Full Swing, Low Frequency	Configure BER Measurement LTSSM Log
Loopback Through: Recovery Link EC: Preset Saved Cursor Lane: 0/8	Link, Lane Number	Loopback through Recovery
Test Pattern: MCP (Modified Compliance Pattern) PPG Starting Preset: P7	PCle 3 PCle 4 Phase0 (Root) Phase1	Test Pattern Compliance
DUT Initial Preset (Preset Hint Tx): P7 v DUT Target Preset (Change Preset): P7 v	Phase2 Phase3 ALL	Timeout

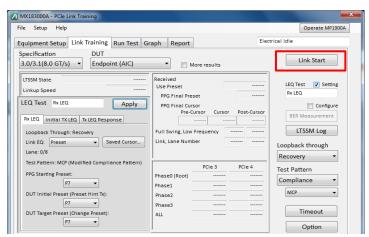
f. Click on **Option** button.

MX183000A - PCIe Link Training		×
File Setup Help		Operate MP1900A
Equipment Setup Link Training Run Test Gra	aph Report Elect	rical Idle
Specification DUT 3.0/3.1(8.0 GT/s) DUT Endpoint (AIC)	More results	Link Start
LTSSM State	Received Use Preset PPG Final Preset PPG Final Cursor Pre-Cursor Cursor Fut Swing, Low Frequency Link, Lane Number	LEQ Test V Setting Rx LEQ BER Measurement LTSSM Log Loopback through Recovery V
Test Pattern: MCP (Modified Compliance Pattern) PPG Starting Preset: P7 UT Initial Preset (Preset Hint Tx): P7 UT Target Preset (Change Preset): P7 V	PCIe 3 PCIe 4 Phase0 (Root) Phase1 Phase2 Phase3 ALL	Test Pattern Compliance MCP Timeout Option

g. Set Algorithm to increment and set Repeat to 12 on Link EQ tab.

1 Option State Machine SKP Link EQ PPG/E	D Trigger	u u
Link EQ (Recovery Phase2,3) Try Algorithm Increment	▼ Repeat 12	PCIe 3.0/3.1
PCIe 3.0/3.1 Use Preset Preset Downstream Downstream (MP1900A) sends Starting Preset un Starting Preset Preset Hint (Rx)	ntil it receives preset from Upstream (AIC). Recovery.EQ.Phase2 Change Preset	Root Complex Downstream port Tx Rx
P7:-6.0, 3.5	P7:-6.0, 3.5 v	Rx Tx Upstream port
Downstream (MP1900A) requests these presets	to Upstream (AIC) Recovery.EQ.Phase3 Change Preset	End Point
Preset Hint (Tx) Preset Hint (Rx) P7: -6.0, 3.5 • -6 dB •	P7 : -6.0, 3.5	
		Close

h. Reset a DUT and click on **Link Start** button.



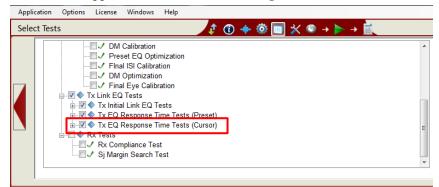
i. When LTSSM State is Loopback.Active.Master, click on Saved Cursor button on LEQ Test window.

MX183000A - PCIe Link Training			×
File Setup Help			Operate MP1900A
Equipment Setup Link Training Run Test Gra	aph Report	Outp	utting Test Pattern
Specification DUT 3.0/3.1(8.0 GT/s) Endpoint (AIC)	More results		Unlink
LTSSM State Loopback.Active.Master Linkup Speed 8.0 Gbps	Received Ise Preset PPG Final Preset	Preset	LEQ Test 📝 Setting Rx LEQ
LEQ Test Rx LEQ Apply Rx LEQ Initial TX LEQ Tx LEQ Response	PPG Final Cursor Pre-Cursor Cursor	Post-Cursor	Configure BER Measurement
Loopback Through: Recovery Link EQ: Preset Saved Cursor Lane: 0/8	Full Swing, Low Frequency Link, Lane Number	63 21 1 0	LTSSM Log Loopback through Recovery
Test Pattern: MCP (Modified Compliance Pattern) PPG Starting Preset: PT DUT Initial Preset (Preset Hint Tx): [PT	Phase0 (Root) Phase1 Complete Phase2 Complete Phase3 Complete	PCIe 4	Test Pattern Compliance
DUT Target Preset (Change Preset):	ALL Complete		Timeout Option

ete the LEQ	Response Te	est. These	e values a	are updat	ed automatic	ally and s	aved by t	the MP19	00A.
	Saved		PCIe 3.0		Saved		PCIe 4.0		
	Cursor	C-1	CO	C+1	Cursor	C-1	CO	C+1	
	V P0	0	47	16	V P0	0	47	16	
	V P1	0	52	11	V P1	0	52	11	
	V P2	0	50	13	V P2	0	50	13	
	V P3	0	55	8	V P3	0	55	8	
	V P4	0	63	0	V P4	0	63	0	
	V P5	6	57	0	V P5	6	57	0	
	V P6	8	55	0	V P6	8	55	0	
	V P7	7	45	11	V P7	7	45	11	
	V P8	8	47	8	V P8	8	47	8	
	V P9	11	52	0	V P9	11	52	0	
	V P10	0	42	21	V P10	0	42	21	

j. If All Saved Cursor check boxes are ON, the steps are finished.

k. Launch GRL application and start Tx EQ Response time (Cursor).



7. Troubleshooting

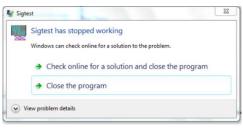
If you encounter any errors during calibration or testing, check as follows.

7.1 Calibration

7.1.1 In case of an error when calibrating Amplitude, Preset, SJ and RJ

- Check the RF connections. Especially, the connection polarity (Pos/Neg) and the trigger connections (PPG Aux Out and Scope Aux In) are easy to mistake.
- Check the software version. A different version of software may cause an unexpected error.
- Check the SigTest version. SigTest version needs to be 3.2.0.3 for Gen3 or 4.0.51 for Gen4. Also, this should be installed to the directory C:¥Program Files (x86). Do not change the installation directory from the default setting.
- 7.1.2 In case of a SigTest error when performing Long Channel Calibration

A SigTest error message is displayed and SigTest has stopped working when calibrating SJ, RJ and EH/EW. Since this message is no effect on calibration results, click **Close the program** to continue the calibration.



To avoid this message:

- Close all applications except the GRL software, MX190000A, MX183000A and scope applications. Especially when VNC is running, SigTest may not work properly.
- If you see this message frequently despite not running other applications on the PC, use another PC with the GRL software installed.
- 7.1.3 When Final Eye calibration cannot be succeeded
 - Use the PCIe 3.0 test fixture. It is recommended to use the calibration fixture distributed by the PCI-SIG.
 - If any components (DC block, Power Divider, Attenuator and Adaptor) are attached to the Noise module output, remove them. These components may affect the waveform.



7.2 Tx and Rx LEQ test

- 7.2.1 When Tx LEQ Response cursor test cannot be started
 - Before starting Rx Test, complete all calibrations or load a calibrated session file.
- 7.2.2 In case of a Link Training error when testing Tx LEQ Response
 - Check the RF connections. Especially, the trigger connections (PPG Aux Out and Scope Aux In) are easy to mistake.
 - If DUT Tx has large insertion loss, adjust the MP1900A CTLE value in the MX183000A screen. Refer to Appendix C for adjusting CTLE.
- 7.2.3 In case of a decode error when testing Rx LEQ Reponses time
 - On the **Configurations** tab, set **CTLE Setting** to **Auto**.

🕅 Anritsu PCIe CEM 4.0 Rx Test	
Application Options License Windows Help	
Configurations	
CTLE Scan End EQ Gain(dB): T X Link EQ Tests T X Response Offline Mode: CTLE Setting: Capture Response Time Waveform Only: R X Tests BER Automation: PCIe Link Training R Tests	Set Default

7.3 Others

- 7.3.1 When a session file cannot be loaded
 - Close the folder where you installed the GRL software and saved PDF report file(s) because the loaded session file accesses and edits the folder.

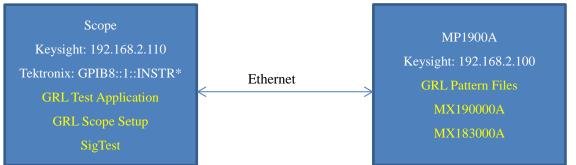
Load Session	×
Incompatible file format or file is being used: Error in loading te	st session
	ОК

- While recalling the session file on CEM spec takes several minutes, it does not mean that the computer is frozen. Wait until the recalling is completed. This function recalls large waveform files which are acquired by Tx initial EQ and Tx LEQ Response time test.

Appendix

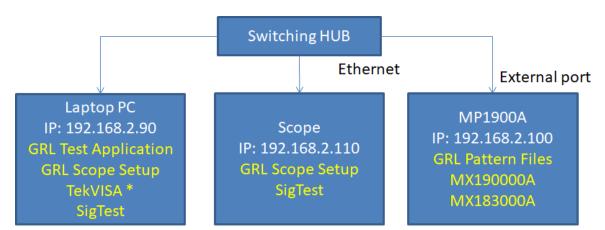
- A. Quick Startup Guide
 - 1. Connect instruments with Ethernet cables as shown below.
 - 2. Set the IP and GPIB addresses as shown below. These can be set in the Network and Sharing Center (Windows OS feature).
 - 3. Install all applications as shown below (Yellow letters).

Recommended connection



* TCP/IP cannot be used when the GRL software is installed on a Tektronix scope. Set the GPIB address as "GPIB8::1::INSTR".

- Optional connection



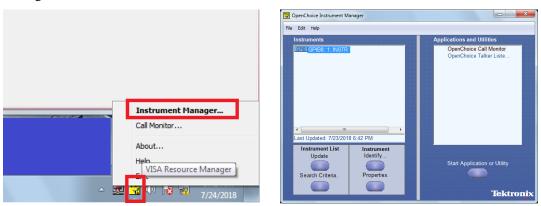
* TekVISA is needed to control Tektronix scopes. But, the PC on which TekVISA is installed cannot control Keysight scopes. Also, this configuration makes the remote control speed slower than the recommended configuration.

4. Launch application and configure equipment settings. Enter the scope address as below, and click \mathcal{G} . If the setting and connection are correct, the button will turn green.

Tektronix Scope

When the GRL software is installed on the laptop: TCPIP0::192.168.2.110::inst0::INSTR When the GRL software is installed on the scope: GPIBX::1::INSTR*

* Tektronix scope cannot use TCP/IP when the GRL software is installed on it. In this case, GPIB VISA should be set. The address can be checked using the VISA instruments Manager.



Keysight Scope

When the GRL software is installed on the laptop: TCPIP0::192.168.2.110::inst0::INSTR When the GRL software is installed on the scope: TCPIP0::localhost::inst0::INSTR

MX190000A: TCPIP0::192.168.2.100::5001::SOCKET* MX183000A: TCPIP0::192.168.2.100::5000::SOCKET* *

Port numbers should be set for MX190000A and MX183000A.

B. Before beginning Tx LEQ response time test

Before beginning Tx LEQ response time test, it is recommended to adjust the **CTLE Gain** value in MX183000A. Especially, this is efficient when DUT Tx has a large Insertion Loss like a System board. Also, in case of a link training error and/or bit error, adjust the **CTLE Gain** value.

Note:

Though the following procedure uses the screenshots for PCIe 4.0, read PCIe 4.0 as PCIe 3.0 here. Set **Specification** to **3.0** (**8 GT/s**), and then adjust the **CTLE Gain** value according to the following procedure.

a. In MX183000A, display the LEQ test settings and BER Measurement screen.

File Setup Help		Operate MP1900A
Equipment Setup Link Training Run Test Graph F	Report	Electrical Idle
Specification DUT		
4.0(16.0 GT/s) Endpoint (AIC) PCIe	4.0 Preset P7 : -6.0, 3	3.5 V Link Start
LTSSM State	CTLE Gain [dB]	0 🚔
	nreshold 1	LEQ Test 💟 Setting Tx LEQ Response
LEQ Test Tx LEQ Response Apply Pass/	/Fail	Configure
Ry LEO, Unitial TY LEO, TX LEO, Response		BER Measurement

b. Set CTLE Gain to 0 (zero) on the BER Measurement panel.

File Setup Help			Operate MP1900A
Equipment Setup Link Training Run Test Gr	aph Report	Electrical	Idle
Specification DUT			
4.0(16.0 GT/s) • Endpoint (AIC)	PCIe 4.0	Preset P7:-6.0.3.5 🔻	Link Start
LTSSM State		CTLE Gain [dB]	
Linkup Speed	EC Threshold	1	LEQ Test V Setting
LEQ Test Tx LEQ Response Apply	Pass/Fail		
Арру	Pass/Fall		Configure
Rx LEQ Initial TX LEQ Tx LEQ Response			BER Measurement

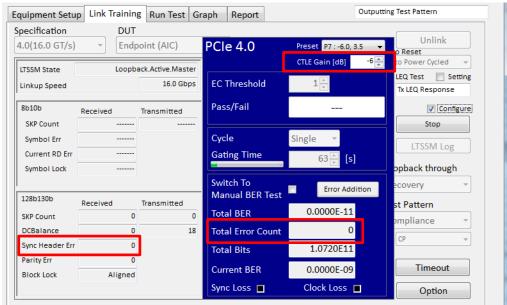
d. On the **Tx LEQ Response** tab of the LEQ test pane, set **PPG Starting Preset** to **7**, **DUT Initial Preset** to **7** and **Target Preset** to **P4**.

File Setup Help			Operate MP1900A
Equipment Setup Link Training Run Test Gra	aph Report	Electrica	lidle
Specification DUT 4.0(16.0 GT/s) ▼ Endpoint (AIC)	PCle 4.0	Preset P7 : -6.0, 3.5 ▼ CTLE Gain [dB] 0 ←	Link Start
LTSSM State	EC Threshold		LEQ Test V Setting Tx LEQ Response
LEQ Test Tx LEQ Response Apply	Pass/Fail		Configure BER Measurement
Rx LEQ Initial TX LIQ Tx LEQ Response Loopback Through: Recovery Link EQ: Preset Saved Cursor	Cycle Gating Time	Single ▼ 63 ★ [5]	LTSSM Log opback through
Lane: 0/8 Test Pattern: CP (Compliance Pattern)	Switch To Manual BER Test	Error Addition	ecovery 🔹
PPG Starting Preset:	Total BER Total Error Count	0.0000E-11 0	ompliance 🔹
DUT Initial Preset (Preset Hint Tx):	Total Bits	5.3760E11	CP 👻
DUT Target Preset (Change Preset)	Current BER Sync Loss 🔳	0.0000E-09 Clock Loss 🔳	Timeout Option

- e. Click Link Start.
- f. If the following conditions are met, adjust the **CTLE Gain** value. If there is no error, this procedure is assumed already to be done, so proceed to step h.
 - LTSSM State is not Loopback.Active.Master.
 - Sync Header Err is other than 0 (zero).

quipment Setu		g Run Test	Graph F	Report			g Test Pattern	
pecification 4.0(16.0 GT/s)	DUT Endp	ooint (AIC)	PCle	4.0	Preset P7:-6.0, 3.		Unlink to Reset	
LTSSM State	Loopb	ack.Active.Maste	er		CTLE Gain [dB]	0 🌲	to Power Cycled	
Linkup Speed		16.0 Gbp	s EC Th	reshold	1		LEQ Test 📃 🗄	Setting
8b10b	Received	Transmitted	Pass/	Fail			Cor	nfigure
SKP Count			•				Stop	
Symbol Err			Cycle		Single 👻		LTSSM Lo	
Current RD Err			Gatin	g Time	63 🔶 [s]			8
Symbol Lock							opback throug	gh
			Switc	h To al BER Test	Error Addi	tion	ecovery	-
128b130b	Received	Transmitted					st Pattern	
SKP Count	0		0 Total	BER			ompliance	-
DCBalance	0	1	8 Total	Error Count			СР	_
Sync Header Err	1057603		Total	Bits			LCP	Ψ
Parity Err	0						Timeout	
Block Lock	Aligned		Curre	nt BER			Timeout	
			Sync	Loss 📕	Clock Loss	1	Option	

h. Increment the **CTLE Gain** value, and run Link Training again until **Sync Header Err** becomes **0** (zero) and **Total Error Count** becomes **0** (zero). In this case, it is considered to be error free with -6 dB.



- i. Repeat steps d to f with DUT target Preset P7.
- j. After adjusting the CTLE Gain value, close the MX183000A application and return to the selector screen. The CTLE Gain value is stored on the MX183000A. And, start GRL Tx LEQ response time test again.