MU196020A PAM4 PPG MU196040A PAM4 ED MU196040B PAM4 ED Operation Manual

13th Edition

- For safety and warning information, please read this manual before attempting to use the equipment.
- Additional safety and warning information is provided within the MP1900A Signal Quality Analyzer-R Operation Manual. Please also refer to it before using the equipment.
- Keep this manual with the equipment.

ANRITSU CORPORATION

Safety Symbols

To prevent the risk of personal injury or loss related to equipment malfunction, Anritsu Corporation uses the following safety symbols to indicate safety-related information. Ensure that you clearly understand the meanings of the symbols BEFORE using the equipment. Some or all of the following symbols may be used on all Anritsu equipment. In addition, there may be other labels attached to products that are not shown in the diagrams in this manual.

Symbols used in manual



This indicates a very dangerous procedure that could result in serious injury or death if not performed properly.



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The following safety symbols are used inside or on the equipment near operation locations to provide information about safety items and operation precautions. Ensure that you clearly understand the meanings of the symbols and take the necessary precautions BEFORE using the equipment.



This indicates a prohibited operation. The prohibited operation is indicated symbolically in or near the barred circle.

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This indicates a warning or caution. The contents are indicated symbolically in or near the triangle.

This indicates a note. The contents are described in the box.

These indicate that the marked part should be recycled.

MU196020A PAM4 PPG MU196040A PAM4 ED MU196040B PAM4 ED Operation Manual

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Anritsu Corporation will repair this equipment free-of-charge if a malfunction occurs within one year after shipment due to a manufacturing fault, and software bug fixes will be performed in accordance with the separate Software End-User License Agreement, provide, however, that Anritsu Corporation will deem this warranty void when:

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- The fault is due to mishandling, misuse, or unauthorized modification or repair of the equipment by the customer.
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- The fault is due to improper or insufficient maintenance by the customer.
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- The fault is due to damage caused by acts of destruction, including civil disturbance, riot, or war, etc.
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Revision History:

February 29th, 2020 December 17th, 2021

CE Conformity Marking

Anritsu affixes the CE conformity marking on the following products in accordance with the Decision 768/2008/EC to indicate that they conform to the EMC, LVD and RoHS directive of the European Union (EU).

CE marking



1. Product Model

Plug-in Units:

MU196020A PAM4 PPG MU196040B PAM4 ED

2. Applied Directive and Standards

When the MU196020A PAM4 PPG and MU196040B PAM4 ED are installed in the MP1900A, the applied directive and standards of this unit conform to those of the MP1900A main frame.

PS: About main frame

Please contact Anritsu for the latest information on the main frame types that MU196020A and MU196040B can be used with.

UKCA Marking

Anritsu affixes the UKCA marking on the following products in accordance with the guidance to indicate that they conform to the EMC, LVD, and RoHS regulations in the United Kingdom.

UKCA marking



1. Product Model

Plug-in Units:

MU196020A PAM4 PPG MU196040B PAM4 ED

2. Applied Regulations and Standards

When the MU196020A PAM4 PPG and MU196040B PAM4 ED are installed in the MP1900A, the applied directive and standards of this unit conform to those of the MP1900A main frame.

PS: About main frame

Please contact Anritsu for the latest information on the main frame types that MU196020A and MU196040B can be used with.

RCM Conformity Marking

Anritsu affixes the RCM mark on the following products in accordance with the regulation to indicate that they conform to the EMC framework of Australia/New Zealand.

RCM marking



1. Product Model

Plug-in Units:

MU196020A PAM4 PPG MU196040A PAM4 ED MU196040B PAM4 ED

2. Applied Directive and Standards

When the MU196020A PAM4 PPG, MU196040A PAM4 ED and MU196040B PAM4 ED are installed in the MP1900A, the applied directive and standards of this unit conform to those of the MP1900A main frame.

PS: About main frame

Please contact Anritsu for the latest information on the main frame types that MU196020A, MU196040A and MU196040B can be used with.

About This Manual

A testing system combining an MP1900A Signal Quality Analyzer-R, module(s), and control software is called a Signal Quality Analyzer-R Series. The operation manuals of the Signal Quality Analyzer-R Series consist of separate documents for the MP1900A, module(s), and control software, as shown below.



Describes the panel details, how to operate, performance test, maintenance, and troubleshooting of the MU183040A, MU183041A, MU183040B, and MU183041B.

Configuration of Signal Quality Analyzer-R Series Operation Manuals (Cont'd)

 $\hfill \square$ indicates this document.

MX190000A Signal Quality Analyzer-R Control Software Operation Manual

Describes the operation of the software that controls the Signal Quality Analyzer-R Series.

Extended Application Operation Manual

Describes the operation of the extended application for the Signal Quality Analyzer-R Series.

MX183000A High-Speed Serial Data Test Software Operation Manual

Describes the setup and operating procedure of MX183000A.

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Chapter 1 Overview

This chapter describes the overview of the following modules.

- MU196020A PAM4 PPG (hereafter, MU196020A)
- MU196040A PAM4 ED (hereafter, MU196040A)
- MU196040B PAM4 ED (hereafter, MU196040B)

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1.1 Product Overview

The MU196020A, MU196040A, and MU196040B (hereinafter "MP1900A modules") are plug-in modules that can be built into the MP1900A Signal Quality Analyzer-R. MP1900A supports error measurement with PRBS patterns, DATA patterns and various PAM4 test patterns at the following bit rates or baud rates:

• MU196020A:

• MU196040A:

- Max. 64.2 Gbit/s or 64.2 Gbaud Max. 32.1 Gbit/s or 32.1 Gbaud
- MU196040B: Max. 64.2 Gbit/s or 58.2 Gbaud

Combination of MU196020A and MU195050A Noise Generator (hereinafter, MU195050A) supports generation of data which common mode noise, differential mode noise and white noise are applied to and which is optimal for signal integrity evaluation of up to 32.1 Gbaud. Various option configurations are available for the MP1900A modules. This module is therefore useful for research, development, and production of various types of digital communication equipment, modules, and devices.

The features of the MP1900A modules are as follows:

MU196020A features

- Capable of generating one channel of NRZ or PAM4 signal at up to 64.2 Gbit/s or 64.2 Gbaud. (MU196020A-003)
- Capable of independently adjusting the amplitude of each eye of PAM4 signal.
- Capable of generating signals of PRBS pattern, DATA pattern and various PAM4 patterns.
- Capable of signal integrity evaluation using 4TAP Emphasis (MU196020A-x11)
- Capable of adding intersymbol interference (ISI) using 4TAP Emphasis. (MU196020A-x40)
- Capable of generating patterns and inserting errors, which support RS-FEC(544,514) and RS-FEC(528,514). (MU196020A-z42)
- Capable of synchronizing operations among channels using multiple MU196020As that are installed in MP1900A.
 This function allows generating synchronous data supported by the application that requires Multi Channel. (MU196020A-x50)

MU196040A features

- Supporting symbol measurement of one channel of PAM4 signal at up to 32.1 Gbaud using the built-in PAM4 Decoder circuit.
- Capable of measuring signals of PRBS pattern, DATA pattern and various PAM4 patterns.

- Long user-programmable patterns (256 Mbits, 256 Msymbol)
- Capable of evaluating serial communication by selecting MU196040A-001 that has one data input channel each for NRZ (32.1 Gbit/s) and PAM4 (32.1 Gbaud).
- Having the input sensitivity (typical values) of NRZ 23 mV (32.1 Gbit/s, Eye Height) and PAM4 23 mV (32.1 Gbaud, Eye Height, per eye) and optimal for signal evaluation.
- Capable of clock recovery on 25.5 to 32.1 Gbaud signals by installing MU196040A-x22.
- Capable of evaluating PAM4 signals by Symbol Error Rate (SER) by installing MU196040A-x41.

MU196040B features

- Supporting symbol measurement of one channel of PAM4 signal at up to 58.2 Gbaud using the built-in PAM4 Decoder circuit.
- Capable of measuring signals of PRBS pattern, DATA pattern and various PAM4 patterns.
- Long user-programmable patterns (256 Mbits, 256 Msymbols)
- Capable of capturing the data pattern of up to 8 Mbits or 4 Msymbols.
- Capable of capturing the data pattern, in which RS-FEC Symbol Error(s) occurred, and counting FEC Symbol Errors.
- Capable of evaluating serial communication by selecting MU196040B-002 or y12 that has one data input channel each for NRZ (64.2 Gbit/s) and PAM4 (58.2 Gbaud).
- Having the input sensitivity (typical values) of NRZ 23 mV (32.1 Gbit/s, Eye Height) and PAM4 23 mV (32.1 Gbaud, Eye Height, per eye) and optimal for signal evaluation.
- Capable of using the Equalizer function by installing the MU196040Bx11.
- Capable of clock recovery on 2.4 to 29.0 Gbaud signals by installing MU196040B-x21.
- Capable of clock recovery on 2.4 to 32.1 Gbaud signals by installing MU196040B-x22.
- Capable of clock recovery on 51.0 to 58.2 Gbaud signals by installing MU196040B-x23.
- Capable of evaluating PAM4 signals by Symbol Error Rate (SER) by installing MU196040B-z41.
- Capable of measuring Uncorrectable Codewords and FEC symbol errors in RS-FEC Scrambled Idle pattern by installing the MU196040B-w42.

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1.2 Product Configuration

1.2.1 Standard configuration

Table 1.2.1-1 and Table 1.2.1-2 below show the standard configurations of the three MP1900A modules respectively.

ltem	Model Name	Product Name	Q'ty	Remarks
Mainframe	MU196020A	PAM4 PPG	1	
Accessories	J1632A	Terminator	4	Clock Output, Aux Output × 2, Gating Output
	V210	Terminator	2	Data Output × 2
	J1341A	Open	2	Ext Clock Input, AUX Input
	J1359A	Coaxial Adaptor (K-P.K-J, SMA)	1	Clock Output
	J1717A	Coaxial Adaptor (SMA-P, SMA-J)	5	Ext Clock Input, Aux Output × 2, Gating Output, AUX Input

Table 1.2.1-1 Standard	Configuration	of MU196020A
------------------------	---------------	--------------

Item	Model Name	Product Name	Q'ty	Remarks
Mainframe	MU196040A	PAM4 ED	1	
Accessories	J1632A	Terminator	2	Aux Output × 2
	J1341A	Open	2	Ext Clock Input, AUX Input
	J1359A	Coaxial Adaptor (K-P.K-J, SMA)	1	Ext Clock Input
	J1717A	Coaxial Adaptor (SMA-P, SMA-J)	3	Aux Output × 2, AUX Input
	When the MU196040.	A-001 is installed:		
	J1341A	Open	2	Data Input × 2
	J1359A	Coaxial Adaptor (K-P.K-J, SMA)	2	Data Input × 2

1.2 Product Configuration

Item	Model Name	Product Name	Q'ty	Remarks
Mainframe	MU196040B	PAM4 ED	1	
Accessories	V210	Terminator	2	Data Input × 2
	J1341A	Open	2	Ext Clock Input, AUX Input
	J1359A	Coaxial Adaptor (K-P.K-J, SMA)	1	Ext Clock Input
	J1632A	Terminator	2	Aux Output × 2
	J1717A	Coaxial Adaptor (SMA-P, SMA-J)	3	Aux Output × 2, AUX Input
	41V-6	Precision Fixed Attenuator	2	Data Input × 2

 Table 1.2.1-3
 Standard Configuration of MU196040B

1.2.2 Options

Table 1.2.2-1 and Table 1.2.2-2 show the options for the MP1900A modules. All options are sold separately.

Notes:

• Option name format is as follows:

MU196020A-x x x

•



For how to install software options, refer to 2.4 "Adding Plug-In Module Options" in the *MX190000A Signal Quality Analyzer-R Control Software Operation Manual.*

Model Name	Product Name	Remarks
MU196020A-001	32G baud	*1
MU196020A-002	58G baud	*1
MU196020A-003	64G baud	*1
MU196020A-y12	32G to 58G baud Extension Retrofit	* 2, * 3
MU196020A-y13	32G to 64G baud Extension Retrofit	* 2, * 3
MU196020A-y23	58G to 64G baud Extension Retrofit	*2, *4
MU196020A-x11	4Tap Emphasis	*5
MU196020A-x30	Data Delay	*5
MU196020A-z40	Adjustable ISI	*6, *7, *8
MU196020A-z42	FEC Pattern Generation	*6, *8
MU196020A-x50	Inter-Module Synchronization	* 5, * 9, * 10

Table 1.2.2-1 Options of MU196020A

*1: Factory-installed hardware option. Select one from among them.

- *2: Hardware retrofit options, which can be selected after shipping from our factory. (y = 1 or 2)
- *3: It can be retrofitted when the Option 001 is installed.

1

Overview

Product Configuration

*4: It can be retrofitted when the Option 002 or y12 is installed.

1.2

- *5: x = 0, 1, or 2
- *6: z = 0, 1, 2, or 3
- *7: It can be retrofitted when the Option x11 is installed.
- *8: Options 040, 142, 140, 142, 240, and 242 work with version 3.01.07 and later of the MX190000A.
 Options 340 and 342 work with version 5.00.90 and later of the MX190000A.
- *9: It can be retrofitted when the Option x30 is installed.
- *10: It works with version 3.01.07 and later of the MX190000A.

Table 1.2.2-2 Options of MU196040A

Model Name	Product Name	Remarks
MU196040A-001	32.1G baud Decoder	*1
MU196040A-x22	25.5G to 32.1G baud Clock Recovery	* 2, * 3
MU196040A-x41	SER Measurement	*2, *4

- *1: Factory-installed hardware option
- *2: x = 0, 1, or 2
- *3: Hardware option
- *4: Software option

Table 1.2.2-3 Options of MU196040B

Model Name	Product Name	Remarks
MU196040B-001	32G baud	*1
MU196040B-002	58G baud	*1
MU196040B-x11	Equalizer	*2
MU196040B-y12	32G to 58G baud Extension	*3, *4
MU196040B-x21	29G baud Clock Recovery	*2, *5, *6, *7
MU196040B-x22	32G baud Clock Recovery	*2, *5, *6, *7
MU196040B-x23	58G baud Clock Recovery Extension	*2, *8
MU196040B-y24	32G baud Clock Recovery Extension	* 3, * 5, * 9
MU196040B-z41	SER Measurement	*10
MU196040B-w42	FEC Analysis	*11

- *1: Factory-installed
- *2: x = 0, 1, or 2
- *3: y = 1 or 2
- *4: MU196040B-001 must be installed.
- *5: Hardware option
- *6: This option can be installed together with MU196040B-x23.

- *7: One of MU196040B-x21 and MU196040B-x22 can be installed.
- *8: MU196040B-002 or MU196040B-y12 must be installed. MU196040B-x21 or MU196040B-x22 must be installed.
- *9: MU196040B-x21 must be installed.

*10: z = 0, 1, 2, or 3

*11: w = 0 or 3

1.2.3 Optional accessories

Table 1.2.3-1 shows the optional accessories for the MP1900A modules. All optional accessories are sold separately.

Model Name	Product Name	Remarks
34VFK50	Precision Adapter	Conversion connector (V-F K-M)
34VKF50	Precision Adapter	Conversion connector (V-M K-F)
41KC-3	Precision Fixed Attenuator 3 dB	K connector
41KC-6	Precision Fixed Attenuator 6 dB	K connector
41KC-10	Precision Fixed Attenuator 10 dB	K connector
41KC-20	Precision Fixed Attenuator 20 dB	K connector
41V-3	Precision Fixed Attenuator 3 dB	V connector
41V-6	Precision Fixed Attenuator 6 dB	V connector
41V-10	Precision Fixed Attenuator 10 dB	V connector
41V-20	Precision Fixed Attenuator 20 dB	V connector
J1342A	Coaxial Cable 0.8 m	APC3.5 connector
J1359A	Coaxial Adaptor (K-P.K-J, SMA)	
J1439A	Coaxial Cable 0.8 m (K connector)	
J1510A	Pick OFF Tee	K connector
J1624A	Coaxial Cable 0.3 m (SMA connector)	
J1625A	Coaxial Cable 1 m (SMA connector)	
J1632A	Terminator	SMA connector
J1678A	ESD Protection Adapter-K	K connector
J1679A	ESD Protection Adapter-V	V connector
J1728A	Electrical Length Specified Coaxial Cable (0.4 m, K connector)	

Table 1.2.3-1	Optional Accessories
---------------	-----------------------------

1.2 Product Configuration

Model Name	Product Name	Remarks
J1748A	Power Splitter (1.5G-18GHz)	
J1758A	ISI Board	
J1789A	Electrical Length Specified Coaxial Cable (0.4m, V connector)	
J1790A	Electrical Length Specified Coaxial Cable (0.8m, V connector)	
J1792A	Skew match pair semirigid cable (V-K connector, Data Input1)	For connecting to the Data Input1 connector of MU195050A
J1793A	Pick OFF Tee	V connector
J1800A	ISI Board V	V connector
K240C	Precision Power Divider	K connector
V210	Terminator	V connector
V240C	Precision Power Divider	V connector
W3976AE	MU196020A/40A/40B Operation Manual	Printed version, English
Z0306A	Wrist strap	
Z1964A	Torque Wrench (Right Angle)	

Table 1.2.3-1 Optional Accessories (Cont'd)

1.3 Specifications

1.3.1 Specifications for MU196020A

Table 1.3.1-1	Operating Baud/Bit Rate
	operating Daua/Dit Nate

Item	Specifications	
Operating Baud/Bit Rate	When the Option 001 is installed.	
	PAM4: 2.4 to 32.1 Gbaud	
	NRZ: 2.4 to 32.1 Gbit/s	
	When the Option 002 or y12 is installed.	
	PAM4: 2.4 to 58.2 Gbaud*1	
	NRZ: 2.4 to 58.2 Gbit/s*1	
	When the Option 003, y13, or y23 is installed.	
	PAM4: 2.4 to 64.2 Gbaud*1	
	NRZ: 2.4 to 64.2 Gbit/s*1	
	The setting range of the baud rate (PAM4 output) and bit rate (NRZ	
	output) is common. Only the baud rate is described hereafter.	
Setting Range / Step	The setting range of the baud rate is determined by the interlocking	
	module (valid only when installed to the same frame as MU196020A),	
	Frequency in Table 1.3.1-12 "Clock Output", and the application used.	
When linking with	$2.400\ 000$ to $25.000\ 000$ Gbaud, $0.000\ 002$ Gbaud step*3, *4, *5	
MU181000A/B*2	25.000 004 to 32.100 000 Gbaud, 0.000 004 Gbaud step*3, *4, *5	
	$25.000\ 004$ to $50.000\ 000$ Gbaud, $0.000\ 004$ Gbaud step*4, *5, *6	
	50.000 008 to 58.200 000 Gbaud, 0.000 008 Gbaud step*4, *7	
	50.000 008 to 64.200 000 Gbaud, 0.000 008 Gbaud step*5, *7	
When linking with	2.400 000 to 3.125 000 Gbaud, 0.000 002 Gbaud step*3, *4, *5	
MU181000A/B and	3.200 002 to 6.250 000 Gbaud, 0.000 002 Gbaud step*3, *4, *5	
$MU181500B^{*2}$	$6.400\ 002$ to $12.500\ 000$ Gbaud, $0.000\ 002$ Gbaud step*3, *4, *5	
	12.800 002 to 25.000 000 Gbaud, 0.000 002 Gbaud step* ^{3, *4, *5}	
	25.600 004 to 32.100 000 Gbaud, 0.000 004 Gbaud step*3, *4, *5	
	25.600 004 to 50.000 000 Gbaud, 0.000 004 Gbaud step*4, *5, *6	
	51.200 008 to 58.200 000 Gbaud, 0.000 008 Gbaud step*4, *7	
	51.200 008 to 64.200 000 Gbaud, 0.000 008 Gbaud step $^{*5, *7}$	
	*1: When BERT for PCIe1-6 is selected:	

PAM4:	2 4 to 32 1 Ghaud	

NRZ:	2.4 to 32.1 Gbit/s

- *2: Linking is not available when **Unit Sync** is **ON**.
- *3: When the Option 001 is installed.
- *4: When the Option 002 or y12 is installed.
- *5: When the Option 003, y13, or y23 is installed.
- *6: When BERT for PCIe1-6 is selected, the upper limit is 32.1 Gbaud.
- *7: Cannot be set in BERT for PCIe1-6.

1.3 Specifications

Item	:	Specifications	
When linking with MU181500B and using external clock			
Clock Output Rate Full Rate	Baud Rate Setting Range	Input Clock Frequency	Relationship Between Baud Rate and Input Clock Frequency
	2.4 to 15.0 Gbaud* ^{3, *4, *5}	2.4 to $15.0~\mathrm{GHz}$	1/1 Clock Input
	15.0 to 30.0 Gbaud* ^{3, *4,*5}	7.5 to $15.0~\mathrm{GHz}$	1/2 Clock Input
	25.0 to 32.1 Gbaud*3, *4, *5	6.25 to $8.025~\mathrm{GHz}$	1/4 Clock Input
Clock Output Rate Half Rate, Quarter Rate	Baud Rate Setting Range	Input Clock Frequency	Relationship Between Baud Rate and Input Clock Frequency
	$2.4 \text{ to } 30.0 \text{ Gbaud}^{*_{3,} *_{4,} *_5}$	1.2 to $15.0~\mathrm{GHz}$	1/2 Clock Input
	30.0 to 32.1 Gbaud* ³	7.5 to $8.025~\mathrm{GHz}$	1/4 Clock Input
	30.0 to 58.2 Gbaud*4, *6	7.5 to $14.55~\mathrm{GHz}$	1/4 Clock Input
	30.0 to 60.0 Gbaud*5, *6	7.5 to $15.0~\mathrm{GHz}$	1/4 Clock Input
	50.0 to 58.2 Gbaud*4, *7	6.25 to $7.275~\mathrm{GHz}$	1/8 Clock Input
	50.0 to 64.2 Gbaud*5, *7	6.25 to $8.025~\mathrm{GHz}$	1/8 Clock Input

Table 1.3.1-1 Operating Baud/Bit Rate (Cont'd)

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ltem	Specifications		
External Clock			
When the Output Clock Rate is set to Full Rate	Baud Rate Setting Range	Input Clock Frequency	Relationship Between Baud Rate and Input Clock Frequency
	2.4 to 16.05 Gbaud* ^{3, *4, *5}	2.4 to $16.05~\mathrm{GHz}$	1/1 Clock Input
	16.05 to 32.1 Gbaud* ^{3, *4, *5}	8.025 to 16.05 GHz	1/2 Clock Input
	25.0 to 32.1 Gbaud* ₃ , * ₄ , * ₅	6.25 to $8.025~\mathrm{GHz}$	1/4 Clock Input
When the Output Clock Rate is set to Half Rate, Quarter Rate	Baud Rate Setting Range	Input Clock Frequency	Relationship Between Baud Rate and Input Clock Frequency
	2.4 to 32.1 Gbaud* ^{3, *4, *5}	1.2 to $16.05~\mathrm{GHz}$	1/2 Clock Input
	25.0 to 32.1 Gbaud*3	6.25 to $8.025~\mathrm{GHz}$	1/4 Clock Input
	25.0 to 50.0 Gbaud*4, *5, *6	6.25 to $12.50~\mathrm{GHz}$	1/4 Clock Input
	32.1 to 58.2 Gbaud* ₄ , * ₆	8.025 to $14.55~\mathrm{GHz}$	1/4 Clock Input
	32.1 to 64.2 Gbaud* ^{5, *6}	8.025 to $16.05~\mathrm{GHz}$	1/4 Clock Input
	50.0 to 58.2 Gbaud*4, *7	6.25 to $7.275~\mathrm{GHz}$	1/8 Clock Input
	50.0 to 64.2 Gbaud* ₅ , * ₇	6.25 to $8.025~\mathrm{GHz}$	1/8 Clock Input
Offset Setting Range/Step	-1000 to +1000 ppm, 1 ppm step		
	The setting range is, however follows: Clock Output Rate Full Rate 12.500 000 Gbaud, 25.00 Clock Output Rate Half Rate	0 000 Gbaud , Quarter Rate	en the bit rate is set as

Table 1.3.1-1 Operating Baud/Bit Rate (Cont'd)

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 Table 1.3.1-2
 Jitter Setting Range

*1: When linking with MU181000A/B and MU181500B

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Table 1.3.1-2 Jitter Setting Range (Cont'd)

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Table 1.3.1-2 Jitter Setting Range (Cont'd)

Chapter 1 Overview



Table 1.3.1-2 Jitter Setting Range (Cont'd)

*2: The modulation frequency (Hz) is 10.01M to 150M when both of the following conditions are met:

Operation Baud Rate is $50 \leq$ Baud rate ≤ 60 Gbaud.

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Relationship between Baud Rate and Input Clock Frequency is set to 1/8 Clock Input with Clock Output Rate Half Rate and Quarter Rate in Table 1.3.1-1.



Table 1.3.1-2 Jitter Setting Range (Cont'd)

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Table 1.3.1-2 Jitter Setting Range (Cont'd)

1.3 Specifications

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Chapter 1 Overview




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Overview



Table 1.3.1-2 Jitter Setting Range (Cont'd)



Table 1.3.1-2 Jitter Setting Range (Cont'd)





Item	Spo	ecifications*1	
Built-in SJ2 Clock	$15 < Baud rate \le 32.1 Gbaud$		
Output Rate	Modulation Frequency (Hz)	Jitter Amplitude (Ulp-p)	
At Full Rate	33k	0 to 1000	
	87M	0 to 0.5	
	100M	0 to 0.5	
	210M	0 to 0.2	
	4 < Baud rate ≤ 15 Gbaud		
	Modulation Frequency (Hz)	Jitter Amplitude (Ulp-p)	
	33k	0 to 500	
	87M	0 to 0.25	
	100M	0 to 0.25	
	210M	0 to 0.1	
	$2.4 \leq \text{Baud rate} \leq 4 \text{ Gbaud}$		
	Modulation Frequency (Hz)	Jitter Amplitude (Ulp-p)	
	33k	0 to 500	
	87M	0 to 0.25	
	100M	0 to 0.25	
Built-in SJ2 Clock	$8 < Baud rate \le 64.2 Gbaud$		
Output Rate	Modulation Frequency (Hz)	Jitter Amplitude (Ulp-p)	
Rate	33k	0 to 1000	
	87M	0 to 0.5	
	100M	0 to 0.5	
	210M	0 to 0.2	
	$2.4 < Baud rate \le 8 Gbaud$		
	Modulation Frequency (Hz)	Jitter Amplitude (Ulp-p)	
	33k	0 to 1000	
	87M	0 to 0.5	
	100M	0 to 0.5	
	100M Baud rate 2.4 Gbaud	0 to 0.5	
	100M Baud rate 2.4 Gbaud Modulation Frequency (Hz)	0 to 0.5 Jitter Amplitude (Ulp-p)	

Table 1.3.1-2 Jitter Setting Range (Cont'd)

Table 1.3.1-3 External Clock Input	
Item	Specifications
Number of Inputs	1 (Single-Ended)
Input frequency range	1.2 to 16.05 GHz
Input amplitude	0.3 to 1.0 Vp·p (-6.5 to +4.0 dBm)
Termination	50Ω , AC Coupling
Connector	SMA connector (f.)

Table 1.3.1-3 External Clock Input

Table 1.3.1-4 Aux Input

Item	Specifications
Number of Inputs	1 (Single-Ended)
Variation	Error Injection, Burst, Unit Sync
Minimum Pulse Width	1/256 of data rate
Input level	• 0/-1 V (H: -0.25 to 0.05 V, L: -1.1 to -0.8 V)
	• 0/-0.5 V (H: -0.05 to 0.05 V, L: -0.55 to -0.45 V)
	• Vth 0 V (Input amplitude: 0.5 to 1.0 Vp-p)
	Select one of the above.
Termination	50Ω , GND
Connector	SMA connector (f.)

Table 1.3.1-5 Aux Output

Item	Specifications
Number of Outputs	2 (Differential output)
Output control	ON/OFF switching
Variation	1/n Clock (n = 8, 12, 16, 201020, 1024), Pattern Sync, Burst Out2
Pattern Sync	
PRBS, PRGM	Position: 1 to {(Least common multiple of Pattern Length' and 256) -263}, in 8 steps
	When the pattern length is 1023 bits or less, Pattern Length' is the length as an integer multiple so that it becomes 1024 bits or more.
Burst Out2	
Burst Trigger Delay	0 to (Burst Cycle -256) bits, 8 bits step
Pulse Width	16 to (Burst Cycle -256) bits, 8 bits step
Output level	0/-0.6 V (H: -0.25 to 0.05 V, L: -0.80 to -0.45 V)
Termination	50Ω , GND
Connector	SMA connector (f.)

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Item	Specifications
Number of Outputs	1 (Single-Ended)
Output control	ON/OFF switching
Variation	Burst, Repeat
Burst	Burst Output
Burst Trigger Delay	0 to (Burst Cycle -256) bits, 8 bits step
Enable Pulse Width	16 to (Burst Cycle -256) bits, 8 bits step
Output Level	0/-1 V (H: -0.25 to 0.05 V, L: -1.25 to -0.8 V)*
Repeat	Timing Signal Output
Timing Signal Cycle	INT $(\frac{\text{Pattern length'}}{256}) \times 256$
Timing Signal Delay	0 to {(Least common multiple of Pattern Length' and 256) –256}
	The maximum settable number is 68 719 476 480, in 8-bit steps
	When the pattern length is 1023 bits or less, Pattern Length' is the length as an integer multiple so that it becomes 1024 bits or more.
Timing Signal Pulse	256 to {(Least common multiple of Pattern Length' and 256) –256}
Width	The maximum settable number is 68 719 476 480, in 8-bit steps
	When the pattern length is 1023 bits or less, Pattern Length' is the
	length as an integer multiple so that it becomes 1024 bits or more.
Output Level	0/-1 V (H: -0.25 to 0.05 V, L: -1.25 to -0.8 V)*
Unit Sync Output	Outputs the timing signal when Unit Sync is set to ON .
Termination	50Ω , GND
Connector	SMA connector (f.)

Table 1.3.1-6	Gating	Output
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*: L: Output Enable, H: Output Disable

Table 1.3.1-7	Generated	Pattern
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ltem	Specifications
PRBS	
Pattern Length	$2^{n}-1$ ($n = 7, 9, 10, 11, 13, 15, 20, 23, 31$)
Mark ratio	1/2 (1/2INV is supported by a logical inversion.)
PRBS generator	$n = 7$: $1 + X^6 + X^7$
polynomial	$n = 9:$ $1 + X^5 + X^9$
	$n = 10: 1 + X^7 + X^{10}$
	$n = 11: 1 + X^9 + X^{11}$
	$n = 13: 1 + X + X^2 + X^{12} + X^{13}$
	$n = 15: 1 + X^{14} + X^{15}$
	$n = 20$: $1 + X^3 + X^{20}$
	n = 23: 1 + X ¹⁸ + X ²³
	$n = 31: 1 + X^{28} + X^{31}$
PRBS Inversion	This is available in PAM4 mode only.
	Logical inversion of PRBS can be set independently for MSB and LSB.

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Overview

ltem	Specifications
Zero-Substitution	This is available in NRZ mode only.
Additional bit	0 bit, 1 bit
Pattern Length	2^{n} (n = 7, 9, 10, 11, 15, 20, 23)
	$2^{n}-1$ (n = 7, 9, 10, 11, 15, 20, 23)
Start position	Bit after the longest run of zero bits
Length of Consecutive	1 to (Pattern Length -1) bits
Zero Bits	If the bit coming after Zero-substitution is "0", then it is replaced with "1".
Data	
Data Length	NRZ: 2 to 268 435 456 bits, 1 bit step
_	PAM4: 2 to 268 435 456 symbols, 1 symbol step
Bit Shift	This is available in PAM4 mode only.
	Bit shift of MSBs can be controlled in the range of ±256 bits (in 1-bit steps).
PAM4 Standard Pattern	Standard-compliant PAM4-mode patterns
CEI	QPRBS13-CEI, QPRBS31-CEI
IEEE	IEEE802.3bs/cd: PRBS13Q, PRBS31Q, SSPRQ, Square Wave
	IEEE802.3bj: QPRBS13, JP03A, JP03B, Transmitter Linearity
InfiniBand	PRBS13Q (InfiniBand), PRBS23Q, PRBS31Q (InfiniBand)
Fibre Channel	PRBS31Q (Fibre Channel)
RS-FEC	When the Option z42 is installed.
	RS-FEC Scrambled Idle 50G 1Lane,
	RS-FEC Scrambled Idle 100G 1Lanes,
	RS-FEC-Int Scrambled Idle 100G 1Lanes,
	RS-FEC Scrambled Idle 100G 2Lanes,
	RS-FEC Scrambled Idle 200G 2Lanes,
	RS-FEC Scrambled Idle 200G 4Lanes,
	RS-FEC Scrambled Idle 400G 4Lanes,
D.G.	RS-FEC Scrambled Idle 400G 8Lanes
PCle	CP in 1b/1b Encoding for PCIe6
	MCP in 1b/1b Encoding for PCIe6
	Jitter Measurement Pattern in 1b/1b Encoding for PCIe6
	High Swing Toggle Pattern in 1b/1b Encoding for PCIe6
	Low Swing Toggle Pattern 1b/1b Encoding for PCIe6
	Jitter Calibration Pattern for PCIe6
	Preset Calibration Pattern for PCIe6

Table 1.3.1-7	Generated Pattern	(Cont'd)
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Item	Specifications
NRZ Standard Pattern	Standard-compliant NRZ-mode pattern
CEI	SSPR
RS-FEC	When the Option z42 is installed.
	RS-FEC Scrambled Idle 25G 1Lane,
	RS-FEC Scrambled Idle 50G 2Lanes RS(544,514),
	RS-FEC Scrambled Idle 100G 4Lanes,
	RS-FEC Scrambled Idle 100G 4Lanes RS(544,514)
PCIe	CP in 8b/10b Encoding for PCIe1
	MCP in 8b/10b Encoding for PCIe1
	Jitter Calibration Pattern for PCIe1
	Preset Calibration Pattern for PCIe1
	CP in 8b/10b Encoding for PCIe2
	MCP in 8b/10b Encoding for PCIe2
	Jitter Calibration Pattern for PCIe2
	Preset Calibration Pattern for PCIe2
	CP in 128b/130b Encoding for PCIe3
	MCP in 128b/130b Encoding for PCIe3
	Jitter Calibration Pattern for PCIe3
	Preset Calibration Pattern for PCIe3
	CP in 128b/130b Encoding for PCIe4
	MCP in 128b/130b Encoding for PCIe4
	Jitter Calibration Pattern for PCIe4
	Preset Calibration Pattern for PCIe4
	CP in 128b/130b Encoding for PCIe5
	MCP in 128b/130b Encoding for PCIe5
	Jitter Calibration Pattern for PCIe5
	Preset Calibration Pattern for PCIe5

Table 1.3.1-7 Generated Pattern (Cont'd)

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Overview

Item	Specifications	
Sequence	Repeat, Burst	
Repeat	Continuous Pattern	
Burst	This is available only when Coding is NRZ.	
Source	Internal, External-Trigger (Aux Input), External-Enable (Aux Input)	
Data Sequence	Restart, Consecutive, Continuous	
Enable period	Internal: 12 800 to 2 147 483 136 bits, 256 bits step	
	External-Trigger, External-Enable:	
	12 800 to 2 147 483 648 bits, 256 bits step	
Burst Cycle	25 600 to 2 147 483 648 bits, 1 024 bits step	

Table 1.3.1-9 Coding

ltem	Specifications
Coding	NRZ, PAM4
NRZ	Normal, Invert
PAM4 Gray Coding	ON, OFF
PAM4 Precoding $(1/(1 + D) \mod 4)^*$	ON, OFF
Delay Symbol	ON, OFF
SKP	No SKP, SKPx1, SKPx2
Preset	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10
SRIS	ON, OFF
EIEOS	ON

*: $(1/(1+D) \mod 4)$ is a generator polynomial defined in the IEEE802.3.

Table 1.3.1-10 Error Addition

Item	Specifications
Туре	Bit, Error on MSB, Error on LSB, Error on LSB&MSB, RS-FEC Symbol Error*
Bit	This is available only when Coding is NRZ.
Source	Internal, External-Trigger (Rise edge trigger), External-Disable (L: Disable)
Error Variation	Repeat, Single (Cannot be selected when Source is External-Trigger.)
Error Rate	*E-n (* = 1 to 9, n = 3 to 12), Upper limit: 3.0E-3
Error Route	Select 1 to 32, Scan
Bit/Burst	Switching between Bit and Burst
Burst Length	1 to 256, 1 step

*: When the Option z42 is installed.

Item	Specifications	
RS-FEC Symbol Error	This is available whether Coding is NRZ or PAM4.*	
	When Coding is PAM4, an error is inserted to make the PAM4 signal	
	change by one level only.	
	NRZ: An error is inserted every 10 bits.	
	PAM4: An error is inserted every 10 or 20 PAM4 symbols.	
FEC Standard	When Coding is NRZ:	
	RS-FEC Scrambled Idle 25G 1Lane,	
	RS-FEC Scrambled Idle 50G 2Lanes RS(544,514),	
	RS-FEC Scrambled Idle 100G 4Lanes,	
	RS-FEC Scrambled Idle 100G 4Lanes RS(544,514)	
	When Coding is PAM4:	
	RS-FEC Scrambled Idle 50G 1Lane,	
	RS-FEC Scrambled Idle 100G 1Lanes,	
	RS-FEC-Int Scrambled Idle 100G 1Lane,	
	RS-FEC Scrambled Idle 100G 2Lanes,	
	RS-FEC Scrambled Idle 200G 2Lanes,	
	RS-FEC Scrambled Idle 200G 4Lanes,	
	RS-FEC Scrambled Idle 400G 4Lanes,	
	RS-FEC Scrambled Idle 400G 8Lanes	
Source	Internal, External-Trigger (Rise edge trigger),	
	External-Disable (L: Disable)	
Error Variation	Repeat, Single (Cannot be selected when Source is External-Trigger.)	
Symbol error per	1 to 20 (When Coding is NRZ.)	
codeword	1 to 20 (When Coding is PAM4.)	
Total BER for All Lane	*E–n (* = 1 to 9, n = 3 to 12), Upper limit: 3.0E–3	
	The error addition range varies depending on the value of Symbol Error per Codeword.	
BER for One Lane/	*E-n (* = 1 to 9, n = 3 to 12), Upper limit:9.0E-3	
SER for One Lane	The error addition range varies depending on the value of Symbol Error per Codeword.	

Table 1.3.1-10	Error Addition (Cont'd)	
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Overview

Item	Specifications
RS-FEC Symbol Error	•
(Cont'd)	
Error Addition Method	Type1:
	Level $0 \rightarrow$ Level 1, Level $1 \rightarrow$ Level 2,
	Level 2 \rightarrow Level 3, Level 3 \rightarrow Level 2
	Type2:
	Level $0 \rightarrow$ Level 1, Level $1 \rightarrow$ Level 2,
	Level 2 \rightarrow Level 1, Level 3 \rightarrow Level 2
	Type3:
	Level $0 \rightarrow$ Level 1, Level $1 \rightarrow$ Level 0,
	Level 2 \rightarrow Level 1, Level 3 \rightarrow Level 2
	Type4:
	Level $0 \rightarrow$ Level 1,
	Level $1 \rightarrow$ Level 0 or Level 2,
	Level 2 \rightarrow Level 1 or Level 3,
	Level $3 \rightarrow$ Level 2
	MSB Only:
	Level $0 \rightarrow$ Level 2, Level $1 \rightarrow$ Level 3,
	Level 2 \rightarrow Level 0, Level 3 \rightarrow Level 1
	LSB Only:
	Level $0 \rightarrow$ Level 1, Level $1 \rightarrow$ Level 0,
	Level 2 \rightarrow Level 3, Level 3 \rightarrow Level 2
	MSB or LSB:
	Level $0 \rightarrow$ Level 1 or Level 2,
	Level $1 \rightarrow$ Level 0 or Level 3,
	Level $2 \rightarrow$ Level 0 or Level 3,
	Level $3 \rightarrow$ Level 1 or Level 2
	MSB and LSB:
	Level $0 \rightarrow$ Level 3, Level $1 \rightarrow$ Level 2,
	Level 2 \rightarrow Level 1, Level 3 \rightarrow Level 0

Table 1.3.1-10	Error Addition	(Cont'd)
	Enor Addition	(oont u)

Item	Specifications	
Error on MSB	Adds the specified symbol error.	
	This is available only when Coding is PAM4.	
	The set error is added to MSB only.	
Source	Internal, External-Trigger (Rise edge trigger), External-Disable (L: Disable)	
Error Variation	Repeat, Single (Cannot be selected when Source is External-Trigger.)	
Symbol Error Rate	*E-n (* = 1 to 9, n = 3 to 12), Upper limit: 3.0E-3	
Symbol/Burst	Switching between Symbol and Burst	
Burst Length	1 to 256, 1 step	
Error on LSB	Adds the specified symbol error.	
	This is available only when Coding is PAM4.	
	The set error is added to LSB only.	
Source	Internal, External-Trigger (Rise edge trigger), External-Disable (L: Disable)	
Error Variation	Repeat, Single (Cannot be selected when Source is External-Trigger.)	
Symbol Error Rate	*E-n (* = 1 to 9, n = 3 to 12), Upper limit: 3.0E-3	
Symbol/Burst	Switching between Symbol and Burst	
Burst Length	1 to 256, 1 step	

Table 1.3.1-10 Error Addition (Cont'd)

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Item	Specifications		
Error on LSB&MSB	Adds the specified symbol error.		
	This is available only when Coding is PAM4.		
	An error is inserted to make the PAM4 signal change by one level only.		
Source	Internal, External-Trigger (Rise edge trigger),		
	External-Disable (L: Disable)		
Error Variation	Repeat, Single (Cannot be selected when Source is External-Trigger.)		
Symbol Error Rate	*E-n (* = 1 to 9, n = 3 to 12), Upper limit: 3.0E-3		
Symbol/Burst	Switching between Symbol and Burst		
Burst Length	1 to 256. 1 step		
Error Addition Method	Type1:		
	Level $0 \rightarrow$ Level 1, Level $1 \rightarrow$ Level 2.		
	Level 2 \rightarrow Level 3, Level 3 \rightarrow Level 2		
	Type2:		
	Level $0 \rightarrow$ Level 1, Level $1 \rightarrow$ Level 2,		
	Level 2 \rightarrow Level 1, Level 3 \rightarrow Level 2		
	Туре3:		
	Level $0 \rightarrow$ Level 1, Level $1 \rightarrow$ Level 0,		
	Level 2 \rightarrow Level 1, Level 3 \rightarrow Level 2		
	Type4:		
	Level $0 \rightarrow$ Level 1,		
	Level $1 \rightarrow$ Level 0 or Level 2,		
	Level $2 \rightarrow$ Level 1 or Level 3,		
	Level 3 7 Level 2		
	MSB Unity.		
	Level $0 \rightarrow$ Level 2, Level $1 \rightarrow$ Level 3, Level $2 \rightarrow$ Level 0, Level $2 \rightarrow$ Level 1		
	Level 2 / Level 0, Level 3 / Level 1		
	Lovel $0 \rightarrow \text{Lovel } 1 \rightarrow \text{Lovel } 0$		
	Level $2 \rightarrow$ Level 3 Level $3 \rightarrow$ Level 2		
	MSB or LSB:		
	Level $0 \rightarrow$ Level 1 or Level 2.		
	Level $1 \rightarrow$ Level 0 or Level 3,		
	Level 2 \rightarrow Level 0 or Level 3,		
	Level $3 \rightarrow$ Level 1 or Level 2		
	MSB and LSB:		
	Level $0 \rightarrow$ Level 3, Level $1 \rightarrow$ Level 2,		
	Level 2 \rightarrow Level 1, Level 3 \rightarrow Level 0		

Item	Specifications*1		
Number of Outputs	2 (Data, XData) Cannot be varied independently		
Waveform	NRZ, PAM4		
NRZ Eye Amplitude			
Setting Range	NRZ: 70 to 800 mVp-p, 2 mV step (Single-Ended)		
Accuracy	When using the J1789A: $\pm 35 \text{ mV} \pm 12 \%$ (Single-Ended)*2		
	When using the J1790A: $\pm 35 \text{ mV} \pm 12 \% \text{ (Single-Ended)} \ast_{3,} \ast_{4,} \ast_{5}$		
PAM4 Eye Amplitude			
PAM4 (0/3 Level) Setting Range	PAM4(0/3 Level):70 to 800 mVp-p, 1 mV step (Single-Ended)*6		
PAM4 (0/3 Level)	When using the J1789A: $\pm 35 \text{ mV} \pm 12 \%$ of Amplitude ^{*2, *7}		
Accuracy	When using the J1790A: $\pm 35 \text{ mV} \pm 12 \%$ of Amplitude ^{*3, *4, *5, *7}		
PAM4 (0/1, 1/2, 2/3	Provided, 20 to 50 %, 1 mV Step (Eye amplitude conversion)		
Level) Independently variable	(PAM4 Amplitude 0/3 level is assumed to be 100 %.)		
PAM4 (0/1, 1/2, 2/3	PAM4(0/1 Level):23 to 266 mVp-p, 1 mV step (Single-Ended)		
Level) Setting Range	PAM4(1/2 Level):24 to 268 mVp-p, 1 mV step (Single-Ended)		
	PAM4(2/3 Level):23 to 266 mVp-p, 1 mV step (Single-Ended)		
PAM4 (0/1, 1/2, 2/3	When using the J1789A: ± 35 mV ± 12 % of Amplitude*8		
Level) Accuracy	When using the J1790A: $\pm 35 \text{ mV} \pm 12 \%$ of Amplitude* ^{9, *10, *11}		
Offset			
Setting Range	-2.0-Eye Amplitude/2 to +3.3-Eye Amplitude/2 Vth, 1 mV step (Single-Ended)		
Accuracy	$\pm 65 \text{ mV} \pm 10 \%$ of offset (Vth) \pm (Eye Amplitude Accuracy / 2)		
	(Except when Emphasis is turned On with the MU196020A-x11 installed.)		
	(For PAM4, when setting each of PAM4 Amplitude (3/2, 2/1 and 1/0) equally to 33 %.)		
Cross Point	Typ. 50 % (fixed)		
Tr/Tf	When using the J1789A:		
	Typ. 9 ps (20-80 %)*12		
	Typ. 8.5 ps (20-80 %)* ₁₃		
	When using the J1790A:		
	Typ. 9.5 ps (20-80 %)*12		
	Typ. 8.8 ps (20-80 %)*13		

 Table 1.3.1-11
 Data Output

*1: Unless otherwise specified, these are specified with the conditions of PRBS2³¹-1, Mark ratio 1/2, and Cross Point 50 %.

The values shall be observed by using an optional accessory, J1789A or J1790A, and a 70-GHz bandwidth sampling oscilloscope.

*2: Setting Range ≤ 700 mVp-p

*3: Setting Range ≤ 700 mVp-p
(≤ 32.1 Gbit/s, when the Options 001, 002, y12, 003, y13 and y23 are installed)

1

- *4: Setting Range ≤ 600 mVp-p
 (≤ 58.2 Gbit/s, when the Options 002, y12, 003, y13 and y23 are installed
- *5: Setting Range ≤ 550 mVp-p
 (≤ 64.2 Gbit/s, when the Options 003, y13 and y23 are installed)
- *6: When PAM4 output signal is directly input to the ED, the lower limit for the error-free amplitude depends on the performance of the ED used.

When using MP1862A as ED, the lower limit for the error-free amplitude (reference data) is as follows:

125 mV (0/3 Level, \leq 32.1 Gbaud, when the Option 001 is installed) 250 mV (0/3 Level, \leq 58.2 Gbaud, when the Options 002, y12, 003, y13 and y23 are installed)

Pattern: PRBS15, at a constant temperature between 20 and 30 $^{\circ}\mathrm{C}$

- *7: Single-Ended, PAM4 0/3 Level, and when setting each of PAM4 Amplitude (3/2, 2/1 and 1/0) equally to 33 %
- *8: Setting Range ≤ 234 mVp-p, Single-Ended, at each amplitude level (Upper, Middle, Lower)
- *9: Setting Range ≤ 234 mVp-p, Single-Ended, at each amplitude level (Upper, Middle, Lower)
 (≤ 32.1 Gbit/s, when the Options 001, 002, y12, 003, y13 and y23 are installed)
- *10: Setting Range ≤ 200 mVp-p, Single-Ended, at each amplitude level (Upper, Middle, Lower)
 (≤ 58.2 Gbit/s, when the Options 002, y12, 003, y13 and y23 are installed
- *11: Setting Range ≤ 184 mVp-p, Single-Ended, at each amplitude level (Upper, Middle, Lower), when using the J1790A coaxial cable (0.8m) (≤ 64.2 Gbit/s, when the Options 003, y13 and y23 are installed)
- *12: NRZ, 32.1 Gbit/s, Eye Amplitude 0.5 Vp-p (Single-Ended), only when Coding is NRZ and Emphasis is Off.
- *13: NRZ, 58.2 Gbit/s (when the Options 002 and y12 are installed), 64.2 Gbit/s (when the Options 003, y13 and y23 are installed), Eye Amplitude 0.5 Vp-p (Single-Ended), only when Coding is NRZ and Emphasis is Off.

Item	Specifications*1	
Half Period Jitter		
Setting Range	-20.0 to +20.0, 0.1 step	
Accuracy	Typ. $\pm 0.04 \text{ UI}^{*_{14}}$	
Jitter		
Measurement	NRZ,	
conditions	Bit rate 32.1 Gbit/s (When the Option 001 is installed),	
	58.2 Gbit/s (When the Options 002 and y12 are installed),	
	64.2 Gbit/s (When the Options 003, y13 and y23 are installed)	
	Eye Amplitude 0.5 Vp-p (Single-Ended)	
	At a constant temperature between 20 and 30 °C, measure with a 70-	
	200 fs (RMS).	
Peak-to-Peak Jitter	Typ. 6 ps p-p (Count of measured jitters: 30)	
Jitter RMS	Typ. 600 fs rms (Count of measured jitters: 30)	
Intrinsic RJ (RMS)	Typ. 170 fs (Repeating pattern of $1,0$)* ₁₅	
Waveform Distortion (0-	Typ. ±110 mV* ₁₆	
peak)		
PAM4 Level Separation	$0.95 \text{ (min.)}^{*17}$	
Mismatch Ratio (R _{LM})		
PAM4 Signal to noise and	$33 \text{ dB} (\text{min.})^{*18, *19}$	
distortion ratio (SNDR)		
Electrical TDECQ	0.9 dB*20	
Output ON/OFF	ON/OFF switching available	
Data / XData Skew	$\pm 1 \text{ ps}$	
	Cable error not included.	
Termination	AC, DC switching	
	For DC: GND, -2V, +1.3V, +3.3V, Open (LVDS), 50 Ω	
Connector	V connector (f.)	

	Table 1.3.1-11	Data Output	(Cont'd)
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*14: 2.4, 8, 16, 26.562 5, 32.1 Gbit/s (When the Option 001 is installed), 2.4, 8, 16, 26.562 5, 32.1, 40, 53.125, 58.2 Gbit/s (When the Options 002 and y12 are installed)
2.4, 8, 16, 26.562 5, 32.1, 40, 53.125, 58.2, 64.2 Gbit/s (When the Options 003, y13 and y23 are installed), Eye Amplitude 0.5 Vp-p (Single-Ended)
*15: NRZ, Bit rate 58.2 Gbit/s (When the Options 002 and y12 are installed),

 $64.2~{\rm Gbit/s}$ (When the Options 003, y13 and y23 are installed)

*16: NRZ, Bit rate 32.1 Gbit/s (When the Option 001 is installed), 58.2 Gbit/s (When the Options 002 and y12 are installed), 64.2 Gbit/s (When the Options 003, y13 and y23 are installed) Eye Amplitude 0.5 Vp-p (Single-Ended)

*17: PAM4, 26.5625 Gbaud (When the Option 001 is installed), 53.125 Gbaud (When the Options 002, y12, 003, y13 and y23 are

1

installed),

 $1.0~\rm Vp\mathchar`-p$ (Differential), refer to the IEEE P802.3bs for equation to calculate.

*18: PAM4, 26.5625 Gbaud (When the Option 001 is installed),53.125 Gbaud (When the Options 002, y12, 003, y13 and y23 are installed),

 $1.0~\mathrm{Vp}\mbox{-}\mathrm{p}$ (Differential), refer to the IEEE P802.3cd for equation to calculate.

*19: 60-GHz bandwidth sampling oscilloscope

*20: 26.5625 Gbaud (When the Option 001 is installed),

53.125 Gbaud (When the Options 002, y12, 003, y13 and y23 are installed),

Using an equalizer, Single, Pattern: SSPRQ

Table 1.3.1-11	Data Output (Cont'd)
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Item	Specifications*1
Offset Reference	Vth
Level Guard	Amplitude, Voh and Vol can be set.
External ATT Factor	-40 to 0 dB, 0.1 dB step
	When the fixed attenuator is connected, the amplitude and offset of the
	signal output via the fixed attenuator are displayed.
Emphasis	When the Option x11 is installed
Emphasis Tap	4 (1post-cursor, 2pre-cursor)
	4 Tap parameter values for all eyes (Upper, Middle and Lower) become
	identical. This means that 4 Tap parameters for Upper, Middle and
General Cetting Denser	Lower Eyes cannot be controlled independently.
Stop	-20 to $+20$ dB, 0.01 dB step (Dest-Current 20leg, Ve/Vb, DreeCurrent 20leg, Ve/Vb)
Breb	(Fost-Cursor: $2010g_{10}$ v a) v b, Fre-Cursor: $2010g_{10}$ v c) v b)
	Provided that the maximum amplitude is restricted by the setting range of emphasis peak voltage.
Accuracy	Typ. ±1 dB
	(16 Gbaud, Amplitude 0.5 Vp-p (Single-Ended),
	De-Emphasis, Pre-Cursor1 = 6 dB, Post Cursor1 = 3.5 dB)
Setting Range of	70 to 800 mVp-p (Single-Ended)
Voltage	
Emphasis ON/OFF	ON/OFF switching

ltem	Specifications*1		
Channel Emulator*21, *22	Normal: Outputs the PPG Data signal whose waveform emulates the connected transmission line with the loaded S parameter.		
	Inverse: Outputs the PPG Data signal whose inverse characteristics emulate the transmission line with the loaded S parameter.		
Response	Normal, Inverse		
S-Parameter file	S2P file (Extension: "*.s2p"), S4P file (Extension: "*.s4p")		
	Supports output files from the MS4640B Series Vector Network Analyzer.		
Channel Emulator ON/OFF	ON/OFF switching		
Gain Adjust	Adjusts the loss to emulate and loss of the loaded S parameter at the specified frequency, when Response is Normal.		
	0GHz, 1GHz, Nyquist Frequency switching		
Adjustable ISI*21	Sets the loss of the channel which generates ISI and outputs the PPG		
	data signal whose waveform emulates the setting.		
Loss Channel	This is available for MU196020A in combination with the following.		
	Not Specified an external loss channel board		
	J1800A×1 Short Channel one J1800A (optional accessory)		
	J1800A×2 Middle Channel: two J1800As (optional accessory)		
	J1758A:		
	MU195050A Noise: an MU195050A Noise Module		
Frequency	Insertion Loss can be set at Nyquist or 1/2 Nyquist Frequency.		
Insertion Loss	Displays the absolute loss that is sum of the loss selected for Loss		
	Channel and the setting value of Tuning Insertion Loss at Nyquist Frequency and 1/2 Nyquist Frequency.		
Tuning Insertion Loss	The relative loss from the loss value of Loss Channel can be set.		
	-8.00 to 8.00 dB, 0.01 dB step, Nyquist Frequency		
	-8.00 to 8.00 dB, 0.01 dB step, 1/2 Nyquist Frequency		
Insertion Loss Accuracy	±1.0 dB Nominal @Nyquist Frequency 6 dB, Repeating pattern of "1,0" *23, *25, *26		
	±1.5 dB Nominal @Nyquist Frequency 6 dB, Repeating pattern of "1,0" *24, *25, *26		
	±1.0 dB Nominal @1/2Nyquist Frequency 3 dB, Repeating pattern of "1,1,0,0" *23, *25, *26		
	±1.5 dB Nominal @1/2Nyquist Frequency 3 dB, Repeating pattern of "1,1,0,0" *24, *25, *26		
Adjustable ISI ON/OFF	ON/OFF switching		

 Table 1.3.1-11
 Data Output (Cont'd)

*21: When the Option x40 is installed.

*22: It is assumed to use for the purpose of compensating the loss of the transmission line.

The following graph shows typical limits for adjustable insertion loss. However, it does not mean that all the responses emulated from the S-Parameter file are compensated as the graph shows.



- *23: Baud Rate 26.6 Gbaud (when Option 001, 002, y12, 003, y13, and y23 installed)
- *24: Baud Rate 53.1 Gbaud (when Option 002, y12, Option 003, y13, and y23 installed)
- *25: Eye Amplitude 0.5 Vp-p, at each spectrum, at a constant temperature between 20 and 30 °C
- *26: The frequency characteristics of Insertion Loss Accuracy when setting 6 dB@Nyquist Frequency and 3 dB@1/2 Nyquist Frequency are shown below.



1

Item	Specifications*
Frequency	
Full Rate	Operation Baud Rate = Clock Output Frequency
	2.4 to 32.1 GHz (Option 001)
Half Rate	Operation Baud Rate = (Clock Output Frequency) $\times 2$
	1.2 to 16.05 GHz (Option 001)
	1.2 to 29.1 GHz (When the Options 002 and y12 are installed)
	1.2 to 32.1 GHz (When the Options 003, y13 and y23 are installed)
Quarter Rate	Operation Baud Rate = (Clock Output Frequency) $\times 4$
	0.6 to 8.025 GHz (Option 001)
	0.6 to 14.55 GHz (When the Options 002 and y12 are installed)
	0.6 to 16.05 GHz (When the Options 003, y13 and y23 are installed)
Number of Outputs	1
Amplitude	Min. 0.3 Vp-p, Max. 1.0 Vp-p
	(Output Frequency $\leq 16.05 \text{ GHz}$)
	Min. 0.4 Vp-p, Max. 1.0 Vp-p
	(Output Frequency > 16.05 GHz)
Output control	ON, OFF switching
Termination	50 Ω, AC Coupling
Connector	K connector (f.)

Table 1.3.1-12 Clock Output

*: These values are monitored using an optional accessory (J1439A) at a sampling oscilloscope bandwidth of 70 GHz.

ltem	Specifications
Phase variable range	-1000 to +1000 mUI, 2 mUI step
Accuracy	±50 mUIp-p*2, *3, *4
	±100 mUIp ⁻ p* ^{2, *3, *5}
mUI – ps switching	Available (internally converted into ps)
Calibration	Available (when jitter modulation is off)
Calibration indicator	This is displayed when one of the following conditions is met:
	• $1/1$ Clock frequency change by ± 250 kHz.
	• Ambient temperature change by $\pm 5^{\circ}$ C.

Table 1.3.1-13 Data Delay*1

- *1: When the Option x30 is installed.
- *2: Measured with a sampling oscilloscope with residual jitter of less than 200 fs (RMS), at a constant amplitude setting.
- *3: Typical value
- *4: Baud rate ≤ 32.1 Gbaud
- *5: Baud rate > 32.1 Gbaud

Item			Sp	pecifications	
Jitter tolerance	For N	RZ output,			
	Bit ra	te: 32.1 Gbit/s	(Option	001)	
		58.2 Gbit/s	(When t	the Options 00	2 and y12 are installed)
		64.2 Gbit/s	(When t	the Options 00)3, y13 and y23 are
	D 44	installed)			
	Patter	$rn \in PRBS2^{31}-1$	C		l-II- and deviation of
	5300 j	opm can be appl	ed simu	ltaneously wit	th RJ with amplitude of 0.3
	These	specifications a	re define	ed assuming th	ne following conditions:
	Loopb	ack connection t	o MU19	6040A (32.1 G	bit/s) or MP1862A +
	MU18	33040B (58.2 Gbi	t/s, 64.2	Gbit/s), at a c	onstant temperature
	betwe	en 20 and 30 °C.	.1	0 - 111	
	When	RJ + BUJ is big	ger than	0.5 Ulp-p or	SJI + Built-in SJ2 + RJ +
	displa	ved on the MU1	81500B	ru value + 0.5 screen	Olp-p, Overload Is
	For de	etails on the may	imum m	odulation iitt	er that depends on the bit
	rate, 1	refer to "Table 1.	3.1-2 Jit	ter Setting Ra	nge".
	32.1 0	dbit/s			
		10000			Max. modulation amplitude Specification
	<u>آ</u>	1000			
	litude	100			
	r Amp	10			
	Jitte	1			
		0.1			
		10 100	1k	10k 100k	1M 10M 100M 1000M
			Mod	lulation Frequer	ncy [Hz]
	l fre	Modulation equency [Hz]	Max. I amplit	modulation tude [Ulp-p]	Specification [Ulp-p]
		10	-	2 000	2 000
		$7\ 500$		$2\ 000$	2 000
		100 000		2 000	150
		1 000 000		200	15
		10 000 000		16	1
		290 000 000		1	1

Table 1.3.1-14 Jitter Tolerance

Overview



Table 1.3.1-14 Jitter Tolerance (Cont'd)

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Overview

Item	Specifications
Multi-Module Synchronization	 A function to synchronize timing of generating patterns among multiple modules^{*2, *3, *4, *5, *6} Baud Rate ≤ 32.1 Gbaud: Capable of synchronizing bit generation timing with an accuracy of less than 1 UI Baud Rate > 32.1 Gbaud: Capable of synchronizing bit generation timing with an accuracy of less than 5 UI
Inter-Module 2ch Combination	This is available only for NRZ.Generates signals of which the first bit generation timing is synchronized between modules.And, generates signals with the bit-interleaved generation bit patterns between modules.Slot1Data1357Slot2Data2468
Inter-Module CH Synchronization	Generates signals of which the first bit generation timing is synchronized between modules. Slot1 Data 1 2 3 4 Slot2, 3, 4 Data 1 2 3 4

Table 1.3.1-15 Multichannel Operation*¹

- *1: When the Option x30 and x50 are installed.
- *2: The following options must be the same among the modules to be synchronized.

Option 001 Option 002 or y12 Option 003, y13, or y23

- *3: Slot 1 to 2: Inter-Module 2ch Combination (only for NRZ)
- *4: Slot 1 to 4: Inter-Module CH Synchronization
- *5: The modules to be synchronized must be installed successively from Slot 1.
- *6: In the range of ±3 °C from the temperature when performing the Multi Channel Calibration function, the bit generation timing is guaranteed.

Item	Specifications		
Output	Only the items to be changed when Multi-Module Synchronization is set are described.		
Phase setting range	$-64\ 000\ to\ +64\ 000\ mUI^{*7}$		
Phase setting resolution	2 mUI*7		
Pattern			
Data length	When CH Combination is set: 4 to 536,870,912 bits, 2 bits step		
	When CH Synchronization is set: same as Sync OFF		
Unit Sync ^{*8, *9}	ON/OFF switching available		
Number of Units	Synchronous control available between up to two MP1900As. Synchronous control of up to 8 channels is available with two MP1900As each installed with four MU196020As.		
Unit Sync Output*10	To output a timing signal from the Gating Out connector when Unit Sync is touched Provided with an inter-unit synchronization status indicator. The status indicator at Unit Sync turns orange when it requires to be timed to the other		
Unit Sync Input*10	To input a timing signal from the AUX In connector		
Bit phase difference between MP1900As	Within ±1024 UI Timing difference between bit generations that occurs when Unit Sync is touched MP1900A (Primary)		
	Slot 1 $X = X = X = X = X = X = X = X = X = X $		

Table 1.3.1-15 Multichannel Operation*1 (Cont'd)

- *7: Each channel can be set independently.
- *8: Available on MX190000A version 3.02.00 or later.
- *9: Available only when using inter-module synchronization.
- *10: Available only when **Unit Sync** is **ON**.

Т Item Specifications Dimensions 21 mm (H), 234 mm (W), 175 mm (D) Excluding protrusions 2.5 kg max. Mass **Operating Temperature** 15 to 30 °C $MP1900A^{\prime}s$ ambient temperature. MU196020A shall operate when installed. Storage Temperature –20 to 60 °C MU196020A installed to MP1900A shall comply with MIL-T-28800E Class 5.

Table 1.3.1-17	Extended Functions

Item	Specifications		
PCIe	Supports the following PCIe tests when controlled by the MX183000A.		
	• MX190000A V4 09 00 or lator		
	 MX183000A V4.09.00 or later MX183000A V4.09.00 or later 		
Applicable Standards	PCI Express Base Specification Revision 4.0 Version1.0		
rr	PCI Express Base Specification Revision 5.0 Version1.0		
	Bit rate: PCIe1/2/3/4/5		
	Number of lanes: x1		
	Subjects of Testing: Root Complex, End Point		
Required Options	Option x11		
Required Software	MX183000A-PL021:		
	Can support negotiation with the DUT and can put the DUT into Loopback state according to the LTSSM of PCIe1 to PCIe4. State transition of LTSSM can be analyzed as a log.(One MU196020A and one MU195040A are required.)		
	MX183000A-PL025:		
	Can extend the functionality of the PL021 option to PCIe5.		
	When the MX183000A-PL001 is installed in addition to the MX183000A-PL021 and MX183000A-PL025, the MX183000A can control the MU196020A, MU181500B, and MU195040A and support Jitter Tolerance Test.		

Overview

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1.3.2 Specifications for MU196040A

Table 1.3.2-1 Operating Baud Rate

Item	Specifications
Operating Baud Rate	When the Option 001 is installed.
	PAM4 input: 2.4 to 32.1 Gbaud
	NRZ input: 2.4 to 32.1 Gbit/s

Table 1.3.2-2 System Clock

ltem	Specifications
System Clock	External, Recovered Clock (When the Option 022 is installed)
	External: Clock input from the Ext Clock Input connector
	Recovered Clock: Clock recovered from the data input from the Data
	Input connector

1

Overview

Item	Specifications		
Number of inputs	2 (Data, XData) (Differential)		
Input Condition	Single-Ended, Differential 50 Ohm, Differential 100 Ohm		
	When set to Differential 50 Ohm or Differential 100 Ohm:		
	Independent, Tracking, Alternate ^{*1}		
	When set to Alternate:		
	Data-XData, XData-Data*2		
	When set to Single-Ended:		
	Data, XData*3		
Signal Type	NRZ, PAM4		
LSB/MSB Diagnostics	When set to PAM4, the PAM4 mode can be switched between as follows:		
	Diagnostics Mode OFF:		
	Treats signals as symbols by receiving LSB and MSB while		
	synchronizing them with each other.		
	Diagnostics Mode ON:		
	Asynchronously receives LSB and MSB.		
Amplitude	NRZ: The range in which the Auto Adjust function operates.		
	PAM4: The range in which the Auto Search PAM4 Fine function		
	operates.		
	NRZ: 0.05 to 1.0 Vp-p*4		
	PAM4: 0.3 to 1.0 Vp-p* ⁵		
Threshold	NRZ, PAM4 Middle Eye Threshold: -3.5 to +3.3 V, 1 mV step ^{*2, *6}		
	PAM4 Upper Eye Threshold: $-3.9 \text{ to } +3.7 \text{ V}, 1 \text{ mV step}^{*7}$		
	PAM4 Lower Eye Threshold: -3.9 to +3.7 V, 1 mV step*7		

Table 1.3.2-3 Data Input

*1: Tracking is available only for NRZ.

- *2: The absolute value of the difference between Data and XData Threshold values shall be 1.5 V or less.
- *3: PAM4 Upper Eye and Lower Eye can be set by relative values to Middle Eye in the range of -0.4 V to +0.4 V.
- *4: Single-Ended, Differential
- *5: 0/3 Level, PRBS31, Single-Ended, Differential, when connecting directly to the MU196020A.
- *6: Data and XData can be set independently.
- *7: Data and XData cannot be set independently, and can be set in the range of ±0.4 V from Middle Eye Threshold.

Item	Specifications	
Sensitivity	Single-Ended , Mark Ratio1/2, wh MU196020A with J1789A.	en connecting directly to the
	When the Option-001 is installed,	34VKF50 shall be included.
	At a constant temperature betwee	en 20 and 30 °C
Eye Amplitude	NRZ, PRBS31	
	Typ. 32 mVp-p, ≤ 50 mVp-p*8	(26.5625 Gbit/s, 32.1 Gbit/s)
Eye Height	NRZ, PRBS31	
	Typ. 23 mV*8	(26.5625 Gbit/s, 32.1 Gbit/s)
	PAM4 0/1 1/2 2/3 Level, PRBS31,	Eye Height where BER is 1E–06,
	when using External Clock	
	Typ. 23 mV, $\leq 50 \text{ mV*}^8$	(26.5625 Gbaud, 32.1 Gbaud)
Phase Margin	When connecting directly to the MU196020A with J1789A.	
	When the Option-001 is installed,	34VKF50 shall be included.
	At a constant temperature betwee	en 20 and 30 °C, when using External
	Clock	
	NRZ, PRBS31, Differential, Mark	Ratio 1/2, when inputting 1.0 Vp-p
	Typ. 25.8 ps*8	(26.5625 Gbit/s)
	Typ. 18.0 ps^{*8}	(32.1 Gbit/s)
	PAM4 0/3 Level, Eye Width where BER is 1E–06, PRBS31, Single- Ended, Mark Ratio1/2, when inputting 0.5 Vp-p,	
	Emphasis ON (Best values in the	range of $1Pre \le 5 \text{ dB}$ and $1Post \le 5 \text{ dB}$)
	Typ. 5.3 ps*8	(26.5625 Gbaud)
	Typ. 4.5 ps*8	(32.1 Gbaud)

Table 1.3.2-3	Data Input (Cont'd)
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*8: When the Option 001 is installed.

Item	Specifications	
Stressed Margin*9		
Stressed Eye Height	PAM4 0/1 1/2 2/3 Level, QPRBS13-CEI, Eye Height where BER is 1E– 06, when using External Clock $\geq 32 \text{ mV}^{*10}$	
Stressed Eye Width	PAM4 0/1 1/2 2/3 Level, QPRBS13-CEI, Eye Width where BER is 1E–06, when using External Clock $\geq 7.15 \text{ ps}^{*10}$	
Termination	50Ω , GND, Variable	
Termination Voltage	When set to Variable: -2.5 to $+3.5$ V, 10 mV step	
Connector	K connector (f.) (When the Option 001 is installed)	

Table 1.3.2-3 Data Input (Cont'd)

*9: Differential, Mark Ratio1/2, when connecting J1758A and MU196020A by using J1789A, 34VKF50 and J1728A.



At a constant temperature between 20 and 30 $^{\circ}$ C, measure with a 70-GHz bandwidth sampling oscilloscope with residual jitter of less than 200 fs (RMS).

Adjust De-Emphasis (2 Pre Cursors and 1 Post Cursor) of MU196020A so that the product of Eye Height (1E–06) and Eye Width (1E–06) can be maximized in the differential waveform.

Calculate the 4th-order Bessel Filter (Cutoff Frequency 50 GHz) + CTLE (+1 dB Peaking at 14 GHz) and calibrate it to a PAM4 waveform with Eye Amplitude of 0.88 Vp-p (Diff) or less and Eye Linearity RLM 0.85 or more.

*10:28 Gbaud, when the Option 001 is installed, BER 1E–12

Table 1.3.2-4	Clock Input

Item	Specifications
External Clock Input	Operation Baud Rate = Clock Input Frequency (When the Option 001 is installed)
Number of inputs	1 (Single-Ended)
Frequency range	When the Option 001 is installed: 2.4 to 32.1 GHz
Amplitude	0.3 to 1.0 Vp·p (–6.5 to +4.0 dBm) (Input Frequency \leq 16.05 GHz)
	0.4 to 1.0 Vp·p (-3.9 to $+4.0$ dBm) (Input Frequency > 16.05 GHz)
Termination	50 Ω, AC Coupling
Connector	K connector (f.)

Table 1.3.2-5 Aux Input

Item	Specifications	
Number of inputs	1 (Single-Ended)	
Variation	External Mask, Burst	
Minimum pulse width	1/256 of Data rate	
Input level	• 0/-1 V (H: -0.25 to 0.05 V, L: -1.1 to -0.8 V)	
	• 0/-0.5 V (H: -0.05 to 0.05 V, L: -0.55 to -0.45 V)	
	• Vth 0 V (Input amplitude 0.5 to 1.0 Vp-p)	
	Select one of the above.	
Termination	$50 \Omega, \text{GND}$	
Connector	SMA connector (f.)	

Table 1.3.2-6 Aux Output

Item	Specifications
Number of outputs	2 (Differential)
Variation	1/n Clock (n = 8, 12, 16, 201020, 1024), Pattern Sync, Sync Gain, Error Output
Pattern Sync PRBS, PRGM	Position: 1 to {(Least common multiple of Pattern Length' and 128) – 135}, 8 step (When the Option 001 is installed) Pattern Length' shall be the value obtained by multiplying Pattern Length setting until it becomes 1024 or more if it is 1023 or less.
Output level	0/-0.6 V (H: -0.25 to 0.05V, L: -0.80 to -0.45 V)
Termination	$50 \Omega, \text{GND}$
Connector	SMA connector (f.)

Item	Specifications		
PRBS			
Pattern length	$2^{n}-1$ (n = 7, 9, 10, 11, 13, 15, 20, 23, 31)		
Mark ratio	1/2, 1/2inv		
PRBS generator	n=7: 1 + X ⁶ + X ⁷		
polynomial	n=9: 1 + X ⁵ + X ⁹		
	$n=10: 1 + X^7 + X^{10}$		
	n=11: $1 + X^9 + X^{11}$		
	n=13: $1 + X + X^2 + X^{12} + X^{13}$		
	n=15: 1 + X ¹⁴ + X ¹⁵		
	n=20: 1 + X ³ + X ²⁰		
	n=23: $1 + X^{18} + X^{23}$		
	n=31: 1 + X^{28} + X^{31}		
PRBS Inversion	This is available in PAM4 mode only.		
	Logically inverted PRBS can be set independently for MSB and LSB.		
Zero-Substitution	This is available in NRZ mode only.		
Additional Bit	0 bit, 1 bit		
Pattern length	2^{n} or $2^{n}-1$ (n = 7, 9, 10, 11, 15, 20, 23)		
Start position	Substitutes the bit coming after the maximum "0" successive bits.		
Zero-Length	1 to (Pattern Length – 1) bits		
	If the bit coming after Zero-substitution is "0," then it is replaced with		
	"1."		
Data			
Data length	NRZ: 2 to 268 435 456 bits, 1 bit step		
	PAM4: 2 to 268 435 456 symbols, 1 symbol step		
Coding	NRZ, PAM4		
NRZ	Normal, Invert		
PAM4 Gray Coding	ON, OFF		
PAM4 Precoding	ON, OFF		
$(1/(1 + D) \mod 4)*$			
PAM4 Standard Pattern	Standard-compliant PAM4-mode patterns		
CEI	QPRBS13-CEI, QPRBS31-CEI		
IEEE	IEEE802.3bs/cd: PRBS13Q, PRBS31Q, SSPRQ, Square Wave		
	IEEE802.3bj: QPRBS13, JP03A, JP03B, Transmitter Linearity		
InfiniBand	PRBS13Q (InfiniBand), PRBS23Q, PRBS31Q (InfiniBand)		
Fibre Channel	PRBS31Q (Fibre Channel)		
NRZ Standard Pattern	Standard-compliant NRZ-mode pattern		
CEI	SSPR		

Table 1.3.2-7 Pattern Detection

*: (1/(1+D) mod 4) is a generator polynomial defined in the IEEE802.3.

1

Overview

Item		Specifications		
Sequence	Repeat, Burst			
Repeat	Continuous Pattern	1		
Burst	This is available on	ly when Coding is NRZ.		
Source	Internal, External-	Enable (Aux Input), External-Trigger (Aux Input)		
Delay	Internal:	0 to 2 147 483 640 bits, 8 bits step		
	External-Trigger, H	External-Trigger, External-Enable:		
		0 to 2 147 483 520 bits, 8 bits step		
	Adjust Method:	Auto, Manual		
Enable Period	Internal:	12 800 to 2 147 482 624 bits, 256 bits step		
	External-Trigger:	12 800 to 2 147 483 136 bits, 256 bits step		
Burst Cycle	25 600 to 2 147 483	25 600 to 2 147 483 648 bits, 1024 bits step		

Table 1.3.2-8 Pattern Sequence

Item		Specifications	
Counter	Error Rate (ER) Total:	0.000 1E–18 to 1.000 0E00	
	Error Count (EC) Total:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17	
	Error Interval:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17	
	%Error Free Interval:	0.000 0 to 100.000 0	
	Error Rate (ER) Insertion	n (INS):	
		0.000 1E–18 to 1.000 0E00	
	Error Count (EC) Inserti	on (INS):	
		0 to 9 999 999, 1.000 0E07 to 9.999 9E17	
	Error Rate (ER) Omissio	n (OMI): $0.000 1E_{10+1} 1.000 0E00$	
		0.000 IE-18 to 1.000 0E00	
	Error Count (EC) Omissi	$\begin{array}{c} \text{On } (\text{OWI}) \\ \text{O to } 0.000 \text{ OOO} 1.000 \text{ OEO7 to } 0.000 \text{ OE17} \\ \end{array}$	
	Freesware	0.0099999999, 1.0000E07099999E17 2.400.000 to 52.200.000 MHz	
	Frequency.	2 400.000 to 58 200.000 MHZ	
	r requency measurement	$+1 \text{ nnm} +1 \text{ kHz}^*$	
	Clock Count:	0 to 9 999 999 1 000 0E07 to 9 999 9E17	
	Sync Loss Interval:	0 to 9 999 999 1 000 0E07 to 9 999 9E17	
	Clock Loss Interval:	0 to 9 999 999 1 000 0E07 to 9 999 9E17	
	Expressions enclosed in a	parentheses are abbreviations	
	The following are evailed	The following are queilable only for DAM4 (Diagnostics Mode ON)	
	measurement	The following are available only for PAM4 (Diagnostics Mode ON)	
	MSB Error Bate (EB) To	tal: 0.000.1E_18 to 1.000.0E00	
	MSB Error Count (EC) T	tar = 0.000 II - 10 to 1.000 OHO	
	MSB Error Interval:	0 to 9 999 999 1 000 0E07 to 9 999 9E17	
	MSB %Error Free Interv	al: $0.0000 \text{ to } 10000000$	
	MSB Error Bate (ER) Inc	artion (INS):	
	MOD EITOI Rate (EIt) III	0.000 1E - 18 to 1.000 0E00	
	MSB Error Count (EC) I	nsertion (INS):	
		0 to 9 999 999. 1.000 0E07 to 9.999 9E17	
	MSB Error Rate (ER) On	nission (OMI):	
		0.000 1E–18 to 1.000 0E00	
	MSB Error Count (EC) C	Omission (OMI):	
		0 to 9 999 999, 1.000 0E07 to 9.999 9E17	
	LSB Error Rate (ER) Tot	al: 0.000 1E–18 to 1.000 0E00	
	LSB Error Count (EC) To	otal: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17	
	LSB Error Interval:	0 to 9 999 999, $1.000 0E07$ to $9.999 9E17$	
	LSB %Error Free Interva	al: 0.000 0 to 100.000 0	
	LSB Error Rate (ER) Ins	ertion (INS):	
		0.000 1E–18 to 1.000 0E00	
	LSB Error Count (EC) In	sertion (INS):	
		0 to 9 999 999, 1.000 0E07 to 9.999 9E17	
	LSB Error Rate (ER) Om	ission (OMI):	
		0.000 1E–18 to 1.000 0E00	
	LSB Error Count (EC) O	mission (OMI):	
		0 to 9 999 999, 1.000 0E07 to 9.999 9E17	
	Expressions enclosed in j	parentheses are abbreviations.	

Table 1.3.2-9 Measurement

*: With a gating system and with MP1900A's reference clock (10 MHz) calibrated

ltem		Specifications
Counter (Cont'd)	The following are available	when the Option x41 SER Measurement is
	installed.	
	The following are available	only for PAM4 (Diagnostics Mode OFF)
	measurement.	
		3
		2
		(
		<u> </u>
		0
	Sumbol Error Rate (SFR)	$0.000.1E_{18,to} 1.000.0E00$
	Symbol Error Count (SEC).	0.000 IE - 10 to 1.000 OE 00 0 to 0.000 QC 1 000 OE 07 to 0.000 QE 17
	Symbol Error Interval	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Symbol Error Free Interval	0 000 0 to 100 000 0
		0.000 0 10 100.000 0
	Level $0 \rightarrow 3$ EC:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Level $0 \rightarrow 2$ EC:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Level $0 \rightarrow 1$ EC:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Level $0 \rightarrow 3$ ER:	0.000 1E–18 to 1.000 0E00
	Level $0 \rightarrow 2$ ER:	0.000 1E–18 to 1.000 0E00
	Level $0 \rightarrow 1 \text{ ER}$:	0.000 1E–18 to 1.000 0E00
	Level 0 EC Total:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Level 0 ER Total:	0.000 1E–18 to 1.000 0E00
	Level $1 \rightarrow 3$ EC:	0 to 9 999 999 1 000 0E07 to 9 999 9E17
	Level $1 \rightarrow 2$ EC:	0 to 9 999 999. 1.000 0E07 to 9.999 9E17
	Level $1 \rightarrow 0$ EC:	0 to 9 999 999. 1.000 0E07 to 9.999 9E17
	Level $1 \rightarrow 3$ ER:	0.000 1E–18 to 1.000 0E00
	Level $1 \rightarrow 2$ ER:	0.000 1E–18 to 1.000 0E00
	Level $1 \rightarrow 0$ ER:	0.000 1E–18 to 1.000 0E00
	Level 1 EC Total:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Level 1 ER Total:	0.000 1E–18 to 1.000 0E00

Table 1.3.2-9 Measurement (Cont'd)

Specifications *1.3*

Item		Specifications	ľ
Counter (Cont'd)	Level 2 \rightarrow 3 EC:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17	
	Level $2 \rightarrow 1$ EC:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17	
	Level $2 \rightarrow 0$ EC:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17	9
	Level 2 \rightarrow 3 ER:	0.000 1E–18 to 1.000 0E00	/er
	Level 2 \rightarrow 1 ER:	0.000 1E–18 to 1.000 0E00	₹.
	Level 2 \rightarrow 0 ER:	0.000 1E–18 to 1.000 0E00	ew
	Level 2 EC Total:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17	
	Level 2 ER Total:	0.0001E–18 to 1.000 0E00	
	Level $3 \rightarrow 2$ EC:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17	
	Level $3 \rightarrow 1$ EC:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17	
	Level $3 \rightarrow 0$ EC:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17	
	Level 3 \rightarrow 2 ER:	0.000 1E–18 to 1.000 0E00	
	Level $3 \rightarrow 1 \text{ ER}$:	0.000 1E–18 to 1.000 0E00	
	Level $3 \rightarrow 0$ ER:	0.000 1E–18 to 1.000 0E00	
	Level 3 EC Total:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17	
	Level 3 ER Total:	0.000 1E–18 to 1.000 0E00	
	Expressions enclosed in p	arentheses are abbreviations.	
Gating	Time, Clock Count, Error	Count	
Gating Unit	Time	1 second to 99 days 23 hours 59 minute 59	
		seconds	
	Clock Count:	>E+4 to $>E+16$	
	Error Count:	>E+4 to $>E+16$	
Cycle	Single, Repeat, Untimed		
Current	On, Off can be set.		
	Calculation:	Progressive, Immediate	
	Interval:	100 ms, 200 ms	
Auto Sync	On, Off can be set.		
	Synchronization threshold:		
		INT, $E-2$ to $E-8$	
Sync Control	PRBS:	Automatic Synchronization	
	Data:	Frame On	
Frame Length	NRZ:	4 to 64 bits, 4 bits step	
	PAM4:	4 to 64 symbols, 4 symbol step	
Frame Mask	Available		
Frame Position	NRZ:	1 to (Pattern Length – Frame Length +1)	
	PAM4:	1 to (Pattern Length – Frame Length +1) symbols, 1 symbol step	
Error/Alarm Conditions		· · · ·	
Error Detection	NRZ:	Insertion/Omission,	
		Transition/Non Transition	
	PAM4:	Not available	
EI/EFI Interval	1 ms, 10 ms, 100 ms, 1 s		

Table 1.3.2-9 Measurement (Cont'd)

Item	Specifications	
Block Window	Excludes the specified data pattern from meas	urement.
Setting resolution	Pattern length (bits)	Step (bits)
	2 to 2 097 152	1
	$2\ 097\ 153$ to $4\ 194\ 304$	2
	$4\ 194\ 305\ { m to}\ 8\ 388\ 608$	4
	8 388 609 to 16 777 216	8
	$16\ 777\ 217\ { m to}\ 33\ 554\ 432$	16
	$33\ 554\ 433$ to $67\ 108\ 864$	32
	$67\ 108\ 865$ to $134\ 217\ 728$	64
	$134\ 217\ 729$ to $268\ 435\ 456$	128
Bit Window	Excludes any channels among internal 32 char (Available only in NRZ mode.)	nnels from measurement.
External Mask	H: Measurement	
	L: Mask	

Table 1.3.2-10 Error Analysis

Table 1.3.2-11 Auto Measurement

Item	Specifications
Auto Adjust	NRZ: Vth direction only (Phase direction not supported.)*1 PAM4: MSB Vth direction only (Phase direction not supported.)*1, *2
Auto Search	NRZ: Available ^{*1} PAM4 (LSB/MSB Diagnostics OFF/ON): Available ^{*1, *2}

*1: PRBS Pattern, Mark Ratio 1/2

*2: Each of amplitudes shall be equal.

Table 1.3.2-12 Vallable Clock Delay	Table 1.3.2-12	Variable Clock Delay
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ltem	Specifications
Phase variable range	-1000 to +1000 mUI, 2 mUI step
Accuracy	±50 mUIp-p*1, *2
mUI – ps switching	Available (internally converted into ps)
Calibration	Available (when jitter modulation is off)
Calibration indicator	This indicator is on when Calibration is required due to:
	• Change in 1/1Clock frequency by ±250 kHz.
	• Change in the ambient temperature by $\pm 5^{\circ}$ C.

*1: Measure using an oscilloscope with residual jitter of less than 200 fs (RMS).

*2: Typical value
ltem					Spe	ecificati	ions			
Jitter tolerance	For Bit Pat Wir ppr The Loo bet Wh the MU	For NRZ output Bit rate: 32.1 Gbit/s Pattern: PRBS2 ³¹ -1 With MU181500B, SSC with frequency of 33 kHz and deviation of 5300 ppm can be applied simultaneously with RJ with amplitude of 0.3 UI. These specifications are defined assuming the following conditions: Loopback connection to the MU196020A, at a constant temperature between 20 and 30 °C. When RJ+BUJ is bigger than 0.5 UIp-p or SJ + RJ + BUJ is bigger than the standard value + 0.3 UIp-p, "Overload" is displayed on the MU181500B screen.								
		10000						Max. me	odulation	amplitude
	[j]	1000						- Specific	ation	
	litude	100								
	r Amp	10								
	Jitte	1								
		0.1								
			10 100	1k 	10k Modul	100k ation Fre	۱۸ equen	и 10М су [Hz]	100M	1000M
	ModulationMax. modulationSpecificationfrequency [Hz]amplitude [Ulp-p][Ulp-p]				1					
			10			2	000		2	000
		7 500 100 000				2	000		2	000
						2	000			150
			1 000 000				200			15
			250 000 000				10			1

Table 1.3.2-13 Jitter Tolerance

Overview

1

Item	Specifications*1				
Operating bit rate	NRZ: 25.5 to 32.1 Gbit/s				
	PAM4: 25.5 to 32.1 Gbaud				
Setting range	25.500 000 to 32.100 000 Gbaud, 0.000 001 Gbaud step				
Supported standard and baud rate	For NRZ mode				
	Standard	Bit Rate [Gbit/s]	Remarks		
	100G ULH	32.100 000			
	32G FC	$28.050\ 000$			
	CEI-28G	28.000 000			
	100G OTU4	$27.952\ 496$			
	$100 \text{GbE}(25.78 \times 4)$	$25.781\ 250$			
	InfiniBand EDR25.781 250For PAM4 mode				
	Standard	Baud Rate [Gbaud]	Remarks		
	64G FC	28.900 000			
	CEI-56G	28.000 000			
	$200 \text{GbE}(26.6 \times 4)$	$26.562\ 500$			
	InfiniBand HDR	26.562 500			
Operating bit rate tracking	Tracks the operating bit rate of the PPG selected from the PPGs installed in the same MP1900A.				
Maximum number of consecutive zeros* ²	72 bit (Zero Substitution 2 ¹⁵)				
Lock range*2	±100 ppm				
Target loop band*3	Baud rate / 1667, Baud rate / 2578, Baud rate / 6640, Jitter Tolerance				

*1: When the Option x22 is installed, these are specified with the conditions of PRBS Pattern and Mark Ratio 1/2 (in PAM4 mode, MSB Mark Ratio 1/2) unless otherwise specified.

*2: The target loop band is specified by 1/1667, 1/2578, 1/6640.

*3: The SSPRQ pattern supports Baud rate / 6640 only. When set to Jitter Tolerance, Baud rate / 1667 or higher.

1

Overview



Table 1.3.2-14 Clock Recovery (Cont'd)

- Loop-back connection to MU196020A
- NRZ input
- Test Pattern (Length): PRBS2³¹–1
- Data input amplitude: 0.1 Vp-p

*5: Typical value, specified at a constant temperature between 20 and 30 °C.

Table 1.3.2-15	Mechanical	Performance
	meenanioan	1 chiormanoc

ltem	Specifications
Dimensions	21 mm (H), 234 mm (W), 175 mm (D), Excluding protrusions
Mass	2.5 kg max.
Operating temperature	15 to 30 °C MP1900A's ambient temperature. MU196040A shall operate when installed.
Storage temperature	-20 to 60 °C MU196040A installed to MP1900A shall comply with MIL-T-28800E Class 5.

1.3.3 Specifications for MU196040B

Table 1.3.3-1 Operating Baud Rate

Item	Specifications
Operating Baud Rate	When the Option 001 is installed.
	PAM4 input: 2.4 to 32.1 Gbaud
	NRZ input: 2.4 to 32.1 Gbit/s
	When the Option 002 or y12 is installed.
	PAM4 input: 2.4 to 58.2 Gbaud*
	NRZ input: 2.4 to 64.2 Gbit/s*
	*: When BERT for PCIe1-6 is selected:
	PAM4 input: 2.4 to 32.1 Gbaud

NRZ input: 2.4 to 32.1 Gbit/s

Table 1.3.3-	2 System	Clock
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Item	Specifications
System Clock	 External, Recovered Clock (When the Option x21, x22, x23, or y24 is installed) External: Clock input from the Ext Clock Input connector For PAM4, select from 2.4 to 32.1 Gbaud, 32.1 to 58.2 Gbaud and Auto. For NRZ, select from 2.4 to 32.1 Gbit/s, 32.1 to 64.2 Gbit/s and Auto. Recovered Clock: Clock recovered from the data input from the Data Input connector

1

Itom	Specifications		
ntem	Specifications		
Number of inputs	2 (Data, XData) (Differential)		
Input Condition	Single-Ended, Differential 50 Ohm, Differential 100 Ohm		
	When set to Differential 50 Ohm or Differential 100 Ohm:		
	Independent, Tracking, Alternate*1		
	When set to Alternate:		
	Data-XData, XData-Data*2		
	When set to Single-Ended:		
	Data, XData ^{*3}		
Signal Type	NRZ, PAM4		
LSB/MSB Diagnostics	When set to PAM4, the PAM4 mode can be switched between as follows:		
	Diagnostics Mode OFF:		
	Treats signals as symbols by receiving LSB and MSB while		
	synchronizing them with each other.		
	Diagnostics Mode UN:		
A 11, 1	Asynchronously receives LSD and MSD.		
Amplitude	NRZ: The range in which the Auto Adjust function and the Auto		
	Search function operate. 0.05 ± 0.10 Vppp*4 *5		
	$0.05 \text{ to } 1.0 \text{ vp p}^{-3}, \text{ o}^{-3}$		
	$0.1 \text{ to } 1.0 \text{ vp} \text{ p}^{-3}$, $0.1 \text{ to } 1.0 \text{ vp} \text{ p}^{-3}$, $0.1 \text{ to } 1.0 \text{ vp} \text{ p}^{-3}$, $0.1 \text{ to } 1.0 \text{ vp} \text{ p}^{-3}$, $0.1 \text{ to } 1.0 \text{ vp} \text{ p}^{-3}$, $0.1 \text{ to } 1.0 \text{ vp} \text{ p}^{-3}$, $0.1 \text{ to } 1.0 \text{ vp} \text{ p}^{-3}$, $0.1 \text{ to } 1.0 \text{ vp} \text{ p}^{-3}$, $0.1 \text{ to } 1.0 \text{ vp} \text{ p}^{-3}$, $0.1 \text{ to } 1.0 \text{ vp} \text{ p}^{-3}$, $0.1 \text{ to } 1.0 \text{ vp} \text{ p}^{-3}$, $0.1 \text{ to } 1.0 \text{ vp} \text{ p}^{-3}$, $0.1 \text{ to } 1.0 \text{ vp} \text{ p}^{-3}$, $0.1 \text{ to } 1.0 \text{ vp} \text{ s}^{-3}$, $0.1 \text{ to } 1.0 \text{ vp} \text{ s}^{-3}$, $0.1 \text{ to } 1.0 \text{ vp} \text{ s}^{-3}$, $0.1 \text{ to } 1.0 \text{ vp} \text{ s}^{-3}$, $0.1 \text{ to } 1.0 \text{ vp} \text{ s}^{-3}$, $0.1 \text{ to } 1.0 \text{ vp} \text{ s}^{-3}$, $0.1 \text{ to } 1.0 \text{ vp} \text{ s}^{-3}$, $0.1 \text{ to } 1.0 \text{ vp} \text{ s}^{-3}$, $0.1 \text{ to } 1.0 \text{ vp} \text{ s}^{-3}$, $0.1 \text{ to } 1.0 \text{ vp} \text{ s}^{-3}$, $0.1 \text{ to } 1.0 \text{ vp} \text{ s}^{-3}$, $0.1 \text{ to } 1.0 \text{ vp} \text{ s}^{-3}$, $0.1 \text{ to } 1.0 \text{ vp} \text{ s}^{-3}$, $0.1 \text{ to } 1.0 \text{ to } 1.$		
	PAM4. The range in which the Auto Search PAM4 Fine function		
	0.3 ± 0.10 Vn-n*7. *8		
	$0.5 \text{ to } 1.0 \text{ Vp p}^{-1.0}$		
Threshold	NBZ PAM4 Middle Eve Threshold: $-3.5 \text{ to } +3.3 \text{ V} + 1 \text{ mV stop}^{*2} \times 10^{-10}$		
THIESHOL	$\frac{1}{2} = \frac{1}{2} = \frac{1}$		
	PAM4 Lower Eve Threshold: -3.9 to $+3.7$ V 1 mV step ^{*11}		

Table 1.3.3-3 Data Input

- *1: Tracking is available only for NRZ.
- *2: The absolute value of the difference between Data and XData Threshold values shall be 1.5 V or less.
- *3: PAM4 Upper Eye and Lower Eye can be set by relative values to Middle Eye in the range of -0.4 V to +0.4 V.
- *4: Single-Ended, Differential, Mark Ratio1/2, the Eye Height shall meet the specification.

Example of waveform input to MU196040B when bit rate is 32.1 Gbit/s



*5: Bit rate \leq 32.1 Gbit/s

- *6: Bit rate >32.1 Gbit/s
- *7: 0/3 Level, PRBS31, Mark Ratio1/2, with connected to the MU196020A using an attenuator, with Emphasis adjusted so that the Eye Height meets the specification



Example of waveform input to MU196040B when baud rate is $32.1\ \mathrm{Gbaud}$



Eye Height: 50 mV or greater

- *8: Single-Ended, Differential, Baud rate ≤32.1 Gbaud
- *9: Differential, Baud rate >32.1 Gbaud
- *10: Data and XData can be set independently.
- *11: Data and XData cannot be set independently, and can be set in the range of ± 0.4 V from Middle Eye Threshold.

1

ltem	Specifications			
Sensitivity	Single-Ended , Mark Ratio1/2, PRBS31, when connecting directly to the MU196020A using J1789A and an attenuator, Emphasis ON, unused connectors on the MU196020A and MU196040B are terminated,			
	At a constant temperature between	n 20 and 30 °C		
Eye Amplitude	NRZ			
	Typ. 25 mVp-p, ≤ 50 mVp-p* ¹²	(26.5625 Gbit/s, 32.1 Gbit/s)		
	Typ. 31 mVp-p, ≤ 55 mVp-p* ¹³	(53.125 Gbit/s)		
	Typ. 43 mVp-p, $\leq 60 \text{ mVp-p}^{*13}$	(64.2 Gbit/s)		
Eye Height	NRZ			
	Typ. 19 mV* ¹²	(26.5625 Gbit/s, 32.1 Gbit/s)		
	Typ. 21 mV* 13	(53.125 Gbit/s)		
	Typ. 32 mV* 13	(64.2 Gbit/s)		
	PAM4			
	0/1 1/2 2/3 Level, PRBS31, when us	sing External Clock		
	Typ. 23 mV, $\leq 50 \text{ mV}^{*12}$	(26.5625 Gbaud, 32.1 Gbaud)		
	Typ. 36 mV, $\leq 60 \text{ mV}^{*13}$	(53.125 Gbaud)		
	Typ. 49 mV, $\leq 70 \text{ mV}^{*13}$	(58.2 Gbaud)		
	Note that 53.125 Gbaud and 58.2 Gbaud are defined by the Eye			
	Height value that results in a dif	fferential waveform having BER of		
	1E-06 by changing the test pattern to QPRBS13-CEI after setting the			
	test pattern to PRBS31 and setti	ing the amplitude value.		
Phase Margin	Differential, Mark Ratio 1/2, PRBS31, when inputting 0.5 Vp-p, when connecting directly to the MU196020A using J1789A and an attenuator.			
	At a constant temperature between 20 and 30 °C, when using External			
	Clock			
	NRZ^{*14}			
	Typ. 25.8 ps^{*12}	(26.5625 Gbit/s)		
	Typ. 18.0 ps^{*12}	(32.1 Gbit/s)		
	Typ. 10.5 ps^{*13}	(53.125 Gbit/s)		
	Typ. 8.7 ps^{*13}	(64.2 Gbit/s)		
	PAM4			
	Typ. 5.3 ps^{*12}	(26.5625 Gbaud)		
	Typ. 4.5 ps^{*12}	(32.1 Gbaud)		
	Typ. 4.1 $ps^{*13}, *14$	(53.125 Gbaud)		
	Typ. 2.5 $ps^{*13, *14}$	(58.2 Gbaud)		

Table 1.3.3-3	Data Input (Cont'd)
	Butu mput (Som a	1

*12: When the Option 001, 002, or y12 is installed.

*13: When the Option 002 or y12 is installed.

*14: Value including RJ equivalent to BER 1E–12 of input signal

Item	Specifications		
Stressed Margin			
Stressed Eye Height	PAM4 0/1 1/2 2/3 Level, QPRBS13-CEI, Eye Height where BER is 1E– 06, when using External Clock $\geq 32 \text{ mV}^{*15, *16}$ $\geq 37 \text{ mV}^{*17, *18}$ PAM4 0/1 1/2 2/2 Level OPPRS12-CEL Eye Width where BER is 1E of		
	when using External Clock $\geq 7.53 \text{ ps}^{*15, *16}$ $\geq 3.76 \text{ ps}^{*17, *18}$		
Termination	50Ω , GND, Variable		
Termination Voltage	When set to Variable: -2.5 to $+3.5$ V, 10 mV step		
Connector	V connector (f.)		
Decision Feedback Equalizer	With a built-in Decision Feedback Equalizer (DFE)*19		
Тар	1		
Coefficient			
Setting Range	0 to 30, 1 step		
Loss Compensation	Nom. 1.4 dB*20		
Low Frequency Equalizer	With a built-in Low Frequency Equalizer ^{*19}		
Gain			
Setting Range	-2.0 to 0 dB, 0.5 dB step		
Accuracy	Typ. ±1.0 dB		
Ideal Frequency			
Response	0.5		
	-0.5		
	₩ -1.0 -0.5 dB		
	-1.0 dB		
	-2.0 -2.0 -1.5 dB		
	-2.5 -2.0 dB		
	0.01 0.1 1 10		
	Frequency [GHz]		

 Table 1.3.3-3
 Data Input (Cont'd)

*15: 26.5625 Gbaud, when installed with the Option 001, 002 or y12 and the Option x11, BER 1E–12

*16: 26.5625 Gbaud, Differential, Mark Ratio1/2, when J1789A is used to connect J1800A (1 pc) and MU196020A

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At a constant temperature between 20 and 30 $^{\circ}$ C, measure with a 70-GHz bandwidth sampling oscilloscope with residual jitter of less than 200 fs (RMS).

Adjust De-Emphasis (2 Pre Cursors and 1 Post Cursor) of MU196020A so that the product of Eye Height (1E–06) and Eye Width (1E–06) can be maximized in the differential waveform.

Calculate the 4th-order Bessel Filter (Cutoff Frequency 40 GHz) + CTLE (+1 dB Peaking at 14 GHz) and calibrate it to a PAM4 waveform with Eye Amplitude of 0.88 Vp-p (Diff) or less and Eye Linearity R_{LM} 0.85 or more.

Activate the DFE and Low Frequency Equalizer in the MU196040B, and perform adjustment.

- *17: 53.125 Gbaud, when the Option 002, y12 and x11 are installed, BER 1E–8 nom.
- *18: 53.125 Gbaud, when the Option 002, y12 and x11 are installed, Differential, Mark Ratio1/2, when connecting a device with 12.0 dB insertion loss and MU196020A.



At a constant temperature between 20 and 30 $^{\circ}$ C, measure with a 70-GHz bandwidth sampling oscilloscope with residual jitter of less than 200 fs (RMS).

Adjust De-Emphasis (2 Pre Cursors and 1 Post Cursor) of MU196020A so that the product of Eye Height (1E–06) and Eye Width (1E–06) can be maximized in the differential waveform.

Calculate the 4th-order Bessel Filter (Cutoff Frequency 43 GHz) + CTLE (+1 dB Peaking at 28 GHz) and calibrate it to a PAM4 waveform with Eye Amplitude of 0.88 Vp-p (Diff) or less and Eye Linearity R_{LM} 0.85 or more.

Activate the DFE and Low Frequency Equalizer in the MU196040B, and perform adjustment.

*19: When the Option x11 is installed.

*20: 53.125 Gbaud, Calculated from the following three:

- The BER result obtained when DFE is OFF under the condition of *18.
- The BER result obtained when DFE is OFF under the condition of *18 and 1.8 dB additional loss.
- The best BER result obtained when DFE is ON under the condition of *18 and 1.8 dB additional loss.

Table 1.3.3-4 Clock Input

Item	Specifications	
External Clock Input	Operation Baud Rate = Clock Input Frequency $\times 2$	
Number of inputs	1 (Single-Ended)	
Frequency range	1.2 to 32.1 GHz	
Amplitude	0.3 to 1.0 Vp-p (–6.5 to +4.0 dBm) (Input Frequency \leq 16.05 GHz)	
	0.4 to 1.0 Vp-p (–3.9 to +4.0 dBm) (Input Frequency > 16.05 GHz)	
Termination	50Ω , AC Coupling	
Connector	K connector (f.)	

Table 1.3.3-5 Aux Input

ltem	Specifications		
Number of inputs	1 (Single-Ended)		
Variation	External Mask, Burst, Capture External Trigger		
Minimum pulse width	1/256 of Data rate		
Input level	 0/-1 V (H: -0.25 to 0.05 V, L: -1.1 to -0.8 V) 0/-0.5 V (H: -0.05 to 0.05 V, L: -0.55 to -0.45 V) Vth 0 V (Input amplitude 0.5 to 1.0 Vp-p) Select one of the above. 		
Termination	$50 \Omega, \text{GND}$		
Connector	SMA connector (f.)		

Table 1.3.3-6 Aux Output

Item	Specifications
Number of outputs	2 (Differential)
Variation	1/n Clock (n = 8, 12, 16, 201020, 1024), Pattern Sync, Sync Gain, Error Output, Capture Trigger
Pattern Sync	
PRBS, PRGM	Position: 1 to {(Least common multiple of Pattern Length' and 256) – 263}, 8 steps (When the Option 001 is installed) Pattern Length' shall be the value obtained by multiplying Pattern
	Length setting until it becomes 1024 or more if it is 1023 or less.
Output level	0/-0.6 V (H: -0.25 to 0.05 V, L: -0.80 to -0.45 V)
Termination	50 Ω, GND
Connector	SMA connector (f.)

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Item	Specifications		
PRBS			
Pattern length	$2^{n}-1$ (n = 7, 9, 10, 11, 13, 15, 20, 23, 31)		
Mark ratio	1/2, 1/2inv		
PRBS generator	n=7: 1 + X ⁶ + X ⁷		
polynomial	n=9: $1 + X^5 + X^9$		
	n=10: 1 + X ⁷ + X ¹⁰		
	n=11: $1 + X^9 + X^{11}$		
	n=13: $1 + X + X^2 + X^{12} + X^{13}$		
	n=15: 1 + X ¹⁴ + X ¹⁵		
	n=20: 1 + X ³ + X ²⁰		
	n=23: $1 + X^{18} + X^{23}$		
	n=31: 1 + X^{28} + X^{31}		
PRBS Inversion	This is available in PAM4 mode only.		
	Logically inverted PRBS can be set independently for MSB and LSB.		
Zero-Substitution	This is available in NRZ mode only.		
Additional Bit	0 bit, 1 bit		
Pattern length	2^{n} or $2^{n}-1$ (n = 7, 9, 10, 11, 15, 20, 23)		
Start position	Substitutes the bit coming after the maximum "0" successive bits.		
Zero-Length	1 to (Pattern Length – 1) bits		
	If the bit coming after Zero-substitution is "0," then it is replaced with "1."		
Data			
Data length	NRZ: 2 to 268 435 456 bits, 1 bit step		
	PAM4: 2 to 268 435 456 symbols, 1 symbol step		

Table 1.3.3-7 Pattern Detection

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Overview

ltem	Specifications		
Coding	NRZ, PAM4		
NRZ	Normal, Invert		
PAM4 Gray Coding	ON, OFF*3		
PAM4 Precoding $(1/(1 + D) \mod 4)^{*1}$	ON, OFF*3		
PAM4 Inverse Gray Coder	ON, OFF^{*_4}		
PAM4 Pre Code Remover*2	ON, OFF*4		
Input Signal Decoder	ON, OFF		
	Fixed to OFF when PAM4 Standard Pattern is one of the following specific patterns:		
	PRBS13Q, QPRBS13-CEI, PRBS13Q(InfiniBand),		
	PRBS23Q, PRBS31Q, QPRBS-CEI, PRBS31Q(InfiniBand),		
	PRBS31Q(Fiber Channel), SSPRQ, QPRBS13, JP03A, JP03B,		
	Transmitter Linearrity, Square Wave, CP in 1b/1b Encoding for PCIe6, MCP in 1b/1b Encoding for PCIe6		
Delay Symbol	ON, OFF		
SKP	No SKP, SKPx1, SKPx2		
Preset	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10		
SRIS	ON, OFF		
EIEOS	ON		
SKP OS Filter	ON, OFF		

Table 1.3.3-7 Pattern Detection (Cont'd)

- *1: (1/(1+D) mod 4) is a generator polynomial defined in the IEEE802.3.
- *2: Uses the generator polynomial (1+D) mod 4 defined in the IEEE802.3.
- *3: Available only when Input Signal Decoder is **OFF**. Not available when it is **ON**.
- *4: Available only when Input Signal Decoder is **ON**. Not available when it is **OFF**.

Item	Specifications			
PAM4 Standard Pattern	Standard-compliant PAM4-mode patterns			
CEI	QPRBS13-CEL QPRBS31-CEI			
IEEE	IEEE802 3bs/cd: PRBS130 PRBS310 SSPR0 Square Wave			
	IEEE802.3bj: QPRBS13, JP03A, JP03B, Transmitter Linearity			
InfiniBand	PRBS13Q (InfiniBand), PRBS23Q, PRBS31Q (InfiniBand)			
Fibre Channel	PRBS31Q (Fibre Channel)			
RS-FEC	RS-FEC Scrambled Idle 50G 1Lane*5,			
	RS FEC Scrambled Idle 100G 1Lane*5,			
	RS FEC-Int Scrambled Idle 100G 1Lane*5,			
	RS FEC Scrambled Idle 100G 2Lanes* ⁵ ,			
	RS-FEC Scrambled Idle 200G 2Lanes* ⁵ ,			
	RS-FEC Scrambled Idle 200G 4Lanes* ⁵ ,			
	RS-FEC Scrambled Idle 400G 4Lanes*5,			
	RS-FEC Scrambled Idle 400G 8Lanes* ⁵			
PCIe	CP in 1b/1b Encoding for PCIe6			
	MCP in 1b/1b Encoding for PCIe6			
NRZ Standard Pattern	Standard-compliant NRZ-mode pattern			
CEI	SSPR			
RS-FEC	RS-FEC Scrambled Idle 25G 1Lane* ⁵ ,			
	RS-FEC Scrambled Idle 50G 2Lanes RS(544,514)*5,			
	RS-FEC Scrambled Idle 100G 4Lanes* ⁵ ,			
	RS-FEC Scrambled Idle 100G 4Lanes RS(544,514)*5			
PCIe	CP in 8b/10b Encoding for PCIe1			
	MCP in 8b/10b Encoding for PCIe1			
	CP in 8b/10b Encoding for PCIe2			
	MCP in 8b/10b Encoding for PCIe2			
	CP in 128b/130b Encoding for PCIe3			
	MCP in 128b/130b Encoding for PCIe3			
	OF III 1200/1300 Encoding for PCIe4 MCP in 128b/130b Encoding for PCIe4			
	CP in 128b/130b Encoding for PCIe5			
	MCP in 128b/130b Encoding for PCIe5			

Table 1 3 3-7	Pattern	Detection	(Cont'd)
	I allein	Delection	(Cont u)

*5: When the Option w42 is installed.

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|--|

Item	Specifications			
Sequence	Repeat, Burst			
Repeat	Continuous Pattern	Continuous Pattern		
Burst	This is available on	This is available only when Coding is NRZ.		
Source	Internal, External-Enable (Aux Input), External-Trigger (Aux Input)		erv	
Delay	Internal:	0 to 2 147 483 640 bits, 8 bits step	/ie	
	External-Trigger, External-Enable:		8	
		0 to 2 147 483 520 bits, 8 bits step		
	Adjust Method:	Auto, Manual		
Enable Period	Internal:	12 800 to 2 147 482 624 bits, 256 bits step		
	External-Trigger:	12 800 to 2 147 483 136 bits, 256 bits step		
Burst Cycle	25 600 to 2 147 483 648 bits, 1024 bits step			

Table 1.3.3-9 Me	easurement
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Item		Specifications	
Counter	Error Rate (ER) Total:	0.000 1E–18 to 1.000 0E00	
	Error Count (EC) Total:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17	
	Error Interval:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17	
	%Error Free Interval:	0.000 0 to 100.000 0	
	Error Rate (ER) Insertion (INS):		
		0.000 1E–18 to 1.000 0E00	
	Error Count (EC) Insertion (INS):		
		0 to 9 999 999, 1.000 0E07 to 9.999 9E17	
	Error Rate (ER) Omission (OMI):		
		0.000 1E–18 to 1.000 0E00	
	Error Count (EC) Omission (OMI):		
	0 to 9 999 999, 1.000 0E07 to 9		
	Frequency:	2 400.000 to $58 200.000$ MHz	
	Frequency measurement accuracy:		
	$\pm 1 \text{ ppm} \pm 1 \text{ kHz}^{*1}$		
	Clock Count:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17	
	Sync Loss Interval:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17	
	Clock Loss Interval:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17	
	Expressions enclosed in parentheses are abbreviations.		

*1: With a gating system and with MP1900A's reference clock (10 MHz) $\,$ calibrated

Item	Specifications			
Counter (Cont'd)	MSB Error Rate (ER) Total:	0.000 1E–18 to 1.000 0E00		
	MSB Error Count (EC) Total:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17		
	MSB Error Interval*2:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17		
	MSB %Error Free Interval*2:	0.000 0 to 100.000 0		
	MSB Error Rate (ER) Insertio	on (INS):		
		0.000 1E–18 to 1.000 0E00		
	MSB Error Count (EC) Insertion (INS):			
		0 to 9 999 999, 1.000 0E07 to 9.999 9E17		
	MSB Error Rate (ER) Omission (OMI):			
	0.000 1E–18 to 1.000 0E00			
	MSB Error Count (EC) Omission (OMI):			
		0 to 9 999 999, 1.000 0E07 to 9.999 9E17		
	LSB Error Rate (ER) Total:	0.000 1E–18 to 1.000 0E00		
	LSB Error Count (EC) Total:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17		
	LSB Error Interval*2:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17		
	LSB %Error Free Interval*2:	0.000 0 to 100.000 0		
	LSB Error Rate (ER) Insertio	n (INS):		
		0.000 1E–18 to 1.000 0E00		
	LSB Error Count (EC) Inserti	on (INS):		
		0 to 9 999 999, 1.000 0E07 to 9.999 9E17		
	LSB Error Rate (ER) Omission (OMI):			
	0.000 1E–18 to 1.000 0E00			
	LSB Error Count (EC) Omission (OMI): 0 to 9 999 999, 1.000 0E07 to 9.999 9E17			
	The following are available only for PAM4 (Diagnostics Mode ON) measurement.			
	MSB Bit Count:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17		
	MSB Clock Count:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17		
	MSB Sync. Loss Interval:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17		
	LSB Bit Count:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17		
	LSB Clock Count:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17		
	LSB Sync. Loss Interval:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17		
	Expressions enclosed in parentheses are abbreviations.			

Table 1.3.3-9 Measurement (Cont'd)

*2: Can be obtained only with remote commands.

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Overview

Item	Specifications	
Counter (Cont'd)	The following are available when the Option z installed. The following are available only for PAM4 (Di measurement	241 SER Measurement is agnostics Mode OFF)
	and the surface of th	
	Symbol Error Rate (SER): 0.000 1E-18 to 1. Symbol Error Count (SEC): 0 to 9 999 999, 1. Symbol Error Interval: 0 to 9 999 999, 1. Symbol %Error Free Interval: 0.000 0 to 100.000 PAM4 Symbol Count: 0 to 9 999 999, 1. Level 3 PAM4 Count: 0 to 9 999 999, 1. Level 2 PAM4 Count: 0 to 9 999 999, 1. Level 1 PAM4 Count: 0 to 9 999 999, 1.	000 0E00 000 0E07 to 9.999 9E17 000 0E07 to 9.999 9E17 0 0 000 0E07 to 9.999 9E17 000 0E07 to 9.999 9E17 000 0E07 to 9.999 9E17 000 0E07 to 9.999 9E17
	Level 0 PAM4 Count: 0 to 9 999 999, 1. Details-Result PAM4-Display1 Level 0 \rightarrow 3 EC: 0 to 9 999 999, 1.00 Level 0 \rightarrow 2 EC: 0 to 9 999 999, 1.00 Level 0 \rightarrow 1 EC: 0 to 9 999 999, 1.00 Level 0 EC Total: 0 to 9 999 999, 1.00 Level 0 ER Total: 0.000 1E-18 to 1.00	000 0E07 to 9.999 9E17 00 0E07 to 9.999 9E17
	Level $1 \rightarrow 3$ EC:0 to 9 999 999, 1.00Level $1 \rightarrow 2$ EC:0 to 9 999 999, 1.00Level $1 \rightarrow 0$ EC:0 to 9 999 999, 1.00Level 1 EC Total:0 to 9 999 999, 1.00Level 1 ER Total:0.000 1E-18 to 1.00	00 0E07 to 9.999 9E17 00 0E07 to 9.999 9E17 00 0E07 to 9.999 9E17 00 0E07 to 9.999 9E17 00 0E07 to 9.999 9E17

 Table 1.3.3-9
 Measurement (Cont'd)

Item		Specifications
Counter (Cont'd)	Level $2 \rightarrow 3$ EC:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Level $2 \rightarrow 1$ EC:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Level 2 \rightarrow 0 EC:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Level 2 EC Total:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Level 2 ER Total:	0.0001E–18 to 1.000 0E00
	Level 3 \rightarrow 2 EC:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Level $3 \rightarrow 1$ EC:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Level 3 \rightarrow 0 EC:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Level 3 EC Total:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Level 3 ER Total:	0.000 1E–18 to 1.000 0E00
	Details-Result PAM4-Dis	play2* ³
	Transition 1level	
	Level $0 \rightarrow 1$ and Le	evel $1 \rightarrow 0$
	SEC:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Level $1 \rightarrow 2$ and Le	evel $2 \rightarrow 1$
	SEC:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Level $2 \rightarrow 3$ and Le	evel $3 \rightarrow 2$
	SEC:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Transition 2level	
	Level $0 \rightarrow 2$ and Le	evel $2 \rightarrow 0$
	SEC:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Level $1 \rightarrow 3$ and Le	evel $3 \rightarrow 1$
	SEC:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Transition 3level	
	Level $0 \rightarrow 3$ and Le	evel $3 \rightarrow 0$
	SEC:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Upper Eye Total SEC:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Middle Eye Total SEC:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Lower Eye Total SEC:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Upper Eye Total SER:	0.000 1E–18 to 1.000 0E00
	Middle Eye Total SER:	0.000 1E–18 to 1.000 0E00
	Lower Eye Total SER:	0.000 1E–18 to 1.000 0E00

Table 1.3.3-9 Measurement (Cont'd)

*3: Available when Input Signal Decoder is **OFF**.

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Overview

Item	Specifications
Counter (Cont'd)	The following items are available only when the Option w42 FEC
	Analysis is installed.
	Uncorrectable Codeword Error Rate (UCWER):
	0.000 1E–18 to 1.000 0E00
	Uncorrectable Codeword Error Count (UCWEC):
	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Uncorrectable Codeword Error Interval:
	Oncorrectable Codeword %Error Free Interval
	0.000 0 to 100.000 0
	ΓEC Symbol Error Rate (ER).
	0.000 IE-18 to 1.000 0E00
	$\begin{array}{c} \text{FEC Symbol Error Count (EC)} \\ 0 + 0 000 000 1 000 0E07 + 0 000 0E17 \end{array}$
	0 10 9 999 999, 1.000 0E07 10 9.999 9E17
	$0 \neq 0 000 000 1 000 000 000 000 000 000 $
	FEC Symbol % Error Error Interval.
	$0.000.0 \pm 0.100.000.0$
	Total Codeword Count: 0 to 9 999 999 1 000 0F07 to 9 999 9F17
	Details-Regult RS-FFC
	MSR FEC Sumbal Error Data (FP) Tatal:
	0.000 1E - 18 to 1.000 0E 00
	MSB FFC Symbol Error Count (FC) Total
	0 to 9 999 999 1 000 0E07 to 9 999 9E17
	LSB FEC Symbol Error Bate (ER) Total:
	0.000 1E - 18 to 1.000 0E00
	LSB FEC Symbol Error Count (EC) Total:
	0 to 9.999.999 1 000.0E07 to 9.999.9E17
	FEC Symbol Error Count
	N = 0 to 31 Codeword Rate:
	0.000 1E–18 to 1.000 0E00
	N = 0 to 31 Codeword Count:
	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Uncorrectable Codeword Rate (UCWR):
	0.000 1E–18 to 1.000 0E00
	Uncorrectable Codeword Count (UCWC):
	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Expressions enclosed in parentheses are abbreviations.
RS-FEC Error Distribution	Available only when the Option w42 FEC Analysis is installed.
	The number of codewords is displayed in a graph by FEC symbol error
	count per codeword.

 Table 1.3.3-9
 Measurement (Cont'd)

ltem		Specifications
Input Signal Decoder	Displays the coding status during PAM4 mode error measurement.	
Indicator	Raw Signal: Display	s error measurement results of input data
	without	decoding it.
	Decoded Signal: Display	s error measurement results of decoded input
Gating	Time, Clock Count, Error	Count
Gating Unit	Time:	1 second to 99 days 23 hours 59 minute 59 seconds
	Clock Count:	>E+4 to >E+16
	Error Count:	>E+4 to >E+16
Cycle	Single, Repeat, Untimed	
Current	On, Off can be set.	
	Calculation:	Progressive, Immediate
	Interval:	100 ms, 200 ms
Auto Sync	On, Off can be set.	
	Synchronization threshol	d:
		INT, $E-2$ to $E-8$
Sync Control	PRBS:	Automatic Synchronization
	Data:	Frame On
Frame Length	NRZ:	4 to 64 bits, 4 bits step
	PAM4:	4 to 64 symbols, 4 symbols step
Frame Mask	Available	
Frame Position	NRZ:	1 to (Pattern Length – Frame Length +1) bits, 1 bit step
	PAM4:	1 to (Pattern Length – Frame Length +1) symbols, 1 symbol step
Error/Alarm Conditions		
Error Detection	NRZ:	Insertion/Omission, Transition/Non Transition
	PAM4:	Not available
EI/EFI Interval	1 ms, 10 ms, 100 ms, 1 s	

Table 1.3.3-9	Measurement (Cont'd)
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Overview

Item		Specif	ications		
Bit Mask (Block Window)	Excludes the specified data pattern from measurement.*1				
Setting resolution	The resolution is set depending on the pattern length as follows:				
	Pattern lengt	h (bits)	S	etting resol	ution (bits)
		2 to 2 09	$7\ 152$	1	
	$2\ 097$	153 to 4 19	$4\ 304$	2	
	4 194	305 to 8 38	$8\ 608$	4	
	8 388 6	509 to 16 77	$7\ 216$	8	
	16 777 2	217 to 33 55	$4\ 432$	16	;
	$33\ 554$ 4	433 to 67 10	$8\ 864$	32	1
	67 108 86	35 to 134 21	$7\ 728$	64	:
	134 217 72	29 to 268 43	$5\ 456$	128	8
Lane Mask (Bit Window)	Excludes any channels measurement.*1 (Availa	among inter Ible only in I	nal 32 chan NRZ mode.)	nels from	
External Mask	H: Measurement				
	L: Mask				
Capture	NRZ, PAM4 (Only FEC Symbol Capture is available when LSB/MSB Diagnostics is set to ON.)				
Conturo Modo	r Alvi4 is available when	i the Option	Z41 SEIV M	leasurement	t is instaneu.
Capture Mode	Sync Mode Capture				
	data and pattorn sott	ient. Synchr	omzation is	required be	etween input
	Raw Data Cantura	iiig.			
	Does not perform erro	r judgment	Synchroniz	zation is not	required
	between input data a	nd pattern s	etting.	2411011 15 1101	requireu
	FEC Symbol Capture ^{*2}	*3	etting.		
	Performs FEC Symbol error judgment. Synchronization is required				
	between input data an	nd pattern s	etting.		
	Judgement is made or	n whether tl	he number o	of FEC Sym	bol errors
exceeds the threshold.		wo Modo th	at aan ha an	antad	
	according to the Inpu	t Signal Dec	oder setting	at can be ex g.	ecuted
		Input Signal Decoder			
	Capture Mode	(Diagnostics Mode = OFF)(Diagnostics Mode = ON)		tics Mode DN)	
		OFF	ON	OFF	ON
	Raw Data Capture	✓			—
	Sync Mode Capture	✓	✓	_	_
	FEC Symbol Capture	✓	✓	✓	✓

 Table 1.3.3-10
 Error Analysis

*1: RS-FEC pattern is excluded.

- *2: Each FEC Symbol consists of data of 10 or 20 bits.
- *3: Occurrence of one or more bit errors in one FEC Symbol is counted as one FEC Symbol error.

Item	S	pecifications		
Capture (Cont'd)				
Auto Launch	Select the result screen you want to display automatically when data is			
	captured.			
	Capture Data			
	Displays the captured patter Hex, Symbol).	rn data nume	rically or by a	string (Bin,
	Error Mapping			
	Displays the captured error This cannot be selected whe	data as a maj n Capture Mo	p. ode is Raw Dat	ta Capture or
	FEC Symbol Capture.			
	• Disable	loss the supervite	~~~~	
Number of Blocks	1 9 4 9 1C 29 C4 199	lay the result	screen.	
Number of Blocks	1, 2, 4, 8, 16, 32, 64, 128		-1)	
block Length	$\mathbf{N}\mathbf{K}\mathbf{Z}$ 8 Molts / n (n-1) $\mathbf{P}\mathbf{A}\mathbf{M}\mathbf{A}$ 4 Maymbols / n (n-2)	Number of blo	cks)	
Triggor	France Dotoet Moteb Pottorn N	Acruel Trigge	ur Extornal T	riggor (Bising
Ingger	Edge). Consecutive Error Dete	ct. Intermitte	nt Error Deteo	tigger (Itishig
	Error Detect cannot be selected	d when Captu	re Mode is Ra	w Data
	Capture.			
	For the relationship between C	Capture Modes	s and selectab	le Triggers,
	refer to the table below.			
		Sync Modo	Paw Data	FEC
	Trigger	Conturo	Raw Dala	Symbol
		Capture	Capture	Capture
	Error Detect	✓	_	—
	Match Pattern	✓	✓	_
	Manual Trigger	✓	✓	✓
	External Trigger	✓	✓	_
	Consecutive Error Detect ^{*4}	_	_	✓
	Intermittent Error Detect ^{*5}	_	—	✓
	Pattern Sync	\checkmark	—	_
Trigger Position	After the Trigger, Around the	Frigger, Befor	e the Trigger	
	After the Trigger and Before th	ne Trigger can	not be selecte	d when
	Capture Mode is FEC Symbol	Capture.		
Match Pattern Length	NRZ: 4 to 64 bits, 1 bit step			
	PAM4: 4 to 64 symbols, 1 sym	bol step		
Match Pattern Mask	NRZ: 4 to 64 bits, 1 bit step	1 - 1 - 4		
	PAM4 \cdot 4 to 64 symbols, 1 sym	bol step		
	*4: Consecutive Error Detect	Starts captur	ring when the	number of
	consecutive FEC Symbol 1	Errors equals	to or exceeds	the threshold
	regardless of codeword.	-		
	*5: Intermittent Error Detect	Starts captu	ring when the	e number of
	FEC Symbol Errors that o	occurred withi	n one codewoi	rd exceeds the

threshold.

Table 1.3.3-10	Error Analysis	(Cont'd)

Specifications *1.3*

Table 1.3.3-10 Error Analysis (Cont'd)		
Item	Specifications	
Capture (Cont'd)		
FEC Symbol Capture		
Setting		Q
Preset	For NRZ: Variable,RS-FEC 25G 1Lane, RS-FEC 50G 2Lanes RS(544,514), RS-FEC 100G 4Lanes, RS-FEC 100G 4Lanes RS(544,514) For PAM4: Variable, RS-FEC 50G 1Lane, RS-FEC 100G 1Lane, RS-FEC-Int 100G 1Lane, RS-FEC 100G 2Lanes, RS-FEC 200G 2Lanes, RS-FEC 200G 4Lanes, PS-FEC 400C 4Lanes, PS-FEC 400C 8Lanes,	erview
Number of FEC Symbols per Lane in a Codeword	68, 132, 136, 272, 528, 544 FEC Symbols, 1 FEC Symbol step	
Bit Length in a FEC Symbol	10, 20 bits	
FEC Symbol Errors in a Codeword	When Trigger is Consecutive Error Detect: 1 to 32 FEC Symbols, 1 FEC Symbol step When Trigger is Intermittent Error Detect: 1 to 32 FEC Symbols, 1 FEC Symbol step	
Comparison	Greater than or equal to, Equal to	

Analysis (Cont'd) Table 1 2 2 10 E

Item	Specifications
Capture (Cont'd)	
Capture Result	
Capture Data	Displays captured results by bit or symbol sequence in NRZ or PAM4 mode.
	When Capture Mode is Sync Mode Capture or FEC Symbol Capture, error bits and symbols are displayed with background color.
Viewer Mode	Sets the view mode of the captured result pattern. NRZ: BIN, HEX
	PAM4: Symbol, BIN(MSB/LSB)
	Waveform display can be turned on and off.
Error display	NRZ: Insertion Error, Omission Error
	When the input signal decoder is OFF :
	PAM4(Symbol): Lower Eye Error, Middle Eye Error,
	Upper Eye Error, Middle/Lower Eye Error,
	Upper/Middle Eye Error,
	When the input signal decoder is ON :
	PAM4(Symbol): MSB LSB MSB+LSB
	PAM4(MSB/LSB):
	Insertion Error, Omission Error
	This is available only when Capture Mode is Sync Mode Capture or FEC Symbol Capture.
Error Search	First: Fist error
	Pre: Previous error
	Next: Next error
	Last: Last error
	In PAM4 mode only, a search target can be selected from All, Upper Eye, Middle Eye and Lower Eye.
	This is available only when Capture Mode is Sync Mode Capture or FEC Symbol Capture.
Continuous Error	Searches for continuous error bits/symbols.
	NRZ: 1 to 256 bits
	PAM4(Symbol): 1 to 256 symbols
	PAM4(MSB/LSB) : 1 to 256 bits
	This is available only when Capture Mode is Sync Mode Capture or FEC Symbol Capture.
Codeword Head	Searches for the beginning of a codeword.
Position Jump	First: Beginning of the first codeword
	Pre: Beginning of the previous codeword
	Next: Beginning of the next codeword
	Last: Beginning of the last codeword
	Available only when Capture Mode is FEC Symbol Capture.

Table 4 2 2 40	Error Analysia	(Contid)
Table 1.3.3-10	Error Analysis	(Cont'a)

1

Item	Specifications		
Capture (Cont'd)			
File Save	Saves the captured results and pattern to a file. NRZ:		
	BIN/HEX Text: Captured result file (It can be opened in the Capture Data screen.)		
	BIN/HEX Text(export): Pattern file including error information (It can be opened in Pattern Editor.)		
	PAM4:		
	Symbol Text:Captured result file (It can be opened in the Capture Data screen.)		
	Symbol Text(export): Pattern file including error information (It can be opened in Pattern Editor.)		
File Open	Redisplays the captured results. NRZ:		
	BIN/HEX Text: Captured result file PAM4:		
	Symbol Text: Captured result file		
Error Mapping	Visually maps errors using bits with colored-background in NRZ or PAM4 mode.		
	This is available only when Capture Mode is Sync Mode Capture.		
Error display	NRZ: Insertion Error, Omission Error		
	When the input signal decoder is OFF :		
	PAM4: Lower Eye Error, Middle Eye Error,		
	Upper Eye Error, Middle/Lower Eye Error,		
	Upper/Middle Lye Error, Upper/Middle/Lower Eve Error		
	When the input signal decoder is ON .		
	PAM4: MSB_LSB_MSB+LSB		
File Open	Remans the cantured results (errors)		
The open	NRZ:		
	BIN/HEX Text: Captured result file		
	PAM4:		
	Symbol Text: Captured result file		

Table 1.3.3-10	Error Analysis (Cont'd)

Item	Specifications
Bath-Tub	NRZ/PAM4: Available*1, *2, *3
Eye Contour	NRZ/PAM4: Available*2, *3, *4, *5
Auto Adjust	NRZ: Vth direction only ^{*6}
	PAM4: MSB Vth direction only*6, *7
Auto Search	NRZ: Available ^{*6}
	PAM4 (LSB/MSB Diagnostics OFF/ON): Available* ^{6, *8}
Advanced Search	Supports adjustment of PRBS Inv, Logic (MSB, LSB), Gray Coder, Inverse Gray Coder, Eye Threshold (Middle, Upper, Lower), Delay, DFE and LFEQ.*9 NRZ: Available*6 PAM4: Available*6, *8, *10
BER/SER Logging	NRZ: With BER Logging PAM4: With SER Logging
	*1: When PAM4 is selected, measurement can be performed by selecting one from Upper, Middle, and Lower Eyes, and SER.

Table 1.3.3-11 Auto Measurement

*2: Not available under the following conditions:

- There is a swap between MSB and LSB patterns in RS-FEC Scrambled Idle Pattern. (Swap lamp: On)
- The measured value of MSB/LSB Diff is other than 0.
- *3: The Option z41 required to use the function.
- *4: When PAM4 is selected, measurement can be performed by selecting one from Upper, Middle, and Lower Eyes.
- *5: The PAM4 waveform (simultaneous display of Upper/Middle/Lower Eye) is displayed by optimizing the delay in the phase direction inside the measuring instrument of each of Upper/Middle/Lower eyes.
- *6: PRBS Pattern, Mark Ratio 1/2
- *7: Each of amplitudes shall be equal.
- *8: Each of 0/1, 1/2 and 2/3 levels is equal.
- *9: The Option x11 is required for adjustment of DEF and LFEQ.
- *10: PRBS Inv, Logic (MSB, LSB), Gray Coder, Inverse Gray Coder, and Eye Threshold (Middle, Upper, Lower) are available only when Modulation Type is PAM4.

	•	
Item	Specifications	
Phase variable range	-1000 to +1000 mUI, 2 mUI step	
Accuracy	$\begin{array}{llllllllllllllllllllllllllllllllllll$	۵
mUI – ps switching	Available (internally converted into ps)	
Calibration	Available (when jitter modulation is off)	
Calibration indicator	 This indicator is on when Calibration is required due to: Change in 1/1Clock frequency by ±250 kHz. Change in the ambient temperature by ±5 °C. 	

 Table 1.3.3-12
 Variable Clock Delay

*1: Measure using an oscilloscope with residual jitter of less than 200 fs (RMS).

*2: Typical value

Item	Specifications			
For NRZ input	Bit rate: 32.1 Gbit/s, 64.2 Gbit/s*1 Pattern: PRBS2 ³¹ -1 32.1 Gbits: With MU181500B, SSC with frequency of 33 kHz and deviation of 5300 ppm can be applied simultaneously with RJ with amplitude of 0.3 UI. 64.2 Gbits: With MU181500B, SSC with frequency of 33 kHz and deviation of 3300 ppm can be applied simultaneously with RJ with amplitude of 0.3 UI. These specifications are defined assuming the following conditions: Loopback connection to the MU196020A, at a constant temperature between 20 and 30 °C. When RJ+BUJ is bigger than 0.5 UIp-p or SJ + RJ + BUJ is bigger than the standard value + 0.3 UIp-p, "Overload" is displayed on the			
	The standard value + 0.3 OTP-p, Overload is displayed on the MU181500B screen. 32.1 Gbit/s 1000 $Max. modulation amplitude 1000 100 Max. modulation amplitude 1000 10$			
		Modulation Freque	ency [Hz]	
	Modulation frequency [Hz]	Max. modulation amplitude [Ulp-p]	Specification [UIp-p]	
	10	2 000	2 000	
	7 500	2 000	2 000	
	100 000	2 000	150	
	1 000 000	200	15	
	150 000 000	16	1	
	L	1		

Table 1.3.3-13 Jitter Tolerance

*1: When the Option 002 or y12 is installed.

1

Overview



Table 1.3.3-13 Jitter Tolerance (Cont'd)

ltem	Specifications			
For PAM4 input	Baud rate: 32.1 Gbaud*2, 58.2 Gbaud*1 Pattern: PRBS31Q 32.1 Gbaud: With MU181500B, SSC with frequency of 33 kHz and deviation of 5300 ppm can be applied simultaneously with RJ with amplitude of 0.3 UI. 58.2 Gbaud: With MU181500B, SSC with frequency of 33 kHz and deviation of 3300 ppm can be applied simultaneously with RJ with amplitude of 0.3 UI. 58.2 Gbaud: With MU181500B, SSC with frequency of 33 kHz and deviation of 3300 ppm can be applied simultaneously with RJ with amplitude of 0.3 UI. These specifications are defined assuming the following conditions: Loopback connection to the MU196020A, at a constant temperature between 20 and 30 °C. When RJ+BUJ is bigger than 0.5 UIp-p or SJ + RJ + BUJ is bigger than the standard value + 0.3 UIp-p, "Overload" is displayed on the MU181500B screen.			
	32.1 Gbaud	1k 10k 100k	Max. modulation amplitude Specification Max. modulation amplitude Max. m	
	Modulation frequency [Hz]	Max. modulation amplitude [Ulp-p]	Specification [UIp-p]	
	10	2 000	2 000	
	7 500	2 000	2 000	
	1 000 000	2 000	150	
	10 000 000	16	1	
	150 000 000	1	1	

Table 1.3.3-13 Jitter Tolerance (Cont'd)

*2: When the Option 001 is installed.

1

Overview



Table 1.3.3-13 Jitter Tolerance (Cont'd)

Item	Specifications*1
Operating Baud rate Setting range*2	When the Option x21 is installed. NRZ: 2.4 to 29.0 Gbit/s PAM4: 2.4 to 29.0 Gbaud When the Option x22, or x21 + y24 is installed. NRZ: 2.4 to 32.1 Gbit/s PAM4: 2.4 to 32.1 Gbit/s PAM4: 2.4 to 32.1 Gbaud When the Option x23 is installed. NRZ: 51.0 to 58.2 Gbit/s PAM4: 51.0 to 58.2 Gbaud When the Option x21 is installed. NRZ: 2.400 000 to 29.000 000 Gbit/s, 0.000 001 Gbit/s step PAM4: 2.400 000 to 29.000 000 Gbaud, 0.000 001 Gbit/s step PAM4: 2.400 000 to 32.100 000 Gbit/s, 0.000 001 Gbit/s step PAM4: 2.400 000 to 32.100 000 Gbaud, 0.000 001 Gbit/s step PAM4: 2.400 000 to 32.100 000 Gbaud, 0.000 001 Gbit/s step PAM4: 2.400 000 to 32.100 000 Gbaud, 0.000 001 Gbit/s step PAM4: 2.400 000 to 32.100 000 Gbaud, 0.000 001 Gbaud step When the Option x23 is installed. NRZ: S1.000 000 to 58.200 000 Gbit/s, 0.000 001 Gbit/s step*3 PAM4: 51.000 000 to 58.200 000 Gbit/s, 0.000 001 Gbit/s step*3
	 *1: When the Option x21, x22, x23, or y24 is installed. The Options x22 and x23 can be installed together. The Option x23 requires one of the Options x21, x22, 002 and y12. The Options x21 and x22 cannot be installed together. The Options x21 and x23 can be installed together. The Option y24 requires the Option x21. These are specified with the conditions of PRBS Pattern and Mark Ratio 1/2 (in PAM4 mode, MSB Mark Ratio 1/2) unless otherwise specified. *2: When the ED is tracking the PPG linked with MU181000A/B and MU181500B, it operates in the same ranges of bit rate and baud rate as the PPG if a recovered clock is used as a system clock. *3: Except when BERT for PCIe1-6 is selected.

Table 1.3.3-14 Clock Recovery

Item	Specifications*1			
Supported standard and	For NRZ mode			
baud rate	Standard	Bit Rate [Gbit/s]	Remarks	
	CEI-56G	56.000 000	*4	
	100G ULH	32.100 000	*5	
	PCIe5	32.000 000	*5	
	32G FC	28.050 000	*6	
	CEI-28G	28.000 000	*6	
	100G OTU4	27.952 496	*6	
	100GAUI-4	$26.562\ 500$	*6	
	50GAUI-2	26.562 500	*6	
	LAUI-2	25.781 250	*6	
	25GAUI	25.781 250	*6	
	CAUI-4 (100GbE (25.78 × 4))	25.781 250	*6	
	InfiniBand EDR	25.781 250	* 6	
	SAS4	22.500 000	*6	
	Thunderbolt2	20.625 000	*6	
	DisplayPort UHBR 20	20.000 000	*6	
	USB4 Gen3	20.000 000	* 6	
	PCIe4	16.000 000	*6	
	InfiniBand FDR	14.062 500	*6	
	16G FC	14.025 000	*6	
	DisplayPort UHBR 13.5	13.500 000	*6	
	SAS3	12.000 000	*6	
	10G FC Over FEC	11.316 800	*6	
	10GbE Over FEC	11.095 700	*6	
	OTU2	10.709 225	*6	
	G975 FEC	10.664 228	*6	
	10G FC	10.518 750	*6	
	CAUI-10 (10GbE)	10.312 500	*6	
	Thunderbolt1	10.312 500	*6	
	DisplayPort UHBR 10	10.000 000	*6	

Table 1.3.3-14	Clock Recovery (Cont'd)
----------------	-------------------------

*4: When the Option x23 is installed.

*5: When the Option x22, or x21 + y24 is installed.

*6: When the Option x21, x22, or x21 + y24 is installed.

1

Item	Specifications*1			
Supported standard and	For NRZ mode			
baud rate	Standard	Bit Rate [Gbit/s]	Remarks	
	USB4 Gen2	10.000 000	*6	
	InfiniBand QDR	10.000 000	*6	
	USB3.1 Gen2	10.000 000	*6	
	OC-192/STM-64	9.953 280	*6	
	8G FC	8.500 000	*6	
	DisplayPort HBR3	8.100 000	*6	
	PCIe3	8.000 000	*6	
	HSBI	6.250 000	*6	
	SATA 6Gb/s	6.000 000	*6	
	DisplayPort HBR2	5.400 000	*6	
	PCIe2	5.000 000	*6	
	InfiniBand DDR	$5.000\ 000$	*6	
	USB3.0	5.000 000	*6	
	4G FC	$4.250\ 000$	*6	
	XAUI	3.125 000	*6	
	OTU1	2.666 060	*6	
	InfiniBand SDR	2.500 000	*6	
	PCIe1	2.500 000	*6	
	OC-48/STM-16	2.488 320	*6	

Table 1.3.3-14 Clock Recovery (Cont'd)

1

Overview

Item	Specifications*1			
Supported standard and	For PAM4 mode			
baud rate (Cont'd)	Standard	Baud Rate [Gbaud]	Remarks	
	CEI 112G	56.000 000	\star_4	
	400GAUI-4 (400GbE (53.1 × 4))	$53.125\ 000$	*4	
	200GAUI-2	$53.125\ 000$	* 4	
	100GAUI-1	$53.125\ 000$	* 4	
	PCIe6	32.000 000	*5	
	64G FC	28.900 000	*6	
	CEI 56G	28.000 000	*6	
	400GAUI-8	$26.562\ 500$	*6	
	200GAUI-4 (200GbE (26.6 × 4))	$26.562\ 500$	*6	
	100GAUI-2	$26.562\ 500$	*6	
	50GAUI-1	$26.562\ 500$	*6	
	InfiniBand HDR	$26.562\ 500$	*6	
Maximum number of	range. When the Option x21, x22, or x21 ·	+ y24 is installed.		
consecutive zeros	72 bit Zero Substitution 2 ¹⁵ , Target loop band: 1/1667, 1/257 1/1667, 1/257	78 at 2.4 to 25.499 999 78, 1/6640 at 25.5 to 32	G, 2.1 G	
	When the Option x23 is installed. 72 bit			
	Zero Substitution 2 ¹⁵ , Target loop band: 1/6640, 1/13280 at 51.0 to 58.2G			
Lock range	When the Option x21, x22, or x21 + ±200 ppm 2.4 to 25.499 999 G, The target l 1/2578. ±100 ppm 25.5 to 32.1 G, The target loop ba	+ y24 is installed. oop band is specified b and is specified by 1/10	y 1/1667, 367, 1/2578,	
	When the Option x23 is installed. $\pm 100 \text{ ppm}$			
	51.0 to 58.2 G, The target loop band is specified by 1/6640, 1/13280.			

Table 1.3.3-14 Clock Recovery (Cont'd)

Item	Specifications*1			
Target loop band	When the Option x21, x22, or x2 25.5 to 32.1 G*7 Baud rate / 1667 Baud rate / 2578 Baud rate / 6640 Jitter Tolerance	1 + y24 is in:	stalled.	
	2.4 to 25.499 999 G Baud rate / 1667 Baud rate / 2578 Jitter Tolerance Variable			
	When Variable is selected, the Baud rate [Gbaud] R $2.400\ 000\ to\ 5.500\ 000$ $5.500\ 001\ to\ 7.500\ 000$ $7.500\ 001\ to\ 7.500\ 000$ $9.500\ 001\ to\ 10.500\ 000$ $10.500\ 001\ to\ 12.500\ 000$ $12.500\ 001\ to\ 12.500\ 000$ $14.500\ 001\ to\ 17.500\ 000$ $15.500\ 001\ to\ 17.500\ 000$ $17.500\ 001\ to\ 19.500\ 000$ $19.500\ 001\ to\ 22.500\ 000$ $22.500\ 001\ to\ 24.500\ 000$ $24.500\ 001\ to\ 25.499\ 999$ When the Option x23 is installed $51.0\ to\ 58.2\ G^{*8}$ Baud rate / 6640 Baud rate / 13280 Hence The State of	ranges are a ange [MHz] 3 3 to 4 3 to 5 3 to 6 3 to 7 3 to 8 3 to 9 3 to 10 3 to 11 3 to 12 3 to 13 3 to 14 3 to 15 4.	as follows: Step [MHz] - 1 1 1 1 1 1 1 1 1 1 1 1 1 1	

Table 1.3.3-14 Clock Recovery (Cont'd)

*7: The SSPRQ pattern supports Baud rate / 6640 only. When set to Jitter Tolerance, Baud rate / 1667 or higher.

*8: The SSPRQ pattern supports Baud rate / 6640 only. When set to Jitter Tolerance, Baud rate / 6640 or higher.
1.3 Specifications



Table 1.3.3-14 Clock Recovery (Cont'd)

*9: Loopback connection to the MU196020A, PRBS 2³¹⁻¹, specified at a constant temperature between 20 and 30 °C.

1

Chapter 1 Overview



Table 1.3.3-14 Clock Recovery (Cont'd)

*10: Loopback connection to the MU196020A, PRBS31Q, specified at a constant temperature between 20 and 30 °C.

1.3 Specifications

Item	Specifications
Dimensions	21 mm (H), 234 mm (W), 175 mm (D), Excluding protrusions
Mass	2.5 kg max.
Operating temperature	15 to 30 °C MP1900A's ambient temperature. MU196040B shall operate when installed.
Storage temperature	-20 to 60 °C MU196040B installed to MP1900A shall comply with MIL-T-28800E Class 5.

 Table 1.3.3-15
 Mechanical Performance

1

This chapter describes preparations required before using the MP1900A modules.

2.1	Installation to MP1900A	2-2
2.2	How to Operate Application	2-2
2.3	Preventing Damage	2-3

2.1 Installation to MP1900A

For information on how to install the MP1900A modules to the MP1900A and how to turn on the power, refer to Chapter 3 "Preparation before Use" in the *MP1900A Signal Quality Analyzer-R Operation Manual*.

2.2 How to Operate Application

The modules connected to the MP1900A are controlled by operating the MX190000A Signal Quality Analyzer-R Control Software (hereinafter, referred to as "MX190000A").

For information on how to start up, shut down, and operate the MX190000A, refer to the *MX190000A Signal Quality Analyzer-R Control Software Operation Manual.*

2.3 Preventing Damage

Always observe the ratings when connecting to the input and output connectors of the MP1900A modules. If an out-of-range signal is input, the MP1900A modules may be damaged.



- When signals are input to the MP1900A modules, avoid excessive voltage beyond the rating. Otherwise, the circuit may be damaged.
- When output is used at the 50 Ω GND terminator, never feed any current or input signals to the output.
- As a countermeasure against static electricity, ground other devices to be connected (including experimental circuits) with ground wires before connecting the I/O connector.
- The outer conductor and core of the coaxial cable may become charged as a capacitor. Use any metal to discharge the outer conductor and core before use.
- Never open the MP1900A modules. If you open it and MP1900A modules have failed or sufficient performance cannot be obtained, we may decline to repair the MP1900A modules.
- The MP1900A modules have many important circuits and parts including hybrid ICs. These parts are extremely sensitive to static electric charges, so never open the case of the MP1900A modules.
- The hybrid ICs used in the MP1900A modules are sealed in airtight containers; never open them. If you open it and the MP1900A modules have failed or sufficient performance cannot be obtained, we may decline to repair the MP1900A.

- To protect the MP1900A modules from electrostatic discharge failure, a conductive sheet should be placed onto the workbench, and the operator should wear an electrostatic discharge wrist strap. Always ground the wrist strap to the workbench antistatic mat or the frame ground of the MP1900A modules.
- When connecting an external device such as a Bias-T to the output connectors of MP1900A modules, if the output signal includes any DC voltage, variations in the output of the DC power supply or load may change the level of the output signal, risking damage to the internal circuits.
 - Do not connect or disconnect any external devices while DC voltage is impressed.
 - Only switch DC power sources ON and OFF when all equipment connections have been completed.

<Recommended procedure>

Measurement Preparation 1:

- 1. Connect all equipment.
- 2. Set the DC power supply output to ON.
- 3. Set the MP1900A modules output to ON and complete measurement.

Measurement Preparation 2

- 1. Set the equipment output to OFF.
- 2. Set the DC power supply output to OFF.
- 3. Disconnect the MP1900A modules, or change the DUT connections.

Since even unforeseen fluctuations in DC voltage and load (open or short circuits at the MP1900A modules output side and changes caused by using a high-frequency probe, etc.,) can damage the DUT and equipment, we recommend connecting a 50–ohm resistance in series with the DC terminal of the Bias-T to prevent risk of damage.



Do not connect/disconnect while DC voltage impressed.

Figure 2.3-1 Bias-T Connection Example

Chapter 2 Before Use

This chapter describes the panel and connectors of the MP1900A modules.

3.1	Panel	Layout	3-2
	3.1.1	MU196020A	3-2
	3.1.2	MU196040A	3-3
	3.1.3	MU196040B	3-4
3.2	Inter-M	Iodule Connection	3-5
	3.2.1	Measuring errors	3-7
	3.2.2	Measuring errors with noise added	3-8
	3.2.3	Adding jitter to output signal	3-10
	3.2.4	Synchronizing multiple channels of PPG.	3-11

3.1 Panel Layout

3.1.1 MU196020A



Figure 3.1.1-1 Panel Layout (MU196020A-x10)

No.	Name	Description		
[1]	Data Output,	Outputs differential Data and $\overline{\text{Data}}$ signals.		
	Data Output	Various interface signals can be output, depending on the installed option (s).		
		Because of differential output, be sure to terminate the unused connector with the coaxial terminator (V210).		
[2]	Gating Out	In case of Repeat: Outputs the timing signals.		
		In case of Burst: Outputs the timing signals for Burst.		
[3]	AUX In	Inputs auxiliary signals.		
		Variation: Error Injection, Burst		
[4]	AUX Out,	Outputs auxiliary signals.		
	AUX Out	Variation: 1/N Clock, Pattern Sync, Burst Output2		
		Because of differential output, be sure to terminate the unused connector with the coaxial terminator (J1632A).		
[5]	Clock Out	Outputs clock signals.		
[6]	Ext Clock In	Inputs clock signals from these units:		
		MU181000A 12.5GHz Synthesizer		
		MU181000B 12.5GHz 4 Port Synthesizer		
		MU181500B Jitter Modulation Source		
		External Synthesizer*		

Table 3.1.1-1	Connectors on Panel

*: We recommend using the MG3690C series as an external synthesizer.

For details about the MG3690C series, contact Anritsu or our sales representative.

3.1.2 MU196040A



Figure 3.1.2-1 Panel Layout (MU196040A)

No.	Name	Description
[1]	Data Input,	Input Data, $\overline{\text{Data}}$ data signals.
	Data Input	Support both differential and single-ended input signals.
[2]	AUX In	Inputs auxiliary signals.
		Variation: External Mask, Burst
[3]	AUX Out,	Outputs auxiliary signals.
	$\overline{\text{AUX}}$ Out	Variation: 1/N Clock, Pattern Sync, Sync Gain, Error Output
		Because of differential output, be sure to connect the coaxial terminator (J1632A) to unused side connector.
[4]	Ext Clock In	Inputs clock signals.
		Mainly connected to the Clock Out connector of the PAM4 PPG.

Table 3 1 2-1	Connectors	on	Panel
1 able 5.1.2-1	Connectors	011	i anei

3.1.3 MU196040B



Figure 3.1.3-1 Panel Layout (MU196040B)

No.	Name	Description
[1]	Data Input, Data Input	Input Data, Data data signals. Support both differential and single-ended input signals.
		Be sure to terminate the unused connector with the coaxial terminator (V210).
[2]	AUX In	Inputs auxiliary signals.
		Variation: External Mask, Burst, Capture External Trigger
[3]	AUX Out,	Outputs auxiliary signals.
	AUX Out	Variation: 1/N Clock, Pattern Sync, Sync Gain, Error Output
		Because of differential output, be sure to connect the coaxial terminator (J1632A) to unused side connector.
[4]	Ext Clock In	Inputs clock signals.
		Mainly connected to the Clock Out connector of the PAM4 PPG.

Table 3 1 3-1	Connectors	on	Panel
1 abie 5.1.5-1	Connectors		I allel

3.2 Inter-Module Connection

Avoid static electricity when handling the devices.

- When signals are input to this MP1900A modules, avoid excessive voltage beyond the rating. Otherwise, the circuit may be damaged.
- As a countermeasure against static electricity, ground other devices to be connected (including experimental circuits) with ground wires before connecting the I/O connector.
- The outer conductor and core of the coaxial cable may become charged as a capacitor. Use any metal to discharge the outer conductor and core before use.
- The power supply voltage rating for the MP1900A is shown on the rear panel. Be sure to operate the MP1900A within the rated voltage range. The MP1900A may be damaged if a voltage out of the rating range is applied.
- To protect the MP1900A modules from electrostatic discharge failure, a conductive sheet should be placed onto the workbench, and the operator should wear an electrostatic discharge wrist strap. Always ground the wrist strap to the workbench antistatic mat or the frame ground of the MP1900A.
- When removing a cable from a connector on the front panel of the MP1900A modules, be careful not to add excessive stress to the connector.
 Addition of excessive stress to a connector may result in characteristic degradation or a failure. Use a torque wrench (recommended torque: 0.9 N-M) when attaching or removing a cable.

The maximum data input level of MU196040A/B is 1.00 Vp-p.

When connecting the Data Output connector of MU195020A/MU183020A directly to the Data Input connector of MU196040A/B to verify operation, make sure that the data output level of MU195020A/MU183020A is 1.00 Vp-p or under.

Avoid inputting the signal exceeding the maximum input level to the Data Input connector of MU196040A/B. Failure to do so can cause damage.

3.2.1 Measuring errors

This section describes a connection example of MU196020A, MU181000B 12.5GHz 4 ports synthesizer (hereafter MU181000B), and MU196040A/B that are installed to an MP1900A.



Figure 3.2.1-1 Inter-Module Connection Example

- 1. Using a coaxial cable, connect the Clock Output connector of the MU181000B and the Ext Clock Input connector of the MU196020A.
- 2. Using a coaxial cable, connect the Clock Output connector of the MU196020A and the Ext Clock Input connector of the MU196040A/B.
- Using a coaxial cable, connect the Data Output connector of the MU196020A and the Data Input connector of the device under test (DUT). Also, using a coaxial cable, connect the Data Output connector of the MU196020A and the Data Input connector of the DUT.
- Using a coaxial cable, connect the Data Output connector of the DUT and the Data Input connector of the MU196040A/B. Also, using a coaxial cable, connect the Data Output connector of the DUT and the Data Input connector of the MU196040A/B.
- 5. Launch MX190000A, and touch **Standard BERT for PAM4** in the Application Selector screen.

Configure the module settings including bit rate, pattern and amplitude.

3.2.2 Measuring errors with noise added

This section describes a connection example of MU196020A, MU181000B, MU181500B Jitter Modulation Source (hereafter MU181500B), MU195050A, and MU196040A/B that are installed to an MP1900A. To connect MU196020A and the Data1 connector of MU195050A, use J1792A (optional accessory).



Figure 3.2.2-1 Inter-Module Connection Example

- 1. Using a coaxial cable, connect the Clock Output connector of the MU181000B and the Ext Clock Input connector of the MU196020A.
- 2. Using the J1792A skew match pair semirigid cables (V-K connector, Data Input1), connect the Data Output and \overline{Data} Output connectors of the MU196020A to the Data Input and \overline{Data} Input connectors of the MU195050A.
- Using a coaxial cable, connect the Data Output connector of the MU195050A and the Data Input connector of the device under test (DUT). Also, using a coaxial cable, connect the Data Output

connector of the MU195050A and the \overline{Data} Input connector of the DUT.

- Using a coaxial cable, connect the Data Output connector of the DUT and the Data Input connector of the MU196040A/B. Also, using a coaxial cable, connect the Data Output connector of the DUT and the Data Input connector of the MU196040A/B.
- 5. Launch MX190000A, and touch **Standard BERT for PAM4** in the Application Selector screen.

Configure the module settings including bit rate, pattern and amplitude.

6. On the **Output** tab of the MU196020A, set **Ext ATT Factor** to 3.3 dB (typ.) as the loss of the MU195050A.

3

3.2.3 Adding jitter to output signal

To add jitter to signals output from PAM4 PPG, use MU181000B and MU181500B.

Figure 3.2.3-1 shows a connection example of MU181000B, MU181500B, MU196020A, and MU196040A/B. MU196040A/B-001 supports up to 32.1 Gbit/s and 32.1 Gbaud.





Figure 3.2.3-1 Connection Example When Adding Jtter to Output Signal

- 1. Using a coaxial cable, connect the Clock Output connector of the MU181000B and the Ext Clock Input connector of the MU181500B.
- 2. Using a coaxial cable, connect the Jittered Clock Output connector of the MU181500B and the Ext Clock Input connector of the MU196020A.
- Using a coaxial cable, connect the Clock Output connector of the MU196020A and the Ext Clock Input connector of the MU196040A/B.
- 4. Using coaxial cables, connect Data Output and $\overline{\text{Data}}$ Output connectors of the MU196020A with Data Input and $\overline{\text{Data}}$ Input connectors of the MU196040A/B (2 connections).
- 5. Launch MX190000A, and touch **Standard BERT for PAM4** in the Application Selector screen.

Configure the module settings including bit rate, pattern and amplitude.

3.2.4 Synchronizing multiple channels of PPG

To synchronize multiple MU196020As installed to MP1900A, use MU181000A/B or external clock.

The following figure shows a connection example when synchronizing two units of MU196020A using MU181000B.



Figure 3.2.4-1 Connection Example When Synchronizing Two Units of PPGs

- 1. Connect two Clock Output connectors on MU181000B to the Ext Clock In connector on each MU196020A with two coaxial cables.
- Start MX190000A and select Menu → Combination Setting on the menu bar. Set Sync ON/OFF of Inter module Combination to Channel Synchronization.

Notes:

- Insert units of MU196020A into slots in order from Slot 1.
- Make sure that the cable phase difference is 10 ps or under.

The following figure shows a connection example when synchronizing four units of MU196020A using MU181000B and MU181500B.



Figure 3.2.4-2 Connection Example When Synchronizing Four Units of PPGs

- 1. Connect the Clock Output connector of MU181000B and the Ext Clock Input connector of MU181500B with a coaxial cable.
- 2 Connect one Jittered Clock Output connecter on MU181500B to the J1748A Power Splitter (1.5G-18GHz), which is an optional accessory, and the other Jittered Clock Output connector on MU181500B to other J1748A, using two coaxial cables.
- 3 Connect two J1748As to the Ext Clock In connector on four MU196020As using four coaxial cables.
- Start MX190000A and select Menu → Combination Setting on the menu bar. Set Sync ON/OFF of Inter module Combination to Channel Synchronization.

Notes:

- Insert units of MU196020A into slots in order from Slot 1.
- Make sure that the cable phase difference is 10 ps or under.

Chapter 4 Usage Examples

This chapter describes usage examples of measurement using the MP1900A modules.

4.1 Evaluating Optical Components in 400GbE Transceiver

This section explains how to evaluate optical components used in a 400GbE optical transceiver by using MU196020A and MU196040A. The optical components are as follows:

- TOSA (transmitter optical subassembly) consisting of a laser diode, driver amp, EML and other parts
- ROSA (receiver optical subassembly) consisting of a photodiode, TIA (transimpedance amplifier) and other parts

The following is the block diagram of this test that uses MP1900A, MU181000B, MU196020A and MU196040A.

If a DUT has four optical channels (lanes) as shown below, the lanes are evaluated one by one.

If four MU196020As or MU196040As are used, the four lanes can be evaluated at a time. Up to four MU196020As or MU196040As can be installed on an MP1900A. For details on the connections, refer to 3.2.4 "Synchronizing Multiple Channels of PPG".



Figure 4.1-1 Block Diagram for Optical Component Evaluation

Measurement

- 1. Connect the MP1900A and DUT to GND.
- 2. Use a coaxial connector to connect the Clock Output connector of the MU181000B and the Ext. Clock In connector of the MU196020A.
- 3. Use a coaxial connector to connect the Clock Out connector of the MU196020A and the Ext. Clock In connector of the MU196040A.
- Use coaxial cables to connect the Data Output connector and Data Output connector of the MU196020A to the Data Input connectors of the DUT (TOSA) (two connections).

MU181000B



Figure 4.1-2 Module Connection Diagram

- 5. Use coaxial cables to connect the Data Input connector and Data Input connector of the MU196040A to the Data Output connectors of the DUT (ROSA) (two connections).
- 6. Connect the DUT and the optical attenuator. Minimize the attenuation.

Test method

- 1. Connect the power cord of the MP1900A.
- 2. Turn on the MP1900A.
- 3. Turn **OFF** data output. Match MU196020A data output interface to DUT's input by adjusting the amplitude and offset on the **Output** tab.
- 4. On the **Pattern** tab of the MU196020A and MP196040A, set the pattern by selecting a test pattern.
- 5. On the **Output** tab of the MU196020A, set the operation bit rate.
- Adjust the data input interface of the MU196040A to the output interface of the DUT.
 On the Input tab of the MU196040A, select a terminal condition at the Input Condition. Since the DUT is connected by the differential interface, select Differential 100 Ohm, and then Tracking.
- Turn on the DUT.
 Be sure to turn on the MP1900A first, and then the DUT.



The DUT may be damaged if a signal line is connected or disconnected while the output is ON. Be sure to turn off the MP1900A before changing the cable connection.

- 8. On the **Output** tab of the MU196020A, set Data/XData to **ON**, and then touch the Output button at the top of the screen to turn it from grey to green (Output).
- Adjust the threshold voltage of the MU196040A.
 Touch the Auto Search module function button. Select the module and mode, and start. If the input level is low, manually adjust it.
- 10. On the **Result** tab of the MU196040A, start the measurement and check the BER measurement result.
- 11. Check that the DUT is operating normally, and then adjust the attenuation of the optical attenuator to measure the sensitivity of the DUT (ROSA).
- 12. Change the connection of TOSA and ROSA, and then repeat steps 3 to 11.

4.2 **Evaluating Devices for 400GbE Transceiver**

In the evaluation of SERDES for 400GbE transceiver, the jitter tolerance of the CDR (Clock Data Recovery) is measured. This test requires the emphasis settings to be configured in order to compensate the frequency characteristics of the transmission channel and devices. This section provides a test example with the configuration where MU196020A is installed to MP1900A.

If four MU196020As or MU196040As are used, the four lanes can be evaluated at a time. Up to four MU196020As or MU196040As can be installed on an MP1900A. For details on the connections, refer to 3.2.4 "Synchronizing Multiple Channels of PPG".



Figure 4.2-1 Block Diagram of SERDES Evaluation

Measurement

- 1. Connect the MP1900A and DUT to GND.
- 2.Use a coaxial connector to connect the Clock Output connector of the MU181000B and the Ext. Clock Input connector of the MU181500B.
- Use a coaxial connector to connect the Jittered Clock Output 3. connector of the MU181500B and the Ext. Clock In connector of the MU196020A.
- Use coaxial cables to connect the Clock Out connector of the 4. MU196020A to the Ext. Clock In connectors of the MU196040A.
- Use coaxial cables to connect the Data Output connector and Data 5.Output connector of the MU196020A to the Data Input connectors of the DUT (two connections).

Δ

Chapter 4 Usage Examples

- Use coaxial cables to connect the Data Input connector and Data Input connector of the MU196040A to the Data Output connectors of the DUT (two connections).
- To input the reference clock to the DUT, connect the Sub-rate Clock Output connector of MU181500B and the Clock Input connector of the DUT with a coaxial cable.





Test method

- 1. Connect the power cord of the MP1900A.
- 2. Turn on the MP1900A.
- Set the frequency and amplitude of the jitter to be added by MU181500B.
 To input the reference clock to the DUT, set the amplitude and
- division ratio of the Sub-rate Clock Output.
 Turn **OFF** data output. Match MU196020A data output interface to
 - DUT's input by adjusting the amplitude and offset on the **Output** tab.
- 5. On the **Output** tab of the MU196020A, set the operation bit rate to **28** Gbit/s.
- 6. On the **Pattern** tab of the MU196020A, select a test pattern.

- 7. On the **Output** tab of the MU196020A, set Data Output to **ON**, and then touch the Output button on the top of the screen to turn it from grey to green (Output).
- Adjust the threshold voltage of the MU196040A.
 Touch the Auto Search module function button. Select the module and mode, and start. If the input level is low, manually adjust it.
- 9. On the **Result** tab of the MU196040A, start the measurement, and check the BER measurement result.
- 10. On the **Emphasis** tab of the MU196020A, configure the emphasis settings.
- 11. While checking the BER measurement results of the MU196040A, edit the emphasis settings for the MU196020A so that the BER can be optimal.
- 12. While checking the BER measurement results of the MU196040A, adjust the frequency and amplitude of the jitter to be added by MU181500B so that the BER can be optimal.

Usage Examples

Chapter 5 Performance Test

This chapter describes the performance testing of the MP1900A modules.

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5.1 Timing of Performance Tests

Performance test is conducted to check that the major performance of the MP1900A modules meets the required specifications.

Conduct performance tests at acceptance inspection, operation check after repair, and periodic testing (once every six months).

5.2 Devices Required for Performance Tests

Before starting performance test, warm up the MP1900A and the measuring instruments for at least 30 minutes. Table 5.2-1 shows the required devices for performance test.

Device Name	Model	Req	uired Pe	rformance
Error detector	MP1900A +	Operating freque	ncy:	2.4 to 32.1 GHz
	MU196040A-001	NRZ Data input s	sensitivit	y:
	or			$50 \text{ mVp-p or less}^{*1}$
	MP1900A +	PAM4 Data input	t sensitiv	vity:
	MU196040B			300 mVp-p or less*2
Sampling oscilloscope		Electrical channe	el:	70 GHz or more band
Signal generator	MP1900A +	When using Ext	Clock:	
	MU196020A +	Operating freque	ncy:	1.2 to $16.05~\mathrm{GHz}$
	MU181000A/B	Output level:		300 to 1000 mVp-p
	or MG3690 series	Waveform:	Rectang	ular wave or sine wave
Electrical Length	J1789A	Bandwidth:	65 GHz,	For connecting data
Specified Coaxial Cable			signals	_
(0.4m, V connector)				
Electrical Length	J1790A	Bandwidth:	65 GHz,	For connecting data
Specified Coaxial Cable			signals	-
(0.8m, V connector)				
Coaxial Cable 0.3 m	J1624A	Bandwidth:	18 GHz,	For connecting clock
(SMA connector)			signals	
Coaxial cable 1 m	J1625A	Bandwidth:	18 GHz,	For connecting trigger
			signals	
Coaxial Attenuator	J0541E	Attenuation:	6 dB	
Precision Fixed	41V-20	Attenuation:	20 dB	
Attenuator 20 dB				
Precision Adaptor	34VFK50	For the Data Inp	ut connee	ctor of MU196040A-001
Power Meter	ML2437A or ML2438A			
Power Sensor + cable	MA2444D			

 Table 5.2-1
 Devices Required for Performance Tests

- *1: PRBS31, 26.5625 Gbit/s, 32.1 Gbit/s, when MU196040A-001 is installed.
- *2: PAM4 0/1 1/2 2/3 Level, PRBS31, Eye height where BER is 1E-06, when using External Clock, 26.5625 Gbaud, when MU196040A-001 is installed.

Note:

Before starting the performance test, warm up the device under test and the measuring instruments for at least 30 minutes, and wait until they become sufficiently stabilized unless otherwise specified.

Maximum measurement accuracy is assured under the following

conditions:

- Measurement is performed at room temperature.
- Fluctuations of AC power supply voltage are small.
- Noise, vibration, dust, and humidity are insignificant.

5.3 Performance Test Items

This section describes the following test items.

- Operating frequency range
- Waveform evaluation test
- Input level
- Pattern
- Error detection

5.3.1 Operating frequency range

(1) Specifications

Table 5.3.1-1 Specifications

Option	Specifications
MU196020A-001	2.4 to 32.1 Gbit/s (Gbaud)
MU196020A-002, y12	2.4 to 58.2 Gbit/s (Gbaud)
MU196020A-003, y23	2.4 to 64.2 Gbit/s (Gbaud)
MU196040A or	2.4 to 32.1 Gbit/s (Gbaud)
MU196040B-001	
MU196040B-002, y12	2.4 to 58.2 Gbaud
	2.4 to 64.2 Gbit/s



Figure 5.3.1-1 Connection Diagram for Operating Frequency Range Test

When using the MU181000A instead of MU181000B, attach the 6 dB Coaxial Attenuator to the Clock Output connector.

5

(3) Procedure

- 1. Mount the MU196020A onto the MP1900A, and turn on the MP1900A with the cables unconnected.
- 2. Set the modulation mode of MU196020A and MU196040A/B to **NRZ**.

[7] PAM4 PPG	NRZ	•	C: OFF				
[6] PAM4 ED	NRZ	•	C 🔘	S 🔘	E 🔘	► Start	E Stop

- 3. On the **Output** tab of the MU196020A, set **Amplitude** to 0.500 Vp-p, and **Offset** to 0.000 V and Vth.
- 4. On the **Pattern** tab of the MU196020A, set **Test Pattern** to **PRBS** and **Length** to **2^31–1**.
- 5. Turn off the MP1900A when setting the parameters completely.
- 6. Connect the measuring instrument cables as shown in Figure 5.3.1-1.
- 7. Turn on the MP1900A and the measuring instruments, and warm them up.
- 8. Enable the MP1900A signal output (ON) to output signals from the MU196020A. The signals can be tested in the range of 2.4 to 32.1 Gbit/s (Gbaud).
- 9. Adjust the phase and threshold voltage of the MU196040A/B to the optimum values.
- 10. Check that no error is detected by the MU196040A/B.
- 11. While varying the operating frequency in the following range different by model and option, check that no error has occurred in the range.

MU196040A and MU196040B-001:2.4 to 32.1 Gbit/s (Gbaud)MU196040B-002:2.4 to 64.2 Gbit/s (Gbaud)

MU196040A and MU196040B-001 do not support the test of the operating frequency exceeding 32.1 Gbit/s (Gbaud).

To check the MU196020A's performance at more than 32.1 Gbit/s when using the MU196040A and MU196040B-001, refer to 5.3.2, "Waveform Evaluation Test".
5.3.2 Waveform evaluation test

(1) Specifications

Table 5.3.2-1 Specifications for MU196020A

ltem	Conditions	Specification
Amplitude	$0.07 \text{ to } 0.70 \text{ Vp-p}^{\star_1, \star_2, \star_3, \star_4}$	$\pm 35 \text{ mV} \pm 12 \%$ of amplitude
	$0.07 \text{ to } 0.60 \text{ Vp-p}^{*5}$	
	$0.07 \text{ to } 0.55 \text{ Vp-p}^{*6}$	
Offset (Vth)	$-2.0 - \frac{\text{Amp}}{2}$ to $+3.3 - \frac{\text{Amp}}{2}$ V	$\pm 65 \text{ mV} \pm 10 \%$ of offset (Vth) \pm (Eye Amplitude Accuracy / 2)*7, *8
Cross point ^{*11}	Amplitude: 0.50 Vp-p	Fixed at 50 %
Tr/Tf^{*11}	Amplitude: 0.50 Vp-p	9.0 ps (20 to 80 %)*1, *7, *9
		8.5 ps (20 to 80 %)* $^{2, *3, *7, *9}$
		9.5 ps (20 to 80 %)*4, $*7, *9$
		8.8 ps (20 to 80 %)*5, *6, *7, *9
Jitter*10,*11,*12	Amplitude: 0.50 Vp-p	6.0 ps p-p*1, *2, *3, *4, *5, *6, *9
		600 fs rms ^{*1, *2, *3, *4, *5, *6, *9}

*1: When using the J1789A cable with MU196020A-001, at 32.1 Gbit/s

*2: When using the J1789A cable with MU196020A-002, at 58.2 Gbit/s

*3: When using the J1789A cable with MU196020A-003, at 64.2 Gbit/s

*4: When using the J1790A cable with MU196020A-001, at 32.1 Gbit/s

- *5: When using the J1790A cable with MU196020A-002, at 58.2 Gbit/s
- *6: When using the J1790A cable with MU196020A-003, at 64.2 Gbit/s
- *7: Except when **Emphasis** is turned **On** with the MU196020A-x11 installed.
- *8: For PAM4, when setting each of PAM4 Amplitude (3/2, 2/1 and 1/0) equally to 33 %.

*9: Typical value

*10: The jitter specification value is defined assuming that the oscilloscope with residual jitter less than 200 fs (RMS) is used.

*11: NRZ

*12: Count of measured jitters: 30, at a constant temperature between 20 and 30 $^{\circ}\mathrm{C}$

Chapter 5 Performance Test



Figure 5.3.2-1 Connection Diagram for Waveform Test

When using the MU181000A instead of MU181000B, attach the 6 dB Coaxial Attenuator to the Clock Output connector.

For waveform test, use a sampling oscilloscope that has a 70 GHz band and that has a residual jitter of less than 200 fs (RMS).

(3) Procedure

MU196020A-003

1. Mount the MU196020A onto the MP1900A, and turn on the MP1900A with the cables unconnected.

 $64.200\ 000$

- 2. Set the modulation mode of the MU196020A to NRZ.
- On the **Output** tab of the MU196020A, set as follows:
 Bit Rate
 MU196020A-001 32.100 000
 MU196020A-002 58.200 000

	Ext ATT Factor	0.000		
	Amplitude	0.070		
	Offset	AC OFF, 0.000, Vth		
	Half Period Jitter	0		
	Delay	0 	<u>.</u> . 1	
	cable used for connectio	n to the sampling oscillosco	name of the pe.	
4.	On the Output tab of the amplitude, offset, and c	e MU196020A, set the Data ross point to be tested.	a output	
5.	On the Pattern tab of th	ne MU196020A, set the test	pattern.	
	Since the specification p pattern observation, set	parameters are evaluated by the test pattern to PRBS, 2	y the eye 2^31–1.	
6.	Select a trigger signal to Select 1/N Clock in the A tab of the MU196020A, the sampling oscilloscop	o input to the sampling osci AUX Output dropdown list and set the division ratio a be used.	lloscope. on the Misc1 ccording to	
7.	Turn off the MP1900A v	when setting the parameter	s completely.	
8.	Connect the measuring instrument cables as shown in Figure 5.3.2-1. Be sure to connect the V210 terminators (standard accessories) to the Output connectors to which cables are not connected.			
9.	Turn on the MP1900A a warm them up.	and the measuring instrume	ents, and	
10.	Enable the MP1900A si	gnal output (ON) and outpu	ıt signals.	
11.	Measure the amplitude with the sampling oscilloscope, and record it.			
12.	On the Output tab of th Amplitude .	e MU196020A, set the valu	e for	
	When using MU19020A	-002 and J1790A cable:	0.600	
	When using MU19020A	-003 and J1790A cable:	0.550	
	Other than those above	:	0.700	
13.	Measure the amplitude record it.	with the sampling oscillosc	ope, and	
14.	On the Output tab of th	e MU196020A, set the valu	e for Offset .	
	When using MU19020A	-002 and J1790A cable:	-2.300	
	When using MU19020A	-003 and J1790A cable:	-2.275	
	Other than those above	:	-2.350	
15.	Measure the middle lev oscilloscope, and record	el of the eye with the sampl it.	ing	

16.	On the Output tab of the MU196020A, set Amplitu and Offset to 3.265.	ide to 0.070
17.	Measure the middle level of the eye with the samp oscilloscope, and record it.	ling
18.	On the Output tab of the MU190020A, set Amplitu and Offset to 0.000.	ide to 0.500
19.	Measure the cross point, Tr/Tf and jitter with the soscilloscope, and record them.	sampling
20.	Set the modulation mode of the MU196020A to $\ensuremath{\textbf{PA}}$	M4 .
21.	On the Output tab of the MU196020A, set Total Ar 0.070 and touch Even .	nplitude to
22.	Measure the amplitude with the sampling oscilloso record it.	cope, and
23.	On the Output tab of the MU196020A, set the value Amplitude .	ue for Total
	When using MU19020A-002 and J1790A cable:	0.600
	When using MU19020A-003 and J1790A cable:	0.550
	Other than those above:	0.700
24.	Measure the amplitude with the sampling oscilloso record it.	cope, and
25.	On the Output tab of the MU196020A, set the value	ue for Offset .
	When using MU19020A-002 and J1790A cable:	-2.300
	When using MU19020A-003 and J1790A cable:	-2.275
	Other than those above:	-2.350
26.	Measure the middle level of Level 2/1 with the sam oscilloscope, and record it.	npling
27.	On the Output tab of the MU196020A, set Total A 0.070 and Offset to 3.265.	mplitude to
28.	Measure the middle level of Level 2/1 with the sam oscilloscope, and record it.	npling
29.	Use a coaxial cable to connect the Data Output con MU196020A and the Input connector of the sampli oscilloscope. Be sure to connect the V210 terminate accessories) to the Output connectors to which cable connected. Repeat the procedure from steps 3 to 28	nnector of the ing ors (standard les are not 3.

5.3.3 Input level

(1) Specifications

Option	Specifications	
MU196040A-001	NRZ Input amplitude:	0.05 to 1.0 Vp-p
	PAM4 Input amplitude:	0.3 to 1.0 Vp-p
	Threshold voltage:	-3.5 to $+3.3$ V
MU196040B-001	NRZ Input amplitude:	0.05 to 1.0 Vp-p
	PAM4 Input amplitude:	0.3 to 1.0 Vp-p
	Threshold voltage:	-3.5 to $+3.3$ V
MU196040B-002,	NRZ Input amplitude (<32.1 Gbit/s):	0.05 to 1.0 Vp-p
MU196040B-001+y12	NRZ Input amplitude (>32.1 Gbit/s):	0.1 to 1.0 Vp-p
	PAM4 Input amplitude (<32.1 Gbaud):	0.3 to 1.0 Vp-p
	PAM4 Input amplitude (>32.1 Gbaud):	0.4 to 1.0 Vp-p
	Threshold voltage:	-3.5 to $+3.3$ V

(2) Connection



Figure 5.3.3-1 Connection Diagram for Input Level Test

(3) Procedure

- 1. Connect devices and configure the settings in the same manner as shown in steps 1 to 5 in Section 5.3.1.
- 2. Connect the measuring instrument cables as shown in Figure 5.3.3-1.
- 3. Turn on the MP1900A and the measuring instruments, and warm them up.
- 4. Configure the settings for the MU196020A and MU196040A/B as shown in items 1 to 4 of Table 5.3.3-2.

To perform a test at more than 32.1 Gbit/s when using the MU196040B, configure the settings as shown in items 1, 3, 5 and 6 of Table 5.3.3-2.

5. Set the output of the MU196020A to ON and touch **Start** of the MU196040A/B.

Performance Test

6.	Touch Auto Search. In the Mode list, select Fine, and then touch Start Check that the threshold voltage and phase are adjusted
	to optimum values and that no error occurs.
7.	Set the modulation mode of MU196020A and MU196040A/B to $\ensuremath{\textbf{PAM4}}$.
8.	Configure the settings for the MU196020A and MU196040A/B as shown in items 1 to 4 of Table 5.3.3-3.
	To perform a test at more than 32.1 Gbaud when using the MU196040B, configure the settings as shown in items 1, 3, 5 and 6 of Table 5.3.3-3 Also, on the Input tab of the MU196040B, in the Input Condition box, select Differential .
9.	Disconnect the cable from the Data Input connector, but leave t the Data Input connector connected. Be sure to connect the V210 terminator (standard accessory) to the Output connector of MU196020A to which a cable is not connected.
10.	On the Input tab of the MU196040A/B. set Single-Ended and

XData for **Input Condition**. Repeat steps 4 to 8 to make sure that no errors have occurred.

Table 5.3.3-2 NRZ Input Level Test Settings (MU196040A/B)

	MU196020A			MU196040A/B	
No.	Termination	Amplitude [Vp-p]	Offset (Vth) [V]	Termination	Threshold Voltage [V]*3
1	GND	0.7	-2.35	GND	-2.350
2		0.05^{*1}	-0.225^{*1}		-0.225
3		0.7	+2.95		+2.950
4		0.05^{*2}	$+0.305^{*2}$		+0.305
5		0.1	-2.05		-2.650
6		0.1	+3.25		+3.250

*1: To output a signal with an amplitude of 0.05 Vp-p and an offset of -0.225 V, connect the Precision Fixed Attenuator 20 dB (optional accessory: 41V-20) and the Precision Adaptor (optional accessory: 34VFK50) respectively to the Data Output and Data Output connectors of the MU196020A. And, set the MU196020A as follows: Amplitude: 0.5 Vp-p Offset: -2.25 V

*2: To output a signal with an amplitude of 0.05 Vp-p and an offset of +0.305 V, connect the Precision Fixed Attenuator 20 dB (optional accessory: 41V-20) and the Precision Adaptor (optional accessory: 34VFK50) respectively to the Data Output and Data Output connectors of the MU196020A. And, set the MU196020A as follows:

Amplitude:	0.5 Vp-p
Offset:	+3.05 V

*3: In the **Mode** list, select **Fine (NRZ)**, and then start Auto Search to adjust the threshold voltage and phase to optimum values.

	MU196020A				MU196040A/B
No.	Termination	Amplitude [Vp-p]	Offset (Vth) [V]	Termination	Threshold Voltage [V]*
1	GND	0.7	-2.35	GND	Upper: -2.350 + 0.233 (-2.117)
					Middle: -2.350
					Lower: $-2.350 - 0.233 (-2.583)$
2		0.3	-2.15		Upper: $-2.150 + 0.100 (-2.050)$
					Middle: -2.150
					Lower: $-2.150 - 0.100 (-2.250)$
3		0.7	+2.95		Upper: +2.950 + 0.233 (+3.183)
					Middle: +2.950
					Lower: $+2.950 - 0.233 (+2.717)$
4		0.3	+3.15		Upper: +3.150 + 0.100 (+3.250)
					Middle: +3.150
					Lower: +3.150 - 0.100 (+3.050)
5		0.4	-2.20		Upper: -2.20 + 0.133 (-2.067)
					Middle: -2.200
					Lower: -2.200 - 0.133 (-2.333)
6		0.4	+3.10		Upper: +3.100 + 0.133 (+3.333)
					Middle: +3.100
					Lower: +3.100 - 0.133 (+2.967)

Table 5.3.3-3 PAM4 Input Level Test Settings (MU196040A/B)

*: In the **Mode** list, select **Fine (PAM4)**, and then start Auto Search to adjust the threshold voltage and phase to optimum values.

Note:

When changing the termination condition, configure the settings of the MU196020A and the MU196040A/B in the following order. The MU196020A and the MU196040A/B may be damaged if the settings are configured in an incorrect order or the termination condition is not set correctly.

- (1) Set the output of the MU196020A to OFF.
- (2) Set the termination condition for the MU196040A/B to GND.
- (3) Change the termination condition for the MU196020A.
- (4) Set the termination condition for the MU196040A/B to that for the MU196020A.

5.3.4 Pattern

(1) Specifications

- PRBS pattern (NRZ, PAM4)
- Zero Substitution pattern (NRZ)
- SSPRQ pattern (PAM4)
- (2) Connection

Refer to Figure 5.3.3-1 for the device connection.

- (3) Procedure
 - 1. Configure the settings in the same manner as shown in steps 1 to 5 in Section 5.3.1.
 - 2. Connect the measuring instrument cables as shown in Figure 5.3.3-1.
 - 3. Turn on the MP1900A and the measuring instruments, and warm them up.
 - 4. Set the modulation mode of MU196020A and MU196040A/B to **NRZ**.
 - 5. Set the output of the MU196020A to ON and touch Start of the MU196040A/B. Adjust the phase as required, and check that no error occurs.
 - 6. On the **Pattern** tab of both of the MU196040A/B and the MU196020A, switch the PRBS pattern length to the following values in order, and check that no error occurs.

2^7-1, 2^9-1, 2^10-1, 2^11-1, 2^13-1, 2^15-1, 2^20-1, 2^23-1, 2^31-1.

 Set the PRBS pattern length of both MU196040A/B and MU196020A to 2^31-1. Then, check that no error occurs for the following four modulation type and logic combinations:

	Modulation Type	Logic	Logic MSB	Logic LSB
1	NRZ	POS	_	-
2	NRZ	NEG	_	
3	PAM4	_	POS	POS
4	PAM4	_	NEG	NEG

Table 5.3.4-1 Modulation Type and Logic Settings

- 8. Set the modulation mode of MU196020A and MU196040A/B to **NRZ**.
- 9. For both the MU196040A/B and the MU196020A, set the test pattern to Zero Substitution, then, switch the Length to the following values in order, and check that no error occurs.

2^7, 2^9, 2^10, 2^11, 2^15, 2^20, 2^23, 2^7-1, 2^9-1, 2^10-1, 2^11-1, 2^15-1, 2^20-1, 2^23-1.

- 10. Set the modulation mode of MU196020A and MU196040A/B to **PAM4**.
- 11. Change the test patterns of both MU196040A/B and MU196020A to SSPRQ, and check that no error occurs.

5.3.5 Error detection

(1) Specifications

MU196040A-0012.4 to 32.1 GHz,MU196040B-0012.4 to 32.1 GHz,MU196040B-0022.4 to 64.2 GHz,Accuracy±(10 ppm + 1 kHz)

(2) Connection

Refer to Figure 5.3.3-1 for the device connection.

- (3) Procedure
 - 1. Configure the settings in the same manner as shown in steps 1 to 5 in Section 5.3.1.
 - 2. Connect the measuring instrument cables as shown in Figure 5.3.3-1.
 - 3. Turn on the MP1900A and the measuring instruments, and warm them up.
 - 4. Set the frequency of the MU181000B to 10 GHz.
 - 5. Set the modulation mode of MU196020A and MU196040A/B to **NRZ**.
 - 6. Check that MU196020A is set to NRZ 20 Gbit/s, turn **ON** the Output, and then touch **Start** of the MU196040A/B. Adjust the phase as required, and check that no error occurs.
 - Turn On error insertion of the MU196020A, and make sure that the ER measurement results on the **Result** tab of the MU196040A/B match the values set on the **Error Addition** tab on the MU196020A.
 - 8. Set "Single" for error insertion of the MU196020A (set Variation to **Single** on the MU196020A **Error Addition** tab).
 - 9. In the Gating field of the **Measurement** tab of the MU196040A/B, set **Cycle** to **Single**, and set the measurement time to 10 seconds.

 Touch the Start button of the MU196040A/B. While the measurement is running for 10 seconds, touch Single once on the Error Addition tab of the MU196020A.

When the measurement has finished, check that the measurement results are as follows.

Error rate (ER):	$5.0000E{-12}$
Error count (EC):	1.0000E-00
Error free interval (%EFI):	99.9900 %
Error interval (EI):	1

This chapter describes maintenance of the MP1900A modules.

6.1	Daily Maintenance	.6-2
6.2	Cautions on Storage	.6-2
6.3	Transportation	.6-3
6.4	Calibration	.6-3

6.1 Daily Maintenance

- Wipe off any external stains with a cloth damped with diluted mild detergent.
- Vacuum away any accumulated dust or dirt with a vacuum cleaner.
- Tighten any loose parts fixed with screws, using the specified tools.

6.2 Cautions on Storage

Wipe off any dust, soil, or stain on the MP1900A modules prior to storage. Install the supplied Opens or Terminators to the connectors on the panel.

Avoid storing the MP1900A modules in any of the following locations:

- In direct sunlight for extended periods
- Outdoors
- In excessively dusty locations
- Where condensation may occur
- In liquids, such as water, oil, or organic solvents, and medical fluids, or places where these liquids may adhere
- In salty air or in place chemically active gases (sulfur dioxide, hydrogen sulfide, chlorine, ammonia, nitrogen dioxide, or hydrogen chloride etc.) are present
- Where toppling over may occur
- In the presence of lubricating oil mists
- In places at an altitude of more than 2,000 m
- In the presence of frequent vibration or mechanical shock, such as in cars, ships, or airplanes
- Under the following temperature and humidity conditions: Temperature range of ≤ -20 °C or ≥ 60 °C Humidity range of ≥ 85 %

Recommended storage conditions

In addition to the abovementioned storage cautions, the following environment conditions are recommended for long-term storage.

- Temperature range of 5 to 30 °C
- Humidity range of 40 to 75 %
- Slight daily fluctuation in temperature and humidity

6.3 Transportation

Use the original packing materials, if possible, when packing the MP1900A modules for transport. If you do not have the original packing materials, pack the MP1900A modules according to the following procedure. When handling the MP1900A modules, always wear clean gloves, and handle it gently so as not to damage it.

<Procedure>

- 1. Use a dry cloth to wipe off any stain or dust on the exterior of the MP1900A module.
- 2. Check for loose or missing screws.
- 3. Provide protection for structural protrusions and parts that can easily be deformed, and wrap the MP1900A module with a sheet of polyethylene. Finally, cover with moisture-proof paper.
- 4. Place the wrapped MP1900A module into a cardboard box, and tape the flaps with adhesive tape. Furthermore, store it in a wooden box as required by the transportation distance or method.
- 5. During transportation, place it under an environment that meets the conditions described in 6.2 "Cautions on Storage".

6.4 Calibration

Regular maintenance such as periodic inspections and calibration is essential for the Signal Quality Analyzer-R series for long-term stable performance. Regular inspection and calibration are recommended for using the Signal Quality Analyzer Series in its prime condition at all times. The recommended calibration cycle after delivery of the Signal Quality Analyzer Series is twelve months.

If you require support after delivery, contact an Anritsu Service and Sales office. Contact information can be found on the last page of the printed version of this manual, and is available in a separate file on the PDF version.

We may not provide calibration or repair if any of the following cases apply.

- Seven or more years have elapsed after production and parts for the instrument are difficult to obtain, or it is determined that reliability cannot be maintained after calibration/repair due to significant wear.
- Circuit changes, repair, or modifications are done without our approval.
- It is determined that the repair cost would be higher than the price of a new item

Chapter 7 Troubleshooting

This chapter describes how to determine if a failure has occurred when a problem occurs during the MP1900A module operation.

7.1	Problems That Occur When Replacing Modules7-2
7.2	Problems That Occur During Output Waveform
	Observation
7.3	Problems That Occur During
	Error Rate Measurement7-4
7.4	Synchronization Failures7-5

7.1 Problems That Occur When Replacing Modules

Symptom **Check Item** Remedy Reinstall the module according to 3.3 "Installing and Module Is the module(s) installed recognition failed. Removing Modules" in the MP1900A Signal Quality properly? Analyzer-R Operation Manual. Confirm the MP1900A software version and the Are the appropriate modules installed? supported modules by visiting the MP1900A Series Signal Quality Analyzers-R product information page in the Anritsu web site (https://www.anritsu.com). If the appropriate modulus are not recognized, it may have failed. Contact an Anritsu Service and Sales office. Contact information can be found on the last page of the printed version of this manual, and is available in a separate file on the PDF version.

Table 7.1-1 Remedies for Problems That Occur When Replacing MP1900A Modules

7.2 Problems That Occur During Output Waveform Observation

Symptom	Check Item	Remedy		
Output waveform cannot be monitored	Is the Data or Clock on the Output tab set to ON ?	On the Output tab, set Data or Clock to be output to ON.		
normally.		Output Emphasis Pattern Error Addition Misc1 Misc2 Output Baud Rate Variable 12.500 000 GBaud 0.000 dB Output Data ON Clock ON 0.070 Vpp When Output is OFF, turn it ON by touching the Output Output<		
		list box.		
	Is Output ON (On the top left corner of the screen, touch \rightarrow Output to turn ON .		
	Is the operating clock supplied normally?	When using the internal clock, check the bit rate setting.When the clock is supplied externally, check the connection interface. Refer to 3.1 "Panel Layout" for the interface.		
	Is the trigger clock set correctly?	It is recommended to use the signal output from the AUX Output connector as the trigger clock. Check the AUX Output connector settings and interface with the sampling oscilloscope which measures the waveforms.		
	Is the electrical interface cable loose?	Tighten the connector.		
Do the cables used have good high-frequency characteristics?Use the cables and GHz or higher freq 32.1 Gbit/s (Gbaud connectors that su frequency band.		Use the cables and connectors that support 65 GHz or higher frequency band. If the bit rate is 32.1 Gbit/s (Gbaud) or less, use the cables and connectors that support 40 GHz or higher frequency band.		

 Table 7.2-1
 Remedies for Problems That Occur During Waveform Observation

7.3 Problems That Occur During Error Rate Measurement

Symptom	Check Item	Remedy
An error occurs.	Is the connection interface with the DUT correct?	Check that the data rate, level, offset and termination conditions match those of the DUT.
	Are the logical patterns correctly set on the MU196020A and the error detector (ED)?	Check if the patterns generated by the MU196020A are set such that they can be received by the DUT, and if the set patterns generated by the DUT and detected by the ED are the same. If the DUT outputs the patterns from the MU196020A as they are, connect the MU196020A and ED directly to check if an error is detected. Prevent the bit rate (baud rate) from exceeding 32.1 Gbit/s (Gbaud) when using MU196040A or MU196040B-001.
	Is the error addition function set to off?	On the Error Addition tab, check that the Error Addition switch is set to OFF .
	Is the electrical interface cable loose?	Tighten the connector.
	Do the cables used have good high-frequency characteristics?	Use the cables and connectors that support 65 GHz or higher frequency band. If the bit rate is 32.1 Gbit/s (Gbaud) or less, use the cables and connectors that support 40 GHz or higher frequency band.
	Are sufficient phase margin and threshold margin are secured?	Adjust the phase and offset to between the MU196020A and the DUT and between the DUT and ED, respectively so that they can be optimal.

 Table 7.3-1
 Remedies for Problems That Occur During Error Rate Measurement

7.4 Synchronization Failures

Table 7.4-1 Remedies for Synchronization Failures

ltem	Check Item	Remedy	
Input conditions	Do the quality, status and length of the connection cables comply with the specifications?	 Replace the cables with appropriate ones in the following cases: Frequency characteristics are not sufficient. Loss is large. Cables and connectors are damaged. Connectors are contaminated. 	
	Is the cable connection correct and secure?	Confirm the destination and check if the connector is tightened securely.	
	Are the single and differential $(50/100 \Omega)$ inputs set correctly?	Set the correct value.	
	Is the input level correct?	Check the level by using an oscilloscope, etc.	
	Are the input bit rate and clock frequency set correctly?	Set the bit rate and clock frequency correctly. <i>Note:</i>	
		Use the frequency counter to check the current clock frequency.	
	Is the frequency set near the bit rate when using clock recovery?	Set the frequency near the bit rate to be used.	
	Has the clock loss display disappeared?	Check the data and clock signals to be input or clock recovery settings.	
Termination conditions	Was the termination potential adjusted?	Set the termination potential correctly. Note: Incorrect setting may result in unit failure.	
Clock setting conditions	Do the clock settings for PAM4 PPG and PAM4 ED match?	PAM4 PPG: On the Misc2 tab, check the settings for Output Clock Rate and Operation Baud Rate (when Clock Source is External). On the Output tab, check the setting for Baud Rate. PAM4 ED: On the Input tab, check the setting for Operation Baud Rate in the Clock area (when Selection is set to External Clock). On the Result tab, check the Clock Count or Frequency value. Note: Without properly configured clock settings, expected measurement results cannot be obtained	

Chapter 7 Troubleshooting

ltem	Check Item	Remedy	
PAM4 symbol synchronization conditions	Has symbol synchronization been established between PAM4 MSB and LSB?	In Diagnostics Mode, check that MSB/LSB Diff is 0. If it is 0, symbol synchronization has been established. If, on the Result tab of the PAM4 ED, either or both of Upper Eye Threshold and Lower Eye Threshold are set to a voltage within the range of Middle Eye Height , "" may be displayed in MSB/LSB Diff . <i>Note:</i>	
		MSB /LSB Diff must be 0 when performing symbol measurement.	
PAM4 Auto Search conditions	Has the Auto Search function failed?	In Diagnostics Mode, check that MSB/LSB Diff is within ±48. Make sure the input level is sufficient. Note:	
		MSB/LSB Diff must be within ±48 when performing Auto Search.	
PAM4 pattern conditions	Is the pattern of PAM4 MSB and LSB different?	In Diagnostics Mode, check that symbol synchronization can be established between MSB and LSB. As necessary, change the logic polarity and coding condition settings for MSB or LSB.	

 Table 7.4-1
 Remedies for Synchronization Failures (Cont'd)

Appendix A Pseudo-Random Pattern

A.1	Pseudo-Random Pattern	A-2
A.2	Zero-Substitution Pattern	A-3

A.1 Pseudo-Random Pattern

Table A.1-1 shows the principle of pseudo-random pattern generation. A pseudo-random pattern is expressed in an N-th degree generating polynomial, with one cycle of 2ⁿ-1. For a PRBS pattern with a cycle of 2ⁿ-1, a pattern of successive "1s" for the number N is generated once in a cycle.

For the output level of the PRBS pattern, "1" indicates the low level and "0" indicates the high level when Logic is set to POS (positive).

The mark ratios of the PRBS pattern are generated as shown in the block diagrams of Table A.1-1.

Cycle	Generating Polynomial	Pattern Generation Block Diagram		
27-1	$1 + X^6 + X^7$	1 - 2 - 3 - 4 - 5 - 6 + 7 + Output		
29-1	$1 + X^5 + X^9$	↓ +1+2+3+4+5+6+7+8+9++>Output		
210-1	$1 + X^7 + X^{10}$	↓ 1 - 2 - 3 - 4 7 - 8 - 9 - 10 -> Output		
211-1	$1 + X^9 + X^{11}$	↓1-2-3-4-5-6-7-8-9+10-11+> Output		
$2^{13}-1$	$1 + X + X^2 + X^{12} + X^{13}$	→1→2→3-410-11-12+13+> Output		
$2^{15}-1$	$1 + X^{14} + X^{15}$	1-2-3-413-14+15+> Output		
$2^{20}-1$	$1 + X^3 + X^{20}$	↓ 1-2-3+4-517-18-19-20+> Output		
$2^{23}-1$	$1 + X^{18} + X^{23}$	↓ 1 - 2 - 3 16 - 17 - 18 + 19 - 20 - 21 - 22 - 23 → Output		
$2^{31}-1$	$1 + X^{28} + X^{31}$	↓ 1 - 2 - 3		
		N : Shift register (N=1, 2, 3) ⊕: Exclusive OR		

 Table A.1-1
 Principle of Pseudo-Random Pattern Generation

A.2 Zero-Substitution Pattern

A string of successive "0s" for the number of set bits is made by substituting "0" for the pattern that follows the longest bit string of successive 0s in a PRBS pattern. In this event, if the bit immediately after the bit substituted to "0" is also "0", it is inverted to "1".

Example: For a PRBS pattern with a cycle of 2⁷, the largest number of successive 0s is 6 bits (7 – 1), and zero substitution starts from the following position:





Appendix B lists the factory default settings for MU196020A, MU196040A, and MU196040B.

To initialize all settings, select $\textbf{Menu} \rightarrow \textbf{Initialize}.$

B.1	MU196020A		
	B.1.1	PAM4	B-2
	B.1.2	NRZ	B-8
B.2	MU196	6040A	B-13
	B.2.1	PAM4	B-13
	B.2.2	NRZ	B-18
B.3	MU196	6040B	B-23
	B.3.1	PAM4	B-23
	B.3.2	NRZ	В-30

B.1 MU196020A

B.1.1 PAM4

Main Item	Secondary Item	Tertiary Item	Default
Baud Rate			Variable
	Baud Rate		12.500 000 Gbaud
Output	Data		ON
	Clock		ON
Level Guard			OFF
	Level Guard Setup	Total Amplitude	0.800 V
		Offset Max(Voh)	3.300 V
		Offset Min(Vol)	-2.800 V
(PAM4 pattern settings)		Offset switching	AC OFF
		Total Amplitude	0.500 Vp-p
		Upper Eye Ratio	33.400 %
		Level2 Voltage	0.083 V
		Offset	0.000 V
		Level1 Voltage	-0.083 V
		Lower Eye Ratio	33.400 %
		External ATT Factor	0.000 dB
Half Period Jitter			0
Cable for Data Output		J1789A 0.4m Cable (Recommend)	
Delay			0 mUI
		Calibration	_
	Jitter Input		OFF
	Relative		0 mUI

Table B.1.1-1 Output Tab

Main Item	Secondary Item	Tertiary Item	Default
Manual Setting	Emphasis		Off
	Standard/Preset	Standard/Preset	
			De-Emphasis
			Preset0
Graph	Total Amplitude		0.500 Vp-p
	Upper Eye		33.400 %
	Lower Eye		33.400 %
	Pre	Cursor2	0.000 dB
		Cursor1	0.000 dB
	Post	Cursor1	0.000 dB
	Coefficient	C-2	0.000 000
		C-1	0.000 000
		СО	1.000 000
		C1	0.000 000
Channel Emulator	Channel Emulator Channel Emulator Function		OFF
	Response		Normal
	Graph Mode		Freq. Domain
	Gain Adjust		1 GHz
ISI	ISI Function	ISI Function	
	Standard/Interface		User
	Loss Channel		Not Specified
	Graph Mode		Freq. Domain
	Multi Point Mode		1point
	Tuning NF Insertion L	088	4.0 dB
	Tuning 1/2 NF Insertio	n Loss	2.0 dB

Table B.1.1-2 Emphasis Tab

Table B.1.1-3 Pattern Tab				
Main Item	Secondary Item	Tertiary Item	Default	
Test Pattern			All List	
	PRBS	Length	2^15-1	
		PRBS Inv MSB	ON	
		PRBS Inv LSB	ON	
		Gray Coder	ON	
		Pre Coder	OFF	
		Logic MSB	POS	
		Logic LSB	POS	
		Bit Shift	0	
	Data	Length	4 bits	
		Gray Coder	ON	
		Pre Coder	OFF	
		Logic MSB	POS	
		Logic LSB	POS	
		Bit Shift	0	
	Data Editor	Data Length	4 bits	
		Format	Hex(Byte)	
		Edit Mode	Overwrite	
		Cursor Addr	0x0000000	
	PRBS23Q,	PRBS Inv MSB	ON	
	PRBS31Q,	PRBS Inv LSB	ON	
	PRBS31Q (Infiniband),	Gray Coder	ON	
	PRBS31Q	Pre Coder	OFF	
	(Fibre Channel)	Logic MSB	POS	
		Logic LSB	POS	
		Bit Shift	0	

Main Item	Secondary Item	Tertiary Item	Default	
Test Pattern				
	PRBS13Q,	PRBS Inv MSB	OFF	
	QPRBS13-CEI,	PRBS Inv LSB	OFF	
	QPRBS31-CEI,	Gray Coder	ON	
	PRBS13Q (Infiniband)	Pre Coder	OFF	
		Logic MSB	POS	
		Logic LSB	POS	
		Bit Shift	0	
	QPRBS13	Seed	Lane 0	
		Gray Coder	ON	
		Pre Coder	ON	
		Logic MSB	POS	
		Logic LSB	POS	
		Bit Shift	0	
	SSPRQ, JP03A,	Logic MSB	POS	
	JP03B, Square Wave,	Logic LSB	POS	
	Transmitter Linearity	Bit Shift	0	
	RS-FEC Scrambled	Gray Coder	ON	
	Idle 50G 1Lane,	Pre Coder	OFF	
	RS-FEC Scrambled Idle 100G 1Lanes,	Logic MSB	POS	
		Logic LSB	POS	
	Scrambled Idle 100G 1Lanes	Bit Shift	0	
	RS-FEC Scrambled	Lane	0	
	Idle 100G 2Lanes,	Gray Coder	ON	
	RS-FEC Scrambled	Pre Coder	OFF	
	Idle 200G 2Lanes,	Logic MSB	POS	
	Idle 200G 4L anos	Logic LSB	POS	
	RS-FEC Scrambled Idle 400G 4Lanes,	Bit Shift	0	
	RS-FEC Scrambled Idle 400G 8Lanes			

 Table B.1.1-3
 Pattern Tab (Cont'd)

Appendix Appendix B

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			
	CP in 1b/1b Encoding	Gray Coder	ON
	for PCIe6	Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Seed	Lane 0
	MCP in 1b/1b	Gray Coder	ON
	Encoding for PCIe6	Pre Coder	ON
		Logic MSB	POS
		Logic LSB	POS
		Seed	Lane 0
		SRIS	OFF
		SKP	SKPx1
		EIEOS	ON
	Jitter Mesurement Pattern in 1b/1b Encoding for PCIe6	Logic MSB	POS
		Logic LSB	POS
	High Swing Toggle Pattern in 1b/1b Encoding for PCIe6		
	Low Swing Toggle Pattern 1b/1b Encoding for PCIe6		
	Jitter Calibration Pattern for PCIe6		
	Preset Calibration Pattern for PCIe6		

Table B.1.1-3	Pattern Tab	(Cont'd)
	i attorn i as	(00111 0)

Main Item	Secondary Item	Tertiary Item	Default
Error Addition			OFF
	Error Addition Mode		Bit Error on MSB
	Bit Error on MSB	Symbol/Burst	Symbol
		Source	Internal
		Variation	Repeat
		Rate	1E3
		Burst Length	1 Symbols

Table B.1.1-4 Error Addition Tab

Table B.1.1-5 Misc1 Tab

Main Item	Secondary Item	Tertiary Item	Default
Pattern Sequence			Repeat
	Gating Output		ON
	Repeat	Pulse Width	256 symbols
		Delay	0 symbols
AUX Input			Error Injection
		Vth	0V
AUX Output			1/N Clock
	1/N Clock	(Divide ratio)	1/64 Clock
	Pattern Sync	Position	1 symbols

Table B.1.1-6 Misc2 Tab

Main Item	Secondary Item	Tertiary Item	Default
Clock Setting	Clock Source		Unit1:Slot4:MU181500B* $_1$
	Baud Rate		$Variable^{*1}$
		Baud Rate	$12.500\ 000\ { m GBaud}^{*1}$
		$Offset^{*1}$	0 ppm
	Output Clock Rate		Halfrate
	Reference Clock*1		Internal
	Operation Bit Rate*2		2.40 – 32.10 GBaud

*1: When the MX190000A is started as Standard BERT for PAM4.

*2: When the MX190000A is started as Expert BERT.

B.1.2 NRZ

Table B.1.2-1Output Tab

Main Item	Secondary Item	Tertiary Item	Default
Bitrate			Variable
	Bitrate		12.500 000 Gbit/s
Output	Data		ON
	Clock		ON
Level Guard			OFF
	Level Guard Setup	Amplitude	0.800 V
		Offset Max(Voh)	3.300 V
		Offset Min(Vol)	-2.800 V
(NRZ pattern		Amplitude	0.500 Vp-p
settings)			
		Offset switching	AC OFF
		Offset	0.000 V
		Offset Position	Vth
		External ATT Factor	0.000 dB
Half Period Jitter			0
Cable for Data Output			J1789A 0.4m Cable
			(Recommend)
Delay			0 mUI
		Calibration	_
	Jitter Input		OFF
	Relative		0 mUI

Main Item	Secondary Item	Tertiary Item	Default
Manual Setting	Emphasis Function	Emphasis Function	
	Standard/Preset		USER
			De-Emphasis
			Preset0
Graph	Amplitude		0.500 Vp-p
	Pre	Cursor2	0.000 dB
		Cursor1	0.000 dB
	Post	Cursor1	0.000 dB
	Coefficient	C-2	0.000 000
		C-1	0.000 000
		СО	1.000 000
		C1	0.000 000
Channel Emulator	Channel Emulator Fun	nction	OFF
	Response		Normal
	Graph Mode		Freq. Domain
	Gain Adjust		1 GHz
ISI	ISI Function		OFF
	Standard/Interface		User
	Loss Channel		Not Specified
	Graph Mode	Graph Mode	
	Multi Point Mode Tuning NF Insertion Loss Tuning 1/2 NF Insertion Loss		1point
			4.0 dB
			2.0 dB

Table B.1.2-2 Emphasis Tab

Table B.1.2-3 Pattern Tab			
Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			All List
	PRBS	Length	2^15-1
		Mark Ratio	1/2
		Logic	POS
	Zero Substitution	Length	2^15
		Zero Substitution Length	1 bits
		Additional Bit	1
		Logic	POS
	Data	Length	2
		Logic	POS
	Data Editor	Data Length	2
		Format	Hex(Byte)
		Edit Mode	Overwrite
		Cursor Addr	0x0000000
	SSPR	Logic	POS
	RS-FEC Scrambled Idle 25G 1Lane	Logic	POS
	RS-FEC Scrambled Idle 50G 2Lanes, RS-FEC Scrambled Idle 100G 4Lanes, RS-FEC Scrambled Idle 100G 4Lanes RS(544,514)	Lane	0
		Logic	POS
	CP in 8b/10b	Seed	Lane 0
	Encoding for PCIe1	Delay Symbol	OFF
	CP in 8b/10b Encoding for PCIe2	SKP	SKPx1
	MCP in 8b/10b	Seed	Lane 0
	Encoding for PCIe1	Delay Symbol	OFF
	MCP in 8b/10b Encoding for PCIe2	SKP	No SKP
	CP in 128b/130b	Preset	PO
	Encoding for PCIe3 CP in 128b/130b Encoding for PCIe4 CP in 128b/130b Encoding for PCIe7	SKP	No SKP

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			
	MCP in 128b/130b	SRIS	OFF
	Encoding for PCIe3	SKP	SKPx1
	MCP in 128b/130b Encoding for PCIe4	EIEOS	ON
	MCP in 128b/130b	SRIS	OFF
	Encoding for PCIe5	SKP	SKPx1
		EIEOS	ON
		Pre Coder	ON
	Jitter Calibration Pattern for PCIe1	Logic	POS
	Preset Calibration Pattern for PCIe1		
	Jitter Calibration Pattern for PCIe2		
	Preset Calibration Pattern for PCIe2		
	Jitter Calibration Pattern for PCIe3		
	Preset Calibration Pattern for PCIe3		
	Jitter Calibration Pattern for PCIe4		
	Preset Calibration Pattern for PCIe4		
	Jitter Calibration Pattern for PCIe5		
	Preset Calibration Pattern for PCIe5		

Table B 1 2-5	Error Addition	Tah
Table D. 1.2-5		Tab

Main Item	Secondary Item	Tertiary Item	Default
Error Addition			OFF
	Error Addition Mode		Bit Error
	Bit Error	Bit/Burst	Bit
		Source	Internal
		Variation	Repeat
		Route	Select
		Rate	1E–3
		Burst Length	1 bits

Main Item	Secondary Item	Tertiary Item	Default	
Pattern Sequence			Repeat	
	Gating Output		ON	
	Repeat	Pulse Width	256 bits	
		Delay	0 bits	
	Burst	Source	Internal	
		Data Sequence	Restart	
		Enable Period	128 000 bits	
		Burst Cycle	128 000 000 bits	
		Delay	0 bits	
		Pulse Width	128 000 bits	
AUX Input	·	·	Error Injection	
		Vth	0V	
AUX Output			1/N Clock	
	1/N Clock	(Divide ratio)	1/64 Clock	
	Pattern Sync	Position	1 bits	

Table B.1.2-6 Misc1 Tab

Table B.1.2-7 Misc2 Tab

Main Item	Secondary Item	Tertiary Item	Default
Clock Setting	Clock Source		Unit1:Slot4:MU181500B* 1
	Bit Rate		$Variable^{*1}$
		Baud Rate	$12.500\ 000\ { m Gbit/s^{*1}}$
		$Offset^{*1}$	0 ppm
	Output Clock Rate		Halfrate
	Reference Clock*1		Internal
	Operation Bit Rate*2		2.40 – 32.10 Gbit/s

*1: When the MX190000A is started as Standard BERT for PAM4.

*2: When the MX190000A is started as Expert BERT.
B.2 MU196040A

B.2.1 PAM4

Main Item	Secondary Item	Tertiary Item	Default
Switch of setting items	Setting display format	Setting display format	
	Input	Upper Eye Threshold	0.095 V
		Middle Eye Threshold	0.000 V
		Lower Eye Threshold	-0.095 V
		UL Threshold	ON
		Delay	0 mUI
	Gating	Cycle	Repeat
		Unit	Time
		Time	0 day 00:00:01
		Current	ON
		Calculation	Progressive
		Interval	100 ms
	Condition	EI/EFI Interval	100 ms
		Bit Mask (Block Window)	OFF
	Auto Sync	Auto Sync	ON
		Threshold	INT
	Sync Control	Frame Length	64 symbols
		Frame Position	1 symbols
Time display format			Date&Time
Error/Alarm display	Details		OFF
	Zoom		OFF

Table B.2.1-1 Result Tab

Main Item	Secondary Item	Tertiary Item	Default
Gating	Cycle		Repeat
	Unit		Time
		Time	0 day 00:00:01
		Clock Count	>E+10
		Error Count	>E+10
	Current		ON
		Calculation	Progressive
		Interval	100 ms
Auto Sync	Auto Sync		ON
	Threshold		INT
Sync Control	Frame Length		64 symbols
	Frame Position		1 symbols
	Mask		All 00
Error/Alarm Condition	EI/EFI Interval		100 ms

Table B.2.1-3 Pattern Tab

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			All List
	PRBS	Length	2^15-1
		PRBS Inv MSB	ON
		PRBS Inv LSB	ON
		Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
	Data	Length	4
		Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
	Data Editor	Data Length	4
		Format	Hex(Byte)
		Edit Mode	Overwrite
		Cursor Addr	0x0000000

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			
	PRBS23Q,	PRBS Inv MSB	ON
	PRBS31Q,	PRBS Inv LSB	ON
	PRBS31Q (Infiniband),	Gray Coder	ON
	PRBS31Q	Pre Coder	OFF
	(Fibre Channel)	Logic MSB	POS
		Logic LSB	POS
	PRBS13Q,	PRBS Inv MSB	OFF
	QPRBS13-CEI,	PRBS Inv LSB	OFF
	QPRBS31-CEI,	Gray Coder	ON
	PRBS13Q (Infiniband)	Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
	QPRBS13	Seed	Lane 0
		Gray Coder	ON
		Pre Coder	ON
		Logic MSB	POS
		Logic LSB	POS
	SSPRQ, JP03A,	Logic MSB	POS
	JP03B, Square Wave,	Logic LSB	POS
	Transmitter Linearity		
Mask	Bit Mask (Block Windo	ow)	OFF
	External Mask		OFF

 Table B.1.2-3
 Pattern Tab (Cont'd)

B-15

Main Item	Secondary Item	Tertiary Item	Default
Data	Input Condition	l	Single-Ended
		Single-Ended	Data
		Differential 500hm	Independent
		Differential 1000hm	Independent
	Termination		GND
	Data	Upper Eye Threshold	0.165 V
		Middle Eye Threshold	0.000 V
		Lower Eye Threshold	–0.165 V
	XData	Upper Eye Threshold	0.165 V
		Middle Eye Threshold	0.000 V
		Lower Eye Threshold	–0.165 V
	UL Threshold		ON
		Differential Selection	Data-XData
		Threshold	0.000 V
Clock	Selection		External Clock
	Operation Baud Rate		$2.40-16.05~\mathrm{GBaud}$
	Input Clock Freq.		$2.40-16.05~\mathrm{GHz}$
			(1/1 Clock)
	Delay		0 mUI
		Relative	0 mUI
		Jitter Input	OFF
Measurement Restart	Data Threshold		OFF
	Clock Delay		OFF

Table	B.2.1-4	Input	Tab
1 4010		mpat	1 00

Table B.2.1-5 Capture Tab

Main Item	Secondary Item	Tertiary Item	Default
Acquisition			Bit Pattern
Condition			
	Number of Block		128
	Condition	Trigger	
	Trigger		Match Pattern
		Position	Тор
	Match Pattern Length		4 bits
	Format		HEX
	Math Pattern		0
	Mask Pattern		0

Main Item	Secondary Item	Tertiary Item	Default	
Pattern Sequence			Repeat	
	Source		External -Enable	
AUX Input			External Mask	
		Vth	0V	
AUX Output			1/N Clock	
	1/N Clock	(Divide ratio)	1/64 Clock	
	Pattern Sync	Position	1 symbols	

Table B.2.1-6 Misc1 Tab

B.2.2 NRZ

Main Item	Secondary Item	Tertiary Item	Default
Switch of setting items	Setting display format		Gating
	Input	Data Threshold	0.000 V
		XData Threshold	_
		Differential Selection	Data-XData
		Threshold	-
		Delay	0 mUI
	Gating	Cycle	Repeat
		Unit	Time
		Time	0 day 00:00:01
		Current	ON
		Calculation	Progressive
		Interval	100 ms
	Condition	Error Detection	Insertion/Omission
		EI/EFI Interval	100 ms
		Bit Mask (Block Window)	OFF
		Lane Mask (Bit Window)	OFF
	Auto Sync	Auto Sync	ON
		Threshold	INT
	Sync Control	Frame Length	64 bits
		Frame Position	1 bit
Result display format			Error/Alarm
Time display format			Date&Time
Error/Alarm display	Zoom		OFF
	All Channel		OFF

Table B.2.2-1 Result Tab

Main Item	Secondary Item	Tertiary Item	Default
Gating	Cycle	·	Repeat
	Unit		Time
		Time	0 day 00:00:01
		Clock Count	>E+10
		Error Count	>E+10
	Current		ON
		Calculation	Progressive
		Interval	100 ms
Auto Sync	Auto Sync		ON
	Threshold		INT
Sync Control	Frame Length		64 bits
	Frame Position		1 bit
	Mask		All 00
Error/Alarm Condition	Error Detection		Insertion/Omission
	EI/EFI Interval		100 ms

Table B.2.2-2Measurement Tab

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			All List
	PRBS	Length	2^15-1
		Mark Ratio	1/2
		Logic	POS
	Zero Substitution	Length	2^15
		Zero Substitution Length	1 bits
		Additional Bit	1
		Logic	POS
	Data	Length	2
		Logic	POS
	Data Editor	Data Length	2
		Format	Hex(Byte)
		Edit Mode	Overwrite
		Cursor Addr	0x0000000
	SSPR	Logic	POS
Mask	Bit Mask (Block Wind	Bit Mask (Block Window)	
	Lane Mask (Bit Wind	Lane Mask (Bit Window)	
	External Mask		OFF

Table B.2.2-3 Pattern Tab

Main Item	Secondary Item	Tertiary Item	Default
Data	Input Condition		Single-Ended
		Single-Ended	Data
		Differential 500hm	Independent
		Differential 1000hm	Independent
	Data Threshold		0.000 V
	Termination		GND
		Variable	0.000 V
	XData Threshold		0.000 V
	Differential Selection		Data-XData
	Threshold		0.000 V
Clock	Selection		External Clock
	Operation Bitrate		2.40 – 16.05 GBit/s
	Input Clock Freq.		$2.40 - 16.05 \; \mathrm{GHz}$
			(1/1 Clock)
	Delay		0 mUI
		Relative	0 mUI
		Jitter Input	OFF
Measurement Restart	Data Threshold		OFF
	Clock Delay		OFF

Table B.2.2-4 Input Tab

Table B.2.2-5	Capture	Tab
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Main Item	Secondary Item	Tertiary Item	Default
Acquisition			Bit Pattern
Condition			
	Number of Block		128
	Condition	Trigger	
	Trigger		Match Pattern
		Position	Тор
	Match Pattern Length		4 bits
	Format		HEX
	Match Pattern		0
	Mask Pattern		0

Main Item	Secondary Item	Tertiary Item	Default
Pattern Sequence		•	Repeat
	Burst	Source	External -Enable
		Delay	0 bits
		Enable Period	128 000 bits
		Burst Cycle	128 000 000 bits
		Auto/Manual	Manual
AUX Input			External Mask
		Vth	0V
AUX Output			1/N Clock
	1/N Clock	(Divide ratio)	1/64 Clock
	Pattern Sync	Position	1 bits

Table	B.2.2-6	Misc1	Tab
IUNIC		1011301	IUN

B.3 MU196040B

B.3.1 PAM4

Main Item	Secondary Item	Tertiary Item	Default
Switch of setting items	Setting display format		Gating
	Input	Upper Eye Threshold	$0.095~\mathrm{V}$
		Middle Eye Threshold	0.000 V
		Lower Eye Threshold	-0.095 V
		U/L Threshold Sync	ON
		Low Frequency	OFF
		Equalizer	0.000 dB
		DFE	OFF
			0
		Delay	0 mUI
	Gating	Cycle	Repeat
		Unit	Time
		Time	0 day 00:00:01
		Current	ON
		Calculation	Progressive
		Interval	100 ms
	Condition	EI/EFI Interval	100 ms
		Bit Mask (Block Window)	OFF
	Auto Sync	Auto Sync	ON
		Threshold	INT
	Sync Control	Frame Length	64 symbols
		Frame Position	1 symbol
	RS-FEC Symbol	Preset	Variable
		Measurement Condition	Intermittent Error Detect
		Codeword Length	544
		FEC Symbol Length	10
		FEC Symbol Error Threshold	16
Time display format			Date&Time
Error/Alarm display	Details		OFF
	Zoom		OFF

Table B.3.1-1 Result Tab

Main Item	Secondary Item	Tertiary Item	Default
Gating	Cycle	•	Repeat
	Unit		Time
		Time	0 day 00:00:01
		Clock Count	>E+10
		Error Count	>E+10
	Current		ON
		Calculation	Progressive
		Interval	100 ms
Auto Sync	Auto Sync		ON
	Threshold		INT
Sync Control	Frame Length		64 symbols
	Frame Position		1 symbol
	Mask		00 00 00 00 00 00 00 00
Error/Alarm Condition	EI/EFI Interval		100 ms
Measurement Restart	Data Threshold		OFF
	Clock Delay		OFF

Table B.3.1-3Pattern Tab

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			All List
	PRBS	Length	2^15-1
		PRBS Inv MSB	ON
		PRBS Inv LSB	ON
		Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Input Signal Decoder	OFF
	Data	Length	4
		Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Input Signal Decoder	OFF

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern (Cont'd)			
	Data Editor	Data Length	4
		Format	Hex(Byte)
		Edit Mode	Overwrite
		Cursor Addr	0x00000000
	PRBS23Q,	PRBS Inv MSB	ON
	PRBS31Q,	PRBS Inv LSB	ON
	PRBS31Q (Infiniband),	Gray Coder	ON
	PRBS31Q	Pre Coder	OFF
	(Fibre Channel)	Logic MSB	POS
		Logic LSB	POS
		Input Signal Decoder	OFF
	PRBS13Q,	PRBS Inv MSB	OFF
	QPRBS13-CEI,	PRBS Inv LSB	OFF
	QPRBS31-CEI,	Gray Coder	ON
	PRBS13Q (Infiniband)	Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Input Signal Decoder	OFF
	QPRBS13	Seed	Lane 0
		Gray Coder	ON
		Pre Coder	ON
		Logic MSB	POS
		Logic LSB	POS
	SSPRQ, JP03A,	Logic MSB	POS
	JP03B, Square Wave,	Logic LSB	POS
	Transmitter Linearity	Input Signal Decoder	OFF

 Table B.3.1-3
 Pattern Tab (Cont'd)

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern (Cont'd)		1	
	RS-FEC Scrambled	Gray Coder	OFF
	Idle 50G 1Lane,	Pre Coder	OFF
	RS-FEC Scrambled	Logic MSB	POS
	Idle 100G 1Lanes,	Logic LSB	POS
	RS-FEC-Int	Input Signal Decoder	ON
	1Lanes	Inverse Gray Coder	ON
	Hanos	Pre-Code Remover	OFF
	RS-FEC Scrambled	Lane	0
	Idle 100G 2Lanes,	Gray Coder	OFF
	RS-FEC Scrambled	Pre Coder	OFF
	Idle 200G 2Lanes,	Logic MSB	POS
	RS-FEC Scrambled	Logic LSB	POS
	RS-FFC Scrambled	Input Signal Decoder	ON
	Idle 400G 4Lanes.	Inverse Gray Coder	ON
	RS-FEC Scrambled Idle 400G 8Lanes	Pre-Code Remover	OFF
	CP in 1b/1b Encoding	Gray Coder	ON
	for PCIe6	Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Seed	Lane 0
		SKP OS Filtering	ON
	MCP in 1b/1b	Gray Coder	ON
	Encoding for PCIe6	Pre Coder	ON
		Logic MSB	POS
		Logic LSB	POS
		Seed	Lane 0
		SRIS	OFF
		SKP	SKPx1
		EIEOS	ON
		SKP OS Filtering	ON
Mask	Bit Mask (Block Window)	OFF	
	External Mask		OFF

|--|

Main Item	Secondary Item	Tertiary Item	Default
Data	Input Condition	Input Condition	
		Single-Ended	Data
		Differential 500hm	Independent
		Differential 1000hm	Independent
	Termination		GND
	Data	Upper Eye Threshold	$0.095~\mathrm{V}$
		Middle Eye Threshold	0.000 V
		Lower Eye Threshold	-0.095 V
	XData	Upper Eye Threshold	0.095 V
		Middle Eye Threshold	0.000 V
		Lower Eye Threshold	-0.095 V
	UL Threshold		ON
		Differential Selection	Data-XData
		Threshold	0.000 V
Equalizer	Low Frequency Equalizer		OFF
		Data	0.000 dB
	Decision Feedback Equalizer		OFF
		Data	0
Clock	Selection	Selection	
	Operation Baud Rate	Operation Baud Rate	
			Auto*2
	Input Clock Freq.		1.20 – 16.05 GHz (1/2 Clock)*1
			1.20 – 32.1 GHz (1/2 Clock)*2
	Delay		0 mUI
		Relative	0 mUI
		Jitter Input	OFF

Table B.3.1-4	Input Tab
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*1: When MU196040B-001 is installed.

*2: When MU196040B-002 or MU196040B-y12 is installed.

Main Item	Secondary Item	Tertiary Item	Default
Capture Mode	Capture Mode		Sync Mode Capture
-	-	State	
Capture Result Display	Auto Launch		Capture Data
Condition	·		
	Number of Blocks		128
	Capture Area		After the Trigger
	Trigger		Match Pattern
	Match Pattern Length	Match Pattern Length	
	Notation		Symbol(PAM4)
	Match Pattern		00 00
	Mask		00 00

Table	B.3.1-5	Capture Tab	
Table	D.0.1-0		

Table B.3.1-6 Misc1 Tab

Main Item	Secondary Item	Tertiary Item	Default
Pattern Sequence			Repeat
	Source		External-Enable
AUX Input			External Mask
		Vth	0V
AUX Output			1/N Clock
	1/N Clock	(Divide ratio)	1/64 Clock
	Pattern Sync	Position	1 symbols

Main Item	Secondary Item	Tertiary Item	Default
BER/SER Logging	Logging		OFF
	Cycle		00:00:05
	ER (Symbol)		OFF
	ER (Bit)		OFF
	ER (MSB)		OFF
	ER (LSB)		OFF
	EC (Symbol)		OFF
	EC (Bit)		OFF
	EC (MSB)		OFF
	EC (LSB)		OFF
	Clock Loss		OFF
	Sync Loss		OFF

Table B.3.1-7 Logging Tab

B.3.2 NRZ

Main Item	Secondary Item	Tertiary Item	Default
Switch of setting	Setting display format	Setting display format	
items	Input	Data Threshold	0.000 V
		XData Threshold	-
		Differential Selection	Data-XData
		Threshold	-
		Delay	0 mUI
		LFE	OFF
			0.000 dB
		DFE	OFF
			0
	Gating	Cycle	Repeat
		Unit	Time
		Time	0 day 00:00:01
		Current	ON
		Calculation	Progressive
		Interval	100 ms
	Condition	Error Detection	Insertion/Omission
		EI/EFI Interval	100 ms
		Bit Mask (Block Window)	OFF
		Lane Mask (Bit Window)	OFF
	Auto Sync	Auto Sync	ON
		Threshold	INT
	Sync Control	Frame Length	64 bits
		Frame Position	1 bit
	RS-FEC Symbol	Preset	Variable
		Measurement Condition	Intermittent Error Detect
		Codeword Length	528
		FEC Symbol Length	10
		FEC Symbol Error Threshold	8
Result display format	1	1	Error/Alarm
Time display format			Date&Time
Error/Alarm display	Zoom		OFF
Litoiniai in dispidy	Show in Window		OFF

Table B.3.2-1 Result Tab

Main Item	Secondary Item	Tertiary Item	Default
Gating	Cycle		Repeat
	Unit		Time
		Time	0 day 00:00:01
		Clock Count	>E+10
		Error Count	>E+10
	Current		ON
		Calculation	Progressive
		Interval	100 ms
Auto Sync	Auto Sync		ON
	Threshold		INT
Sync Control	Frame Length		64 bits
	Frame Position		1 bit
	Mask		All 00
Error/Alarm Condition	Error Detection		Insertion/Omission
	EI/EFI Interval		100 ms
Measurement Restart	Data Threshold		OFF
	Clock Delay		OFF

Table B.3.2-2	Measurement Tab

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			All List
	PRBS	Length	2^15-1
		Mark Ratio	1/2
		Logic	POS
	Zero Substitution	Length	2^15
		Zero Substitution Length	1 bits
		Additional Bit	1
		Logic	POS
	Data	Length	2
		Logic	POS
	Data Editor	Data Length	2
		Format	Hex(Byte)
		Edit Mode	Overwrite
		Cursor Addr	0x0000000
	SSPR	Logic	POS
	RS-FEC Scrambled Idle 25G 1Lane	Logic	POS
	RS-FEC Scrambled Idle 50G 2Lanes RS(544,514),	Lane	0
		Logic	POS
	RS-FEC Scrambled		
	Idle 100G 4Lanes,		
	Idle 100G 4Lanes RS(544,514)		
	CP in 8b/10b	Seed	Lane 0
	Encoding for PCIe1	Delay Symbol	OFF
	CP in 8b/10b	SKP	SKPx1
	Encoding for PCIe2	SKP OS Filtering	ON
	MCP in 8b/10b	Seed	Lane 0
	Encoding for PCIe1	Delay Symbol	OFF
	MCP in 8b/10b	SKP	No SKP
	Encoding for PCIe2	SKP OS Filtering	ON

Table B 3 2-3 Pattern Tab

Appendix B List of Default Settings

Main Item	Secondary Item	Tertiary Item	Default			
Test Pattern						
	CP in 128b/130b	Preset	P0			
	Encoding for PCIe3	SKP	No SKP			
	CP in 128b/130b Encoding for PCIe4	SKP OS Filtering	OFF			
	CP in 128b/130b Encoding for PCIe5					
	MCP in 128b/130b	SRIS	OFF			
	Encoding for PCIe3 MCP in 128b/130b Encoding for PCIe4 MCP in 128b/130b Encoding for PCIe5	SKP	SKPx1			
		EIEOS	ON			
		SKP OS Filtering	ON			
		SRIS	OFF			
		SKP	SKPx1			
		EIEOS	ON			
		Pre Coder	ON			
		SKP OS Filtering	ON			
Mask	Bit Mask (Block Window)		OFF			
	Lane Mask (Bit Windo	Lane Mask (Bit Window)				
	External Mask		OFF			

Main Item	Secondary Item	Tertiary Item	Default
Data	Input Condition		Single-Ended
		Single-Ended	Data
		Differential 500hm	Independent
		Differential 1000hm	Independent
	Data Threshold		0.000 V
	Termination		GND
		Variable	0.000 V
	XData Threshold		0.000 V
	Differential Selection	Data-XData	
	Threshold		0.000 V
Equalizer	Low Frequency Equaliz	zer	OFF
		Data	0.000 dB
	Decision Feedback Equalizer		OFF
		Data	0
Clock	Selection		External Clock
	Operation Bitrate		$2.40 - 32.10 \text{ Gbit/s}^{*1}$
			Auto*2
	Input Clock Freq.		$1.20-16.05 \text{ GHz} (1/2 \text{ Clock})^{*1}$
			1.20–32.1 GHz (1/2 Clock)*2
	Delay		0 mUI
		Relative	0 mUI
		Jitter Input	OFF

Table B.3.2-4	Input Tab

*1: When MU196040B-001 is installed.

*2: When MU196040B-002 or MU196040B-y12 is installed.

Main Item	Secondary Item	Tertiary Item	Default
Capture Mode	Capture Mode		Sync Mode Capture
		State	
Capture Result Display	Auto Launch		Capture Data
Condition			
	Number of Blocks		128
	Capture Area		After The Trigger
	Trigger	Trigger	
	Match Pattern Length	Match Pattern Length	
	Notation	Notation	
	Match Pattern	Match Pattern	
	Mask		0000

Table B.3.2-5 Capture Tab

Table B.3.2-6 Misc1 Tab

Main Item	Secondary Item	Tertiary Item	Default
Pattern Sequence			Repeat
	Burst	Source	External -Enable
		Delay	0 bits
		Enable Period	128 000 bits
		Burst Cycle	12 800 000 bits
		Auto/Manual	Manual
AUX Input			External Mask
		Vth	0V
AUX Output			1/N Clock
	1/N Clock	(Divide ratio)	1/64 Clock
	Pattern Sync	Position	1 bits

Main Itom	Secondary Item	Tortiary Itom	Default
	Secondary Item	Tertiary item	Delault
BER/SER Logging	Logging		OFF
	Cycle		00:00:05
	ER (Total)		OFF
	ER (INS)		OFF
	ER (OMI)		OFF
	EC (Total)		OFF
	EC (INS)		OFF
	EC (OMI)		OFF
	Clock Loss		OFF
	Sync Loss		OFF

Table	B.3.2-7	Logging	Tab
lanc	D.J.Z-1	Logging	1 ab

Appendix C Performance Test Record Sheet

C.1 Performance Test Result Sheet

Document number:			
Test Location:			
Date:			
Test person in charge:			
Product name:			
Serial number:			
Software version:			
Option:			
Power voltage:	V		
Power frequency:	Hz		
Ambient temperature	°C		
Relative humidity	%		
Instruments used: Model na	me	Serial number	
<u>Model na</u>	me	Serial number	
<u>Model na</u>	me	Serial number	
<u>Model na</u>	me	Serial number	
Remarks			

C.2 MU196020A

C.2.1 MU196020A-001

Table C.2.1-1 Operating Frequency Range

Specification		Results	
Specification	Data	Data	
No errors occur within the range from 2.4 to 32.1 Gbit/s.*			
No errors occur within the range from 2.4 to 32.1 Gbaud.*			

*: Pattern PRBS, 2^31–1

Table C.2.1-2 MU196020A-001 Waveform Evaluation Test- Amplitude (NRZ)

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (Vp-p)	Upper Limit (Vp-p)	Data	Data
32.1 Gbit/s	0.70	0.581	0.819		
	0.07	0.027	0.113		

Table C.2.1-3 MU196020A-001 Waveform Evaluation Test- 0/3 Level Amplitude (PAM4)

Settings		Specification		Results	
Baud rate	Amplitude (Vp-p)	Lower Limit (Vp-p)	Upper Limit (Vp-p)	Data	Data
32.1 Gbaud	0.70	0.581	0.819		
	0.07	0.027	0.113		

Table C.2.1-4 MU196020A-001 Waveform Evaluation Test- Offset (NRZ)

Settings		Specification		Results	
Bit rate	Offset (Vth)	Lower Limit (V)	Upper Limit (V)	Data	Data
32.1 Gbit/s	3.265	2.817	3.713		
	-2.35	-2.590	-2.111		

Settings		Specification		Results	
Baud rate	Offset (Vth)	Lower Limit (V)	Upper Limit (V)	Data	Data
32.1 Gbaud	3.265	2.817	3.713		
	-2.35	-2.590	-2.111		

Table C.2.1-5 MU196020A-001 Waveform Evaluation Test- Offset (PAM4)

Table C.2.1-6	MU196020A-001	Waveform	Evaluation	Test-Cross	point (NI	RZ)
---------------	---------------	----------	-------------------	-------------------	-----------	-----

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (%)	Upper Limit (%)	Data	Data
32.1 Gbit/s	0.50	40	60		

Table C.2.1-7	MU196020A-001 Waveform Evaluation Test- Tr/Tf (NRZ)

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (ps)	Upper Limit (ps)	Data	Data
32.1 Gbit/s	0.50	—	9.0^{*1}		
		_	9.5^{*2}		

*1: When J1789A cables are used.

*2: When J1790A cables are used.

Table C.2.1-8 MU196020A-001 Waveform Evaluation Test- Jitter (NRZ)

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (ps)	Upper Limit (ps p-p)	Data	Data
32.1 Gbit/s	0.50	_	6.0		

C.2.2 MU196020A-002

Table C.2.2-1	Operating	Frequency	Range
---------------	-----------	-----------	-------

Specification		Results	
Specification	Data	Data	
No errors occur within the range from 2.4 to 32.1 Gbit/s.*			
No errors occur within the range from 2.4 to 32.1 Gbaud.*			

*: Pattern PRBS, 2^31–1

Table C 2 2-2	MI 1196020A-002 Wayoform Evaluation Tost- Amplitudo (NP7	١.
Table C.2.2-2	MU196020A-002 Waveform Evaluation Test- Amplitude (NRZ))

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (Vp-p)	Upper Limit (Vp-p)	Data	Data
58.2 Gbit/s	0.70^{*1}	0.581	0.819		
	0.60^{*2}	0.493	0.707		
	0.07	0.027	0.113		

- *1: When J1789A cables are used.
- *2: When J1790A cables are used.

Table C.2.2-3	MU196020A-002 Waveform Evaluation Test-0/3 Level
	Amplitude (PAM4)

Settings		Specification		Results	
Baud rate	Amplitude (Vp-p)	Lower Limit (Vp-p)	Upper Limit (Vp-p)	Data	Data
58.2 Gbaud	0.70*1	0.581	0.819		
	0.60^{*2}	0.493	0.707		
	0.07	0.027	0.113		

- *1: When J1789A cables are used.
- *2: When J1790A cables are used.

Fable C.2.2-4	MU196020A-002 Waveform	Evaluation Test	Offset (NRZ)
---------------	------------------------	------------------------	--------------

Settings		Specification		Results	
Bit rate	Offset (Vth)	Lower Limit (V)	Upper Limit (V)	Data	Data
58.2 Gbit/s	3.265	2.817	3.713		
	-2.30^{*1}	-2.489	-2.112		
	-2.35^{*2}	-2.590	-2.111		

*1: When J1790A cables are used, Amplitude 0.60 Vp-p

*2: When J1789A cables are used, Amplitude 0.70 Vp-p

Settings		Specification		Results	
Baud rate	Offset (Vth)	Lower Limit (V)	Upper Limit (V)	Data	Data
58.2 Gbaud	3.265	2.817	3.713		
	-2.30^{*1}	-2.489	-2.112		
	-2.35^{*2}	-2.590	-2.111		

Table C.2.2-5 MU196020A-002 Waveform Evaluation Test- Offset (PAM4)

*1: When J1790A cables are used, Amplitude 0.60 Vp-p

*2: When J1789A cables are used, Amplitude 0.70 Vp-p

Table C.2.2-6 MU196020A-002 Waveform Evaluation Test- Cross point (NRZ)

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (%)	Upper Limit (%)	Data	Data
58.2 Gbit/s	0.50	40	60		

Table C.2.2-7 MU196020A-002 Waveform Evaluation Test- Tr/Tf (NRZ)

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (ps)	Upper Limit (ps)	Data	Data
58.2 Gbit/s	0.50	_	8.5^{*1}		
		_	8.8^{*2}		

- *1: When J1789A cables are used.
- *2: When J1790A cables are used.

Table C.2.2-8	MU196020A-002 Waveform Evaluation Test- Jitter (NR	Z)
		-,

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (ps)	Upper Limit (ps p-p)	Data	Data
58.2 Gbit/s	0.50	_	6.0		

Appendix Appendix C

C.2.3 MU196020A-003

Table C.2.3-1 Operating Frequency Range

Specification		ults
Specification	Data	Data
No errors occur within the range from 2.4 to 32.1 Gbit/s.*		
No errors occur within the range from 2.4 to 32.1 Gbaud.*		

*: Pattern PRBS, 2^31–1

Table C 2 3-2	MU196020A_003 Wayoform Evaluation Tost- Amplitudo (NPZ)	•
Table C.2.3-2	WO 196020A-003 Waveform Evaluation Test- Amplitude (NRZ)	

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (Vp-p)	Upper Limit (Vp-p)	Data	Data
64.2 Gbit/s	0.70^{*1}	0.581	0.819		
	0.55^{*2}	0.405	0.595		
	0.07	0.027	0.113		

- *1: When J1789A cables are used.
- *2: When J1790A cables are used.

Table C.2.3-3	MU196020A-003 Waveform Evaluation Test-0/3 Level
	Amplitude (PAM4)

Settings		Specification		Results	
Baud rate	Amplitude (Vp-p)	Lower Limit (Vp-p)	Upper Limit (Vp-p)	Data	Data
64.2 Gbaud	0.70*1	0.581	0.819		
	0.55^{*2}	0.405	0.595		
	0.07	0.027	0.113		

- *1: When J1789A cables are used.
- *2: When J1790A cables are used.

	Fable C.2.3-4	MU196020A-003 Waveform Evaluation Test- Offset (NRZ)
--	---------------	--	------

Settings		Specifi	cation	Results	
Bit rate	Offset (Vth)	Lower Limit (V)	ower Limit Upper Limit (V) (V)		Data
64.2 Gbit/s	3.265	2.817	3.713		
	-2.275^{*1}	-2.438	-2.112		
	-2.35^{*2}	-2.590	-2.111		

*1: When J1790A cables are used, Amplitude 0.55 Vp-p

*2: When J1789A cables are used, Amplitude 0.70 Vp-p

Settings		Specif	Specification		Results	
Baud rate	Offset (Vth)	Lower Limit (V) (V)		Data	Data	
64.2 Gbaud	3.265	2.817	3.713			
	-2.275^{*1}	-2.438	-2.112			
	-2.35^{*2}	-2.590	-2.111			

Table C.2.3-5 MU196020A-003 Waveform Evaluation Test- Offset (PAM4)

*1: When J1790A cables are used, Amplitude 0.55 Vp-p

*2: When J1789A cables are used, Amplitude 0.70 Vp-p

Table C.2.3-6 MU196020A-003 Waveform Evaluation Test - Cross point (NRZ)

Settings		Specifi	cation	Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (%)	Upper Limit (%)	Data	Data
64.2 Gbit/s	0.50	40	60		

Table C.2.3-7 MU196020A-003 Waveform Evaluation Test - Tr/Tf (NRZ)

Settings		Specif	Specification		Results	
Bit rate	it rate Amplitude Lower (Vp-p) (p		Upper Limit (ps)	Data	Data	
64.2 Gbit/s	0.50	_	8.5^{*1}			
		_	8.8^{*2}			

*1: When J1789A cables are used.

*2: When J1790A cables are used.

Table C.2.3-8	MU196020A-003 Waveform Evaluation Test- Jitter (NR	Z)
---------------	--	------------

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit Upper Limit (ps) (ps p-p)		Data	Data
64.2 Gbit/s	0.50	_	6.0		

C.3 MU196040A

		Setting		Baa	ulto		
MU196020A MU196040A					Specification	Results	
Termi nation	Amplitude (Vp-p)	Offset (Vth) (V)	Termi nation	Threshold Voltage (V)		Data	Data
GND	0.7	-2.35	GND	-2.350	No errors		
	0.05	-0.225		-0.225	occur.		
	0.7	+2.95		+2.950			
	0.05	+0.305		+0.305			

Table C.3-1 Input Level Range (NRZ)

					(1 / 111 /)		
		Setting		Dee			
	MU196020	DA MU196040A		IU196040A	Specification	Results	
Termi nation	Amplitude (Vp-p)	Offset (Vth) (V)	Termi Threshold nation Voltage (V)		opeeneation	Data	Data
GND	0.7	-2.35	GND	Upper: -2.117	No errors		
				Middle: -2.350	occur.		
				Lower: -2.583			
	0.3	-2.15		Upper: -2.050			
				Middle: -2.150			
				Lower: -2.250			
	0.7	+2.95		Upper: 3.183			
				Middle: 2.950			
				Lower: 2.717			
	0.3	+3.15		Upper: 3.250			
				Middle: 3.150			
				Lower: 3.050			

Table C.3-2 Input Level Range (PAM4)

C.3 MU196040A

	Sett	ings	_	Dee			
MU19	6020A	MU19	6040A	Specification	Results		
Length	Logic	Length	Logic		Data	Data	
2^7-1	POS	2^7-1	POS	No errors			
2^9-1	POS	2^9-1	POS	occur.			
2^11-1	POS	2^11-1	POS				
2^13-1	POS	2^13-1	POS				
2^15-1	POS	2^15-1	POS				
2^20-1	POS	2^20-1	POS				
2^23-1	POS	2^23-1	POS				
2^31-1	POS	2^31-1	POS				
2^31-1	NEG	2^31-1	NEG				

Table C.3-3 Test Pattern (PRBS-NRZ)

Table C.3-4	Test Pattern	(PRBS-PAM4)
-------------	--------------	-------------

		Sett	ings		Dec			
M	MU196020A MU19		MU196040A		Specification	Res	suits	
Length	Logic MSB	Logic LSB	Length	Logic MSB	Logic LSB		Data	Data
2^7-1	POS	POS	2^7-1	POS	POS	No errors		
2^9-1	POS	POS	2^9-1	POS	POS	occur.		
2^11-1	POS	POS	2^11-1	POS	POS			
2^15-1	POS	POS	2^15-1	POS	POS			
2^20-1	POS	POS	2^20-1	POS	POS			
2^23-1	POS	POS	2^23-1	POS	POS			
2^31-1	POS	POS	2^31-1	POS	POS			
2^31-1	NEG	NEG	2^31-1	NEG	NEG			

	Sett	ings			Dee	
MU19	6020A	MU19	6040A	Specification	Results	
Length	Logic	Length	Logic		Data	Data
2^7	POS	2^{7}	POS	No errors		
2^9	POS	2^9	POS	occur.		
2^10	POS	2^10	POS			
2^11	POS	2^11	POS			
2^15	POS	2^{15}	POS			
2^20	POS	2^20	POS			
2^{2}	POS	2^23	POS			
2^7-1	POS	2^7-1	POS			
2^9-1	POS	2^9-1	POS			
2^10-1	POS	2^10-1	POS			
2^11-1	POS	2^11-1	POS			
2^15-1	POS	2^15-1	POS			
2^20-1	POS	2^20-1	POS]		
2^23-1	POS	2^23-1	POS			

Table C.3-5 Test Pattern (Zero Substitution-NRZ)

Table C.3-6 Test Pattern (SSPRQ-PAM4)

	Sett	ings		Poculto		
MU19	MU196020A MU19604			Specification	Results	
Pattern	Logic	Pattern	Logic		Data	Data
SSPRQ	POS	SSPRQ	POS	No errors occur.		

Table C.3-7 Error Detection

ltom	Specification	Results	
Item	Specification	Data	Data
Error rate (ER)	5.0000E-12		
Error count (EC)	1.0000E-00		
Error free interval (%EFI)	99.9900%		
Error interval (EI)	1		

C.4 MU196040B

Settings						Bee	
MU196020A MU196040B				Specification	Results		
Termi nation	Amplitude (Vp-p)	Offset (Vth) (V)	Termi nation	Threshold Voltage (V)	opeoneouten	Data	Data
GND	0.7	-2.35	GND	-2.350	No errors		
	0.05	-0.225		-0.225	occur.		
	0.7	+2.95		+2.950			
	0.05	+0.305		+0.305			

Table C.4-1 Input Level Range (NRZ ≤32.1 Gbit/s)

Table C.4-2 In	put Level Range (NRZ >32.1 Gbit/s)	

Settings						Results	
MU196020A MU196040B				Specification			
Termi nation	Amplitude (Vp-p)	Offset (Vth) (V)	Termi nation	Threshold Voltage (V)		Data	Data
GND	0.7	-2.35	GND	-2.350	No errors		
	0.1	-2.05		-2.050	occur.		
	0.7	+2.95		+2.950			
	0.1	+3.25		+3.250			

Appendix C Performance Test Record Sheet

	Settings					Posulte	
MU196020A			MU196040B		Specification	Results	
Termi nation	Amplitude (Vp-p)	Offset (Vth) (V)	Termi nation	Threshold Voltage (V)		Data	Data
GND	0.7	-2.35	GND	Upper: -2.117	No errors		
				Middle: -2.350	occur.		
	-			Lower: -2.583	-		
	0.3	-2.15		Upper: -2.050			
				Middle: -2.150			
				Lower: -2.250			
	0.7	+2.95		Upper: 3.183			
				Middle: 2.950			
				Lower: 2.717			
	0.3	+3.15		Upper: 3.250			
				Middle: 3.150			
				Lower: 3.050			

Table C.4-3	Input Level Range (PAM4 ≤32.1	Gbaud

Table C 4-4	Input Level Range	(PAM4 >32 1	Gbaud)
	input Level Mange		Obauu)

Settings						Bosulte	
MU196020A			MU196040B		Specification	Results	
Termi nation	Amplitude (Vp-p)	Offset (Vth) (V)	Termi nation	Threshold Voltage (V)	opcontration	Data	Data
GND	0.7	-2.35	GND	Upper: -2.117	No errors		
				Middle: -2.350	occur.		
				Lower: -2.583			
	0.4	-2.20		Upper: -2.067			
				Middle: -2.200			
				Lower: -2.333			
	0.7	+2.95		Upper: 3.183			
				Middle: 2.950			
				Lower: 2.717			
	0.4	+3.10]	Upper: 3.233			
				Middle: 3.100			
				Lower: 2.967			
C.4 MU196040B

	Sett	ings		Desults		
MU19	6020A	MU19	6040B	Specification	Res	suits
Length	Logic	Length	Logic		Data	Data
2^7-1	POS	2^7-1	POS	No errors		
2^9-1	POS	2^9-1	POS	occur.		
2^11-1	POS	2^11-1	POS			
2^13-1	POS	2^13-1	POS			
2^15-1	POS	2^15-1	POS			
2^20-1	POS	2^20-1	POS			
2^23-1	POS	2^23-1	POS			
2^31-1	POS	2^31-1	POS			
2^31-1	NEG	2^31-1	NEG			

Table C.4-5 Test Pattern (PRBS-NRZ)

Table C.4-6	Test Pattern	(PRBS-PAM4)
-------------	--------------	-------------

		Sett	ings			Decul		
м	IU196020	Α	м	U196040	В	Specification	Res	SUITS
Length	Logic MSB	Logic LSB	Length	Logic MSB	Logic LSB		Data	Data
2^7-1	POS	POS	2^7-1	POS	POS	No errors		
2^9-1	POS	POS	2^9-1	POS	POS	occur.		
2^11-1	POS	POS	2^11-1	POS	POS			
2^{15-1}	POS	POS	2^{15-1}	POS	POS			
2^20-1	POS	POS	2^20-1	POS	POS			
2^23-1	POS	POS	2^23-1	POS	POS			
2^31-1	POS	POS	2^31-1	POS	POS			
2^31-1	NEG	NEG	2^31-1	NEG	NEG			

Appendix C Performance Test Record Sheet

	Set	ings		Dec		
MU19	6020A	MU19	6040B	Specification	Res	uits
Length	Logic	Length	Logic		Data	Data
2^7	POS	2^7	POS	No errors		
2^9	POS	2^9	POS	occur.		
2^10	POS	2^10	POS			
2^11	POS	2^11	POS			
2^15	POS	2^15	POS			
2^20	POS	2^20	POS			
2^23	POS	2^23	POS			
2^7-1	POS	2^7-1	POS			
2^9-1	POS	2^9-1	POS			
2^10-1	POS	2^10-1	POS			
2^11-1	POS	2^11-1	POS			
2^15-1	POS	2^15-1	POS]		
2^20-1	POS	2^20-1	POS]		
2^23-1	POS	2^23-1	POS			

Table C.4-7 Test Pattern (Zero Substitution -NRZ)

Table C.4-8 Test Pattern (SSPRQ-PAM4)

Settings					Populto	
MU196020A		MU196040B		Specification	Results	
Pattern	Logic	Pattern	Logic		Data	Data
SSPRQ	POS	SSPRQ	POS	No errors occur.		

Table C.4-9 Error Detection

lterr	Creation	Results	
Item	Specification	Data	Data
Error rate (ER)	5.0000E-12		
Error count (EC)	1.0000E-00		
Error free interval (%EFI)	99.9900%		
Error interval (EI)	1		

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