MP1900A Signal Quality Analyzer-R Plug-in Module Operation Manual

24th Edition

- **For safety and warning information, please read this manual before attempting to use the equipment.**
- **Additional safety and warning information is provided within the MP1900A Signal Quality Analyzer-R Operation Manual. Please also refer to it before using the equipment.**
- **Keep this manual with the equipment.**

ANRITSU CORPORATION

Document No.: M-W3976AE-24.0

Safety Symbols

To prevent the risk of personal injury or loss related to equipment malfunction, ANRITSU CORPORATION uses the following safety symbols to indicate safety-related information. Ensure that you clearly understand the meanings of the symbols BEFORE using the equipment. Some or all of the following symbols may be used on all Anritsu equipment. In addition, there may be other labels attached to products that are not shown in the diagrams in this manual.

Symbols used in manual

⚠ DANGER This indicates a very dangerous procedure that could result in serious injury or death if not performed properly.

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Safety Symbols Used on Equipment and in Manual

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This indicates a prohibited operation. The prohibited operation is indicated symbolically in or near the barred circle.



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This indicates a warning or caution. The contents are indicated symbolically in or near the triangle.



This indicates a note. The contents are described in the box.





These indicate that the marked part should be recycled.

MP1900A Signal Quality Analyzer-R
Plug-in Module
Operation Manual

1 December 2018 (First Edition)
12 August 2026 (24th Edition)

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- In places where high-intensity static electric charges or electromagnetic fields are present
- In places where abnormal power voltages (high or low) or instantaneous power failures occur
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ANRITSU CORPORATION Contact

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Revision History:

February 29th, 2020
December 17th, 2021
March 11th, 2024

CE Conformity Marking

Anritsu affixes the CE conformity marking on the following products in accordance with the Decision 768/2008/EC to indicate that they conform to the EMC, LVD and RoHS directive of the European Union (EU).

CE marking

1. Product Model

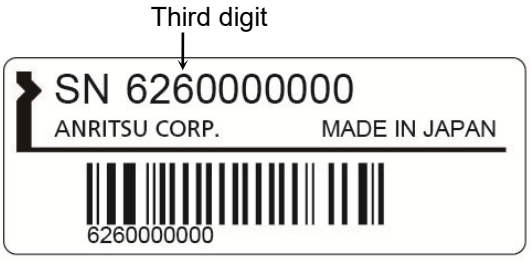
Plug-in Units:
- MU191000A Synthesizer
- MU195020A 21G/32G bit/s SI PPG
- MU195040A 21G/32G bit/s SI ED
- MU195050A Noise Generator PG
- MU196020A PAM4 PPG
- MU196020C PAM4 PPG
- MU196040B PAM4 ED
- MU196050B Noise Generator
- MU196060A 32G baud NRZ/PAM4 Re-Driver

2. Applied Directive and Standards

When the MU191000A Synthesizer, MU195020A 21G/32G bit/s SI PPG, MU195040A 21G/32G bit/s SI ED, MU195050A Noise Generator PG, MU196020A PAM4 PPG, MU196020C PAM4 PPG, MU196040B PAM4 ED, MU196050B Noise Generator and MU196060A 32G baud NRZ/PAM4 Re-Driver are installed in the MP1900A, the applied directive and standards of this unit conform to those of the MP1900A main frame.

PS: About main frame
Please contact Anritsu for the latest information on the main frame types that MU191000A, MU195020A, MU195040A, MU195050A, MU196020A, MU196020C, MU196040B, MU196050B and MU196060A can be used with.

If the third digit of the serial number is "7", the product complies with Directive 2011/65/EU as amended by (EU) 2015/863.
(Pb,Cd,Cr6+,Hg,PBB,PBDE,DEHP,BBP,DBP,DIBP)
If the third digit of the serial number is "6", the product complies with Directive 2011/65/EU.
(Pb,Cd,Cr6+,Hg,PBB,PBDE)



Serial number example

UKCA Marking

Anritsu affixes the UKCA marking on the following products in accordance with the guidance to indicate that they conform to the EMC, LVD, and RoHS regulations in the United Kingdom.

UKCA marking

1. Product Model

Plug-in Units: MU191000A Synthesizer
MU195020A 21G/32G bit/s SI PPG
MU195040A 21G/32G bit/s SI ED
MU195050A Noise Generator PG
MU196020A PAM4 PPG
MU196020C PAM4 PPG
MU196040B PAM4 ED
MU196050B Noise Generator
MU196060A 32G baud NRZ/PAM4 Re-Driver

2. Applied Regulations and Standards

When the MU191000A Synthesizer, MU195020A 21G/32G bit/s SI PPG, MU195040A 21G/32G bit/s SI ED, MU195050A Noise Generator PG, MU196020A PAM4 PPG, MU196020C PAM4 PPG, MU196040B PAM4 ED, MU196050B Noise Generator and MU196060A 32G baud NRZ/PAM4 Re-Driver are installed in the MP1900A, the applied regulations and standards of this unit conform to those of the MP1900A main frame.

PS: About main frame
Please contact Anritsu for the latest information on the main frame types that MU191000A, MU195020A, MU195040A, MU195050A, MU196020A, MU196020C, MU196040B, MU196050B and MU196060A can be used with.

RCM Conformity Marking

Anritsu affixes the RCM mark on the following products in accordance with the regulation to indicate that they conform to the EMC framework of Australia/New Zealand.

RCM marking



1. Product Model

Plug-in Units: MU191000A Synthesizer
MU195020A 21G/32G bit/s SI PPG
MU195040A 21G/32G bit/s SI ED
MU195050A Noise Generator PG
MU196020A PAM4 PPG
MU196020C PAM4 PPG
MU196040B PAM4 ED
MU196050B Noise Generator
MU196060A 32G baud NRZ/PAM4 Re-Driver

2. Applied Standards

When the MU191000A Synthesizer, MU195020A 21G/32G bit/s SI PPG, MU195040A 21G/32G bit/s SI ED, MU195050A Noise Generator PG, MU196020A PAM4 PPG, MU196020C PAM4 PPG, MU196040B PAM4 ED, MU196050B Noise Generator and MU196060A 32G baud NRZ/PAM4 Re-Driver are installed in the MP1900A, the applied directive and standards of this unit conform to those of the MP1900A main frame.

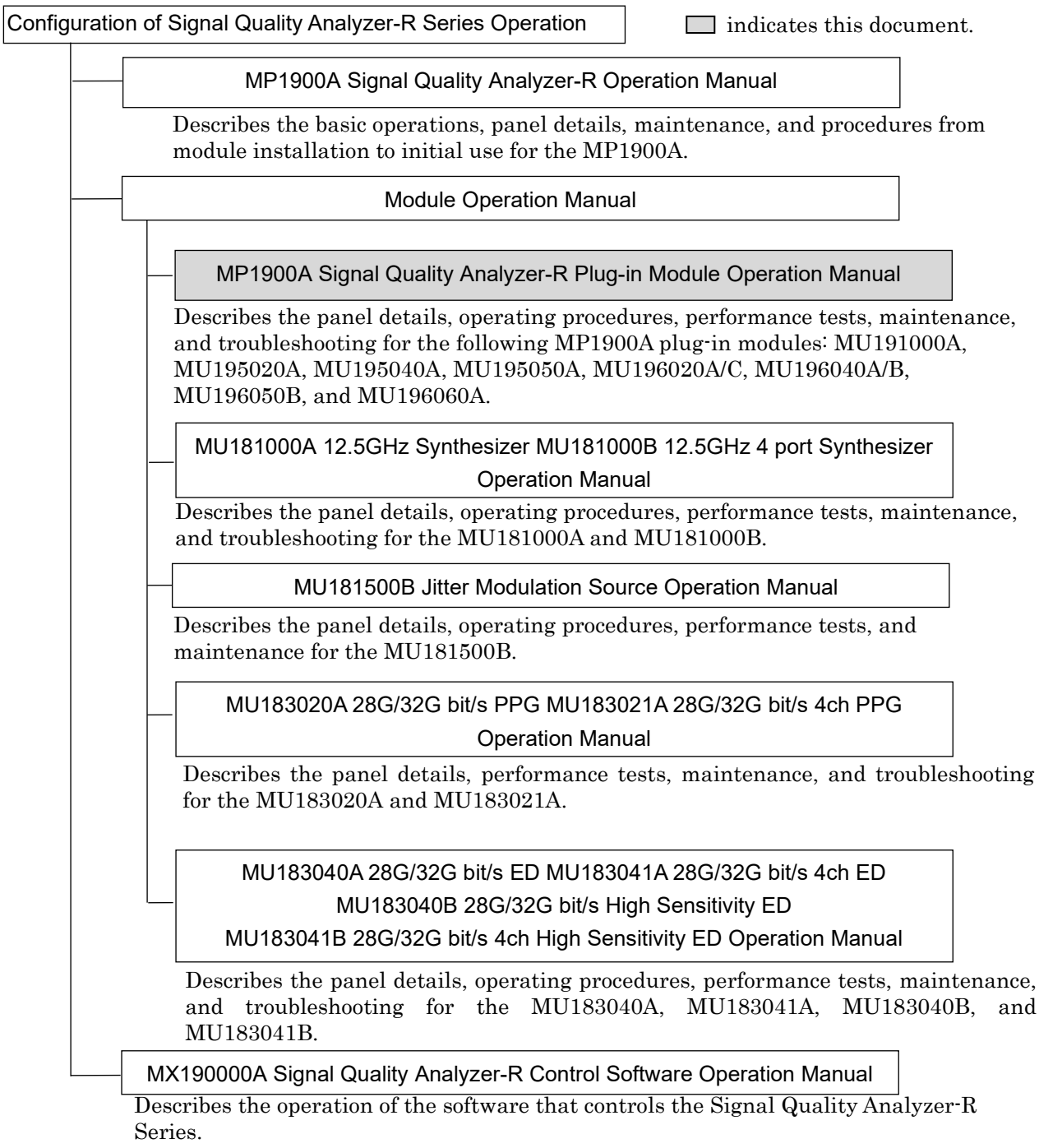
PS: About main frame
Please contact Anritsu for the latest information on the main frame types that MU191000A, MU195020A, MU195040A, MU195050A, MU196020A, MU196020C, MU196040B, MU196050B and MU196060A can be used with.

About This Manual

This operation manual applies to the following plug-in modules:

- MU191000A Synthesizer
- MU195020A 21G/32G bit/s SI PPG
- MU195040A 21G/32G bit/s SI ED
- MU195050A Noise Generator
- MU196020A PAM4 PPG
- MU196020C PAM4 PPG
- MU196040A PAM4 ED
- MU196040B PAM4 ED
- MU196050B Noise Generator
- MU196060A 32G baud NRZ/PAM4 Re-Driver

A testing system combining an MP1900A Signal Quality Analyzer-R, module(s), and control software is called a Signal Quality Analyzer-R Series. The operation manuals of the Signal Quality Analyzer-R Series consist of separate documents for the MP1900A, module(s), and control software, as shown below.


Configuration of Signal Quality Analyzer-R Series Operation
indicates this document.
MP1900A Signal Quality Analyzer-R Operation Manual
Describes the basic operations, panel details, maintenance, and procedures from module installation to initial use for the MP1900A.
Module Operation Manual
MP1900A Signal Quality Analyzer-R Plug-in Module Operation Manual
Describes the panel details, operating procedures, performance tests, maintenance, and troubleshooting for the following MP1900A plug-in modules: MU191000A, MU195020A, MU195040A, MU195050A, MU196020A/C, MU196040A/B, MU196050B, and MU196060A.
MU181000A 12.5GHz Synthesizer MU181000B 12.5GHz 4 port Synthesizer Operation Manual
Describes the panel details, operating procedures, performance tests, maintenance, and troubleshooting for the MU181000A and MU181000B.
MU181500B Jitter Modulation Source Operation Manual
Describes the panel details, operating procedures, performance tests, and maintenance for the MU181500B.
MU183020A 28G/32G bit/s PPG MU183021A 28G/32G bit/s 4ch PPG Operation Manual
Describes the panel details, performance tests, maintenance, and troubleshooting for the MU183020A and MU183021A.
MU183040A 28G/32G bit/s ED MU183041A 28G/32G bit/s 4ch ED
MU183040B 28G/32G bit/s High Sensitivity ED
MU183041B 28G/32G bit/s 4ch High Sensitivity ED Operation Manual
Describes the panel details, operating procedures, performance tests, maintenance, and troubleshooting for the MU183040A, MU183041A, MU183040B, and MU183041B.
MX190000A Signal Quality Analyzer-R Control Software Operation Manual
Describes the operation of the software that controls the Signal Quality Analyzer-R Series.

Configuration of Signal Quality Analyzer-R Series Operation Manuals (Cont'd)

 indicates this document.

Extended Application Operation Manual

Describes the operation of the extended application software for the Signal Quality Analyzer-R Series.

MX183000A High-Speed Serial Data Test Software Operation Manual

Describes the setup and operating procedures for the High-Speed Serial Data Test Software.

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Chapter 1 Overview

This chapter describes the overview of the following modules.

- MU191000A Synthesizer (hereafter, MU191000A)
- MU195020A 21G/32G bit/s SI PPG (hereafter, MU195020A)
- MU195040A 21G/32G bit/s SI ED (hereafter, MU195040A)
- MU195050A Noise Generator (hereafter, MU195050A)
- MU196020A PAM4 PPG (hereafter, MU196020A)
- MU196020C PAM4 PPG (hereafter, MU196020C)
- MU196040A PAM4 ED (hereafter, MU196040A)
- MU196040B PAM4 ED (hereafter, MU196040B)
- MU196050B Noise Generator (hereafter, MU196050B)
- MU196060A 32G baud NRZ/PAM4 Re-Driver (hereafter, MU196060A)

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1.1 Product Overview

The MU191000A, MU195020A, MU195040A, MU195050A, MU196020A/C, MU196040A/B, MU196050B, and MU196060A are plug-in modules that can be installed in the MP1900A Signal Quality Analyzer-R, and are hereinafter referred to as “MP1900A modules”.

The MU196020A/C, MU196040A/B, and MU196060A are plug-in modules that can be built into the MP1900A Signal Quality Analyzer-R. MP1900A supports error measurement with PRBS patterns, DATA patterns and various PAM4 test patterns at the following bit rates or baud rates:

- MU196020A/C: Max. 64.2 Gbit/s or 64.2 Gbaud
- MU196040A: Max. 32.1 Gbit/s or 32.1 Gbaud
- MU196040B: Max. 64.2 Gbit/s or 64.2 Gbaud

With the MU196020A/C and the MU195050A or MU196050B installed, the MP1900A generates data suitable for signal integrity evaluation up to 64.2 Gbaud with applied common-mode noise, differential-mode noise, and white noise.

The MU195020A, MU195040A, and MU195050A support error measurement for PRBS, DATA, Zero-Substitution, and Mixed patterns within the operating frequency range.
With the MU195020A and MU195050A installed, the MP1900A generates data suitable for signal integrity evaluation with applied common-mode noise, differential-mode noise, and white noise.

Various option configurations are available for the MP1900A modules. This module is therefore useful for research, development, and production of various types of digital communication equipment, modules, and devices.

The features of the MP1900A modules are as follows:

MU191000A features

- 4-port synthesizer module with a single-slot configuration
- Center frequency setting from 100 MHz to 16.05 GHz in 1 kHz steps
- SSC (Spread Spectrum Clocking) output for PCIe Gen3/4/5/6/7 (8 GHz)
- Configurable spread method (Center/Down) and deviation (1500/3000/5000 ppm)
- Buzzer settings and system alarm display on PLL unlock

MU195020A features

- PRBS, DATA, Zero-Substitution, Mixed, PAM4, and Sequence pattern generation.
- Channel combination between two channels inside the module using a multiplexer (MUX) for multiplexed signal generation (MU195020A-x20)
- Multi-channel synchronous data generation through channel combination using multiple MU195020A modules installed in the MP1900A
- Signal integrity evaluation using 10Tap Emphasis (MU195020A-x11/x21)
- Variable ISI addition using 10Tap Emphasis (MU195020A-x40/x41)

MU195040A features

- PRBS, Data, Zero-Substitution, Mixed, PAM4, and HSSB Data pattern measurement
- User-programmable patterns up to 256 Mbits
- 64 Gbit/s serial communication evaluation with 2-channel 32 Gbit/s data input (MU195040A-x20)
- High-sensitivity signal evaluation (typ. 25 mVp-p input sensitivity)
- Clock recovery or clock and data recovery (MU195040A-x22)
- Loss signal evaluation using CTLE (Continuous Time Linear Equalizer) (MU195040A-x11/x21)

MU195050A features

- Common-mode and differential-mode noise addition to input data
- White noise addition with a bandwidth of 10 MHz to 10 GHz (MU195050A-x01)

MU196020A features

- Single-channel NRZ/PAM4 signal generation up to 64.2 Gbit/s or 64.2 Gbaud (MU196020A-003)
- Independent PAM4 eye amplitude adjustment
- PRBS, DATA, and various PAM4 pattern generation
- Signal integrity evaluation using 4Tap Emphasis (MU196020A-x11)
- ISI addition using 4Tap Emphasis (MU196020A-x40)
- Pattern generation and error insertion for RS-FEC (544,514) and RS-FEC (528,514) (MU196020A-z42)
- Inter-channel synchronization using multiple MU196020A modules installed in the MP1900A for multi-channel synchronous data generation (MU196020A-x50)
- PCIe6 FEC pattern generation and error insertion (MU196020A-w43)
- Independent PAM3 eye amplitude adjustment

- PRBS, PRTS, DATA, and various PAM3 pattern generation
- USB4 Gen4 pattern generation (MU196020A-z45)
- User-defined pattern output compliant with PCIe encoding schemes (8b10b and 128b130b/1b1b) (MU196020A-z51)
- Synchronized output using the Sequence Editor function with up to four MU196020A modules installed in the MP1900A (MU196020A-z52)
- PCIe6– and CXL3–compliant flit generation and SKP insertion using the Sequence Editor function (MU196020A-z56)

MU196020C features

- Single-channel NRZ/PAM4 signal generation up to 64.2 Gbit/s or 64.2 Gbaud (MU196020C-003)
- Signal integrity evaluation using 4Tap Emphasis (MU196020C-x11)
- Flexible ISI addition and signal adjustment using a high-speed emphasis switching circuit (MU196020C-x11/z40)
- Independent PAM4 eye amplitude adjustment
- PRBS, DATA, and various PAM4 pattern generation, and PCIe7 pattern generation (CP/MCP/JMP/HSTP/LSTP/SHSTP)
- Pattern generation and error insertion for RS-FEC (544,514) and RS-FEC (528,514) (MU196020C-z42/z43)
- Inter-channel synchronization using multiple MU196020C modules installed in the MP1900A for multi-channel synchronous data generation (MU196020C-x50)
- Pattern generation for USB4 Gen4 (MU196020C-z45)

MU196040A features

- PAM4 symbol measurement for one channel up to 32.1 Gbaud using the built-in PAM4 decoder circuit
- PRBS, DATA, and various PAM4 pattern measurement
- Long user-programmable patterns (up to 256 Mbits or 256 Msymbols)
- Serial communication evaluation with one-channel data input for NRZ (32.1 Gbit/s) and PAM4 (32.1 Gbaud) (MU196040A-001)
- Typical input sensitivity: NRZ 23 mV (32.1 Gbit/s, eye height), PAM4 23 mV (32.1 Gbaud, eye height per eye)
- Clock recovery for 25.5 to 32.1 Gbaud signals (MU196040A-x22)
- PAM4 signal evaluation by symbol error rate (SER) (MU196040A-x41)

MU196040B features

- PAM4 symbol measurement for one channel up to 64.2 Gbaud using the built-in PAM4 decoder circuit
- PRBS, DATA, and various PAM4 pattern measurement
- Long user-programmable patterns (up to 256 Mbits or 256 Msymbols)
- Data pattern capture (up to 8 Mbits or 4 Msymbols)

- Capture of data patterns with RS-FEC symbol errors and FEC symbol error counting
- Serial communication evaluation with one-channel data input for NRZ (64.2 Gbit/s) and PAM4 (58.2 Gbaud) (MU196040B-002 or y12)
- PAM4 signal evaluation up to 64.2 Gbaud (MU196040B-005 or 115/125)
- Typical input sensitivity: NRZ 23 mV (32.1 Gbit/s, eye height), PAM4 23 mV (32.1 Gbaud, eye height per eye)
- Equalizer function (MU196040B-x11)
- Clock recovery for 2.4 to 29.0 Gbaud signals (MU196040B-x21)
- Clock recovery for 2.4 to 32.1 Gbaud signals (MU196040B-x22)
- Clock recovery for 51.0 to 58.2 Gbaud signals (MU196040B-x23)
- PAM4 signal evaluation by symbol error rate (SER) (MU196040B-z41)
- Measurement of uncorrectable codewords and FEC symbol errors in RS-FEC scrambled idle patterns (MU196040B-w42)
- Measurement of flit errors and FEC symbol errors in PCIe6 FEC patterns (MU196040B-w43)
- Evaluation of PCIe– and CXL–compliant patterns (8b10b and 128b130b/1b1b) generated by the Sequence Editor (MU196040B-z51)

MU196050B features

- Common-mode and differential-mode noise output

MU196060A features

- 32Gbaud NRZ/PAM4 loss compensation by using CTLE
  PCIe5/6 CEM return path loss compensation in combination with the MU196040B
  PCIe5 CEM specification support in combinination with the MU195040A SI ED (hereinafter referred to as “MU195040A”)
- Clock recovery under the following conditions (MU196040B-x23)
  - 2.5 Gbit/s, 5 Gbit/s, 8 Gbit/s for NRZ (MX183000A PCIe Link Training only)
  - 16 Gbaud, 19.0 to 32.1 Gbaud for NRZ and PAM4

  PCIe4 to PCIe6 SRIS (SSC clock) measurement support in combination with the MU196040B

1.2 Product Configuration

1.2.1 Standard configuration

Table 1.2.1-1, Table 1.2.1-2, Table 1.2.1-3, Table 1.2.1-4, Table 1.2.1-5, Table 1.2.1-6, Table 1.2.1-7, Table 1.2.1-8, Table 1.2.1-9, and Table 1.2.1-10 below show the standard configurations of the three MP1900A modules respectively.

Table 1.2.1-1 Standard Configuration of MU191000A

Item	Model name/symbol	Product name	Q'ty	Remarks
Mainframe	MU191000A	Synthesizer	1	
Accessories	J1341A	Open	3	10MHz Input/Output 100MHz Input For SMA connector protection
	J1632A	Terminator (SMA)	5	Clock/AUX Output For SMA connector termination
	J1717A	Coaxial Adaptor (SMA-P, SMA-J)	5	Clock/AUX Output For SMA connector protection
	J1624A	Coaxial Cable 0.3M(SMA connector)	4	Clock Output

Table 1.2.1-2 Standard Configuration of MU195020A

Item	Model name/symbol	Product name	Q'ty	Remarks
Mainframe	MU195020A	21G/32G bit/s SI PPG	1	
Accessories	J1632A	Terminator (SMA)	5	Clock Output, Aux Output × 2, Gating Output × 2
	J1341A	Open	2	Ext Clock Input, AUX Input
	J1359A	Coaxial Adaptor (K-P.K-J, SMA)	1	Clock Output
	J1717A	Coaxial Adaptor (SMA-P, SMA-J)	6	Ext Clock Input, Aux Output × 2, Gating Output × 2, AUX Input
	When the MU195020A-x10 is installed:			
	J1632A	Terminator (SMA)	2	Data Output × 2
	J1359A	Coaxial Adaptor (K-P.K-J, SMA)	2	Data Output × 2
	When the MU195020A-x20 is installed:			
	J1632A	Terminator (SMA)	4	Data Output × 4
	J1359A	Coaxial Adaptor (K-P.K-J, SMA)	4	Data Output × 4

Table 1.2.1-3 Standard Configuration of MU195040A

Item	Model name/symbol	Product name	Q'ty	Remarks
Mainframe	MU195040A	21G/32G bit/s SI ED	1	
Accessories	J1632A	Terminator (SMA)	2	Aux Output × 2
	J1341A	Open	2	Ext Clock Input, AUX Input
	J1717A	Coaxial Adaptor (SMA-P, SMA-J)	4	Ext Clock Input, Aux Output × 2, AUX Input
	When the MU195040A-x10 is installed:			
	J1341A	Open	2	Data Input × 2
	J1359A	Coaxial Adaptor (K-P.K-J, SMA)	2	Data Input × 2 (Supplied separately from the mainframe)
	J1887A	Fixed Attenuator (6 dB, K connector)	2	Data Input × 2 (Fitted to this module when shipped.)
	When the MU195040A-x20 is installed:			
	J1341A	Open	4	Data Input × 4
	J1359A	Coaxial Adaptor (K-P.K-J, SMA)	4	Data Input × 4 (Supplied separately from the mainframe)
	J1887A	Fixed Attenuator (6 dB K connector)	4	Data Input × 4 (Fitted to this module when shipped.)

Table 1.2.1-4 Standard Configuration of MU195050A

Item	Model name/symbol	Product name	Q'ty	Remarks
Mainframe	MU195050A	Noise Generator	1	
Accessories	J1632A	Terminator (SMA)	4	Data Output × 4*1
	J1359A	Coaxial Adaptor (K-P.K-J, SMA)	4	Data Output × 4*2
	J1717A	Coaxial Adaptor (SMA-P, SMA-J)	2	External Input × 2*2
	J1341A	Open	6	Data Input × 4*1 External Input × 2*1
	J1746A	Skew match pair semirigid cable (K connector, Data Input1)	1 set	Data Input1 × 2*3
	J1747A	Skew match pair semirigid cable (K connector, Data Input2)	1 set	Data Input2 × 2*4
	J1792A	Skew match pair semirigid cable (V-K connector, Data Input1)	1 set	Data Input1 × 2*5

*1: Fitted to this module when shipped.

*2: It is recommended to keep it connected to the MU195050A connector.

*3: Semi-rigid cable to connect Data Output1 of MU195020A and Data Input1 of MU195050A at the shortest length.

*4: Semi-rigid cable to connect Data Output2 of MU195020A and Data Input2 of MU195050A at the shortest length.

*5: Semi-rigid cable to connect Data Output of MU196020A PAM4 PPG and Data Input1 of MU195050A at the shortest length.

Table 1.2.1-5 Standard Configuration of MU196020A

Item	Model name/symbol	Product Name	Q'ty	Remarks
Mainframe	MU196020A	PAM4 PPG	1	
Accessories	J1632A	Terminator (SMA)	4	Clock Output, AUX Output × 2, Gating Output
	J1889A	Terminator	2	Data Output × 2
	J1341A	Open	2	Ext Clock Input, AUX Input
	J1359A	Coaxial Adaptor (K-P.K-J, SMA)	1	Clock Output
	J1717A	Coaxial Adaptor (SMA-P, SMA-J)	5	Ext Clock Input, AUX Output × 2, Gating Output, AUX Input

Table 1.2.1-6 Standard Configuration of MU196020C

Item	Model name/symbol	Product Name	Q'ty	Remarks
Mainframe	MU196020C	PAM4 PPG	1	
Accessories	J1632A	Terminator (SMA)	4	Clock Output, AUX Output × 2, Gating Output
	J1889A	Terminator	2	Data Output × 2
	J1341A	Open	2	Ext Clock Input, AUX Input
	J1359A	Coaxial Adaptor (K-P.K-J, SMA)	1	Clock Output
	J1717A	Coaxial Adaptor (SMA-P, SMA-J)	5	Ext Clock Input, AUX Output × 2, Gating Output, AUX Input

Table 1.2.1-7 Standard Configuration of MU196040A

Item	Model name/symbol	Product Name	Q'ty	Remarks
Mainframe	MU196040A	PAM4 ED	1	
Accessories	J1632A	Terminator (SMA)	2	AUX Output × 2
	J1341A	Open	2	Ext Clock Input, AUX Input
	J1359A	Coaxial Adaptor (K-P.K-J, SMA)	1	Ext Clock Input
	J1717A	Coaxial Adaptor (SMA-P, SMA-J)	3	AUX Output × 2, AUX Input
	When the MU196040A-001 is installed:			
	J1341A	Open	2	Data Input × 2
	J1359A	Coaxial Adaptor (K-P.K-J, SMA)	2	Data Input × 2

Table 1.2.1-8 Standard Configuration of MU196040B

Item	Model name/symbol	Product Name	Q'ty	Remarks
Mainframe	MU196040B	PAM4 ED	1	
Accessories	J1889A	Terminator (SMA)	2	Data Input × 2
	J1341A	Open	2	Ext Clock Input, AUX Input
	J1359A	Coaxial Adaptor (K-P.K-J, SMA)	1	Ext Clock Input
	J1632A	Terminator	2	AUX Output × 2
	J1717A	Coaxial Adaptor (SMA-P, SMA-J)	3	AUX Output × 2, AUX Input
	J1888A	Precision Fixed Attenuator	2	Data Input × 2

Table 1.2.1-9 Standard Configuration of MU196050B

Item	Model name/symbol	Product Name	Q'ty	Remarks
Mainframe	MU196050B	Noise Generator	1	
Accessories	J1717A	Coaxial Adaptor (SMA-P, SMA-J)	4	Noise Output × 2*1, *2 External Input × 2*1, *2
	J1632A	Terminator (SMA)	2	Noise Output × 2*1
	J1341A	Open	2	External Input × 2*1
	J1948A	Coaxial Skew Matched Cable Pair (0.4m, SMA Connector)	1 set	Noise Output × 2*3
	J1793A	Pick OFF Tee	2	V Connector*4

*1: (Fitted to this module when shipped.)

*2: It should remain connected to the connector on the MU196050B at all times.

*3: Used for connecting the MU196050B Noise Output to J1793A.

*4: Used for connecting to the MU196020A/C Data Output.

Table 1.2.1-10 Standard Configuration of MU196060A

Item	Model name/symbol	Product Name	Q'ty	Remarks
Mainframe	MU196060A	32G baud NRZ/PAM4 Re-Driver	1	
Accessories	J1916A	Open (V)	4	Data/XData Input × 2, Data/XData Output × 2
	J1341A	Open	1	Clock Output
	J1898A	Coaxial Cable Set for MU196060A	1	For connection with MU196040B Ext Clock In:J1917A × 1, Data/XData Input:J1932A × 1

1.2.2 Options

Table 1.2.2-1, Table 1.2.2-2, Table 1.2.2-3, Table 1.2.2-4, Table 1.2.2-5, Table 1.2.2-6, Table 1.2.2-7, and Table 1.2.2-8 show the options for the MP1900A modules. All options are sold separately.

Note:

The option name format is as follows:

MU195020A-x x x

- Indicates function.
  This value is recognized by the MP1900A.
- Anritsu management number.
  This value is not recognized by the mainframe.
  - 0: Installed at time of shipping
  - 1: Retrofitted option.
    Must be returned to Anritsu (Japan) when installing.
  - 2: Retrofitted option.
    Must be returned to an Anritsu Service and Sales office when installing.
  - 3: Retrofitted option.
    The user can install the option.

- For how to install software options, refer to 2.4 “Adding Plug-In Module Options” in the *MX190000A Signal Quality Analyzer-R Control Software Operation Manual*.

Table 1.2.2-1 Options of MU195020A

Model Name	Product Name	Remarks
MU195020A-y01	32Gbit/s Extension	*1
MU195020A-x10	1ch Data Output	*2,*3
MU195020A-x20	2ch Data Output	*2,*3
MU195020A-y11	1ch 10Tap Emphasis	*1,*4
MU195020A-y21	2ch 10Tap Emphasis	*1,*5
MU195020A-y30	1ch Data Delay	*1,*4
MU195020A-y31	2ch Data Delay	*1,*5
MU195020A-w40	1ch Variable ISI	*4,*6,*9,*10
MU195020A-w41	2ch Variable ISI	*5,*7,*9,*10
MU195020A-z50	Sequence Editor Function	*8,*11,*14
MU195020A-z51	Sequence Editor Function PCIe5 Extension	*8,*12,*13,*14

*1: The y in the model name represents 0, 1, or 2.

*2: The x in the model name represents 0 or 1.

*3: Select either of them.

*4: The MU195020A-x10 is required.

*5: The MU195020A-x20 is required.

*6: The MU195020A-y11 is required.

*7: The MU195020A-y21 is required.

*8: The z in the model name represents 0 or 3.

*9: The w in the model name represents 0, 1, 2, or 3.

*10: The MU195020A-340 and MU195020A-341 work with version 5.00.90 and later of the MX190000A.

*11: It works with version 5.00.90 and later of the MX190000A.

*12: It works with version 7.02.00 and later of the MX190000A.

*13: The MU195020A-y01 and MU195020A-z50 are required.

*14: Software option.

Table 1.2.2-2 Options of MU195040A

Model Name	Product Name	Remarks
MU195040A-y01	32Gbit/s Extension	*1
MU195040A-x10	1ch ED	*2,*3
MU195040A-x20	2ch ED	*2,*3
MU195040A-y11	1ch CTLE	*1,*4
MU195040A-y21	2ch CTLE	*1,*5
MU195040A-y22	Clock Recovery	*1

*1: The y in the model name represents 0, 1, or 2.

*2: The x in the model name represents 0 or 1.

*3: Select either of them.

*4: The MU195040A-x10 is required.

*5: The MU195040A-x20 is required.

Table 1.2.2-3 Option of MU195050A

Model Name	Product Name	Remarks
MU195050A-x01	White Noise	*

*: The x in the model name represents 0 or 1.

Table 1.2.2-4 Options of MU196020A

Model Name	Product Name	Remarks
MU196020A-001	32G baud	*1
MU196020A-002	58G baud	*1
MU196020A-003	64G baud	*1
MU196020A-y12	32G to 58G baud Extension Retrofit	*2, *3
MU196020A-y13	32G to 64G baud Extension Retrofit	*2, *3
MU196020A-y23	58G to 64G baud Extension Retrofit	*2, *4
MU196020A-x11	4Tap Emphasis	*5
MU196020A-x30	Data Delay	*5
MU196020A-z40	Adjustable ISI	*6, *7, *8, *14
MU196020A-z42	FEC Pattern Generation	*6, *8, *14
MU196020A-w43	FEC Error Insertion for PCIe6	*12, *13, *14
MU196020A-z45	USB4 Gen4 Pattern Generation	*6, *14, *15
MU196020A-x50	Inter-Module Synchronization	*5, *9, *10
MU196020A-z51	Sequence Editor Function	*6, *14, *16
MU196020A-z52	Sequence Editor Function for Multi-Channel	*6, *14, *16, *17
MU196020A-z56	Sequence Editor Function PCIe6 and CXL3 Flits Extension	*6, *14, *17, *18
MU196020A-z60	PCIe6 LEQ	*6, *7, *11

*1: Factory-installed software option. Select one from among them.

*2: Software retrofit options, which can be selected after shipping from our factory. (y = 1 or 2)

*3: Available as a retrofit when Option 001 is installed.

*4: Available as a retrofit when Option 002 or y12 is installed.

*5: x = 0, 1, or 2

*6: z = 0, 1, 2, or 3

*7: Available as a retrofit when Option x11 is installed.

*8: Options 040, 042, 140, 142, 240, and 242 are compatible with MX190000A version 3.01.07 or later.
Options 340 and 342 are compatible with MX190000A version 5.00.90 or later.

*9: Available as a retrofit when Option x30 is installed.

*10: Compatible with MX190000A version 3.01.07 or later.

*11: Compatible with MX190000A version 9.00.00 or later.

*12: w = 0 or 3

*13: Compatible with MX190000A version 10.00.00 or later.

*14: Software option.

*15: Compatible with MX190000A version 10.03.00 or later.

*16: Compatible with MX190000A version 10.05.00 or later.

*17: Available as a retrofit when Option z51 is installed.

*18: Compatible with MX190000A version 10.08.00 or later.

Table 1.2.2-5 Options of MU196020C

Model Name	Product Name	Remarks
MU196020C-001	32G baud	*1
MU196020C-002	58G baud	*1
MU196020C-003	64G baud	*1
MU196020C-y12	32G to 58G baud Extension Retrofit	*2, *3
MU196020C-y13	32G to 64G baud Extension Retrofit	*2, *3
MU196020C-y23	58G to 64G baud Extension Retrofit	*2, *4
MU196020C-x11	4Tap Emphasis	*5, *9
MU196020C-x30	Data Delay	*5, *9
MU196020C-z40	Adjustable ISI	*6, *8, *9
MU196020C-z42	FEC Pattern Generation	*8, *9
MU196020C-z43	FEC Error Insertion for PCIe6	*8, *9
MU196020C-z45	USB4 Gen4 Pattern Generation	*8, *9
MU196020C-x50	Inter-Module Synchronization	*5, *7, *9

*1: Factory-installed software option. Select one from among them.

*2: Software retrofit options, which can be selected after shipping from our factory. (y = 1 or 2)

*3: Available as a retrofit when Option 001 is installed.

*4: Available as a retrofit when Option 002 or y12 is installed.

*5: x = 0, 1, or 2

*6: Available as a retrofit when Option x11 is installed.

*7: Available as a retrofit when Option x30 is installed.

*8: z = 0, 1, 2, or 3

*9: Software option

Table 1.2.2-6 Options of MU196040A

Model Name	Product Name	Remarks
MU196040A-001	32.1G baud Decoder	*1
MU196040A-x22	25.5G to 32.1G baud Clock Recovery	*2, *3
MU196040A-x41	SER Measurement	*2, *4

*1: Factory-installed hardware option.

*2: x = 0, 1, or 2

*3: Hardware option

*4: Software option

Table 1.2.2-7 Options of MU196040B

Model Name	Product Name	Remarks
MU196040B-001	32G baud	*1, *14
MU196040B-002	58G baud	*1, *14
MU196040B-005	64G baud	*5, *18
MU196040B-x11	Equalizer	*2, *14
MU196040B-y12	32G to 58G baud Extension	*3, *4, *14
MU196040B-115	32G to 64G baud Extension	*3, *4, *5, *18
MU196040B-125	58G to 64G baud Extension	*3, *5, *17, *18
MU196040B-x21	29G baud Clock Recovery	*2, *5, *6, *7
MU196040B-x22	32G baud Clock Recovery	*2, *5, *6, *7
MU196040B-x23	58G baud Clock Recovery Extension	*2, *8, *14
MU196040B-y24	32G baud Clock Recovery Extension	*3, *5, *9
MU196040B-z41	SER Measurement	*10, *14
MU196040B-w42	FEC Analysis	*11, *14
MU196040B-w43	FEC Analysis for PCIe6	*11, *12, *13, *14
MU196040B-z51	PCIe Sequence Editor Pattern Analysis	*10, *14, *15, *16

*1: Installed when shipped.

*2: x = 0, 1, or 2

*3: y = 1 or 2

*4: MU196040B-001 must be installed.

*5: Hardware option

*6: This option can be installed together with MU196040B-x23.

*7: Only one of MU196040B-x21 and MU196040B-x22 can be installed.

*8: MU196040B-002 or MU196040B-y12 must be installed.
MU196040B-x21 or MU196040B-x22 must be installed.

*9: MU196040B-x21 must be installed.

*10: z = 0, 1, 2, or 3

*11: w = 0 or 3

*12: Compatible with MX190000A version 10.00.00 or later.

*13: MU196040B-z41 must be installed.

*14: Software option

*15: Compatible with MX190000A version 10.05.00 or later.

*16: The MU196040B-z41 is required for PAM4 signal (PCIe6) analysis.

*17: MU196040B-002 must be installed.

*18: Operates only with MX190000A version 11.

Table 1.2.2-8 Options of MU196060A

Model Name	Product Name	Remarks
MU196060A-x01	Clock Recovery for SSC	*1, *2

*1: w = 0 or 3

*2: Software option

1.2.3 Optional accessories

Table 1.2.3-1 shows the optional accessories for the MP1900A modules (SI). All optional accessories are sold separately.

Table 1.2.3-1 Optional Accessories

Model Name	Product Name	Remarks
J1449A	Measurement kit (K connector)	Coaxial cable (K connector) 0.8 m × 2 Coaxial cable 0.8 m × 2 Coaxial cable 1.0 m × 1
34VFK50A	Precision Adapter	Conversion connector (V-F K-M)
34VKF50A	Precision Adapter	Conversion connector (V-M K-F)
41KC-3	Precision Fixed Attenuator 3 dB	K connector
41KC-6	Precision Fixed Attenuator 6 dB	K connector
41KC-10	Precision Fixed Attenuator 10 dB	K connector
41KC-20	Precision Fixed Attenuator 20 dB	K connector
41VA-3	Precision Fixed Attenuator 3 dB	V connector
J1888A	Precision Fixed Attenuator 6 dB	V connector
41VA-10	Precision Fixed Attenuator 10 dB	V connector
41VA-20	Precision Fixed Attenuator 20 dB	V connector
J1342A	Coaxial cable 0.8 m	APC 3.5 mm connector
J1359A	Coaxial Adaptor (K-P.K-J, SMA)	
J1439A	Coaxial Cable 0.8 m (K connector)	
J1510A	Pick OFF Tee	K connector
J1624A	Coaxial Cable 0.3 m (SMA connector)	
J1625A	Coaxial cable 1 m	
J1550A	Coaxial skew match cable (0.8 m, APC 3.5 connector)	APC 3.5 mm connector, Pair cable
J1551A	Coaxial skew match cable (0.8 m, K connector)	K connector, Pair cable
J1887A	Fixed Attenuator (6 dB, K connector)	
J1632A	Terminator (SMA)	SMA connector
J1678A	ESD Protection Adapter-K	K connector
J1679A	ESD Protection Adapter-V	V connector
J1728A	Electrical Length Specified Coaxial Cable (0.4 m, K connector)	
J1741A	Electrical Length Specified Coaxial Cable (0.8 m, K Connector)	
J1742A	Electrical Length Specified Coaxial Cable (0.84 m, K Connector)	
J1735A	Combiner	
G0375A	32Gbaud Power PAM4 Converter	

Table 1.2.3-1 Optional accessories (Cont'd)

Model Name	Product Name	Remarks
G0376A	32Gbaud PAM4 Decoder with CTLE	
G0374A	64Gbaud PAM4 DAC	
G0361A	64Gbaud 2-bit DAC with MUX	
J1748A	Power Splitter (1.5G-18GHz)	
J1758A	ISI Board	
J1789A	Electrical Length Specified Coaxial Cable (0.4m, V connector)	
J1790A	Electrical Length Specified Coaxial Cable (0.8m, V connector)	
J1792A	Skew match pair semirigid cable (V-K connector, Data Input1)	For connecting to the Data Input1 connector of MU195050A
J1793A	Pick OFF Tee	V connector
J1800A	ISI Board V	V connector
J1900A	Passive Low Frequency Equalizer	
J1917A	Coaxial Semi-rigid Cable	For connection between MU196040B Ext Clock In and MU196060A Clock Output
J1932A	Coaxial Skew Matched Cable Pair (0.8m, V Connector)	
K240C	Precision Power Divider	
J1889A	Terminator	V connector
V240C	Precision Power Divider	V connector
W3976AE	MP1900A Signal Quality Analyzer-R Plug-in Module Operation Manual	Printed version, English
Z0306A	Wrist strap	
MZ1834A/B	4PAM Converter	
MZ1838A	8PAM Converter	
Z1964A	Torque Wrench (Right Angle)	
J1943A	MP1900A USB4v2 Measurement Component Set	*
J1821A	Coaxial Skew Matched Cable Pair (0.8m, K Connector)	
J1759A	BNC-SMA Connector Cable (1m)	
G0447A	PCIe6 External Re-Driver	

*: For the configuration of the MP1900A USB4v2 Measurement Component Set, refer to "Table 1.2.3-2".

Table 1.2.3-2 Configuration of J1943A MP1900A USB4v2 Measurement Component Set

Model Name	Product Name	Remarks
J1888A	Fixed Attenuator (6dB, V Connector)	2
K261	ULTRA WIDE BAND DC BLOCK, 40 GHz	2
J1789A	Electrical Length Specified Coaxial Cable (0.4m, V connector)	2
J1821A	Coaxial Skew Matched Cable Pair (0.8m, K Connector)	4
J1748A	Power Splitter (1.5G-18GHz)	2
J1632A	Terminator (SMA)	2
J1792A	Skew match pair semirigid cable (V-K connector, Data Input1)	1
J1808A	KJ-KJ Adaptor	2
J1820A	Electrical Length Specified Coaxial Cable (0.4m, K connector)	4
J1949A	Coaxial Skew Matched Cable Pair (0.6m, K Connector)	1

1.3 Specifications

1.3.1 Synthesizer

1.3.1.1 Specifications for MU191000A

Table 1.3.1.1-1 Specifications

Item		Specifications
Electrical performance Clock Output	Number of outputs	4
	Frequency range	0.1 to 16.05 GHz*1
	Setting resolution	1 kHz Offset function: –1000 to +1000 ppm Resolution: 1 ppm steps
	Amplitude	0.7±0.3 Vp-p (0.4 to 1.0 Vp-p)
	Duty	50±10 % (40 to 60 %)
	Output skew	≤ 10 ps (16.05 GHz)
	Phase noise	≤ –110 dBc/Hz at 10 kHz offset*2
		≤ –111 dBc/Hz at 100 kHz offset*2
		≤ –110 dBc/Hz at 1 MHz offset*2
	Internal SSC modulation	SSC 33kHz Center / Down Spread OFF / 1500 ppm / 3000 ppm / 5000 ppm
	Impedance	50 Ω / AC Coupling
	Connector	SMA-Jack

*1: The AUX Output uses the same setting as the Clock Output.

*2: Non-harmonic spurious components are excluded

Table 1.3.1.1-1 Specifications (Cont'd)

Item		Specifications
10 MHz reference signal Ref. Input	Frequency	10 MHz±2 ppm
	Level	0.5 to 2.0 Vp-p
	Impedance	50 Ω / AC Coupling
	Connector	SMA-Jack
10 MHz reference signal Ref. Output	Level	1.0±0.3 Vp-p (0.7 to 1.3 Vp-p)
	Impedance	50 Ω / AC Coupling
	Waveform	Sine wave
	Connector	SMA-Jack
100 MHz reference signal Ref. Input*3	Frequency	100MHz with SSC 30 to 33kHz Center/Down Spread 0 to 5000 ppm
	Level	0.15 to 1.45 Vp-p
	Impedance	50 Ω / AC Coupling
	Connector	SMA-Jack
Reference frequency source		Internal/External 10MHz/External 100MHz
AUX Output*4	Number of outputs	1
	Level	0.5±0.25 Vp-p (0.25 to 0.75 Vp-p)
	Duty	50±10 % (40 to 60 %)
	Impedance	50 Ω / AC Coupling (Always terminate with 50 Ω)
	Connector	SMA-Jack
Environmental performance	Operating temperature range	+15 to +35 °C (Ambient temperature range of the MP1900A in which this module operates when installed.)
	Storage temperature range	–20 to +60 °C (MIL-T-28800E Class 5 compliant when installed in the MP1900A.)
Mechanical performance	Mass	1.1 kg or less
	Dimensions	21 mm(H) x 234 mm(W) x 175 mm(D), excluding protrusions

*3: When a valid reference signal is detected at the 100 MHz Ref. Input, the PLL automatically resynchronizes to the reference. However, the PLL may remain unlocked if a momentary interruption of 1 second or less occurs, or if a signal outside the specified frequency range is applied. In such cases, resynchronize the PLL using one of the following methods:

- Apply a valid reference signal. Then change the Spectrum Spread-SSC selection from **ON (Ext Ref 100MHz)** to another option, and finally set it back to **ON (Ext Ref 100MHz)**.
- Interrupt the input signal for more than 1 second, and then apply it again.

*4: The frequency is set to the same value as the Clock Output.

1.3.2 PPG

1.3.2.1 Specifications for MU195020A

Table 1.3.2.1-1 Operating Bit Rate

Item	Specifications
Operating Bit Rate	2.4 to 21.0 Gbit/s*1 2.4 to 32.1 Gbit/s*2
Setting Range	The range of the operating bit rate is determined by the interlocking module*2 and Table 1.3.2.1-13 “Clock Output”.
MU181000A/B synchronized operation ON*5	This item can be specified when MU181000A or MU181000B are installed to the same unit.
Setting Range	2.400 000 to 21.000 000 Gbit/s, 0.000 002 Gbit/s step*1 2.400 000 to 25.000 000 Gbit/s, 0.000 002 Gbit/s step*2 25.000 004 to 32.100 000 Gbit/s, 0.000 004 Gbit/s step*2
Offset	–1000 to +1000 ppm, 1 ppm step*3
MU181500B synchronized operation ON*5	This item can be specified when MU181000A, MU181000B and MU181500B are installed to the same unit.
Setting Range	2.400 000 to 3.125 000 Gbit/s, 0.000 002 Gbit/s step 3.200 002 to 6.250 000 Gbit/s, 0.000 002 Gbit/s step 6.400 002 to 12.500 000 Gbit/s, 0.000 002 Gbit/s step 12.800 002 to 21.000 000 Gbit/s, 0.000 002 Gbit/s step*1 12.800 002 to 25.000 000 Gbit/s, 0.000 002 Gbit/s step*2 25.600 004 to 32.100 000 Gbit/s, 0.000 004 Gbit/s step*2
Offset	–1000 to +1000 ppm, 1 ppm step*4

*1: Without Option x01

*2: With Option x01

*3: Available only when installed in the same mainframe as the MU195020A.

*4: Offset setting range depends on the bit rate. The range is –1000 to 0 ppm at the following bit rate.

Full Rate: 12.500000 Gbit/s, 25.000000 Gbit/s

Half Rate: 25.000000 Gbit/s

*5: Synchronization with MU181000A/B or with MU181000A/B + MU181500B Jitter is not supported when **Unit Sync** is set to **ON**.

Table 1.3.2.1-1 Operating Bit Rate (Cont'd)

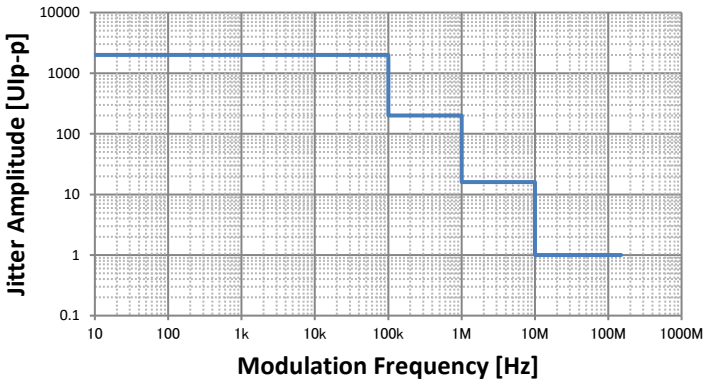
<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>External Clock
When the Output Clock Rate is set to Full Rate

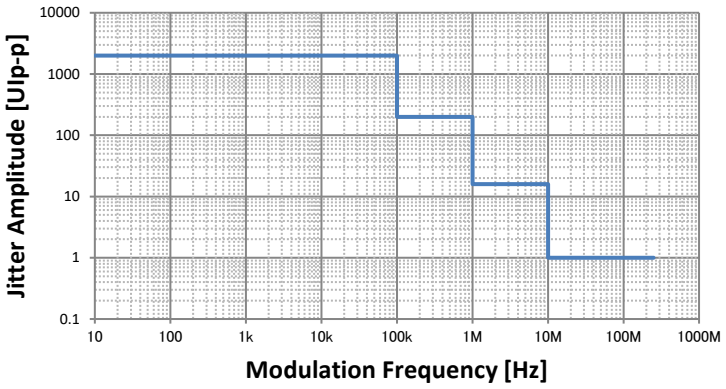
When the Output Clock Rate is set to Half Rate</td><td>
<table>
<tr><th>Operating bit rate range</th><th>Input Clock Frequency</th><th>Relationship Between Bitrate and Clock Frequency</th></tr>
<tr><td>2.4 to 16.0 Gbit/s</td><td>2.4 to 16.0 GHz</td><td>Operate at 1/1 clock</td></tr>
<tr><td>16.0 to 20.0 Gbit/s*1</td><td>8.0 to 10.0 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>20.0 to 21.0 Gbit/s*1</td><td>10.0 to 10.5 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>16.0 to 20.0 Gbit/s*2</td><td>8.0 to 10.0 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>20.0 to 32.1 Gbit/s*2</td><td>10.0 to 16.05 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>25.0 to 32.1 Gbit/s*2</td><td>6.25 to 8.025 GHz</td><td>Operate at 1/4 clock</td></tr>
</table>
<table>
<tr><th>Operating bit rate range</th><th>Input Clock Frequency</th><th>Relationship Between Bitrate and Clock Frequency</th></tr>
<tr><td>2.4 to 28.1 Gbit/s*1</td><td>1.2 to 10.5 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>2.4 to 32.1 Gbit/s*2</td><td>1.2 to 16.05 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>25.0 to 32.1 Gbit/s*2</td><td>6.25 to 8.025 GHz</td><td>Operate at 1/4 clock</td></tr>
</table>
</td></tr>
<tr><td>Tracking with external clock MU181500B
When the Output Clock Rate is set to Full Rate

When the Output Clock Rate is set to Half Rate</td><td>
<table>
<tr><th>Operating bit rate range</th><th>Input Clock Frequency</th><th>Relationship Between Bitrate and Clock Frequency</th></tr>
<tr><td>2.4 to 15.0 Gbit/s</td><td>2.4 to 15.0 GHz</td><td>Operate at 1/1 clock</td></tr>
<tr><td>15.0 to 20.0 Gbit/s*1</td><td>7.5 to 10.0 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>20.0 to 21.0 Gbit/s*1</td><td>10.0 to 10.5 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>15.0 to 20.0 Gbit/s*2</td><td>7.5 to 10.0 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>20.0 to 30.0 Gbit/s*2</td><td>10.0 to 15.0 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>25.0 to 32.1 Gbit/s*2</td><td>6.25 to 8.025 GHz</td><td>Operate at 1/4 clock</td></tr>
</table>
<table>
<tr><th>Operating bit rate range</th><th>Input Clock Frequency</th><th>Relationship Between Bitrate and Clock Frequency</th></tr>
<tr><td>2.4 to 21.0 Gbit/s*1</td><td>1.2 to 10.5 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>2.4 to 30.0 Gbit/s*2</td><td>1.2 to 15.0 GHz</td><td>Operate at 1/2 clock</td></tr>
<tr><td>25.0 to 32.1 Gbit/s*2</td><td>6.25 to 8.025 GHz</td><td>Operate at 1/4 clock</td></tr>
</table>
</td></tr>
</table>

Table 1.3.2.1-2 Jitter Setting Range

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>SJ1 Clock Output Rate

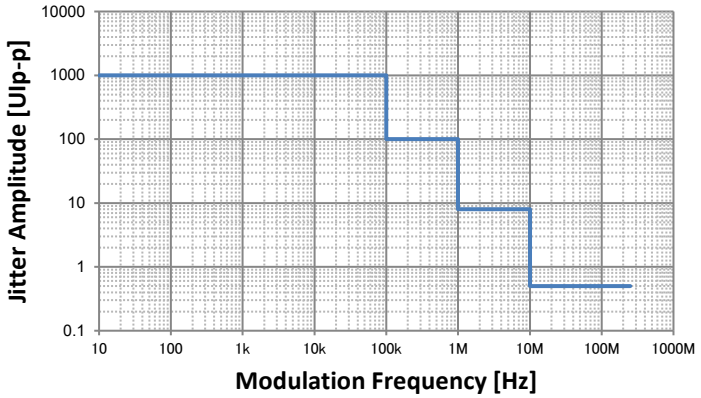
SJ1 Clock Output Rate
At Full Rate</td><td>At MU181000A/B and MU181500B synchronized operation
When Built-in SJ2 is selected as SJ2, the Jitter Amplitude setting range is narrowed by half.
30 < Bit rate ≤ 32.1 Gbit/s, 15 < Bit rate ≤ 17 Gbit/s
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (Ulp-p)</th></tr>
<tr><td>10 to 100k</td><td>0 to 2000</td></tr>
<tr><td>100.1k to 1M</td><td>0 to 200</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 16</td></tr>
<tr><td>10.01M to 150M</td><td>0 to 1</td></tr>
</table>
17 < Bit rate ≤ 30 Gbit/s
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (Ulp-p)</th></tr>
<tr><td>10 to 100k</td><td>0 to 2000</td></tr>
<tr><td>100.1k to 1M</td><td>0 to 200</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 16</td></tr>
<tr><td>10.01M to 250M</td><td>0 to 1</td></tr>
</table></td></tr>
</table>

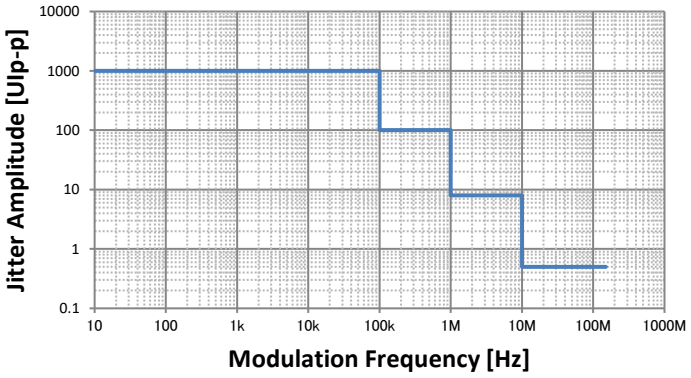
Table 1.3.2.1-2 Jitter Setting Range (Cont'd)

Item	Specifications
SJ1 Clock Output Rate At Full Rate (Cont'd)	8.5 < Bit rate ≤ 15 Gbit/s



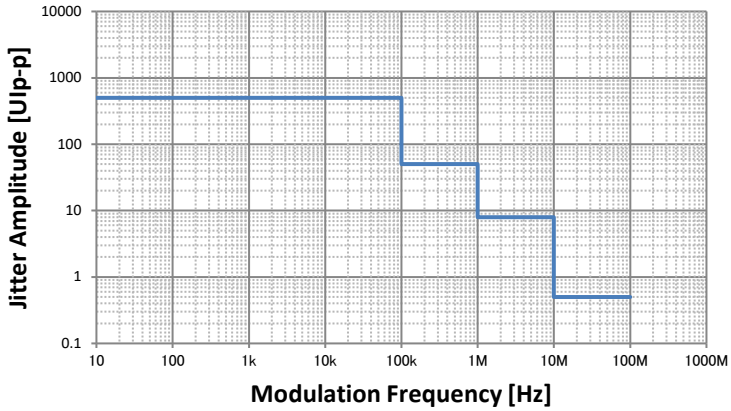
Modulation Frequency (Hz)	Jitter Amplitude (UIp-p)
10 to 100k	0 to 1000
100.1k to 1M	0 to 100
1.001M to 10M	0 to 8
10.01M to 250M	0 to 0.5

4 < Bit rate ≤ 8.5 Gbit/s



Modulation Frequency (Hz)	Jitter Amplitude (UIp-p)
10 to 100k	0 to 1000
100.1k to 1M	0 to 100
1.001M to 10M	0 to 8
10.01M to 150M	0 to 0.5

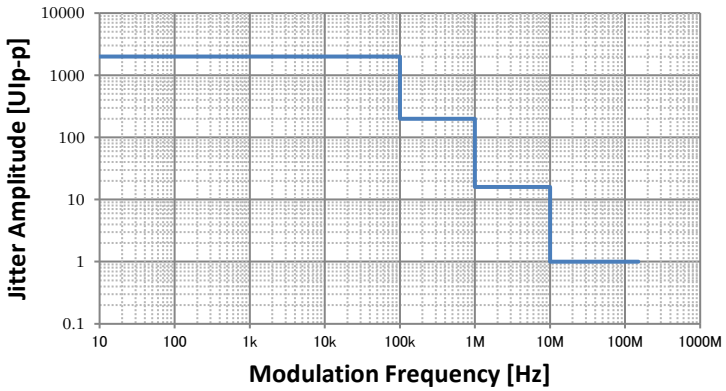
Table 1.3.2.1-2 Jitter Setting Range (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>SJ1 Clock Output Rate
At Full Rate (Cont'd)</td><td>2.4 < Bit rate ≤ 4 Gbit/s
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 100k</td><td>0 to 500</td></tr>
<tr><td>100.1k to 1M</td><td>0 to 50</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 8</td></tr>
<tr><td>10.01M to 100M</td><td>0 to 0.5</td></tr>
</table></td></tr>
</table>

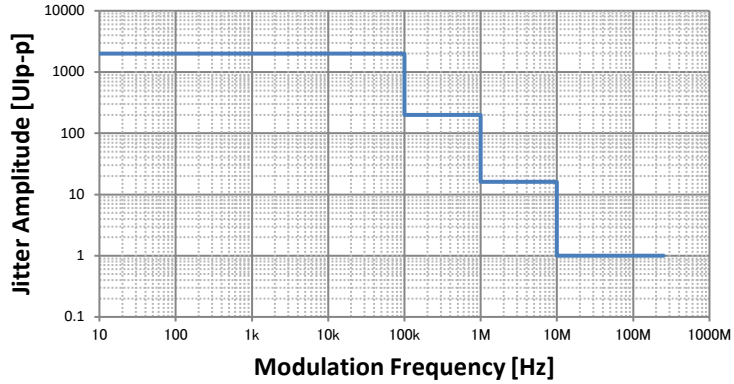
Table 1.3.2.1-2 Jitter Setting Range (Cont'd)

Item	Specifications
SJ1 Clock Output Rate At Half Rate	30 < Bit rate ≤ 32.1 Gbit/s, 8 < Bit rate ≤ 17 Gbit/s



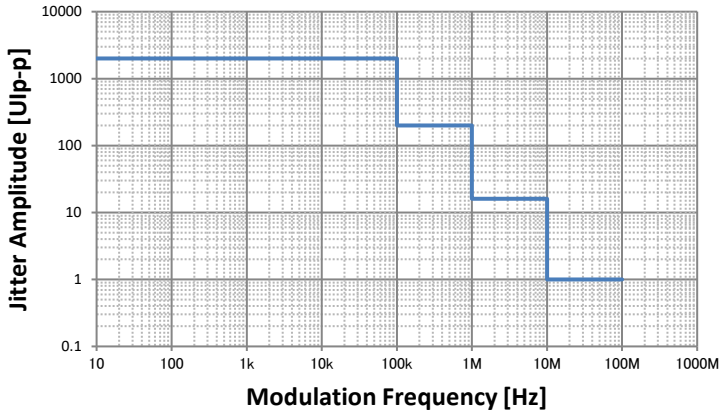
Modulation Frequency (Hz)	Jitter Amplitude (UIp-p)
10 to 100k	0 to 2000
100.1k to 1M	0 to 200
1.001M to 10M	0 to 16
10.01M to 150M	0 to 1

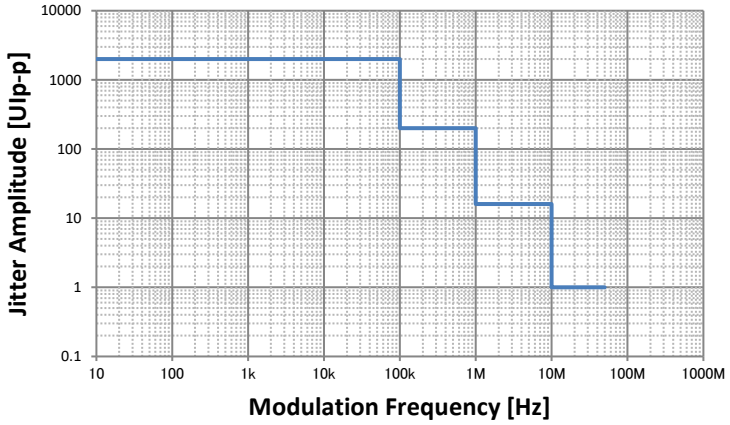
17 < Bit rate ≤ 30 Gbit/s



Modulation Frequency (Hz)	Jitter Amplitude (UIp-p)
10 to 100k	0 to 2000
100.1k to 1M	0 to 200
1.001M to 10M	0 to 16
10.01M to 250M	0 to 1

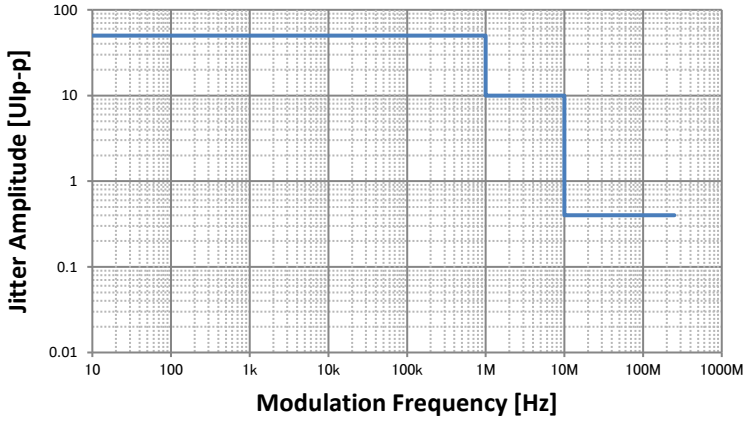
Table 1.3.2.1-2 Jitter Setting Range (Cont'd)

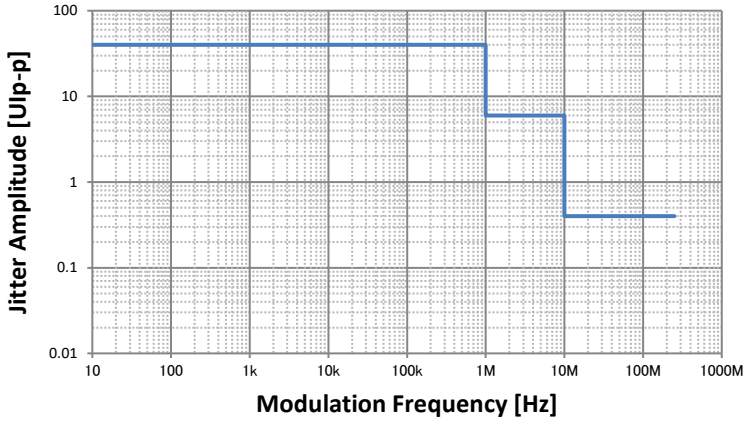
<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>SJ1 Clock Output Rate
At Half Rate (Cont'd)</td><td>
2.4 < Bit rate ≤ 8 Gbit/s


<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 100k</td><td>0 to 2000</td></tr>
<tr><td>100.1k to 1M</td><td>0 to 200</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 16</td></tr>
<tr><td>10.01M to 100M</td><td>0 to 1</td></tr>
</table>
Bit rate 2.4 Gbit/s


<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 100k</td><td>0 to 2000</td></tr>
<tr><td>100.1k to 1M</td><td>0 to 200</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 16</td></tr>
<tr><td>10.01M to 50M</td><td>0 to 1</td></tr>
</table>
</td></tr>
</table>

Table 1.3.2.1-2 Jitter Setting Range (Cont'd)

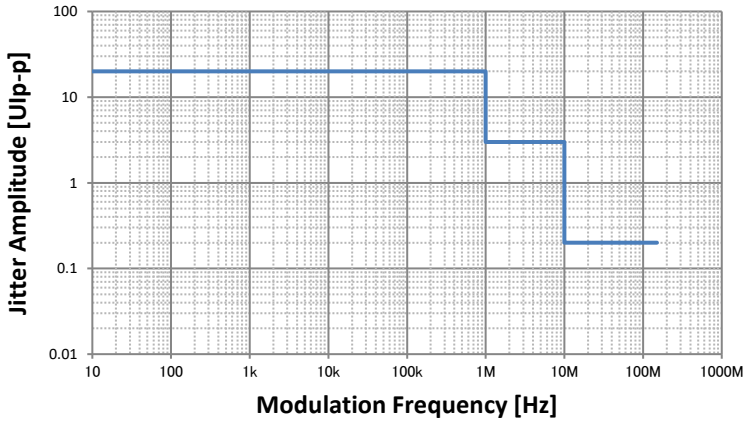
<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>SJ2 Clock Output Rate
SJ2 via MU181000A Clock Output Rate
At Full Rate*1</td><td>15.000 001 ≤ Bit rate ≤ 32.1 Gbit/s
 

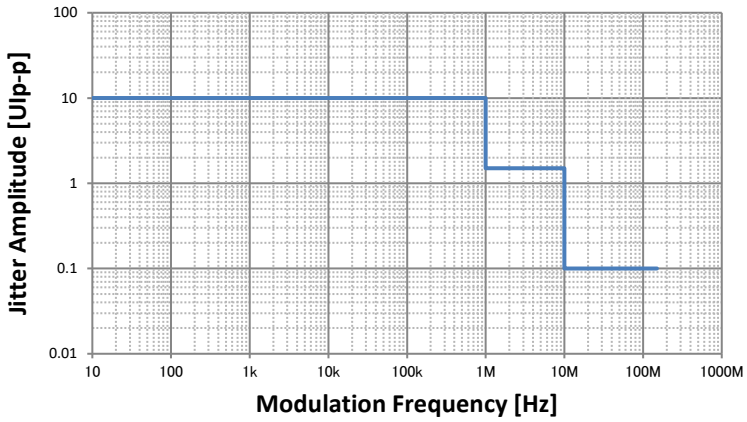
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 1M</td><td>0 to 50</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 10</td></tr>
<tr><td>10.01M to 250M</td><td>0 to 0.4</td></tr>
</table>
6.400 001 ≤ Bit rate ≤ 15 Gbit/s
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 1M</td><td>0 to 40</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 6</td></tr>
<tr><td>10.01M to 250M</td><td>0 to 0.4</td></tr>
</table></td></tr>
</table>

*1: Mutually exclusive with Built-in SJ2.

Table 1.3.2.1-2 Jitter Setting Range (Cont'd)

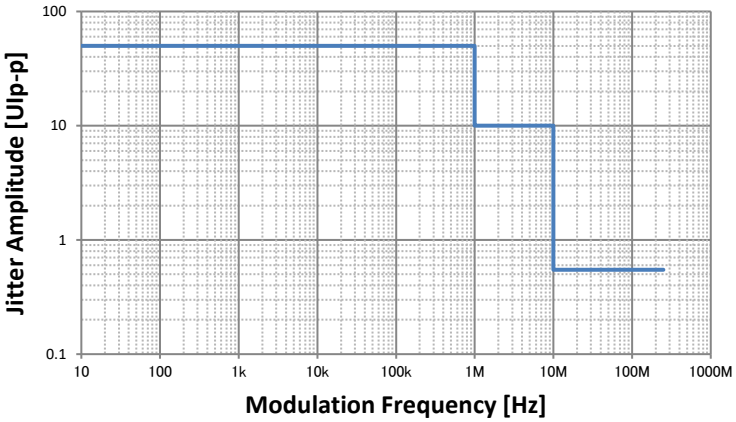
<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>SJ2 via MU181000A Clock Output Rate
At Full Rate*1 (Cont'd)</td><td>3.200 001 ≤ Bit rate ≤ 6.25 Gbit/s
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 1M</td><td>0 to 20</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 3</td></tr>
<tr><td>10.01M to 150M</td><td>0 to 0.2</td></tr>
</table>
2.4 ≤ Bit rate ≤ 3.125 Gbit/s
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 1M</td><td>0 to 10</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 1.5</td></tr>
<tr><td>10.01M to 150M</td><td>0 to 0.1</td></tr>
</table>
</td></tr>
</table>

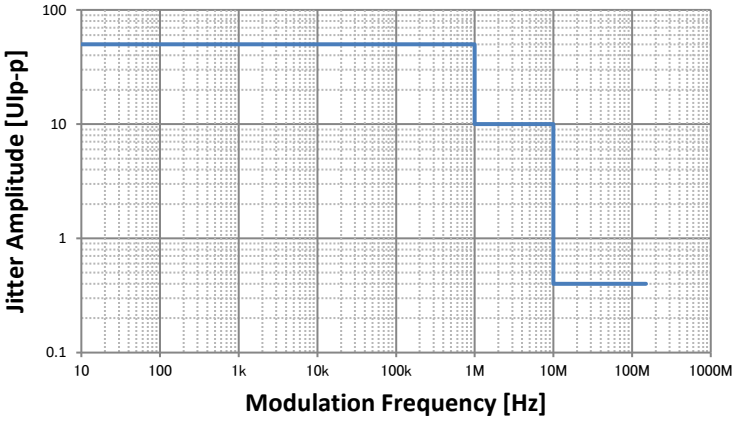
Table 1.3.2.1-2 Jitter Setting Range (Cont'd)

Item	Specifications
SJ2 via MU181000A Clock Output Rate At Half Rate*1	12.800001 ≤ Bit rate ≤ 32.1 Gbit/s



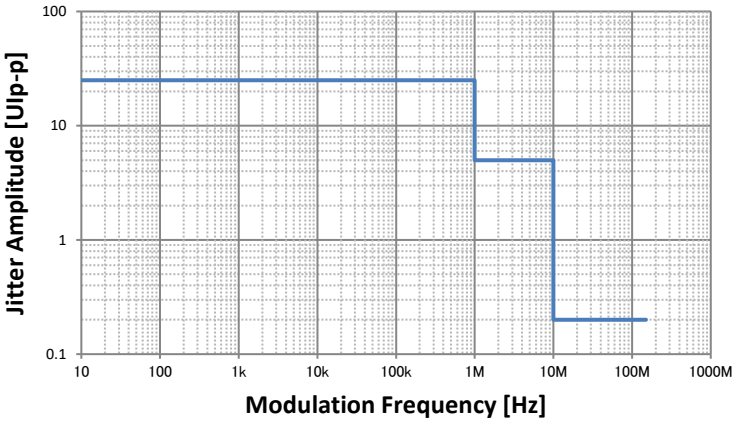
Modulation Frequency (Hz)	Jitter Amplitude (UIp-p)
10 to 1M	0 to 50
1.001M to 10M	0 to 10
10.01M to 250M	0 to 0.548

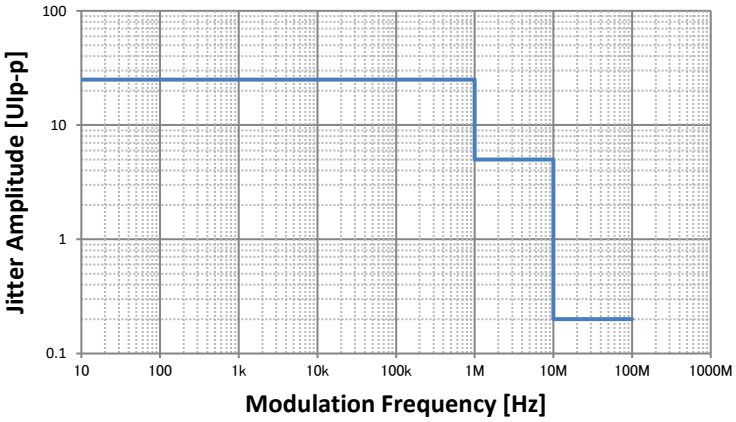
6.400001 ≤ Bit rate ≤ 12.5 Gbit/s



Modulation Frequency (Hz)	Jitter Amplitude (UIp-p)
10 to 1M	0 to 50
1.001M to 10M	0 to 10
10.01M to 150M	0 to 0.4

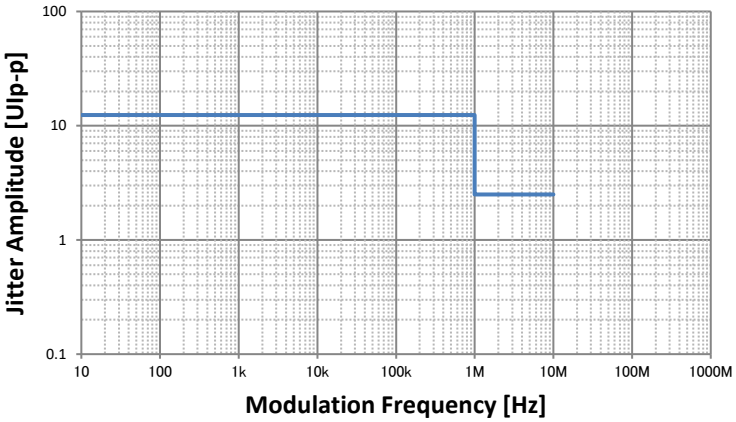
Table 1.3.2.1-2 Jitter Setting Range (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>SJ2 via MU181000A Clock Output Rate
At Half Rate*1 (Cont'd)</td><td>3.600001 ≤ Bit rate ≤ 6.25 Gbit/s
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 1M</td><td>0 to 25</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 5</td></tr>
<tr><td>10.01M to 150M</td><td>0 to 0.2</td></tr>
</table>
3.200001 < Bit rate ≤ 3.6 Gbit/s
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 1M</td><td>0 to 25</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 5</td></tr>
<tr><td>10.01M to 100M</td><td>0 to 0.2</td></tr>
</table></td></tr>
</table>

Table 1.3.2.1-2 Jitter Setting Range (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>SJ2 via MU181000A Clock Output Rate
At Half Rate*1 (Cont'd)</td><td>2.4 ≤ Bit rate ≤ 3.125 Gbit/s
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 1M</td><td>0 to 12.4</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 2.5</td></tr>
</table></td></tr>
<tr><td>Built-in SJ2 Clock Output Rate

Built-in SJ2 Clock Output Rate
At Full Rate*2</td><td>At MU181000A/B and MU181500B synchronized operation

15 < Bit rate ≤ 32.1 Gbit/s
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>33k</td><td>0 to 1000</td></tr>
<tr><td>100M</td><td>0 to 0.5</td></tr>
<tr><td>210M</td><td>0 to 0.2</td></tr>
</table>
4 < Bit rate ≤ 15 Gbit/s
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>33k</td><td>0 to 500</td></tr>
<tr><td>100M</td><td>0 to 0.25</td></tr>
<tr><td>210M</td><td>0 to 0.1</td></tr>
</table>
2.4 ≤ Bit rate ≤ 4 Gbit/s
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>33k</td><td>0 to 500</td></tr>
<tr><td>100M</td><td>0 to 0.25</td></tr>
</table></td></tr>
</table>

*2: Available only when installed in the MP1900A, and mutually exclusive with the SJ2 via MU180000A

Table 1.3.2.1-2 Jitter Setting Range (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Built-in SJ2 Clock Output Rate
At Half Rate*2</td><td>8 < Bit rate ≤ 32.1 Gbit/s
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (Ulp-p)</th></tr>
<tr><td>33k</td><td>0 to 1000</td></tr>
<tr><td>100M</td><td>0 to 0.500</td></tr>
<tr><td>210M</td><td>0 to 0.200</td></tr>
</table>
2.4 < Bit rate ≤ 8 Gbit/s
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (Ulp-p)</th></tr>
<tr><td>33k</td><td>0 to 1000</td></tr>
<tr><td>100M</td><td>0 to 0.5</td></tr>
</table>
Bit rate 2.4 Gbit/s
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (Ulp-p)</th></tr>
<tr><td>33k</td><td>0 to 1000</td></tr>
</table></td></tr>
</table>

Table 1.3.2.1-3 External Clock Input

Item	Specifications
Number of Input	1 (Single-Ended)
Frequency	1.2 to 16.05 GHz
Amplitude	0.3 to 1.0 Vp-p (–6.5 to +4.0 dBm)
Termination	AC, 50 Ω
Connector	SMA connector (f.)

Table 1.3.2.1-4 Aux Input and Output

Item	Specifications
Aux Input	
Number of Input	1 (Single-Ended)
Validation	Error Injection, Burst, Sequence Trigger*1, Unit Sync*2
Minimum Pulse Width	1/128 of data rate
Input level	0/–1 V (H: –0.25 to 0.05 V L: –1.1 to –0.8 V) 0/–0.5 V(H: –0.05 to 0.05 V L: –0.55 to –0.45 V)*2 Vth 0 V (Input amplitude: 0.5 to 1.0 Vp-p) Select one of the above.
Termination	GND, 50 Ω
Connector	SMA connector (f.)
Aux Output	
Number of Output	2 (Differential output)
Output ON/OFF	ON, OFF switching
Validation	1/n Clock (n = 4, 6, 8, 10...510, 512), Pattern Sync, Burst Out2, LTSSM Trigger*1, Unit Sync*2
Pattern Sync	
PRBS, PRGM	Position: 1 to {(Least common multiple of Pattern Length' and 128) –135}, in 8-bit steps When the pattern length' is 511 bits or less, Pattern Length' is the length as an integer multiple so that it becomes 512 bits or more.
Pattern Change Trigger	Outputs a trigger when Data is selected in Test Pattern and Current Outputting Pattern is changed.
Mixed Data	Block No. setting: 1 to the Block No. specified for Mixed Data, in 1-steps Row No. setting: 1 to the Row No. specified for Mixed Data, in 1-steps
Burst Out2	
Burst Trigger Delay	0 to (Burst Cycle – 128) bits, in 8-bit steps
Pulse Width	0 to (Burst Cycle – 128) bits, in 8-bit steps
Unit Sync	Outputs timing signals for Unit Sync when **Unit Sync** is set to **ON**.
Output level	0/–0.6 V (H: –0.25 to 0.05 V, L: –0.80 to –0.45 V)
Termination	GND, 50 Ω
Connector	SMA connector (f.)

*1: Sequence Trigger and LTSSM Trigger can be selected only when **Test Pattern** is set to **Sequence**.

*2: This is selected automatically and fixed when **Unit Sync** is set to **ON**.

Table 1.3.2.1-5 Gating Output

Item	Specifications
Number of Output	2 (Differential output)
Output ON/OFF	ON, OFF switching
Validation	Burst*1, Repeat*1, LFPS*2
Burst	Burst Output
Burst Trigger Delay	0 to (Burst Cycle – 128) bits, in 8-bit steps
Enable Pulse Width	128 to (Burst Cycle – 128) bits, in 8-bit steps
Output Level	0/–1 V (H: –0.25 to 0.05 V, L: –1.25 to –0.8 V)*3
Repeat	Timing Signal Output
Timing Signal Cycle	INT ($\frac{\text{PatternLength}}{128}$) × 128 (other than Mixed)
Timing Signal Pulse Width	For PRBS, Zero-Substitution, Data: 128 to {(Least common multiple of Pattern Length' and 128) –128}, in 8-bit steps The maximum settable number is 34 359 738 240. When the pattern length is 511 bits or less, Pattern Length' is the length as an integer multiple so that it becomes 512 bits or more. For Mixed: 128 to (Row length × Number of rows × Number of blocks –128), in 8-bit steps The maximum settable number is 2 415 918 976.
Timing Signal Delay	Same value as the timing signal pulse width.
Output Level	0/–1 V (H: –0.25 to 0.05 V, L: –1.25 to –0.8 V)*3
Termination	GND, 50 Ω
Connector	SMA connector (f.)

*1: Available only when **Test Pattern** is set to other than **Sequence**.

*2: Available only when **Test Pattern** is set to **Sequence** and **Specification** is set to **USB3.0** or **USB3.1 Gen2**.

*3: L: Output Enable, H: Output Disable

Table 1.3.2.1-6 Pattern Generation

Item	Specifications
PRBS	
Pattern Length	2^n-1 (n = 7, 9, 10, 11, 13, 15, 20, 23, 31)
Mark ratio	1/2 (1/2INV is supported by a logical inversion.)
Zero-Substitution	
Additional bit	0 bit, 1 bit
Pattern Length	2^n or 2^n-1 (n = 7, 9, 10, 11, 15, 20, 23
Start position	Substitutes the bit coming after the maximum “0” successive bits.
Length of Consecutive Zero Bits	1 to (Pattern Length–1) bits If the bit coming after Zero-substitution is “0”, then it is replaced with “1”.
Data	
Data Length	2 to 268 435 456 bits, in 1-bit steps
Current Outputting Pattern	1 to 10, 1 step Outputs the pattern of the selected number. Patterns can be switched glitch-free.
Maximum List Num	1 to 10, 1 step
Mixed Pattern	
Pattern	Data
Mixed Block	To the smaller of the following values: 1 to 511 Block, 1-Block steps $\mathrm{INT}\left(\frac{268435456}{\text{ROW count}}\times\text{Data length}\right)$ bits $\mathrm{INT}\left(\frac{268435456+2^{31}}{\text{ROW length}}\times\text{ROW count}\right)$ bits
Mixed Row Length	2048 to 268435456 + 2^{31}, in 1024-bit steps (Data + PRBS Length)
Data Length	1024 to 268435456 bits, in 1-bit steps
Number of rows	1 to 16, in 1-steps
Number of blocks	1 to 511, in 1-steps
PRBS Pattern Length, Mark ratio	Same as PRBS.
PRBS Sequence	Restart, Consecutive
Scramble	Can be set per PRBS and Data for each Block (except the Data area for Block 1)

Table 1.3.2.1-6 Pattern Generation (Cont'd)

Item	Specifications
PAM4*1	
Sequence	Square Wave, JP03A, JP03B, PRQS10, SSPR, QPRBS13, QPRBS13-CEI, SSPRQ, Transmitter Linearity, PRBS13Q, PRBS31Q, User Define
User Define in detail	
Raw Data	PRBS, Data
PRBS Pattern Length	Same as PRBS.
PRBS Inversion	Logic Inversion/Non-Inversion of PRBS part
Data Length	Same as Data
Gray Coding	Gray Coding ON, OFF
Raw Data	PRBS, Data
PRBS Pattern Length, Mark Ratio	Same as PRBS.
PRBS Inversion	Logic Inversion/Non-Inversion of PRBS part
Data Length	Same as Data
Gray Coding	Gray Coding ON, OFF
Sequence*2	
Specification	PCIe1, PCIe2, PCIe3, PCIe4, PCIe5, USB3.0, USB3.1 Gen2 Options y01, z50, and z51 are all required to select PCIe5.
Logic	POS, NEG
PRBS Inversion	ON, OFF
Transmit	Starts transmitting the sequence pattern. The LED lights up during transmission.
Manual	Enabled when Manual Trigger is set.
Trigger Block No.	Sets the block number of the sequence to output an LTSSM Trigger signal from AUX Output connector. 1 to 128 Block No., 1 step

*1: This is available only when 2ch Combination or 64G x 2ch Combination is set.

*2: The MU195020A-z50 is required. This is available only when Module Combination is set to **Independent**.
If either Ch1 or Ch2 is set to Sequence, the other channel is also set to Sequence.

Table 1.3.2.1-7 Sequence Editor

Item	Specifications
Preset	Emphasis Preset settings PCIe1, PCIe2, PCIe3, PCIe4, PCIe5 2.5G: P0 to P10 5.0G: P0 to P10 8.0G: P0 to P10 16.0G: P0 to P10 32.0G: P0 to P10 USB3.0 5.0G: P0 to P10 USB3.1 Gen2 10.0G: P0 to P10
Break	External(LFPS)*1 External(Edge) Manual OFF
Loop	Time, Num Enabled when Break is set to OFF.
Loop Time	1 to 1,000,000 µsec, 1 µsec step
Loop Num	2 to 1,000,000 times, 2 time step
Insert OS SKP OS EIEOSQ SYNC OS Scrambler Seed	 SKP OS Insertion: ON, OFF SKP OS Reset: ON, OFF EIEOSQ Insertion: ON, OFF EIEOSQ Reset: ON, OFF EIEOSQ Interval: 1 to 65536 pattern repeats, 1 step Enabled when Specification is PCIe1, PCIe2, PCIe3, PCIe4, and PCIe5 SYNC OS Insertion: ON, OFF SYNC OS Reset: ON, OFF SYNC OS Interval: 1 to 65536 pattern repeats, 1 step Enabled when Specification is USB3.1 Gen2. 8b10b: FFFF 128b130b: Lane0, Lane1, Lane2, Lane3, Lane4, Lane5, Lane6, Lane7 128b132b: 1DBFBC

*1: Enabled when the Specification is USB3.0 or USB3.1.

Table 1.3.2.1-7 Sequence Editor (Cont'd)

Item	Specifications
PCIe1	
Bitrate	2.5 Gbit/s
Coding	8b10b
Block number	1 to 128 blocks
Pattern Length	32 to 1024 bit, 8 bit step (8b10b) 2 to 268,435,450 bit, 1 bit step (General) 2^n-1 (n = 7, 9, 10, 11, 13, 15, 20, 23, 31) (General)
Pattern type	Electrical Idle, 8b10b, General*2
SKP Ordered Set Insertion	Length: COM+1, COM+2, COM+3, COM+4, COM+5 Interval: 76 to 3076 symbols, 2 step Symbol Length x2: ON, OFF
PCIe2	
Bitrate	2.5 Gbit/s, 5.0 Gbit/s
Coding	8b10b
Block number	1 to 128 blocks
Pattern Length	32 to 1024 bit, 8 bit step (8b10b) 2 to 268,435,450 bit, 1 bit step (General) 2^n-1 (n = 7, 9, 10, 11, 13, 15, 20, 23, 31) (General)
Pattern type	Electrical Idle, 8b10b, General*2
SKP Ordered Set Insertion	Length: COM+1, COM+2, COM+3, COM+4, COM+5 Interval: 76 to 3076 symbols, 2 step Symbol Length x2: ON, OFF
PCIe3	
Bitrate	2.5 Gbit/s, 5.0 Gbit/s, 8.0 Gbit/s
Coding	8b10b, 128b130b 128b130b can be set only when **Bitrate** is set to 8.0 Gbit/s.
Block number	1 to 128 blocks
Pattern Length	32 to 1024 bit, 8 bit step (8b10b) 128 to 1024 bit, 128 bit step (128b130b) 2 to 268,435,450 bit, 1 bit step (General) 2^n-1 (n = 7, 9, 10, 11, 13, 15, 20, 23, 31) (General)
Pattern type	Electrical Idle, 8b10b, 128b130b, General*2
SKP Ordered Set Insertion	8b10b Length: COM+1, COM+2, COM+3, COM+4, COM+5 Interval: 76 to 3076 symbols, 2 step Symbol Length x2: ON, OFF 128b130b Length: 8, 12, 16, 20, 24 Interval: 20 to 750 blocks, 1 step Symbol Length x2: ON, OFF

*2: General can be set to only the last line of Sequence.

Table 1.3.2.1-7 Sequence Editor (Cont'd)

Item	Specifications
PCIe4	
Bitrate	2.5 Gbit/s, 5.0 Gbit/s, 8.0 Gbit/s, 16.0 Gbit/s
Coding	8b10b, 128b130b 128b130b can be set only when **Bitrate** is set to **8.0 Gbit/s** and **16.0 Gbit/s**.
Block number	1 to 128 blocks
Pattern Length	32 to 1024 bit, 8 bit step (8b10b) 128 to 1024 bit, 128 bit step (128b130b) 2 to 268,435,450 bit, 1 bit step (General) 2^n-1 (n = 7, 9, 10, 11, 13, 15, 20, 23, 31) (General)
Pattern type	Electrical Idle, 8b10b, 128b130b, General*2
SKP Ordered Set Insertion	8b10b Length: COM+1, COM+2, COM+3, COM+4, COM+5 Interval: 76 to 3076 symbols, 2 step Symbol Length x2: ON, OFF 128b130b Length: 8, 12, 16, 20, 24 Interval: 20 to 750 blocks, 1 step Symbol Length x2: ON, OFF
PCIe5	
Bitrate	2.5 Gbit/s, 5.0 Gbit/s, 8.0 Gbit/s, 16.0 Gbit/s, 32.0 Gbit/s
Coding	8b10b, 128b130b 128b130b can be set only when **Bitrate** is set to **8.0 Gbit/s**, **16.0 Gbit/s**, and **32.0 Gbit/s**.
Block number	1 to 128 blocks
Pattern Length	32 to 1024 bit, 8bit step (8b10b) 128 to 1024 bit, 128bit step (128b130b) 2 to 268,435,450 bit, 1bit step (General) 2^n-1 (n = 7, 9, 10, 11, 13, 15, 20, 23, 31) (General)
Pattern type	Electrical Idle, 8b10b, 128b130b, General*2
SKP Ordered Set Insertion	8b10b Length: COM+1, COM+2, COM+3, COM+4, COM+5 Interval: 76 to 3076 symbols, 2 step Symbol Length x2: ON, OFF 128b130b Length: 8, 12, 16, 20, 24 Interval: 20 to 750 blocks, 1 step Symbol Length x2: ON, OFF
Precoding for 32.0 GT/s	ON, OFF

Table 1.3.2.1-7 Sequence Editor (Cont'd)

Item	Specifications
USB3.0	
Bitrate	5.0 Gbit/s
Coding	8b10b
Block number	1 to 128 blocks
Pattern Length	32 to 1024 bit, 8 bit step 2 to 268,435,450 bit, 1 bit step (General) 2^n-1 (n = 7, 9, 10, 11, 13, 15, 20, 23, 31) (General)
Pattern type	LFPS*3,*4 Warm Reset, Polling LFPS, Ping LFPS, Loopback Exit, SCD1, SCD2, End of SCD, PHY Capability LBPM, PHY Ready LBPM, End of LBPM Preset Pattern TS1, TS2, TSEQ, Idle Data, CP0 General*2
SKP Ordered Set Insertion	Length: 2, 4, 6 Interval: 76 to 708 symbols, 1 step
USB3.1 Gen2	
Bitrate	10.0 Gbit/s
Coding	128b132b
Block number	1 to 128 blocks
Pattern Length	128 to 1024 bit, 128 bit step
Pattern type	LFPS*3,*4 Warm Reset, Ping LFPS, Loopback Exit, SCD1, SCD2, End of SCD, PHY Capability LBPM, PHY Ready LBPM, End of LBPM Preset Pattern TS1, TS2, TSEQ, Idle Data, CP9 General*2
SKP Ordered Set Insertion	Length: 8, 12, 16, 20, 24, 28, 32, 36, 40 Interval: 20 to 80 Blocks, 1 Step Symbol Length x2: ON, OFF

*3: LFPS can be transmitted on CH1 only

*4: LFPS is a fixed pattern and cannot be edited by the user.

Table 1.3.2.1-7 Sequence Editor (Cont'd)

Item	Specifications
8b10b Pattern Editor	
Notation	Symbol, Bin, Hex
Scrambler Enable	Scrambles the selected symbols. ON, OFF
Scrambler Reset	Resets the seed value of scrambler on the selected symbols. ON, OFF
Code	K-code, D-code
K code	K28.0, K28.1, K28.2, K28.3, K28.4, K28.5, K28.6, K28.7 K23.7, K27.7, K29.7, K30.7
D code	D0.0 to D31.7
MSB First / LSB First	MSB First, LSB First
128b130b Pattern Editor	
Notation	Bin, Hex
Scrambler Enable	Scrambles the selected symbols. ON, OFF
Scrambler Reset	Resets the seed value of scrambler on the selected symbols. ON, OFF
DC Balance	Adds DC balance to the symbol 14 and 15. ON, OFF
Sync Header	Defines 2-bits Sync Header.
MSB First / LSB First	MSB First, LSB First
128b132b Pattern Editor	
Notation	Symbol Bin, Symbol Hex
Scrambler Enable	Scrambles the selected symbols. ON, OFF
Scrambler Reset	Resets the seed value of scrambler on the selected symbols. ON, OFF
DC Balance	Adds DC balance to the symbol 14 and 15. ON, OFF
Sync Header	Defines 4-bits Sync Header.
MSB First / LSB First	MSB First, LSB First

Table 1.3.2.1-8 Pattern Sequence

Item	Specifications
Sequence	Repeat, Burst
Repeat	Continuous Pattern
Burst	
Source	Internal, External-Trigger (Aux Input)*, External-Enable (Aux Input)*
Data Sequence	Restart, Consecutive, Continuous
Burst Cycle	25600 to 2147483648 bits, in 1024-bit steps
Enable period	Internal: 12800 to 2147483392 bits, in 256-bit steps Ext Trigger: 12800 to 2147483648 bits, in 256-bit steps

*: Available only when **Unit Sync** is set to **OFF**.

Table 1.3.2.1-9 Pre-Code

Item	Specifications
ON/OFF	Sets Pre-Code function ON, OFF*
Modulation type	2ch Combination: DQPSK
Initial Data	Choose 0 or 1.

*: Available only when **Pattern Sequence** is set to **Repeat**.

Table 1.3.2.1-10 Error Addition

Item	Specifications
Area	ALL, Specific Block (Can be selected only for Mixed.)
Internal trigger	
Error Variation	Repeat, Single
Error Ratio	*E– n (*=1 to 9, n=3 to 12), Upper limit is 5.0E–3
Insertion CH	1 to 32, or channel scan (Only when Internal is set.)
External trigger*1, *2	
Control Method	External-Trigger (Rise edge trigger), External-Disable (L: Disable)
Bit/Burst	Selects Bit Error or Burst Error
Burst Length	1 to 127, 1 step

*1: Available only when **Test Pattern** is set to other than **Sequence**.

*2: Available only when **Unit Sync** is set to **OFF**.

Table 1.3.2.1-11 Data Output

Item	Specifications*1
Number of outputs	Option x10: 2 (Data, XData) Option x20: 4 (Data1, XData1, Data2, XData2)
Eye amplitude	
Setting range	0.1 to 1.3 Vp-p, 2 mV step
Accuracy	±50 mV± 17 %
Offset	
Setting range	$-2.0-\frac{\text{Amp.}}{2}$ to $+3.3-\frac{\text{Amp.}}{2}$ Vth, 1mV step
Accuracy	±65 mV ±10 % of offset (Vth) ± (Eye Amp. Accuracy / 2)*2
Defined Interface	NECL, SCFL, NCML, PCML, LVPECL
Cross Point	50 % Fixed
Rising/falling time	12 ps (20 to 80 %)*2,*3,*5, ≤15 ps (20 to 80 %)*2,*3
Half Period Jitter	
Setting range	–100 to 100*4, in 1-steps
Accuracy	±0.02 UI*5,*6

*1: Unless otherwise specified, these are defined with the conditions of PRBS2^{31}–1, Mark ratio 1/2, and Cross Point 50 %.

These values are monitored using an applicable part (J1439A coaxial cable, 0.8 m, K connector) at a sampling oscilloscope bandwidth of 70 GHz.

*2: With Option x11 or Option x21, excluding Emphasis is set.

*3: 21 Gbit/s without Option x01; 32.1 Gbit/s with Option x01. Amplitude: 1.0 Vp-p

*4: If set to 21 or higher or –21 or lower, waveforms may not be output correctly. It is recommend to use while observing waveforms with an oscilloscope, or to use calibrated waveforms.

*5: Typical value

*6: When the value is set to 0.

Table 1.3.2.1-11 Data Output (Cont'd)

Item	Specifications*1
Intrinsic Jitter	
Peak-to-Peak Jitter (p-p)	6 ps p-p (Measurement count 30)*3,*5,*7
Random Jitter (RMS)	300 fs rms (1,0 repeat pattern)*3,*5,*7 115 fs rms (28 Gbit/s 1,0 repeat pattern)*3,*5,*8
Total Jitter (Total)	6 ps*3,*5,*7,*9
Waveform Distortion (0-peak)	±25 mV ±15 %*3,*5
Output ON/OFF	ON, OFF switching
Data/XData skew	±1 ps*5,*10
Skew between channels*11	±0.25 UI
Termination	AC, DC switching, 50 Ω For DC: GND, –2 V, +1.3 V, +3.3 V, Open (LVDS)
Connector	K (f.)
Offset Reference level	Vth
Level Guard	Amplitude, Voh, and Vol can be specified.
External ATT factor	0 to 40 dB, in 1 dB steps

*7: Using oscilloscope with residual jitter of less than 200 fs (RMS).

*8: Using oscilloscope with residual jitter of less than 70 fs (RMS).

*9: Defined by PRBS2^{15}-1 and BER 10^{-12}.

*10: Cable error is not included.

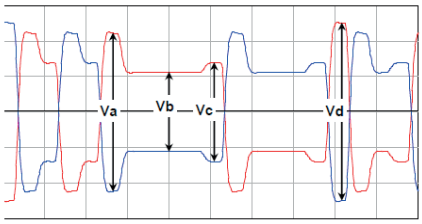
*11: With Option x20.

Table 1.3.2.1-12 10 Tap Emphasis*1

Item	Specifications
Emphasis Tap	10 (6 post-cursor, 3 pre-cursor)
Cursor Setting Range	–20 to 20 dB, in 0.1 dB steps*2
Accuracy	±1 dB*3,*4
Emphasis Peak Voltage Setting Range	0.1 to 1.5 Vp-p (Single-Ended)
Emphasis ON/OFF	ON, OFF switching
Transition Time from Idle State	≤ 8 ns*5
Channel Emulator*6,*7	Normal: Outputs the PPG Data signal whose waveform emulates the connected transmission line with the loaded S parameter. Inverse: Outputs the PPG data signal whose waveform emulates the De-Emphasis compensating the loss of the transmission line with the loaded S parameter.
Response	Normal, Inverse
S-Parameter file	S2P file (Extension: "*.s2p"), S4P file (Extension: "*.s4p") Supports output files from Vector Network Analyzer MS4640B Series.
Variable ISI*6	Sets the loss of the channel which generates ISI and outputs the PPG data signal whose waveform emulates the setting. (The output waveform amplitude is standardized by the amplitude settings.) This is available only when combining with the optional accessory J1758A ISI Board (select "J1758A") or the external channel board (select "Not Specified").
Frequency Setting	Insertion Loss configurable at Nyquist Frequency or 1/2 Nyquist Frequency
Insertion Loss Setting	1.5 to 25 dB in 0.01 dB steps @Nyquist Frequency 0 to 25 dB in 0.01 dB steps @1/2Nyquist Frequency
Insertion Loss Accuracy*8	±1dB Nominal @Nyquist Frequency 10 dB, Repeating pattern of "1,0", ±1dB Nominal @1/2Nyquist Frequency 5 dB, Repeating pattern of "1,1,0,0", Bit rate 16 Gbit/s, 25 Gbit/s (with Option 01), Eye Amplitude 1.0 Vp-p, at each spectrum
ON/OFF	ON, OFF switching
Glitch-free ON/OFF*9	Glitch-free switching that does not interrupt the PPG's output at frequency fluctuations ON, OFF switching

*1: With Option x11 or Option x21.

*2: Post-cursor: $20\log_{10}(\frac{V_a}{V_b})$, Pre-cursor: $20\log_{10}(\frac{V_c}{V_b})$



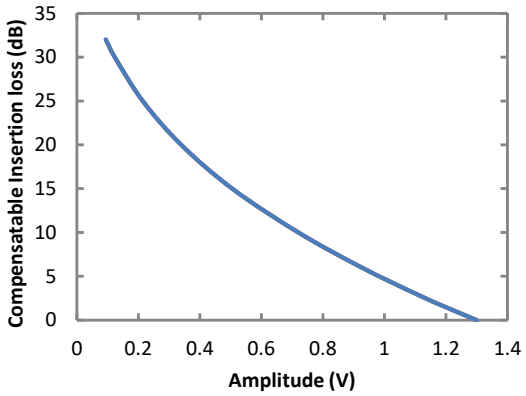
*3: Typical value

*4: Defined for the preset of 8 Gbit/s, 16 Gbit/s, and 25 Gbit/s for PCIe 3 and PCIe 4 respectively.

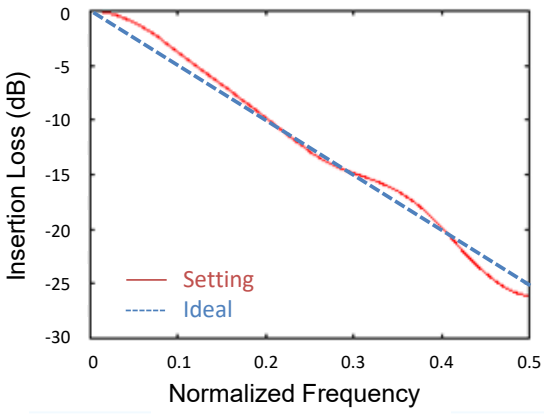
*5: Maximum time to transition to valid diff signaling after leaving Electrical Idle

*6: With Option x40 or Option x41.

*7: The compensable maximum transmission line loss without decreasing the amplitude by the Channel Emulator function is shown in the following graph.



*8: The frequency characteristics of Insertion Loss Accuracy when setting 25 dB@Nyquist Frequency and 12.5 dB@1/2 Nyquist Frequency are shown below. (Nominal)



*9: Fixed to **OFF** when **Unit Sync** is set to **ON**.

Table 1.3.2.1-13 Clock Output

Item	Specifications*1
Frequency	
Full Rate	2.4 to 21.0 GHz*2 2.4 to 32.1 GHz*3 Operation bit rate is same as clock output frequency.
Half Rate	1.2 to 10.5 GHz*2 1.2 to 16.05 GHz*3 Operation bit rate is double of clock output frequency.
Number of Output	1
Amplitude	0.3 to 1.0 Vp-p
ON/OFF	ON, OFF switching
Termination	AC, 50 Ω
Connector	K (f.)

*1: These values are monitored using an applicable part (J1439A coaxial cable, 0.8 m, K connector) at a sampling oscilloscope bandwidth of 70 GHz.

*2: Without Option x01.

*3: With Option x01.

Table 1.3.2.1-14 Data Delay*1

Item	Specifications
Phase setting range	–1000 to +1000 mUI, in 2 mUI steps
Accuracy	±50 mUIp-p*2,*3
mUI – ps switching	Available
Calibration	Available
Calibration indicator	This indicator is on when Calibration is required due to: • 1/1 Clock frequency change by ±250 kHz. • Ambient temperature change by ±5 °C.

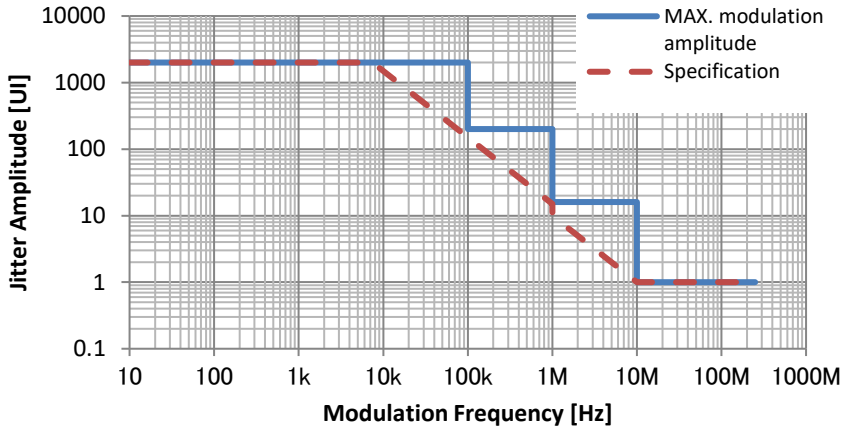
*1: With Option x30 or Option x31.

*2: When using an item with an oscilloscope residual jitter of less than 200 fs (RMS).

*3: Typical value

Table 1.3.2.1-15 Jitter Tolerance

Item	Specifications
Jitter tolerance mask	Bit rate: 16 Gbit/s, 28.1 Gbit/s*, 32.1 Gbit/s* Pattern: PRBS2^{31}–1 SSC with a 5300 ppm amplitude and RJ of 0.3 UI can be simultaneously applied by using MU181500B. These specifications are defined assuming the following conditions: Loopback connection to the MU195040A (when Ext Clock Input is used), defined by one specific temperature in the range of 20 to 30 °C. When RJ + BUJ/SJ3 is bigger than 0.5 UIp-p or SJ1 + Built-in SJ2 + RJ + BUJ/SJ3 is bigger than the standard value + 0.3 UIp-p, "Overload" is displayed on the MU181500B screen. Note that if Modulation Frequency is 33 kHHz, and RJ+BUJ/SJ3 is bigger than 0.5UIp-p or SJ1 is bigger than 550 UIp-p, "Overload" is displayed on the MU181500B screen.



Modulation frequency [Hz]	MAX. modulation amplitude [UIp-p]	Specification [UIp-p]
10	2,000	2,000
7,500	2,000	2,000
100,000	2,000	150
1,000000	200	15
10,000,000	16	1
250,000,000	1	1

*: With Option x01.

Table 1.3.2.1-16 Multichannel Operation

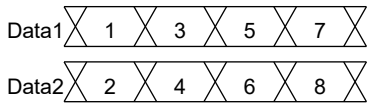
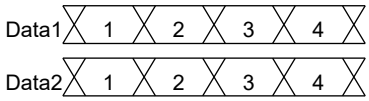
Item	Specifications
Combination Setting	Combination Setting condition: • Multichannel operation cannot be set when Test Pattern is set to Sequence. • Option x31 is required.
2ch Combination	Generates signals with bit phase shift as 42/64 Gbit/s band signal source. Supports 2ch Combination.  Image of 2ch Combination Combination condition: • Combination using multiple modules is not supported.
Channel Synchronization	Generates patterns with first bits aligned as a source of parallel signals. Each channel has an independent Test Pattern and is controlled so that the timing of generation in the same. Supports 2ch Channel Synchronization.  Image of Channel Synchronization

Table 1.3.2.1-16 Multichannel Operation (Cont'd)

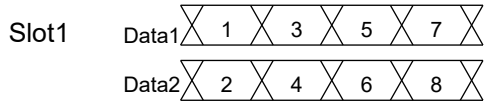
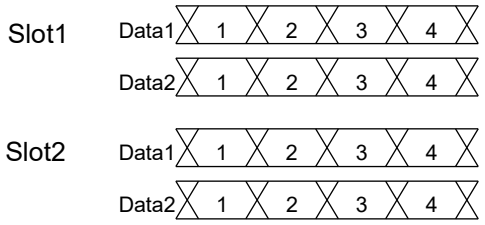
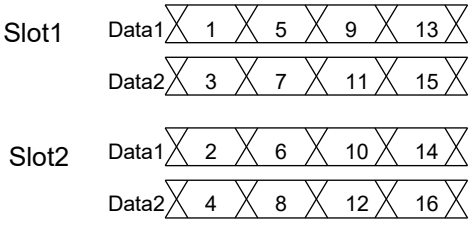
Item	Specifications
Inter-modules combination	Combination Setting condition: • Multichannel operation cannot be set when Test Pattern is set to Sequence. • Option x31 is required. • The presence or absence of Option x01 must be the same across synchronized modules. • Slot 1 to 4: 2ch CH Sync, CH Sync, 64G × 2ch Combination • When modules to be combined are installed sequentially from slot 1.
2ch CH Sync	Inter-modules synchronization of 2ch Combination: DataXs of each module synchronize.  Image of 2ch CH Sync
CH Sync	Inter-modules synchronization: Pattern bits of each Data channel synchronize.  Image of CH Sync
64G × 2ch Combination	Inter-modules synchronization of 2ch Combination: Pattern bits of DataX channel of each module shift in 1/4 period.  Image of 64G × 2ch Combination

Table 1.3.2.1-16 Multichannel Operation (Cont'd)

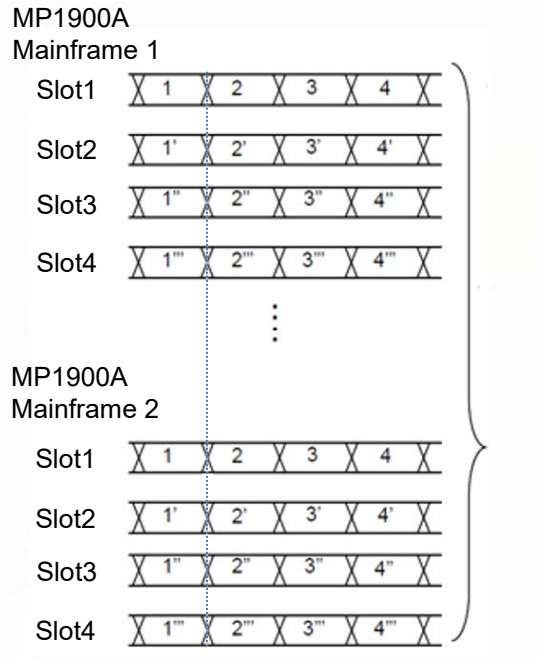
Item	Specifications
Output	
Phase variable range	–64 000 to +64 000 mUI*1
Phase variable step	2 mUI*1
Pattern	
Data	
Data Length	2 × n to 268435456 × n bits, in n-bit steps*2
Mixed	
Row Length	(2048 × n) to {(268435456 +2^{31}) × n}, in (1024 × n)-bit steps*2
Data Length	(1024 × n) to 268435456 × n bits, in n-bit steps*2
Burst	
Burst Cycle	(25600 × n) to (2147483648 × n) bits, in (1024 × n)-bit steps*2
Enable period	Internal: (12800 × n) to 2147483392 × n bits, in (256 × n)-bit steps*2 Ext Trigger: (12800 × n) to 2147483648 × n bits, in (256 × n)-bit steps*2
Pulse Width	0 to {(Burst Cycle – 128) × n} bits, in (8 × n)-bit steps*2
Delay	0 to {(Burst Cycle – 128) × n} bits, in (8 × n)-bit steps*2
Gating Output Repeat (Data)	
Pulse Width	0 × n to (268435328 × n), in (8 × n)-bit steps*2
Delay	0 × n to (268435328 × n), in (8 × n)-bit steps*2
Repeat (Mixed)	
Pulse Width	0 × n to (2^{31} + 268435456 – 128) × n, in (8 × n)-bit steps*2
Delay	0 × n to (2^{31} + 268435456 – 128) × n, in (8 × n)-bit steps*2

*1: A separate value can be set for each channel. This value is common to both Channel Combination and Channel Synchronization.

*2: Common to every channel specified by Combination Setting.

Table 1.3.2.1-16 Multichannel Operation (Cont'd)

Item	Specifications
Unit Sync*1, *2, *3	ON, OFF switching
Number of Unit	Synchronous control is available for up to two MP1900A units. Maximum synchronous control: 16 channels (2 channels per SI PPG × 4 SI PPGs per MP1900A × 2 MP1900A units)
Unit Sync Output*4	Outputs a timing signal from the AUX Out connector when **Unit Sync** is touched. Provided with an inter-unit synchronization status indicator. The color of the **Unit Sync** indicator changes according to the following conditions: Normal (under synchronous control between two MP1900A units): Black When **Unit Sync** needs to be touched: Orange When **Unit Sync** is touched: Green
Unit Sync Input*4	To input a timing signal from the AUX In connector
Unit Offset*4	–128 to +128UI /1 UI Step The same value shall apply to all slots when the **Unit Offset** value is set.
Delay	
Phase variable range	–128,000 to +128,000 mUI (A separate value can be set for each channel.)
Phase variable step	2 mUI (A separate value can be set for each channel.)
Bit phase difference between MP1900A units	Within ±256 UI Indicates the initial amount of bit phase difference when **Unit Sync** is touched. This value remains constant within this range unless the bit rate is changed. Bit shift between MP1900A units can be eliminated by adjusting the Unit Offset and Delay settings.



*1: Available on MX190000A version 10.07.00 or later.

*2: Available only when **Sync Type** is set to **Inter-Module Synchronization** in the Expert BERT application.

*3: With Options 20 and 31. (The option configuration must be the same across modules used for Unit Sync.)

*4: Available only when **Unit Sync** is set to **ON**.

Table 1.3.2.1-17 General

Item	Specifications
Dimensions	21 mm (H), 234 mm (W), 175 mm (D) Excluding protrusions
Mass	2.5 kg max.
Operating Temperature	15 to 35 °C
Storage Temperature	–20 to 60 °C

Table 1.3.2.1-18 Extension Function

Item	Specifications
PCIe	Supports the following PCIe tests when controlled by MX183000A.
Supported standards	PCI Express Base Specification Revision 4.0 Version 0.5, 0.7, 1.0 PCI Express Base Specification Revision 5.0 Version 1.0 Bitrate: PCIe Gen1, Gen2, Gen3, Gen4, Gen5 Lane number: × 1 Test target: Root Complex, End Point
Required option	Option 10/11 or 20/21
Required software	MX183000A-PL011: Follows the PCIe LTSSM to generate the training sequence required to transition the DUT to Loopback state. MX183000A-PL021: Follows the PCIe LTSSM to support negotiation with the DUT and provides LTSSM state transition logging and analysis. One MU195020A and one MU195040A are required. MX183000A-PL025: Extends the PL021 functionality to support PCIe 5.0. Adding MX183000A-PL001 to each software option enables control of MU195020A, MU181500B, and MU195040A and supports Jitter Tolerance Test.
Loopback Through	Configuration, Recovery
Test pattern	Modified Compliance Pattern Insert Delay Symbol: Enable, Disable (Available for Gen1 and Gen2) Insert SRIS: Enable, Disable (Available for Gen3, Gen4, and Gen5) Compliance Pattern Insert Delay Symbol: Enable, Disable (Available for Gen1 and Gen2) User PRBS, Data (8. The pattern defined in Table 1.3.2.1-6 “Pattern Generation”)
SKP Ordered Set Insertion	Enable, Disable
SKP Length/Insertion	For Gen1, Gen2 Length: COM+1, COM+2, COM+3, COM+4, COM+5 Interval: 768 to 3076, 1-steps For Gen3, Gen4, Gen5 Length: 8, 12, 16, 20, 24 Interval: 187 to 750, 1-steps
Dynamic Link Training	Available only when using MX183000A-PL021.
Ling training repeat	1 to 15 (when using MX183000A-PL021)

Table 1.3.2.1-18 Extension Function (Cont'd)

Item	Specifications
Counter	Tx SKP Count, Rx SKP Count (when using MX183000A-PL021) Error Rate, Error Count (when using MX183000A-PL021)
Error Addition	Defined for Modified Compliance Pattern, Compliance Pattern
Error Variation	Repeat, Single
Error Ratio	*E– n (*=1 to 9, n=3 to 12), upper limit is 5.0E–3.
PAM4	Supports the following by combining MU195020A with MZ1834A/B and G0375A. PAM4 signal generation • Amplitude (Single-ended) 0.048 to 0.310 Vp-p (MZ1834A) • Amplitude (Single-ended) 0.048 to 0.489 Vp-p (MZ1834B) • Amplitude (Single-ended) 0.3 to 1.95 Vp-p (G0375A) PAM4 Emphasis signal generation (with Option x11 or Option x21) • Emphasis Peak Voltage (Single-ended) 0.048 to 0.357 Vp-p (MZ1834A) • Emphasis Peak Voltage (Single-ended) 0.048 to 0.564 Vp-p (MZ1834B) • Emphasis Peak Voltage (Single-ended) 0.3 to 2.25 Vp-p (G0375A)
USB	Supports the following USB tests when controlled by MX183000A.
Supported standards	USB3.0/3.1/3.2
Required option	For USB3.2x1: Option 10/11 or 20/x21 For USB3.2x2: Option 20/21/31*
Required software	MX183000A-PL022: Follows the USB LTSSM to support negotiation with the DUT and provides LTSSM state transition logging and analysis (One MU195020A and one MU195040A are required.) Adding MX183000A-PL001 to MX183000A-PL022 enables control of MU195020A, MU181500B, and MU195040A and supports Jitter Tolerance Test. Adding MX183000A-PL023 to MX183000A-PL022 enables control of MU195020A and MU195040A and supports USB3.2x2 Link Training.

*: MX183000A-PL023 is required.

1.3.2.2 Specifications for MU196020A

Table 1.3.2.2-1 Operating Baud/Bit Rate

Item	Specifications
Operating Baud/Bit Rate	With Option 001 PAM4/PAM3*1: 2.4 to 32.1 Gbaud*3 NRZ: 2.4 to 32.1 Gbit/s*3 With Option 002 or y12 PAM4/PAM3*1: 2.4 to 58.2 Gbaud*2, *3 NRZ: 2.4 to 58.2 Gbit/s*2, *3 With Option 003, y13, or y23 PAM4/PAM3*1: 2.4 to 64.2 Gbaud*2, *3 NRZ: 2.4 to 64.2 Gbit/s*2, *3 The baud rate of the PAM4/PAM3 output and the bit rate of the NRZ output have a common numerical value range. Only the baud rate is described hereafter. For each application, refer to the relevant item.
Setting Range / Step	The setting range of the baud rate is determined by the interlocking module (valid only when installed to the same frame as MU196020A), Frequency in Table 1.3.2.2-12 “Clock Output”, and the application used.
When linking with MU181000A/B*2	2.400 000 to 25.000 000 Gbaud, in steps of 0.000 002 Gbaud *5, *6, *7 25.000 004 to 32.100 000 Gbaud, in steps of 0.000 004 Gbaud *5, *6, *7 25.000 004 to 50.000 000 Gbaud, in steps of 0.000 004 Gbaud *6, *7, *8 50.000 008 to 58.200 000 Gbaud, in steps of 0.000 008 Gbaud *6, *9 50.000 008 to 64.200 000 Gbaud, in steps of 0.000 008 Gbaud *7, *9
When linking with MU181000A/B and MU181500B*2	2.400 000 to 3.125 000 Gbaud, in steps of 0.000 002 Gbaud *5, *6, *7 3.200 002 to 6.250 000 Gbaud, in steps of 0.000 002 Gbaud *5, *6, *7 6.400 002 to 12.500 000 Gbaud, in steps of 0.000 002 Gbaud *5, *6, *7 12.800 002 to 25.000 000 Gbaud, in steps of 0.000 002 Gbaud *5, *6, *7 25.600 004 to 32.100 000 Gbaud, in steps of 0.000 004 Gbaud *5, *6, *7 25.600 004 to 50.000 000 Gbaud, in steps of 0.000 004 Gbaud *6, *7, *8 51.200 008 to 58.200 000 Gbaud, in steps of 0.000 008 Gbaud *6, *9 51.200 008 to 64.200 000 Gbaud, in steps of 0.000 008 Gbaud *7, *9

*1: PAM3 can be selected in version 10.03.00 or later.

*2: When the BERT for PCIe1-7 or BERT for PCIe1-5 and PCIe6 Base is selected:
PAM4/PAM3: 2.4 to 32.1 Gbaud
NRZ: 2.4 to 32.1 Gbit/s

*3: When the BERT for PCIe1-6 Forced Link is selected:
PAM4: 32.0 Gbaud
NRZ: 2.5, 5.0, 8.0, 16.0, 32.0 Gbit/s
PAM3: Cannot be set.

*4: Linking is not available when **Unit Sync** is **ON**.

*5: With Option 001

*6: With Option 002 or y12

*7: With Option 003, y13, or y23

*8: The upper limit is 32.1 Gbaud when the BERT for PCIe1-7 or BERT for PCIe1-5 and PCIe6 Base is selected.

*9: Available only when neither the BERT for PCIe1-7 nor BERT for PCIe1-5 and PCIe6 Base application is selected.

Table 1.3.2.2-1 Operating Baud/Bit Rate (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>When linking with MU181500B and using external clock
Clock Output Rate Full Rate</td><td>
<table>
<tr><th>Baud Rate Setting Range</th><th>Input Clock Frequency</th><th>Relationship Between Baud Rate and Input Clock Frequency</th></tr>
<tr><td>2.4 to 15.0 Gbaud*5, *6, *7</td><td>2.4 to 15.0 GHz</td><td>1/1 Clock Input</td></tr>
<tr><td>15.0 to 30.0 Gbaud*5, *6 ,*7</td><td>7.5 to 15.0 GHz</td><td>1/2 Clock Input</td></tr>
<tr><td>25.0 to 32.1 Gbaud*5, *6, *7</td><td>6.25 to 8.025 GHz</td><td>1/4 Clock Input</td></tr>
</table>
Clock Output Rate Half Rate, Quarter Rate
<table>
<tr><th>Baud Rate Setting Range</th><th>Input Clock Frequency</th><th>Relationship Between Baud Rate and Input Clock Frequency</th></tr>
<tr><td>2.4 to 30.0 Gbaud*5, *6, *7</td><td>1.2 to 15.0 GHz</td><td>1/2 Clock Input</td></tr>
<tr><td>30.0 to 32.1 Gbaud*5</td><td>7.5 to 8.025 GHz</td><td>1/4 Clock Input</td></tr>
<tr><td>30.0 to 58.2 Gbaud*6, *8</td><td>7.5 to 14.55 GHz</td><td>1/4 Clock Input</td></tr>
<tr><td>30.0 to 60.0 Gbaud*7, *8</td><td>7.5 to 15.0 GHz</td><td>1/4 Clock Input</td></tr>
<tr><td>50.0 to 58.2 Gbaud*6, *9</td><td>6.25 to 7.275 GHz</td><td>1/8 Clock Input</td></tr>
<tr><td>50.0 to 64.2 Gbaud*7, *9</td><td>6.25 to 8.025 GHz</td><td>1/8 Clock Input</td></tr>
</table>
</td></tr>
</table>

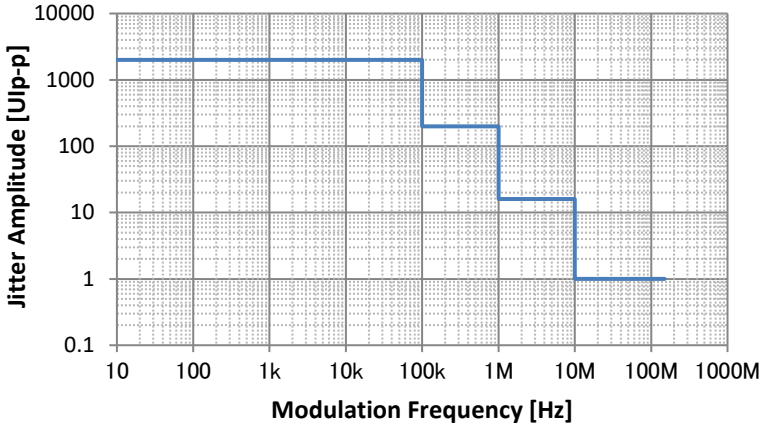
Table 1.3.2.2-1 Operating Baud/Bit Rate (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>External Clock
Clock Output Rate Full Rate

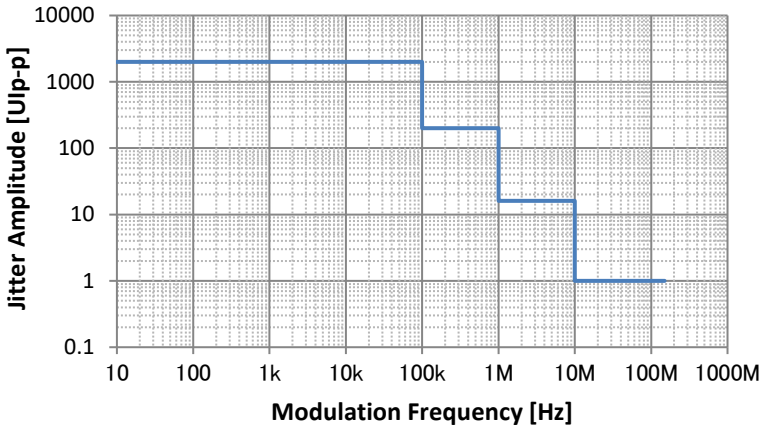
Clock Output Rate Half Rate, Quarter Rate</td><td>
<table>
<tr><th>Baud Rate Setting Range</th><th>Input Clock Frequency</th><th>Relationship Between Baud Rate and Input Clock Frequency</th></tr>
<tr><td>2.4 to 16.05 Gbaud*5, *6, *7</td><td>2.4 to 16.05 GHz</td><td>1/1 Clock Input</td></tr>
<tr><td>16.05 to 32.1 Gbaud*5, *6, *7</td><td>8.025 to 16.05 GHz</td><td>1/2 Clock Input</td></tr>
<tr><td>25.0 to 32.1 Gbaud*5, *6, *7</td><td>6.25 to 8.025 GHz</td><td>1/4 Clock Input</td></tr>
</table>
<table>
<tr><th>Baud Rate Setting Range</th><th>Input Clock Frequency</th><th>Relationship Between Baud Rate and Input Clock Frequency</th></tr>
<tr><td>2.4 to 32.1 Gbaud*5, *6, *7</td><td>1.2 to 16.05 GHz</td><td>1/2 Clock Input</td></tr>
<tr><td>25.0 to 32.1 Gbaud*5</td><td>6.25 to 8.025 GHz</td><td>1/4 Clock Input</td></tr>
<tr><td>25.0 to 50.0 Gbaud*6, *7, *8</td><td>6.25 to 12.50 GHz</td><td>1/4 Clock Input</td></tr>
<tr><td>32.1 to 58.2 Gbaud*6, *8</td><td>8.025 to 14.55 GHz</td><td>1/4 Clock Input</td></tr>
<tr><td>32.1 to 64.2 Gbaud*7, *8</td><td>8.025 to 16.05 GHz</td><td>1/4 Clock Input</td></tr>
<tr><td>50.0 to 58.2 Gbaud*6, *9</td><td>6.25 to 7.275 GHz</td><td>1/8 Clock Input</td></tr>
<tr><td>50.0 to 64.2 Gbaud*7, *9</td><td>6.25 to 8.025 GHz</td><td>1/8 Clock Input</td></tr>
</table>
</td></tr>
<tr><td>Offset Setting Range/Step</td><td>–1000 to +1000 ppm, in steps of 1 ppm
This is available only when linking with MU181000A/B.
Note: The setting range is limited to –1000 to 0 ppm for the following bit rate settings:
Clock Output Rate Full Rate
12.500 000 Gbaud, 25.000 000 Gbaud
Clock Output Rate Half Rate, Quarter Rate
25.000 000 Gbaud, 50.000 000 Gbaud</td></tr>
</table>

Table 1.3.2.2-2 Jitter Setting Range

<table>
<tr><th>Item</th><th>Specifications*1</th></tr>
<tr><td>SJ1 Setting Range

SJ1 Clock Output Rate At Full Rate</td><td>When SJ2 switch is the built-in SJ2, the settable Jitter Amplitude is halved.
30 < Baud rate ≤ 32.1 Gbaud, 15 < Baud rate ≤ 17 Gbaud
 

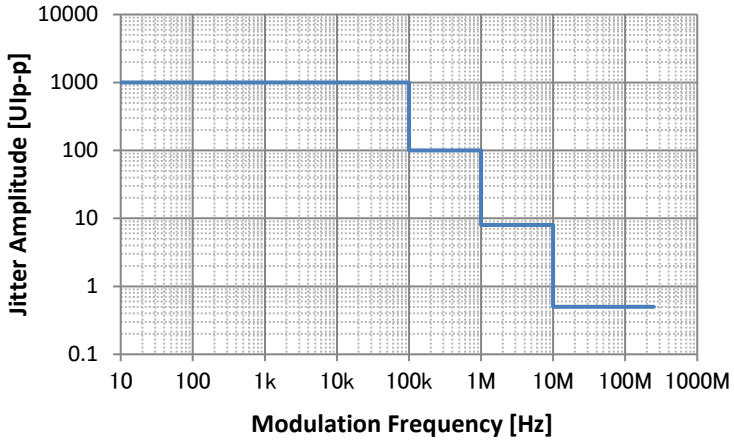
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (Ulp-p)</th></tr>
<tr><td>10 to 100k</td><td>0 to 2000</td></tr>
<tr><td>100.1k to 1M</td><td>0 to 200</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 16</td></tr>
<tr><td>10.01M to 150M</td><td>0 to 1</td></tr>
</table>

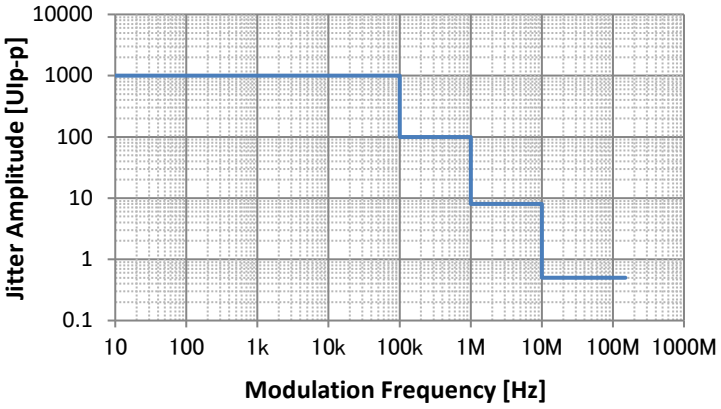
17 < Baud rate ≤ 30 Gbaud
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (Ulp-p)</th></tr>
<tr><td>10 to 100k</td><td>0 to 2000</td></tr>
<tr><td>100.1k to 1M</td><td>0 to 200</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 16</td></tr>
<tr><td>10.01M to 250M</td><td>0 to 1</td></tr>
</table>
</td></tr>
</table>

*1: When linking with MU181000A/B and MU181500B

Table 1.3.2.2-2 Jitter Setting Range (Cont'd)

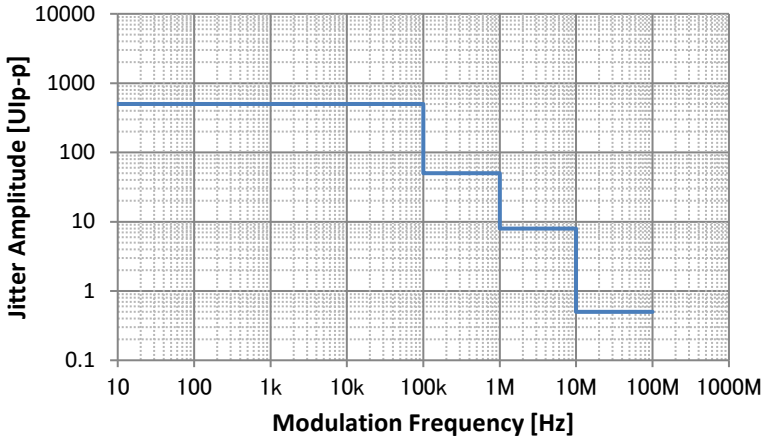
<table>
<tr><th>Item</th><th>Specifications*1</th></tr>
<tr><td>SJ1 Clock Output Rate
At Full Rate (Cont'd)</td><td>8.5 < Baud rate ≤ 15 Gbaud
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 100k</td><td>0 to 1000</td></tr>
<tr><td>100.1k to 1M</td><td>0 to 100</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 8</td></tr>
<tr><td>10.01M to 250M</td><td>0 to 0.5</td></tr>
</table>
4 < Baud rate ≤ 8.5 Gbaud
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 100k</td><td>0 to 1000</td></tr>
<tr><td>100.1k to 1M</td><td>0 to 100</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 8</td></tr>
<tr><td>10.01M to 150M</td><td>0 to 0.5</td></tr>
</table>
</td></tr>
</table>

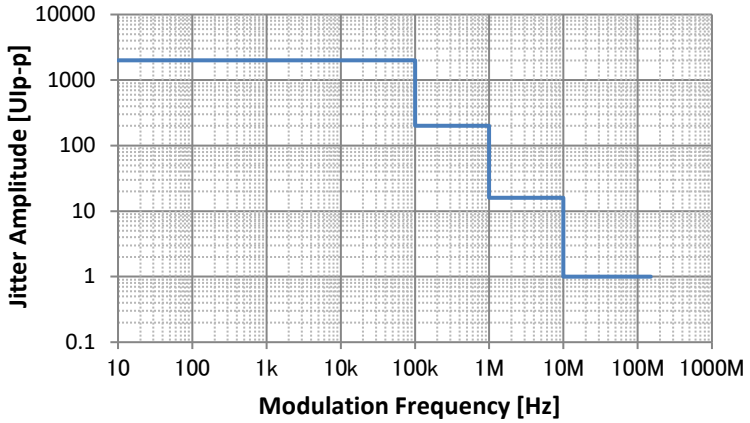
Table 1.3.2.2-2 Jitter Setting Range (Cont'd)

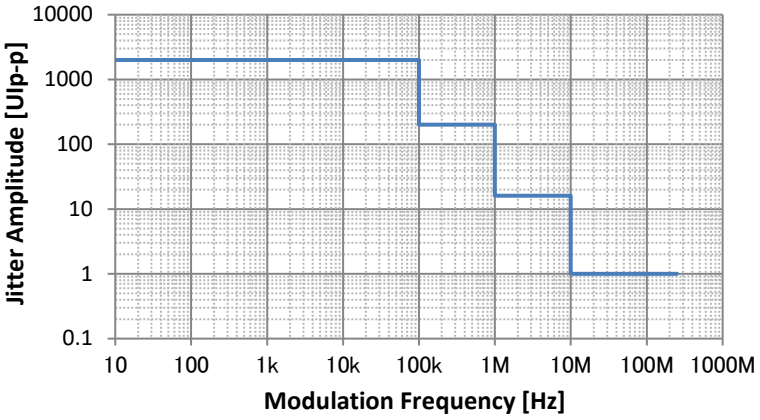
Item	Specifications*1
SJ1 Clock Output Rate At Full Rate (Cont'd)	2.4 ≤ Baud rate ≤ 4 Gbaud



Modulation Frequency (Hz)	Jitter Amplitude (UIp-p)
10 to 100k	0 to 500
100.1k to 1M	0 to 50
1.001M to 10M	0 to 8
10.01M to 100M	0 to 0.5

Table 1.3.2.2-2 Jitter Setting Range (Cont'd)

<table>
<tr><th>Item</th><th>Specifications*1</th></tr>
<tr><td>SJ1 Clock Output Rate
At Half Rate, Quarter Rate</td><td>
60 < Baud rate ≤ 64.2 Gbaud,
30 < Baud rate ≤ 34 Gbaud,
8 < Baud rate ≤ 17 Gbaud


<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 100k</td><td>0 to 2000</td></tr>
<tr><td>100.1k to 1M</td><td>0 to 200</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 16</td></tr>
<tr><td>10.01M to 150M</td><td>0 to 1</td></tr>
</table>
34 < Baud rate ≤ 60 Gbaud*2, 17 < Baud rate ≤ 30 Gbaud


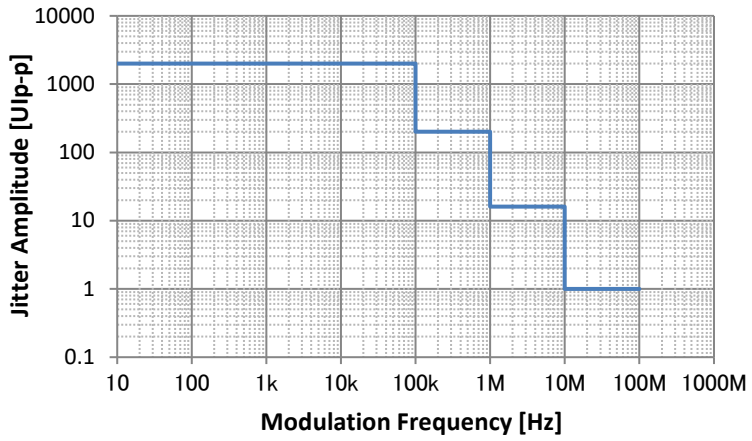
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 100k</td><td>0 to 2000</td></tr>
<tr><td>100.1k to 1M</td><td>0 to 200</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 16</td></tr>
<tr><td>10.01M to 250M*2</td><td>0 to 1</td></tr>
</table>
</td></tr>
</table>

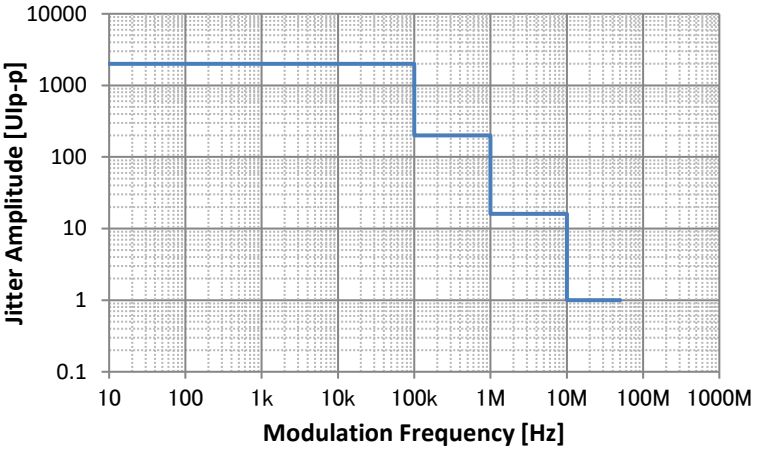
*2: The modulation frequency (Hz) is 10.01M to 150M when both of the following conditions are met:

- Operation Baud Rate is 50 ≤ Baud rate ≤ 60 Gbaud.

- Relationship between Baud Rate and Input Clock Frequency is set to 1/8 Clock Input with Clock Output Rate Half Rate and Quarter Rate in Table 1.3.2.2-1.

Table 1.3.2.2-2 Jitter Setting Range (Cont'd)

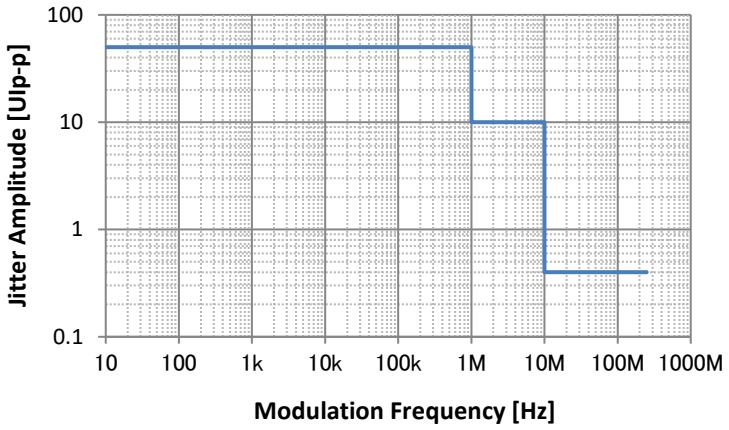
<table>
<tr><th>Item</th><th>Specifications*1</th></tr>
<tr><td>SJ1 Clock Output Rate At Half Rate, Quarter Rate (Cont'd)</td><td>
2.4 < Baud rate ≤ 8 Gbaud


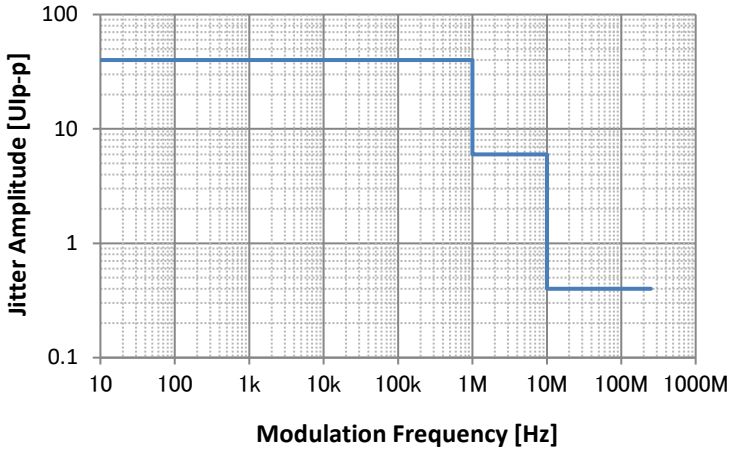
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 100k</td><td>0 to 2000</td></tr>
<tr><td>100.1k to 1M</td><td>0 to 200</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 16</td></tr>
<tr><td>10.01M to 100M</td><td>0 to 1</td></tr>
</table>
Baud rate 2.4 Gbaud


<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 100k</td><td>0 to 2000</td></tr>
<tr><td>100.1k to 1M</td><td>0 to 200</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 16</td></tr>
<tr><td>10.01M to 50M</td><td>0 to 1</td></tr>
</table>
</td></tr>
</table>

Table 1.3.2.2-2 Jitter Setting Range (Cont'd)

<table>
<tr><th>Item</th><th>Specifications*1</th></tr>
<tr><td>SJ2 Setting Range

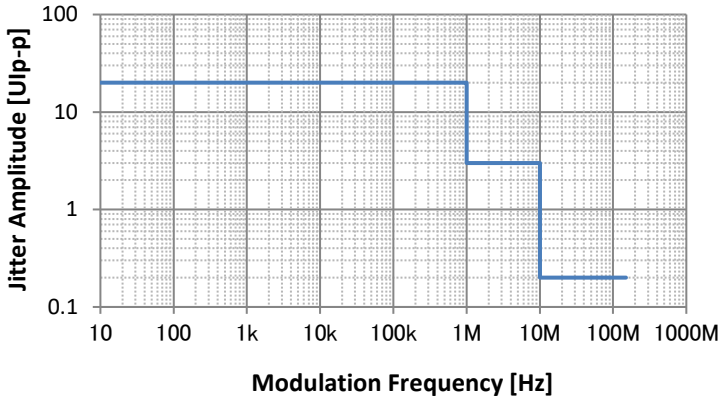
SJ2 via MU181000 Clock Output Rate At Full Rate</td><td>The SJ2 via MU181000 Clock and the Built-in SJ2 can be set exclusively.
15.000 001 ≤ Baud rate ≤ 32.1 Gbaud
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 1M</td><td>0 to 50</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 10</td></tr>
<tr><td>10.01M to 250M</td><td>0 to 0.4</td></tr>
</table>
6.400 001 ≤ Baud rate ≤ 15 Gbaud
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 1M</td><td>0 to 40</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 6</td></tr>
<tr><td>10.01M to 250M</td><td>0 to 0.4</td></tr>
</table></td></tr>
</table>

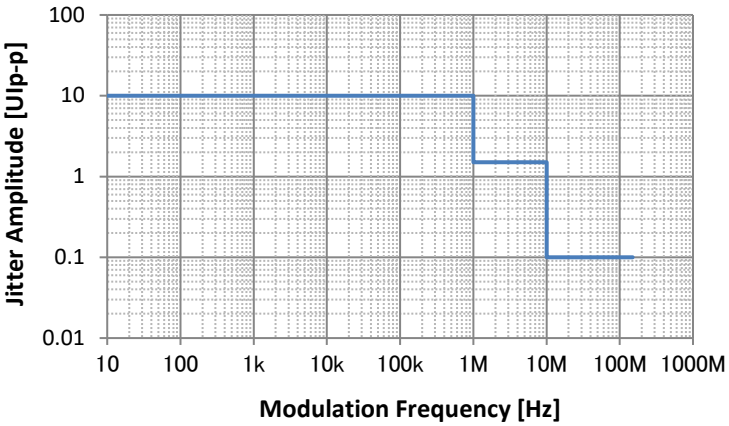
Table 1.3.2.2-2 Jitter Setting Range (Cont'd)

Item	Specifications*1
SJ2 via MU181000 Clock Output Rate At Full Rate (Cont'd)	3.200 001 ≤ Baud rate ≤ 6.25 Gbaud



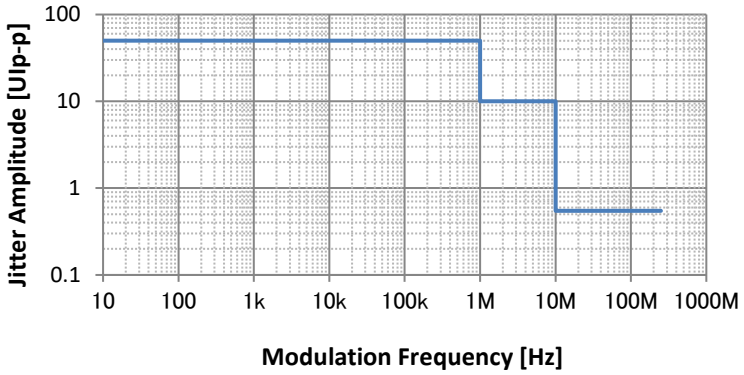
Modulation Frequency (Hz)	Jitter Amplitude (UIp-p)
10 to 1M	0 to 20
1.001M to 10M	0 to 3
10.01M to 150M	0 to 0.2

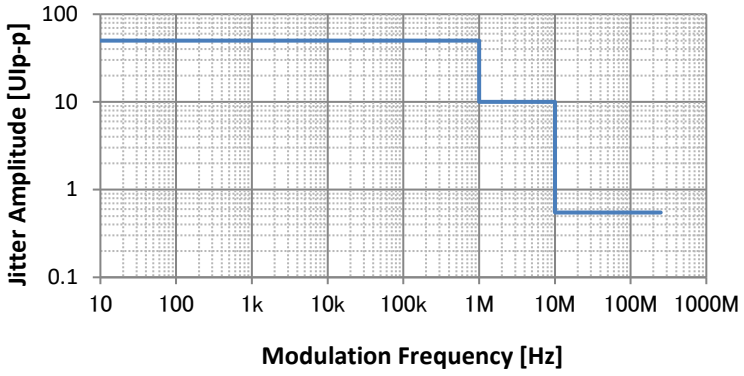
2.4 ≤ Baud rate ≤ 3.125 Gbaud



Modulation Frequency (Hz)	Jitter Amplitude (UIp-p)
10 to 1M	0 to 10
1.001M to 10M	0 to 1.5
10.01M to 150M	0 to 0.1

Table 1.3.2.2-2 Jitter Setting Range (Cont'd)

<table>
<tr><th>Item</th><th>Specifications*1</th></tr>
<tr><td>SJ2 via MU181000
Clock Output Rate
At Half Rate, Quarter Rate</td><td>60.000 001 ≤ Baud rate ≤ 64.2 Gbaud
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 1M</td><td>0 to 50</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 10</td></tr>
<tr><td>10.01M to 250M</td><td>0 to 0.544</td></tr>
</table>
30.000 001 ≤ Baud rate ≤ 60.0 Gbaud
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 1M</td><td>0 to 50</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 10</td></tr>
<tr><td>10.01M to 250M</td><td>0 to 0.548</td></tr>
</table>
</td></tr>
</table>

Table 1.3.2.2-2 Jitter Setting Range (Cont'd)

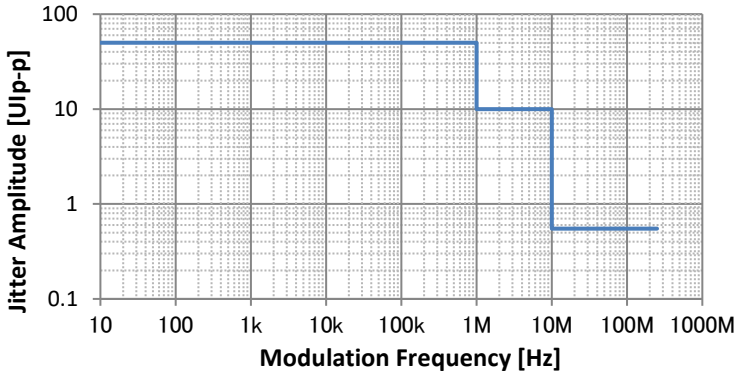
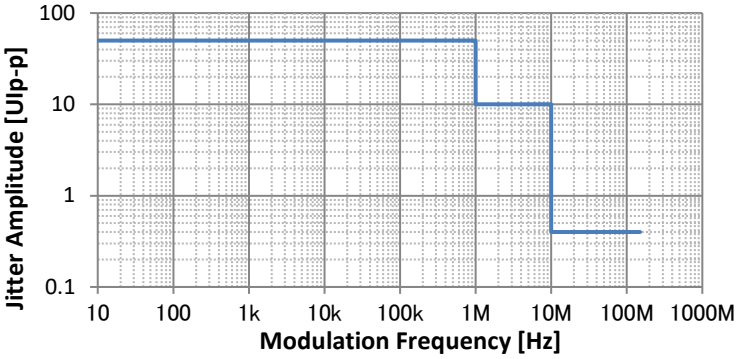
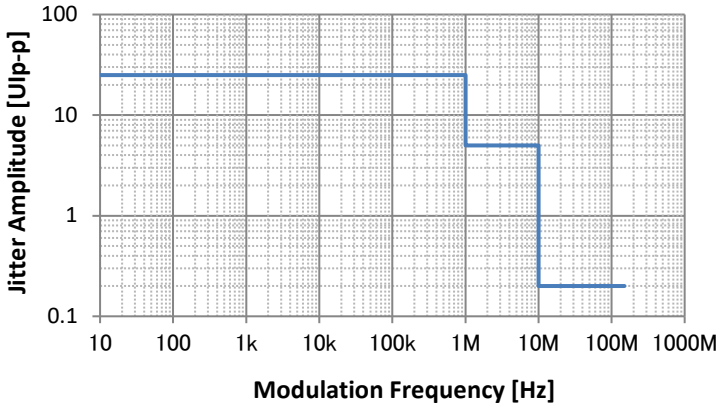
Item	Specifications*1
SJ2 via MU181000 Clock Output Rate At Half Rate, Quarter Rate (Cont'd)	12.800001 ≤ Baud rate ≤ 30.0 Gbaud  **Modulation Frequency (Hz) / Jitter Amplitude (UIp-p)** 10 to 1M: 0 to 50 1.001M to 10M: 0 to 10 10.01M to 250M: 0 to 0.55 6.400001 ≤ Baud rate ≤ 12.5 Gbaud  **Modulation Frequency (Hz) / Jitter Amplitude (UIp-p)** 10 to 1M: 0 to 50 1.001M to 10M: 0 to 10 10.01M to 150M: 0 to 0.4

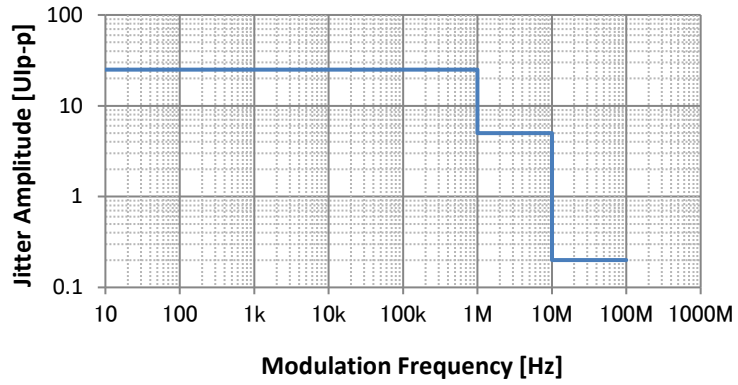
Table 1.3.2.2-2 Jitter Setting Range (Cont'd)

Item	Specifications*1
SJ2 via MU181000 Clock Output Rate At Half Rate, Quarter Rate (Cont'd)	3.600001 ≤ Baud rate ≤ 6.25 Gbaud



Modulation Frequency (Hz)	Jitter Amplitude (UIp-p)
10 to 1M	0 to 25
1.001M to 10M	0 to 5
10.01M to 150M	0 to 0.2

3.200001 < Baud rate ≤ 3.6 Gbaud



Modulation Frequency (Hz)	Jitter Amplitude (UIp-p)
10 to 1M	0 to 25
1.001M to 10M	0 to 5
10.01M to 100M	0 to 0.2

Table 1.3.2.2-2 Jitter Setting Range (Cont'd)

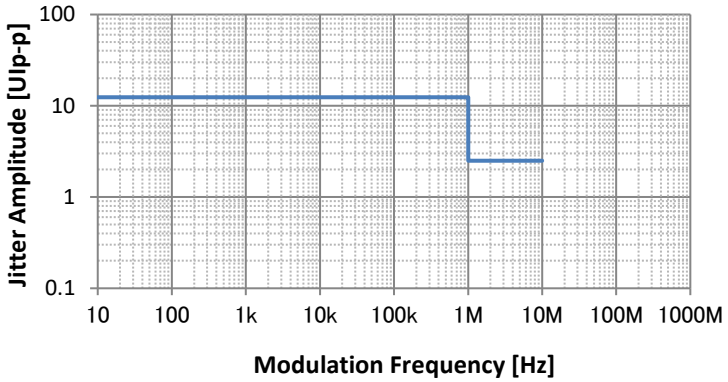
Item	Specifications*1
SJ2 via MU181000 Clock Output Rate At Half Rate, Quarter Rate (Cont'd)	2.4 ≤ Baud rate ≤ 3.125 Gbaud  **Modulation Frequency (Hz)** / **Jitter Amplitude (UIp-p)** 10 to 1M / 0 to 12.4 1.001M to 10M / 0 to 2.5

Table 1.3.2.2-2 Jitter Setting Range (Cont'd)

<table>
<tr><th>Item</th><th>Specifications*1</th></tr>
<tr><td>Built-in SJ2 Clock Output Rate
At Full Rate</td><td>15 < Baud rate ≤ 32.1 Gbaud
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (Ulp-p)</th></tr>
<tr><td>33k</td><td>0 to 1000</td></tr>
<tr><td>87M</td><td>0 to 0.5</td></tr>
<tr><td>100M</td><td>0 to 0.5</td></tr>
<tr><td>210M</td><td>0 to 0.2</td></tr>
</table>
4 < Baud rate ≤ 15 Gbaud
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (Ulp-p)</th></tr>
<tr><td>33k</td><td>0 to 500</td></tr>
<tr><td>87M</td><td>0 to 0.25</td></tr>
<tr><td>100M</td><td>0 to 0.25</td></tr>
<tr><td>210M</td><td>0 to 0.1</td></tr>
</table>
2.4 ≤ Baud rate ≤ 4 Gbaud
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (Ulp-p)</th></tr>
<tr><td>33k</td><td>0 to 500</td></tr>
<tr><td>87M</td><td>0 to 0.25</td></tr>
<tr><td>100M</td><td>0 to 0.25</td></tr>
</table></td></tr>
<tr><td>Built-in SJ2 Clock Output Rate
At Half Rate, Quarter Rate</td><td>8 < Baud rate ≤ 64.2 Gbaud
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (Ulp-p)</th></tr>
<tr><td>33k</td><td>0 to 1000</td></tr>
<tr><td>87M</td><td>0 to 0.5</td></tr>
<tr><td>100M</td><td>0 to 0.5</td></tr>
<tr><td>210M</td><td>0 to 0.2</td></tr>
</table>
2.4 < Baud rate ≤ 8 Gbaud
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (Ulp-p)</th></tr>
<tr><td>33k</td><td>0 to 1000</td></tr>
<tr><td>87M</td><td>0 to 0.5</td></tr>
<tr><td>100M</td><td>0 to 0.5</td></tr>
</table>
Baud rate 2.4 Gbaud
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (Ulp-p)</th></tr>
<tr><td>33k</td><td>0 to 1000</td></tr>
</table></td></tr>
</table>

Table 1.3.2.2-3 External Clock Input

Item	Specifications
Number of Inputs	1 (Single-Ended)
Input frequency range	1.2 to 16.05 GHz
Input amplitude	0.3 to 1.0 Vp-p (–6.5 to +4.0 dBm)
Termination	50 Ω, AC Coupling
Connector	SMA connector (f.)

Table 1.3.2.2-4 AUX Input

Item	Specifications
Number of Inputs	1 (Single-Ended)
Variation	Error Injection, Burst, Unit Sync, Jitter Sync
Minimum Pulse Width	1/256 of data rate
Input level	• 0/–1 V (H: –0.25 to 0.05 V, L: –1.1 to –0.8 V) • 0/–0.5 V (H: –0.05 to 0.05 V, L: –0.55 to –0.45 V) • Vth 0 V (Input amplitude: 0.5 to 1.0 Vp-p) Select one of the above.
Termination	50 Ω, GND
Connector	SMA connector (f.)

Table 1.3.2.2-5 AUX Output

Item	Specifications
Number of Outputs	2 (Differential output)
Output control	ON/OFF switching
Variation	1/n Clock (n = 8, 12, 16, 20...1020, 1024), Pattern Sync, Burst Out2
Pattern Sync PRBS, PRGM	Position: 1 to {(Least common multiple of Pattern Length' and 256) –263}, in 8 steps When the pattern length is 1023 bits or less, Pattern Length' is the length as an integer multiple so that it becomes 1024 bits or more.
Burst Out2 Burst Trigger Delay Pulse Width	 0 to (Burst Cycle – 256) bits, in steps of 8 bits 16 to (Burst Cycle – 256) bits, in steps of 8 bits
Output level	0/–0.6 V (H: –0.25 to 0.05 V, L: –0.80 to –0.45 V)
Termination	50 Ω, GND
Connector	SMA connector (f.)

Table 1.3.2.2-6 Gating Output

Item	Specifications
Number of Outputs	1 (Single-Ended)
Output control	ON/OFF switching
Variation	Burst, Repeat
Burst	Burst Output
Burst Trigger Delay	0 to (Burst Cycle – 256) bits, in steps of 8 bits
Enable Pulse Width	16 to (Burst Cycle – 256) bits, in steps of 8 bits
Output Level	0/–1 V (H: –0.25 to 0.05 V, L: –1.25 to –0.8 V)*
Repeat	Timing Signal Output
Timing Signal Cycle	INT ($\frac{\text{Pattern length'}}{256}$) × 256
Timing Signal Delay	0 to {(Least common multiple of Pattern Length' and 256) –256} The maximum settable number is 68 719 476 480, in steps of 8 bits When the pattern length is 1023 bits or less, Pattern Length' is the length as an integer multiple so that it becomes 1024 bits or more.
Timing Signal Pulse Width	256 to {(Least common multiple of Pattern Length' and 256) –256} The maximum settable number is 68 719 476 480, in steps of 8 bits When the pattern length is 1023 bits or less, Pattern Length' is the length as an integer multiple so that it becomes 1024 bits or more.
Output Level	0/–1 V (H: –0.25 to 0.05 V, L: –1.25 to –0.8 V)*
Unit Sync Output	Outputs the timing signal when **Unit Sync** is set to **ON**.
Termination	50 Ω, GND
Connector	SMA connector (f.)

*: L: Output Enable, H: Output Disable

Table 1.3.2.2-7 Pattern Generation

Item	Specifications
PRBS	
Pattern Length	2^n–1 (n = 7, 9, 10, 11, 13, 15, 20, 23, 31)
Mark ratio	1/2 (1/2INV is supported by a logical inversion.)
PRBS generator polynomial	n = 7: $1 + X^6 + X^7$ n = 9: $1 + X^5 + X^9$ n = 10: $1 + X^7 + X^{10}$ n = 11: $1 + X^9 + X^{11}$ n = 13: $1 + X + X^2 + X^{12} + X^{13}$ n = 15: $1 + X^{14} + X^{15}$ n = 20: $1 + X^3 + X^{20}$ n = 23: $1 + X^{18} + X^{23}$ n = 31: $1 + X^{28} + X^{31}$
PRBS Inversion	This is available in PAM4 mode only. Logical inversion of PRBS can be set independently for MSB and LSB.
PRBS 1st Bit	MSB or LSB can be selected to set the 1st bit of the PRBS Generator.

Table 1.3.2.2-7 Pattern Generation (Cont'd)

Item	Specifications
Zero-Substitution	This is available in NRZ mode only.
Additional bit	0 bit, 1 bit
Pattern Length	2^n (n = 7, 9, 10, 11, 15, 20, 23) 2^n–1 (n = 7, 9, 10, 11, 15, 20, 23)
Start position	Bit after the longest run of zero bits
Length of Consecutive Zero Bits	1 to (Pattern Length – 1) bits If the bit coming after Zero-substitution is "0", then it is replaced with "1".
Data	
Data Length	NRZ: 2 to 268 435 456 bits, in steps of 1 bit PAM4/PAM3: 2 to 268 435 456 symbols, in steps of 1 symbol
Bit Shift	This is available in PAM4 mode only. Bit shift of MSBs can be controlled in the range of ±256 bits (in steps of 1 bit).
PAM4 Standard Pattern	Standard-compliant PAM4-mode patterns
CEI	QPRBS13-CEI, QPRBS31-CEI
IEEE	IEEE802.3bs/cd: PRBS13Q, PRBS31Q, SSPRQ, Square Wave IEEE802.3bj: QPRBS13, JP03A, JP03B, Transmitter Linearity
InfiniBand	PRBS13Q (InfiniBand), PRBS23Q, PRBS31Q (InfiniBand)
Fibre Channel	PRBS31Q (Fibre Channel)
RS-FEC	With Option z42 RS-FEC Scrambled Idle 50G 1Lane, RS-FEC Scrambled Idle 100G 1Lanes, RS-FEC-Int Scrambled Idle 100G 1Lanes, RS-FEC Scrambled Idle 100G 2Lanes, RS-FEC Scrambled Idle 200G 2Lanes, RS-FEC Scrambled Idle 200G 4Lanes, RS-FEC Scrambled Idle 400G 4Lanes, RS-FEC Scrambled Idle 400G 8Lanes
PCIe	CP in 1b/1b Encoding for PCIe6 MCP in 1b/1b Encoding for PCIe6 Jitter Measurement Pattern in 1b/1b Encoding for PCIe6 High Swing Toggle Pattern in 1b/1b Encoding for PCIe6 Low Swing Toggle Pattern 1b/1b Encoding for PCIe6 Jitter Calibration Pattern for PCIe6 Preset Calibration Pattern for PCIe6 With Option w43 NOP Flit Layout in a x1 Link NOP Flit Layout in a x2 Link NOP Flit Layout in a x4 Link NOP Flit Layout in a x8 Link NOP Flit Layout in a x16 Link

Table 1.3.2.2-7 Pattern Generation (Cont'd)

Item	Specifications
NRZ Standard Pattern	Standard-compliant NRZ-mode pattern
CEI	SSPR
RS-FEC	With Option z42 RS-FEC Scrambled Idle 25G 1Lane, RS-FEC Scrambled Idle 50G 2Lanes RS(544,514), RS-FEC Scrambled Idle 100G 4Lanes, RS-FEC Scrambled Idle 100G 4Lanes RS(544,514)
PCIe	CP in 8b/10b Encoding for PCIe1 MCP in 8b/10b Encoding for PCIe1 Jitter Calibration Pattern for PCIe1 Preset Calibration Pattern for PCIe1 CP in 8b/10b Encoding for PCIe2 MCP in 8b/10b Encoding for PCIe2 Jitter Calibration Pattern for PCIe2 Preset Calibration Pattern for PCIe2 CP in 128b/130b Encoding for PCIe3 MCP in 128b/130b Encoding for PCIe3 Jitter Calibration Pattern for PCIe3 Preset Calibration Pattern for PCIe3 CP in 128b/130b Encoding for PCIe4 MCP in 128b/130b Encoding for PCIe4 Jitter Calibration Pattern for PCIe4 Preset Calibration Pattern for PCIe4 CP in 128b/130b Encoding for PCIe5 MCP in 128b/130b Encoding for PCIe5 Jitter Calibration Pattern for PCIe5 Preset Calibration Pattern for PCIe5
PRTS	
PRTS Length	3^n-1 (n = 7, 19)
PRTS generator polynomial	n=7 : $1 + X^2 + 2X^7$ Over GF(3) n=19 : $1 + X^2 + 2X^{19}$ Over GF(3)

Table 1.3.2.2-7 Pattern Generation (Cont'd)

Item	Specifications
PAM3 Standard Pattern	With Option z45
USB4 Gen4	PRBS TS2.clksw USB4 Gen4 Power Management State Signal USB4 Gen4 Rx Frequency Variation Training Sequence
USB4 Gen4 Power Management State Signal	
tPeriod	20 to 80 ns, in steps of 10 ns
Duty Cycle	45%, 50%, 55 %
tPreData	80 to 120 ns, in steps of 10 ns
LFPS Diff.Amp	Displays the differential amplitude of the LFPS signal.
LFPS Repetition	50 to 150 times, in steps of 10 times
USB4 Data	PRBSn (n = 7, 9, 10, 11, 13, 15, 20, 23, 31) PRTS7, 19 Data TS2.clksw
Transmit	Starts the LFPS signal transmission.
Manual	Transitions the state from the LFPS signal to USB4 Data.
Break	Manual, Auto Manual: Transitions to the next state, triggered by clicking **Manual**. Auto: Transitions to the next state at the time set to switch.
LFPS Swing	High, Low Sets the amplitude of the LFPS. High: Outputs the amplitude of 0/2 Level. Low: Outputs the amplitude of 0/1 Level.
USB4 Gen4 Rx Frequency Variation Training Sequence	Linked with the MU181500B's SSC Clock switching function.
Transmit	Starts the Rx Frequency Variation Training Sequence signal transmission.
Manual	Changes the output pattern.
Time	Sets the output time by pattern. Pattern output time for other than the final state 10.0 to 20.0 us, in steps of 0.1 us Pattern output time for the final state 1 to 10,000 ms, in steps of 1 ms

Table 1.3.2.2-7 Pattern Generation (Cont'd)

Item	Specifications
Pattern	Sets the sequence pattern. PRBSn (n = 7, 9, 10, 11, 13, 15, 20, 23, 31) PRTS7, 19 TS2.clksw*1
Break	Manual, Auto Manual: Transitions to the next state, triggered by clicking **Manual**. Auto: Transitions to the next state at the time set to switch.

*1: Only when Type II is selected, this is automatically fixed at Flow No3.

Table 1.3.2.2-7 Pattern Generation (Cont'd)

Item	Specifications
Sequence	With Option 51, when the BERT for PCIe1-6 Forced Link application is executed:
Specification	NRZ: PCIe1, PCIe2, PCIe3, PCIe4, PCIe5/CXL1-2 PAM4: PCIe6/CXL3
Logic	POS, NEG
PRBS Inversion	ON, OFF NRZ: Sets the logic inversion of the PRBS. PAM4: Sets the logic inversion of the PRBS for both the MSB and LSB simultaneously.
Transmit	Starts the Sequence pattern transmission. The green LED on the button is lit during transmission.
Manual	Available only when Trigger is set to Manual Trigger.
Trigger Block No.	Sets the block number of the sequence that outputs an LTSSM Trigger signal from the AUX Output connector. 1 to 256 Block No., in steps of 1 block
Sequence Editor	When Option 51 is installed. When the BERT for PCIe1-6 Forced Link application is executed.
Preset	Sets the Emphasis Preset for each PCIe standard. A preset number can be individually assigned to each standard. PCIe1 to PCIe5 and CXL1 to CXL2 share a common Emphasis preset. 2.5G, 5.0G, 8.0G, 16.0G, 32.0G: P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10 64.0G: Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10
Break	External, Manual, OFF
Loop	Time, Num
Loop Time	1 to 1 000 000 us, in steps of 1 us
Loop Num	If the pattern length is not a multiple of 16, the value can range from 2 to 1 000 000 in increments of 2. If the pattern length is a multiple of 16, the value can range from 1 to 1 000 000 in increments of 1.
Insert OS	
SKP OS	
SKP OS Insertion	ON, OFF
SKP OS Reset	ON, OFF
Symbol Length	Sets the symbol length of the SKP OS. This setting applies to all blocks. 8b10b: COM+1, COM+2, COM+3, COM+4, COM+5 128b130b: 8, 12, 16, 20, 24 1b1b: 24, 32, 40, 48, 56

Table 1.3.2.2-7 Pattern Generation (Cont'd)

Item	Specifications
Interval for Common Clock/SRNS	Sets the interval length of the SKP OS. This setting applies to all blocks. 8b10b: 76 to 3076 symbols, in steps of 2 symbols 128b130b: 20 to 750 blocks, in steps of 1 block 1b1b: 38 to 1500 blocks, in steps of 1 block
Interval for SRIS	Sets the interval length of the SRIS. This is enabled only when **SRIS** is set to **ON**. This setting applies to the block set by Enable SRIS from Block and all subsequent blocks. 8b10b: 76 to 3076 symbols, in steps of 2 symbols 128b130b: 20 to 750 blocks, in steps of 1 block 1b1b: 38 to 152 blocks, in steps of 1 block
Symbol Length x2	Sets whether to double the symbol length of the SKP OS. This setting applies to all blocks. ON, OFF
SRIS	ON, OFF
Link Width	Sets the total number of transmission lanes. x1, x2, x4 *2
Enable SRIS from Block #	Sets the Block No. to which the SRIS setting is applied. This is enabled only when **SRIS** is set to **ON**. 1 to 256 blocks, in steps of 1 block
68B NULL Flit SKP OS Interval	With Option 56 Sets the SKP Interval length of the 68B NULL Flit. Sync Header Bypass ON: 20 to 750 Blocks, 1 Block step Sync Header Bypass OFF: 20 to 750 Blocks, 1 Block step
256B Flit SKP OS Interval for Common Clock/SRNS	With Option 56 Sets the SKP interval length for 256B Flit under Common Clock/SRNS. 128b130b: 11 to 186 Flits, 1 Flit step 1b1b: 23 to 374 Flits, 1 Flit step
256B Flit SKP OS Interval for SRIS	With Option 56 Enabled only when **SRIS** is set to **ON**. This setting applies to all 256B Flit blocks after the block specified in "Enable SRIS from Block". Sets the SKP interval length for 256B Flit under SRIS. 128b130b: 1 to 18 Flits, 1 Flit step 1b1b: 2 to 36 Flits, 1 Flit step

*2: Only x1 can be selected without Option z52

Table 1.3.2.2-7 Pattern Generation (Cont'd)

Item	Specifications
EIEOSQ	
EIEOSQ Insertion	ON, OFF
EIEOSQ Reset	ON, OFF
EIEOSQ Interval	1 to 65536 pattern repeats, 1 step
EIEOS Count	Sets the number of EIEOS in the EIEOSQ. 2.5G, 5.0G, 8.0G, 16.0G: 1 32.0G: 2 64.0G: 1, 4
Coding	
Scrambler Seed	Sets the Seed value. This setting applies to all blocks. 8b10b: FFFF 128b130b/1b1b: Lane0, Lane1, Lane2, Lane3, Lane4, Lane5, Lane6, Lane7
Scrambler Type	2.5G, 5.0G, 8.0G, 16.0G, 32.0G: NRZ 64.0G: NRZ, PAM4
Pre Coder	2.5G, 5.0G, 8.0G, 16.0G: OFF 32.0G, 64.0G: ON, OFF
Gray Coder	2.5G, 5.0G, 8.0G, 16.0G, 32.0G: OFF 64.0G: ON, OFF
Sync Header Bypass	With Option 56 Sets whether to insert the Sync Header for CP and MCP patterns in 128b130b encoding. Within a continuous bit-rate section bounded by Electrical Idle, the same setting applies. 2.5G, 5.0G, 64.0G: OFF 8.0G, 16.0G, 32.0G: ON, OFF

Table 1.3.2.2-7 Pattern Generation (Cont'd)

Item	Specifications
PCIe1	
Bitrate	2.5 Gbit/s
Coding	8b10b
Block number	1 to 256 blocks
Pattern Length	8b10b: 32 to 1024 bits, in steps of 8 bits Idle Flit 8b10b: 2048/x bits (x = 1, 2, 4 (Setting value of Lane Width)) General Pattern (PRBS): 2n–1 (n = 7, 9, 10, 11, 13, 15, 20, 23, 31) General Pattern (Data): 2 to 268 435 456 bits, in steps of 1 bit
Pattern Type	Electrical Idle, 8b10b, Idle Flit 8b10b, General Can be set to **General** for the last block only.
PCIe2	
Bitrate	2.5, 5.0 Gbit/s
Coding	8b10b
Block number	1 to 256 blocks
Pattern Length	8b10b: 32 to 1024 bits, in steps of 8 bits Idle Flit 8b10b: 2048/x bits (x = 1, 2, 4 (Setting value of Lane Width)) General Pattern (PRBS): 2n–1 (n = 7, 9, 10, 11, 13, 15, 20, 23, 31) General Pattern (Data): 2 to 268 435 456 bits, in steps of 1 bit
Pattern Type	Electrical Idle, 8b10b, Idle Flit 8b10b, General Can be set to **General** for the last block only.
PCIe3	
Bitrate	2.5, 5.0, 8.0 Gbit/s
Coding	8b10b: Available only when the bitrate is 2.5 Gbit/s or 5.0 Gbit/s. 128b130b: Available only when the bitrate is 8.0 Gbit/s.
Block number	1 to 256 blocks
Pattern Length	8b10b: 32 to 1024 bits, in steps of 8 bits Idle Flit 8b10b: 2048/x bits (x = 1, 2, 4 (Setting value of Lane Width)) 128b130b: 128 to 1024 bits, in steps of 128 bits Idle Flit 128b130b: 2048/x bits (x = 1, 2, 4 (Setting value of Lane Width)) 68B NULL Flit128b130b: 128 to 1024 bits, 128 bits step 256B NULL Flit128b130b: 128 to 1024 bits, 128 bits step SDS 128b130b: 128 to 1024 bits, 128 bits step General Pattern (PRBS): 2n–1 (n = 7, 9, 10, 11, 13, 15, 20, 23, 31) General Pattern (Data): 2 to 268 435 456 bits, in steps of 1 bit
Pattern Type	Electrical Idle, 8b10b, Idle Flit 8b10b, 128b130b, Idle Flit 128b130b, General With Option 56, the following settings are supported: 68B NULL Flit 128b130b, 256B NULL Flit 128b130b, SDS 128b130b Can be set to **General** for the last block only.

Table 1.3.2.2-7 Pattern Generation (Cont'd)

Item	Specifications
PCIe4	
Bitrate	2.5, 5.0, 8.0, 16.0 Gbit/s
Coding	8b10b: Available only when the bitrate is 2.5 Gbit/s or 5.0 Gbit/s. 128b130b: Available only when the bitrate is 8.0 Gbit/s or 16.0 Gbit/s.
Block number	1 to 256 blocks
Pattern Length	8b10b: 32 to 1024 bits, in steps of 8 bits Idle Flit 8b10b: 2048/x bits (x = 1, 2, 4 (Setting value of Lane Width)) 128b130b: 128 to 1024 bits, in steps of 128 bits Idle Flit 128b130b: 2048/x bits (x = 1, 2, 4 (Setting value of Lane Width)) 68B NULL Flit128b130b: 128 to 1024 bits, 128 bits step 256B NULL Flit128b130b: 128 to 1024 bits, 128 bits step SDS 128b130b: 128 to 1024 bits, 128 bits step General Pattern (PRBS): 2^n-1 (n = 7, 9, 10, 11, 13, 15, 20, 23, 31) General Pattern (Data): 2 to 268 435 456 bits, in steps of 1 bit
Pattern Type	Electrical Idle, 8b10b, Idle Flit 8b10b, 128b130b, Idle Flit 128b130b, General With Option 56, the following settings are supported: 68B NULL Flit 128b130b, 256B NULL Flit 128b130b, SDS 128b130b Can be set to **General** for the last block only.
PCIe5/CXL1-2	
Bitrate	2.5, 5.0, 8.0, 16.0, 32.0 Gbit/s
Coding	8b10b: Available only when the bitrate is 2.5 Gbit/s or 5.0 Gbit/s. 128b130b: Available only when the bitrate is 8.0 Gbit/s, 16.0 Gbit/s, or 32.0 Gbit/s.
Block number	1 to 256 blocks
Pattern Length	8b10b: 32 to 1024 bits, in steps of 8 bits Idle Flit 8b10b: 2048/x bits (x = 1, 2, 4 (Setting value of Lane Width)) 128b130b: 128 to 1024 bits, in steps of 128 bits Idle Flit 128b130b: 2048/x bits (x = 1, 2, 4 (Setting value of Lane Width)) 68B NULL Flit128b130b: 128 to 1024 bits, 128 bits step 256B NULL Flit128b130b: 128 to 1024 bits, 128 bits step SDS 128b130b: 128 to 1024 bits, 128 bits step General Pattern (PRBS): 2^n-1 (n = 7, 9, 10, 11, 13, 15, 20, 23, 31) General Pattern (Data): 2 to 268 435 456 bits, in steps of 1 bit
Pattern Type	Electrical Idle, 8b10b, Idle Flit 8b10b, 128b130b, Idle Flit 128b130b, General With Option 56, the following settings are supported: 68B NULL Flit 128b130b, 256B NULL Flit 128b130b, SDS 128b130b Can be set to **General** for the last block only.

Table 1.3.2.2-7 Pattern Generation (Cont'd)

Item	Specifications
PCIe6/CXL3	
Bitrate	2.5, 5.0, 8.0, 16.0, 32.0 Gbit/s, 32.0 GBaud PAM4
Coding	8b10b: Available only when the bitrate is 2.5 Gbit/s or 5.0 Gbit/s. 128b130b: Available only when the bitrate is 8.0 Gbit/s, 16.0 Gbit/s, or 32.0 Gbit/s. 1b1b: Available only when the bitrate is 32.0 GBaud PAM4.
Block number	1 to 256 blocks
Pattern Length	8b10b: 32 to 1024 bits, in steps of 8 bits Idle Flit 8b10b: 2048/x bits (x = 1, 2, 4 (Setting value of Lane Width)) 128b130b: 128 to 1024 bits, in steps of 128 bits Idle Flit 128b130b: 2048/x bits (x = 1, 2, 4 (Setting value of Lane Width)) 68B NULL Flit128b130b: 128 to 1024 bits, 128 bits step 256B NULL Flit128b130b: 128 to 1024 bits, 128 bits step SDS 128b130b: 128 to 1024 bits, 128 bits step 1b1b: 128 to 2048 bits, in steps of 128 bits Idle Flit 1b1b: 2048/x bits (x = 1, 2, 4 (Setting value of Lane Width)) 256B NULL Flit1b1b: 128 to 2048 bits, 128 bits step SDS 1b1b: 128 to 2048 bits, 128 bits step General Pattern (PRBS): 2^n-1 (n = 7, 9, 10, 11, 13, 15, 20, 23, 31) General Pattern (Data): 4 to 536 870 912 bits, in steps of 2 bits
Pattern Type	Electrical Idle, 8b10b, Idle Flit 8b10b, 128b130b, Idle Flit 128b130b, 1b1b, Idle Flit 1b1b, General With Option 56, the following settings are supported: 68B NULL Flit 128b130b, 256B NULL Flit 128b130b, SDS 128b130b, 256B NULL Flit 1b1b, SDS 1b1b Can be set to **General** for the last block only.
Block Loop Function*	Up to two levels of loop configuration are supported (Inner Loop and Outer Loop). Sequence execution can be controlled by configuring the Inner Loop and Outer Loop.
Block Loop Break	External, Manual, OFF The loop terminates at the last block when a break is detected. Inner Loop is available only when Block Loop Break is set to OFF.
Block Loop Count	Enabled only when Block Loop Break is set to OFF. 1 to 1024 times, 1 time step

*: Available in MX190000A version 10.08.00 or later.

Table 1.3.2.2-7 Pattern Generation (Cont'd)

Item	Specifications
PCIe Encoding Pattern Editor	With Option 51 and when the BERT for PCIe1-6 Forced Link application is executed:
8b10b Pattern Editor	
Notation	Symbol (8b10b), Bin, Hex
Scramble Enable	Scrambles the selected symbols. ON, OFF
Scramble Reset	Resets the scrambler seed value for the selected symbols. ON, OFF
Code	K-code, D-code
K code	K28.0, K28.1, K28.2, K28.3, K28.4, K28.5, K28.6, K28.7, K23.7, K27.7, K30.7
D code	D0.0 to D31.7
MSB/LSB First	MSB First, LSB First
128b130b Pattern Editor	
Notation	Bin, Hex
Scramble Enable	Scrambles the selected symbols. ON, OFF
Scramble Reset	Resets the scrambler seed value for the selected symbols. ON, OFF
DC Balance	Adds DC balance to Symbols 14 and 15. ON, OFF
Sync Header	Defines a 2-bit Sync Header.
MSB/LSB First	MSB First, LSB First
1b1b Pattern Editor	
Notation	Symbol (PAM4), Bin, Hex
Scramble Enable	Scrambles the selected symbols. ON, OFF
Scramble Reset	Resets the scrambler seed value for the selected symbols. ON, OFF
DC Balance	Adds DC balance to Symbols 7 and 15. ON, OFF
MSB/LSB First	MSB First, LSB First

Table 1.3.2.2-8 Pattern Sequence

Item	Specifications
Sequence	Repeat, Burst
Repeat	Continuous Pattern
Burst	This is available only when **Coding** is set to **NRZ**.
Source	Internal, External-Trigger (AUX Input), External-Enable (AUX Input)
Data Sequence	Restart, Consecutive, Continuous
Enable period	Internal: 12 800 to 2 147 483 136 bits, in steps of 256 bits External-Trigger, External-Enable: 12 800 to 2 147 483 648 bits, in steps of 256 bits
Burst Cycle	25 600 to 2 147 483 648 bits, in steps of 1 024 bits

Table 1.3.2.2-9 Coding

Item	Specifications
Coding	NRZ, PAM4, PAM3
NRZ	Normal, Invert
PAM4 Gray Coding	ON, OFF
PAM4 Precoding (1/(1 + D) mod 4)*1	ON, OFF
Delay Symbol	ON, OFF
SKP	No SKP, SKPx1, SKPx2
Preset	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10
SRIS	ON, OFF
EIEOS	ON
PAM3 Precoding (1/(1+D) mod 3) *2	ON, OFF
Polarity Inverse	ON, OFF Sets the polarity of the PAM3 signal.

*1: (1/(1+D) mod 4) is a generator polynomial defined in the IEEE802.3.

*2: (1/(1+D) mod 3) is a generator polynomial defined in the USB4.

Table 1.3.2.2-10 Error Addition

Item	Specifications
Type	Bit, Error on MSB, Error on LSB, Error on LSB&MSB, RS-FEC Symbol Error*1, PCIe6 FEC Symbol Error*2
Bit	This is available only when **Coding** is set to **NRZ**.
Source	Internal, External-Trigger (Rising edge trigger), External-Disable (L: Disable)
Error Variation	Repeat, Single (Cannot be selected when Source is External-Trigger.)
Error Rate	*E–n (* = 1 to 9, n = 3 to 12), Upper limit: 3.0E–3
Error Route	Select 1 to 32, Scan
Bit/Burst	Switching between Bit and Burst
Burst Length	1 to 256, 1 step

*1: With Option z42

*2: With Option w43

Table 1.3.2.2-10 Error Addition (Cont'd)

Item	Specifications
RS-FEC Symbol Error	This is available whether Coding is NRZ or PAM4.*1 When Coding is PAM4, an error is inserted to make the PAM4 signal change by one level only. NRZ: An error is inserted every 10 bits. PAM4: An error is inserted every 10 or 20 PAM4 symbols.
FEC Standard	When Coding is NRZ: RS-FEC Scrambled Idle 25G 1Lane, RS-FEC Scrambled Idle 50G 2Lanes RS(544,514), RS-FEC Scrambled Idle 100G 4Lanes, RS-FEC Scrambled Idle 100G 4Lanes RS(544,514) When Coding is PAM4: RS-FEC Scrambled Idle 50G 1Lane, RS-FEC Scrambled Idle 100G 1Lanes, RS-FEC-Int Scrambled Idle 100G 1Lane, RS-FEC Scrambled Idle 100G 2Lanes, RS-FEC Scrambled Idle 200G 2Lanes, RS-FEC Scrambled Idle 200G 4Lanes, RS-FEC Scrambled Idle 400G 4Lanes, RS-FEC Scrambled Idle 400G 8Lanes
Source	Internal, External-Trigger (Rising edge trigger), External-Disable (L: Disable)
Error Variation	Repeat, Single (Cannot be selected when Source is External-Trigger.)
Symbol error per codeword	1 to 20 (When Coding is NRZ.) 1 to 20 (When Coding is PAM4.)
Total BER for All Lane	*E–n (* = 1 to 9, n = 3 to 12), Upper limit: 3.0E–3 The error addition range varies depending on the value of Symbol Error per Codeword.
BER for One Lane/ SER for One Lane	*E–n (* = 1 to 9, n = 3 to 12), Upper limit:9.0E–3 The error addition range varies depending on the value of Symbol Error per Codeword.

Table 1.3.2.2-10 Error Addition (Cont'd)

Item	Specifications
RS-FEC Symbol Error (Cont'd) Error Addition Method	Type1: Level 0 → Level 1, Level 1 → Level 2, Level 2 → Level 3, Level 3 → Level 2 Type2: Level 0 → Level 1, Level 1 → Level 2, Level 2 → Level 1, Level 3 → Level 2 Type3: Level 0 → Level 1, Level 1 → Level 0, Level 2 → Level 1, Level 3 → Level 2 Type4: Level 0 → Level 1, Level 1 → Level 0 or Level 2, Level 2 → Level 1 or Level 3, Level 3 → Level 2 MSB Only: Level 0 → Level 2, Level 1 → Level 3, Level 2 → Level 0, Level 3 → Level 1 LSB Only: Level 0 → Level 1, Level 1 → Level 0, Level 2 → Level 3, Level 3 → Level 2 MSB or LSB: Level 0 → Level 1 or Level 2, Level 1 → Level 0 or Level 3, Level 2 → Level 0 or Level 3, Level 3 → Level 1 or Level 2 MSB and LSB: Level 0 → Level 3, Level 1 → Level 2, Level 2 → Level 1, Level 3 → Level 0

Table 1.3.2.2-10 Error Addition (Cont'd)

Item	Specifications
Error on MSB	Adds the specified symbol error. This is available only when **Coding** is set to **PAM4**. The set error is added to MSB only.
Source	Internal, External-Trigger (Rising edge trigger), External-Disable (L: Disable)
Error Variation	Repeat, Single (Cannot be selected when Source is External-Trigger.)
Symbol Error Rate	*E–n (* = 1 to 9, n = 3 to 12), Upper limit: 3.0E–3
Symbol/Burst	Switching between Symbol and Burst
Burst Length	1 to 256, 1 step
Error on LSB	Adds the specified symbol error. This is available only when **Coding** is set to **PAM4**. The set error is added to LSB only.
Source	Internal, External-Trigger (Rising edge trigger), External-Disable (L: Disable)
Error Variation	Repeat, Single (Cannot be selected when Source is External-Trigger.)
Symbol Error Rate	*E–n (* = 1 to 9, n = 3 to 12), Upper limit: 3.0E–3
Symbol/Burst	Switching between Symbol and Burst
Burst Length	1 to 256, 1 step

Table 1.3.2.2-10 Error Addition (Cont'd)

Item	Specifications
Error on LSB&MSB	Adds the specified symbol error. This is available only when **Coding** is set to **PAM4**. An error is inserted to make the PAM4 signal change by one level only.
Source	Internal, External-Trigger (Rising edge trigger), External-Disable (L: Disable)
Error Variation	Repeat, Single (Cannot be selected when Source is External-Trigger.)
Symbol Error Rate	*E–n (* = 1 to 9, n = 3 to 12), Upper limit: 3.0E–3
Symbol/Burst	Switching between Symbol and Burst
Burst Length	1 to 256, 1 step
Error Addition Method	Type1: Level 0 → Level 1, Level 1 → Level 2, Level 2 → Level 3, Level 3 → Level 2 Type2: Level 0 → Level 1, Level 1 → Level 2, Level 2 → Level 1, Level 3 → Level 2 Type3: Level 0 → Level 1, Level 1 → Level 0, Level 2 → Level 1, Level 3 → Level 2 Type4: Level 0 → Level 1, Level 1 → Level 0 or Level 2, Level 2 → Level 1 or Level 3, Level 3 → Level 2 MSB Only: Level 0 → Level 2, Level 1 → Level 3, Level 2 → Level 0, Level 3 → Level 1 LSB Only: Level 0 → Level 1, Level 1 → Level 0, Level 2 → Level 3, Level 3 → Level 2 MSB or LSB: Level 0 → Level 1 or Level 2, Level 1 → Level 0 or Level 3, Level 2 → Level 0 or Level 3, Level 3 → Level 1 or Level 2 MSB and LSB: Level 0 → Level 3, Level 1 → Level 2, Level 2 → Level 1, Level 3 → Level 0

Table 1.3.2.2-10 Error Addition (Cont'd)

Item	Specifications
PCIe6 FEC Symbol Error	This is available only when **Coding** is set to **PAM4**.*2 An error is inserted to make the PAM4 signal change by one level only. PAM4: An error is inserted every 4 or 12 PAM4 symbols.
Source	Internal, External-Trigger (Rising edge trigger), External-Disable (L: Disable)
Error Variation	Repeat, Single (Cannot be selected when Source is External-Trigger.)
PCIe6 Standard	x1 Link Common CLK/SRNS Mode x2 Link Common CLK/SRNS Mode x4 Link Common CLK/SRNS Mode x8 Link Common CLK/SRNS Mode x16 Link Common CLK/SRNS Mode x1 Link SRIS Mode x2 Link SRIS Mode x4 Link SRIS Mode x8 Link SRIS Mode x16 Link SRIS Mode
SKP	No SKP, SKPx1, SKPx2
Flit Error Interval	Add every 8 Bits(Do not distinguish ECC groups) Add every 24 Bits(Add to only ECC Group)
PAM4 Symbol Error per Flit	1 to 8 FEC Symbols, in steps of 1 FEC Symbol The upper limit value is "4" if PCIe6 Standard is set to one of the following: x16 Link Common CLK/SRNS Mode x16 Link SRIS Mode
Flit Error per Control SKP Interval	1 to 4 Flits, in steps of 1 Flit
Total BER for All Lane	*E–n (* = 1 to 9, n = 3 to 12), Upper limit: 4.0E–3 The error addition range varies depending on the PCIe6 Standard and the values set for PAM4 Symbol Error per Flit and Flit Error per Control SKP Interval.
PAM4 Symbol Error for One Lane	*E–n (* = 1 to 9, n = 3 to 12), Upper limit: 8.0E–3 The error addition range varies depending on the PCIe6 Standard and the values set for PAM4 Symbol Error per Flit and Flit Error per Control SKP Interval.

Table 1.3.2.2-10 Error Addition (Cont'd)

Item	Specifications
PCIe6 FEC Symbol Error (Cont'd)	
Error Addition Method	Type1: Level 0 → Level 1, Level 1 → Level 2, Level 2 → Level 3, Level 3 → Level 2 Type2: Level 0 → Level 1, Level 1 → Level 2, Level 2 → Level 1, Level 3 → Level 2 Type3: Level 0 → Level 1, Level 1 → Level 0, Level 2 → Level 1, Level 3 → Level 2 Type4: Level 0 → Level 1, Level 1 → Level 0 or Level 2, Level 2 → Level 1 or Level 3, Level 3 → Level 2 MSB Only: Level 0 → Level 2, Level 1 → Level 3, Level 2 → Level 0, Level 3 → Level 1 LSB Only: Level 0 → Level 1, Level 1 → Level 0, Level 2 → Level 3, Level 3 → Level 2 MSB or LSB: Level 0 → Level 1 or Level 2, Level 1 → Level 0 or Level 3, Level 2 → Level 0 or Level 3, Level 3 → Level 1 or Level 2 MSB and LSB: Level 0 → Level 3, Level 1 → Level 2, Level 2 → Level 1, Level 3 → Level 0
PAM3 Error Addition	This is available only when **Coding** is set to **PAM3**.
Error on LSB&MSB	Add the specified Symbol Error.
Source	Internal, External-Trigger (Rise edge trigger), External-Disable (L: Disable)
Error Variation	Repeat, Single (Cannot be selected when Source is External-Trigger.)
Symbol Error Rate	*E–n (* = 1 to 9, n = 3 to 12). Upper limit: 3.0E–3
Symbol/Burst	Symbol, Burst switching
Burst Length	1 to 256, 1 step
Error Addition Method	Type6: Level 0 → Level 2, Level 1 → Level 0, Level 2 → Level 0

Table 1.3.2.2-11 Data Output

Item	Specifications*1
Number of Outputs Waveform	2 (Data, XData) Cannot be varied independently NRZ, PAM4, PAM3
NRZ Eye Amplitude Setting Range Accuracy	 NRZ: 70 to 800 mVp-p, in steps of 2 mV (Single-Ended) When using the J1789A: ±35 mV ±12 % (Single-Ended)*2 When using the J1790A: ±35 mV ±12 % (Single-Ended)*3, *4, *5

*1: Unless otherwise specified, these are specified with the conditions of PRBS2^{31}–1, Mark ratio 1/2, and Cross Point 50 %.

The values shall be observed by using an optional accessory, J1789A or J1790A, and a 70-GHz bandwidth sampling oscilloscope.

*2: Setting Range ≤ 700 mVp-p

*3: Setting Range ≤ 700 mVp-p (≤ 32.1 Gbit/s)

*4: Setting Range ≤ 600 mVp-p (32.1 < Bit rate ≤ 58.2 Gbit/s)

*5: Setting Range ≤ 550 mVp-p (58.2 < Bit rate ≤ 64.2 Gbit/s)

Table 1.3.2.2-11 Data Output (Cont'd)

Item	Specifications*1
PAM3/PAM4 Eye Amplitude	
PAM4 (0/3 Level) Setting Range	PAM4(0/3 Level): 70 to 800 mVp-p, in steps of 1 mV (Single-Ended)*6
PAM4 (0/3 Level) Accuracy	When using the J1789A: ±35 mV ±12 % of Amplitude*2, *7 When using the J1790A: ±35 mV ±12 % of Amplitude*3, *4, *5, *7
PAM4 (0/1, 1/2, 2/3 Level) Independently variable	Provided, 20 to 50 %, in steps of 1 mV (Eye amplitude conversion) (PAM4 Amplitude 0/3 level is assumed to be 100 %.)
PAM4 (0/1, 1/2, 2/3 Level) Setting Range	PAM4(0/1 Level): 23 to 266 mVp-p, in steps of 1 mV (Single-Ended) PAM4(1/2 Level): 24 to 268 mVp-p, in steps of 1 mV (Single-Ended) PAM4(2/3 Level): 23 to 266 mVp-p, in steps of 1 mV (Single-Ended)
PAM4 (0/1, 1/2, 2/3 Level) Accuracy	When using J1789A: ±35 mV ±12 % of Amplitude*8 When using J1790A: ±35 mV ±12 % of Amplitude*9, *10, *11
PAM3 (0/2 Level) Setting Range	PAM3(0/2 Level): 48 to 532 mVp-p, in steps of 1 mV (Single-Ended)
PAM3 (0/2Level) Accuracy	When using J1789A: ±35 mV ±12 % of Amplitude*12, *16 When using J1790A: ±35 mV ±12 % of Amplitude*13, *14, *15, *16
PAM3 (0/1, 1/2 Level) Independently variable	Available, 20.0 to 80.0%, in steps of 0.1% (PAM3 Amplitude 0/2 level is assumed to be 100%.)
PAM3 (0/1, 1/2 Level) Setting Range	PAM3(0/1 Level): 24 to 266 mVp-p, in steps of 1 mV (Single-Ended) PAM3(1/2 Level): 24 to 266 mVp-p, in steps of 1 mV (Single-Ended) However, when the eye ratio is set, the amplitude can be set with a resolution finer than 1 mV.
PAM3 (0/1, 1/2 Level) Accuracy	When using J1789A: ±35 mV ±12 % of Amplitude*17 When using J1790A: ±35 mV ±12 % of Amplitude*18, *19, *20

*6: When PAM4 output signal is directly input to the ED, the lower limit for the error-free amplitude depends on the performance of the ED used.

When using MP1862A as ED, the lower limit for the error-free amplitude (reference data) is as follows:
125 mV (0/3 Level, ≤ 32.1 Gbaud)
250 mV (0/3 Level, ≤ 58.2 Gbaud)
Pattern: PRBS15, at a constant temperature between 20 and 30 °C

*7: Single-Ended, PAM4 0/3 Level, and when setting each of PAM4 Amplitude (3/2, 2/1 and 1/0) equally to 33 %

*8: Setting Range ≤ 234 mVp-p, Single-Ended, at each amplitude level (Upper, Middle, Lower)

*9: Setting Range ≤ 234 mVp-p, Single-Ended, at each amplitude level (Upper, Middle, Lower)
(≤ 32.1 Gbaud)

*10: Setting Range ≤ 200 mVp-p, Single-Ended, at each amplitude level (Upper, Middle, Lower)
(32.1 < Baud rate ≤ 58.2 Gbaud)

*11: Setting Range ≤ 184 mVp-p, Single-Ended, at each amplitude level (Upper, Middle, Lower)
(58.2 < Baud rate ≤ 64.2 Gbaud)

*12: Setting Range ≤ 466 mVp-p

*13: Setting Range ≤ 466 mVp-p
(≤ 32.1 Gbaud)

*14: Setting Range ≤ 400 mVp-p
(32.1 < Baud rate ≤ 58.2 Gbaud)

*15: Setting Range ≤ 366 mVp-p
(58.2 < Baud rate ≤ 64.2 Gbaud)

*16: Single-Ended, PAM3 0/2 Level, when setting each of PAM3 Amplitude (2/1 and 1/0) equally to 50%

*17: Setting Range ≤ 234 mVp-p, Single-Ended, at each amplitude level (Upper, Lower)

*18: Setting Range ≤ 234 mVp-p, Single-Ended, at each amplitude level (Upper, Lower)
(≤ 32.1 Gbaud)

*19: Setting Range ≤ 200 mVp-p, Single-Ended, at each amplitude level (Upper, Lower)
(32.1 < Baud rate ≤ 58.2 Gbaud)

*20: Setting Range ≤ 184 mVp-p, Single-Ended, at each amplitude level (Upper, Lower)
(58.2 < Baud rate ≤ 64.2 Gbaud)

Table 1.3.2.2-11 Data Output (Cont'd)

Item	Specifications*1
Offset Setting Range Accuracy	 –2.0–Eye Amplitude/2 to +3.3–Eye Amplitude/2 Vth, in steps of 1 mV (Single-Ended) ±65 mV ±10 % of offset (Vth) ± (Eye Amplitude Accuracy/2) (Except when Emphasis is turned On with the MU196020A-x11 installed.) (For PAM4, when setting each of PAM4 Amplitude (3/2, 2/1 and 1/0) equally to 33 %.) (For PAM3, when setting each of PAM3 Amplitude (2/1 and 1/0) equally to 50%.)
Glitch-free ON/OFF	Glitch-free switching that does not interrupt the PPG's output at frequency fluctuations ON, OFF switching
Cross Point	Typ. 50 % (fixed)
Tr/Tf	When using the J1789A: Typ. 9 ps (20-80 %)*21 Typ. 8.5 ps (20-80 %)*22 When using the J1790A: Typ. 9.5 ps (20-80 %)*21 Typ. 8.8 ps (20-80 %)*22
Half Period Jitter Setting Range	 –20.0 to +20.0, in steps of 0.1
Accuracy	Typ. ±0.04 UI*23

*21: NRZ, 32.1 Gbit/s, Eye Amplitude 0.5 Vp-p (Single-Ended), only when **Coding** is set to **NRZ** and **Emphasis** is set to **Off**.

*22: NRZ, 58.2 Gbit/s (with Option 002 or y12), 64.2 Gbit/s (with Option 003, y13, or y23), Eye Amplitude 0.5 Vp-p (Single-Ended), only when **Coding** is set to **NRZ** and **Emphasis** is set to **Off**.

*23: 2.4, 8, 16, 26.5625, 32.1 Gbit/s (with Option 001),
2.4, 8, 16, 26.5625, 32.1, 40, 53.125, 58.2 Gbit/s (with Option 002 or y12)
2.4, 8, 16, 26.5625, 32.1, 40, 53.125 ,58.2 ,64.2 Gbit/s (with Option 003, y13, or y23), Eye Amplitude 0.5 Vp-p (Single-Ended)

Table 1.3.2.2-11 Data Output (Cont'd)

Item	Specifications*1
Jitter	
Measurement conditions	NRZ, Bit rate 32.1 Gbit/s (with Option 001), 58.2 Gbit/s (with Option 002 or y12), 64.2 Gbit/s (with Option 003, y13, or y23) Eye Amplitude 0.5 Vp-p (Single-Ended) At a constant temperature between 20 and 30 °C, measure with a 70-GHz bandwidth sampling oscilloscope with residual jitter of less than 200 fs (RMS).
Peak-to-Peak Jitter	Typ. 6 ps p-p (Count of measured jitters: 30)
Jitter RMS	Typ. 600 fs rms (Count of measured jitters: 30)
Intrinsic RJ (RMS)	Typ. 170 fs (Repeating pattern of 1,0)*24
Waveform Distortion (0-peak)	Typ. ±110 mV*25
PAM4 Level Separation Mismatch Ratio (R_{LM})	0.95 (min.)*26
PAM4 Signal to noise and distortion ratio (SNDR)	33 dB (min.)*27, *28
PAM3 Signal to noise and distortion ratio (SNDR)	32.5 dB (min.)*29, *30

*24: NRZ, Bit rate 58.2 Gbit/s (with Option 002 or y12),
64.2 Gbit/s (with Option 003, y13, or y23)

*25: NRZ, Bit rate 32.1 Gbit/s (with Option 001),
58.2 Gbit/s (with Option 002 or y12),
64.2 Gbit/s (with Option 003, y13, or y23)
Eye Amplitude 0.5 Vp-p (Single-Ended)

*26: PAM4, 26.5625 Gbaud (with Option 001),
53.125 Gbaud (When Options 002, y12, 003, y13, and y23 are installed),
1.0 Vp-p (Differential), refer to the IEEE P802.3bs for equation to calculate.

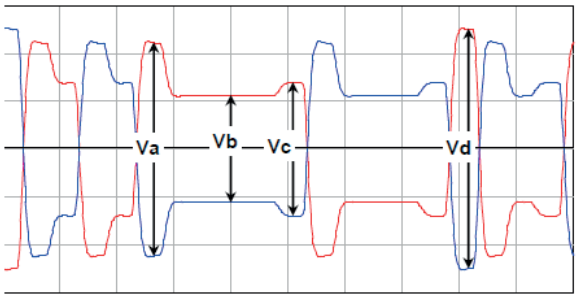
*27: PAM4, 26.5625 Gbaud (When Option 001 is installed),
53.125 Gbaud (When Options 002, y12, 003, y13, and y23 are installed),
1.0 Vp-p (Differential), refer to the IEEE P802.3cd for equation to calculate.

*28: 60-GHz bandwidth sampling oscilloscope

*29: PAM3, 25.600004 Gbaud
Refer to the calculation method of 1.0 Vp-p (Differential) and USB4 Gen4.

*30: 25 GHz bandwidth real-time oscilloscope

Table 1.3.2.2-11 Data Output (Cont'd)

Item	Specifications*1
Electrical TDECQ	0.9 dB*31
Output ON/OFF	ON/OFF switching available
Data / XData Skew	±1 ps Cable error not included.
Termination	AC, DC switching For DC: GND, –2V, +1.3V, +3.3V, Open (LVDS), 50 Ω
Connector	V connector (f.)
Offset Reference	Vth
Level Guard	Amplitude, Voh and Vol can be set.
External ATT Factor	–40 to 0 dB, in steps of 0.1 dB When the fixed attenuator is connected, the amplitude and offset of the signal output via the fixed attenuator are displayed.
Emphasis	With Option x11
Emphasis Tap	4 (1post-cursor, 2pre-cursor) 4 Tap parameter values for all eyes (Upper, Middle and Lower) become identical. This means that 4 Tap parameters for Upper, Middle and Lower Eyes cannot be controlled independently.
Cursor Setting Range / Step	–20 to +20 dB, in steps of 0.01 dB (Post-Cursor: $20\log_{10}Va/Vb$, Pre-Cursor: $20\log_{10}Vc/Vb$)  Provided that the maximum amplitude is restricted by the setting range of emphasis peak voltage.
Accuracy	Typ. ±1 dB (16 Gbaud, Amplitude 0.5 Vp-p (Single-Ended), De-Emphasis, Pre-Cursor1 = 6 dB, Post Cursor1 = 3.5 dB)
Setting Range of Emphasis Peak Voltage	• For NRZ and PAM4 modes 70 to 800 mVp-p (Single-Ended) • For PAM3 mode 48 to 532 mVp-p (Single-Ended)
Emphasis ON/OFF	ON/OFF switching

*31: 26.5625 Gbaud (with Option 001),
53.125 Gbaud (When Options 002, y12, 003, y13, and y23 are installed),
Using an equalizer, Single, Pattern: SSPRQ

Table 1.3.2.2-11 Data Output (Cont'd)

Item	Specifications*1
Channel Emulator*32, *33	Normal: Outputs the PPG Data signal whose waveform emulates the connected transmission line with the loaded S parameter. Inverse: Outputs the PPG Data signal whose inverse characteristics emulate the transmission line with the loaded S parameter.
Response	Normal, Inverse
S-Parameter file	S2P file (Extension: "*.s2p"), S4P file (Extension: "*.s4p") Supports output files from the MS4640B Series Vector Network Analyzer.
Channel Emulator ON/OFF	ON/OFF switching
Gain Adjust	Adjusts the loss to emulate and loss of the loaded S parameter at the specified frequency, when Response is Normal. 0GHz, 1GHz, Nyquist Frequency switching
Adjustable ISI*32	Sets the loss of the channel which generates ISI and outputs the PPG data signal whose waveform emulates the setting.
Loss Channel	This is available for MU196020A in combination with the following. Not Specified: an external loss channel board J1800A×1 Short Channel: one J1800A (optional accessory) J1800A×2 Middle Channel: two J1800As (optional accessory) J1800A×3 Long Channel: three J1800As (optional accessory) J1758A: a J1758A (optional accessory) MU195050A Noise: an MU195050A Noise Module
Frequency	Insertion Loss can be set at Nyquist or 1/2 Nyquist Frequency.

*32: With Option x40

*33: It is assumed to use for the purpose of compensating the loss of the transmission line.

The following graph shows typical limits for adjustable insertion loss. However, it does not mean that all the responses emulated from the S-Parameter file are compensated as the graph shows.

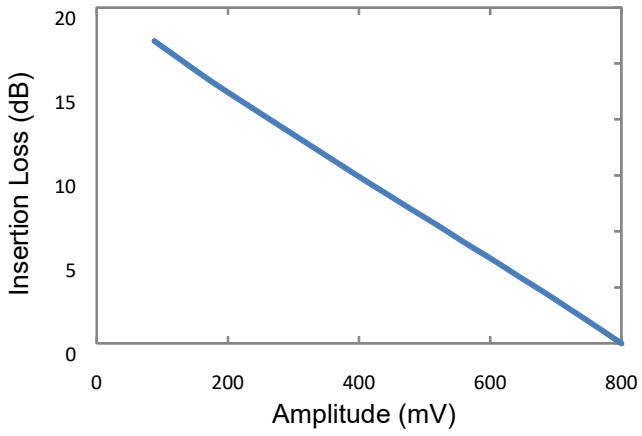


Table 1.3.2.2-11 Data Output (Cont'd)

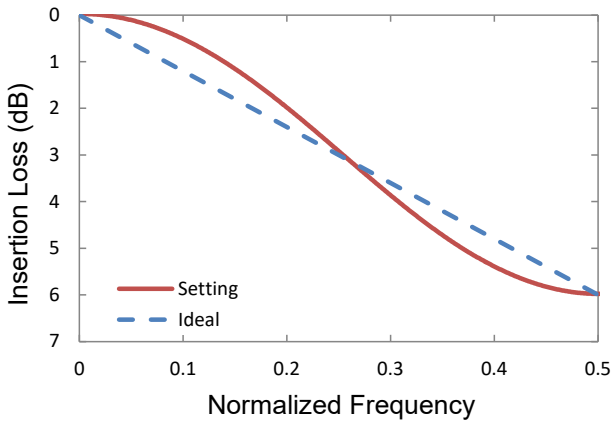
Item	Specifications*1
Insertion Loss	Displays the absolute loss that is sum of the loss selected for Loss Channel and the setting value of Tuning Insertion Loss at Nyquist Frequency and 1/2 Nyquist Frequency.
Tuning Insertion Loss	The relative loss from the loss value of Loss Channel can be set. –8.00 to 8.00 dB, in steps of 0.01 dB, Nyquist Frequency –8.00 to 8.00 dB, in steps of 0.01 dB, 1/2 Nyquist Frequency
Insertion Loss Accuracy	±1.0 dB Nominal @Nyquist Frequency 6 dB, Repeating pattern of "1,0" *34, *36, *37 ±1.5 dB Nominal @Nyquist Frequency 6 dB, Repeating pattern of "1,0" *35, *36, *37 ±1.0 dB Nominal @1/2Nyquist Frequency 3 dB, Repeating pattern of "1,1,0,0" *34, *36, *37 ±1.5 dB Nominal @1/2Nyquist Frequency 3 dB, Repeating pattern of "1,1,0,0" *35, *36, *37
Adjustable ISI ON/OFF	ON/OFF switching
Insertion Loss Compensation	With Options 11 and 45 Modulation: PAM3, Baud Rate: USB4 Gen4: Corrects the insertion loss at the Nyquist frequency by using Emphasis.
Setting Range	0.0 to 2.0 dB, in steps of 0.1 dB
Insertion Loss Accuracy	Since the BERT Insertion Loss*38 is calibrated using an oscilloscope, the accuracy of the setting value is not guaranteed, and it is set to Typ.
Insertion Loss Compensation ON/OFF	ON, OFF switching

*34: Baud Rate 26.6 Gbaud (when Option 001, 002, y12, 003, y13, and y23 installed)

*35: Baud Rate 53.1 Gbaud (when Option 002, y12, Option 003, y13, and y23 installed)

*36: Eye Amplitude 0.5 Vp-p, at each spectrum, at a constant temperature between 20 and 30 °C

*37: The frequency characteristics of Insertion Loss Accuracy when setting 6 dB@Nyquist Frequency and 3 dB@1/2 Nyquist Frequency are shown below.



*38: BERT Insertion Loss is a required specification for measuring instruments in the USB4 Version 2 GEN4 Electrical Compliance Test Specification (CTS).

Table 1.3.2.2-12 Clock Output

Item	Specifications*
Frequency	
Full Rate	Operation Baud Rate = Clock Output Frequency 2.4 to 32.1 GHz (Option 001)
Half Rate	Operation Baud Rate = (Clock Output Frequency) × 2 1.2 to 16.05 GHz (Option 001) 1.2 to 29.1 GHz (with Option 002 or y12) 1.2 to 32.1 GHz (with Option 003, y13, or y23)
Quarter Rate	Operation Baud Rate = (Clock Output Frequency) × 4 0.6 to 8.025 GHz (Option 001) 0.6 to 14.55 GHz (with Option 002 or y12) 0.6 to 16.05 GHz (with Option 003, y13, or y23)
Number of Outputs	1
Amplitude	Min. 0.3 Vp-p, Max. 1.0 Vp-p (Output Frequency ≤ 16.05 GHz) Min. 0.4 Vp-p, Max. 1.0 Vp-p (Output Frequency > 16.05 GHz)
Output control	ON, OFF switching
Termination	50 Ω, AC Coupling
Connector	K connector (f.)

*: These values are monitored using an optional accessory (J1439A) at a sampling oscilloscope bandwidth of 70 GHz.

Table 1.3.2.2-13 Data Delay*1

Item	Specifications
Phase variable range	–1000 to +1000 mUI, in steps of 2 mUI
Accuracy	±50 mUIp-p*2, *3, *4 ±100 mUIp-p*2, *3, *5
mUI – ps switching	Available (internally converted into ps)
Calibration	Available (when jitter modulation is off)
Calibration indicator	This is displayed when one of the following conditions is met: ● 1/1 Clock frequency change by ±250 kHz. ● Ambient temperature change by ±5°C.

*1: With Option x30

*2: Measured with a sampling oscilloscope with residual jitter of less than 200 fs (RMS), at a constant amplitude setting.

*3: Typical value

*4: Baud rate ≤ 32.1 Gbaud

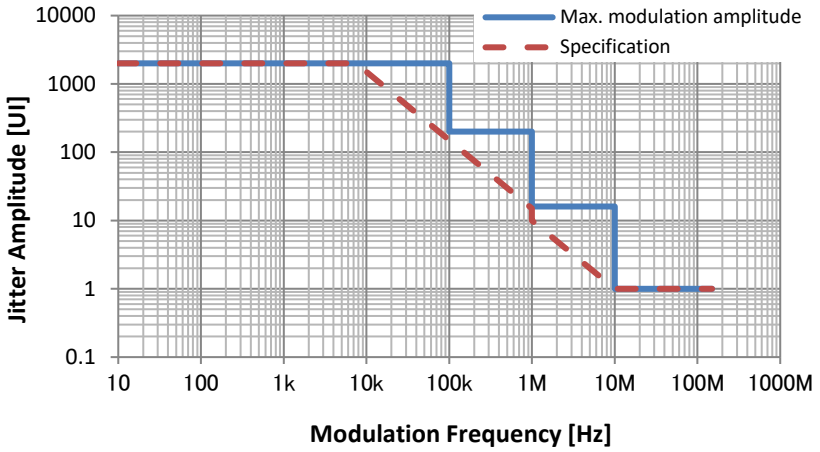
*5: Baud rate > 32.1 Gbaud

Table 1.3.2.2-14 Jitter Tolerance

Item	Specifications
Jitter tolerance	For NRZ output, Bit rate: 32.1 Gbit/s (Option 001) 58.2 Gbit/s (with Option 002 or y12) 64.2 Gbit/s (with Option 003, y13, or y23) Pattern: PRBS2^{31}–1 32.1 Gbits: With MU181500B, SSC with frequency of 33 kHz and deviation of 5300 ppm can be applied simultaneously with RJ with amplitude of 0.3 UI. 58.2 Gbit/s, 64.2 Gbits: With MU181500B, SSC with frequency of 33 kHz and deviation of 3300 ppm can be applied simultaneously with RJ with amplitude of 0.3 UI. These specifications are defined assuming the following conditions: Loopback connection to MU196040A (32.1 Gbit/s), MU196040B (32.1 Gbit/s, 64.2 Gbit/s) or MP1862A + MU183040B (58.2 Gbit/s, 64.2 Gbit/s), at a constant temperature between 20 and 30 °C. When RJ + BUJ/SJ3 is bigger than 0.5 UIp-p or SJ1 + Built-in SJ2 + RJ + BUJ/SJ3 is bigger than the standard value + 0.3 UIp-p, “Overload” is displayed on the MU181500B screen. Note that if Modulation Frequency is 33 kHHz, and RJ+BUJ/SJ3 is bigger than 0.5UIp-p or SJ1 is bigger than 550 UIp-p, “Overload” is displayed on the MU181500B screen. For details on the maximum modulation jitter that depends on the bit rate, refer to “Table 1.3.2.2-2 Jitter Setting Range”.

Table 1.3.2.2-14 Jitter Tolerance (Cont'd)

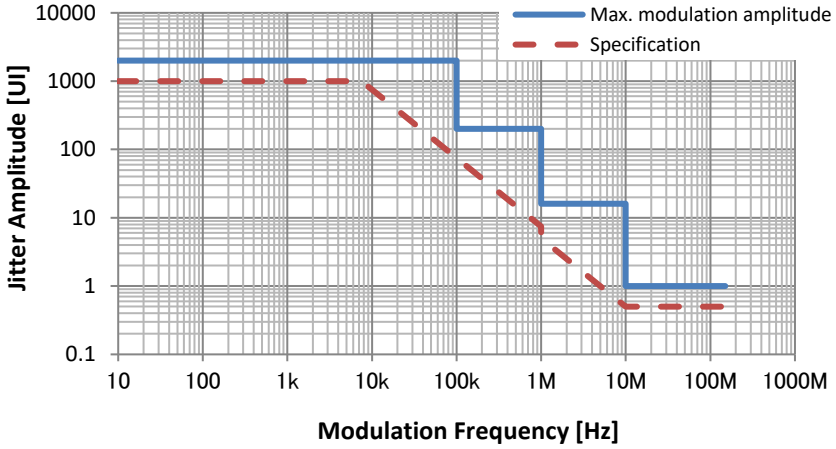
Item	Specifications
Jitter tolerance (Cont'd)	32.1 Gbit/s



Modulation frequency [Hz]	Max. modulation amplitude [UIp-p]	Specification [UIp-p]
10	2 000	2 000
7 500	2 000	2 000
100 000	2 000	150
1 000 000	200	15
10 000 000	16	1
150 000 000	1	1

Table 1.3.2.2-14 Jitter Tolerance (Cont'd)

Item	Specifications
Jitter tolerance (Cont'd)	58.2 Gbit/s, 64.2 Gbit/s



Modulation frequency [Hz]	Max. modulation amplitude [UIp-p]	Specification [UIp-p]
10	2 000	1 000
7 500	2 000	1 000
100 000	2 000	75
1 000 000	200	7.5
10 000 000	16	0.5
150 000 000	1	0.5

Table 1.3.2.2-14 Jitter Tolerance (Cont'd)

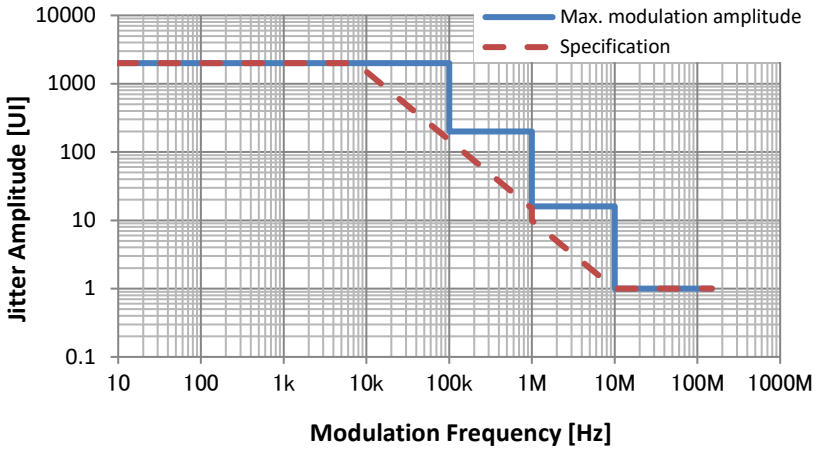
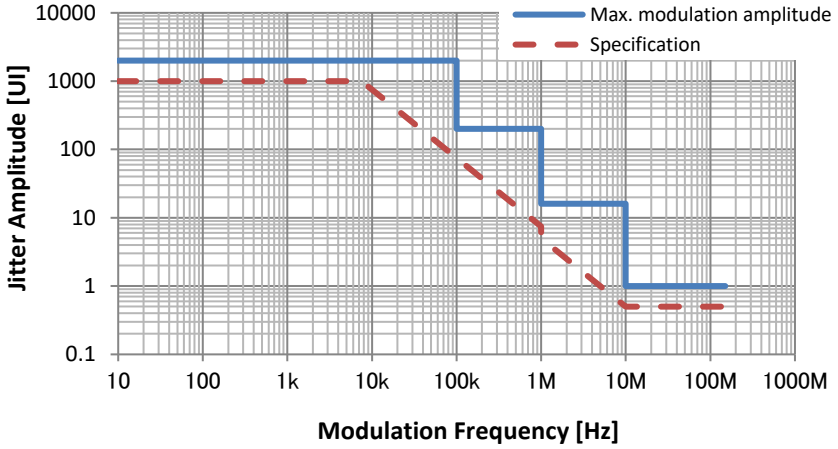
Item	Specifications
Jitter tolerance (Cont'd)	For PAM4 output, Bit rate: 32.1 Gbaud (Option 001) 58.2 Gbaud (When Options 002 and y12, or Options 003, y13, and y23 are installed) Pattern: PRBS2^{31}–1 32.1 Gbaud: With MU181500B, SSC with frequency of 33 kHz and deviation of 5300 ppm can be applied simultaneously with RJ with amplitude of 0.3 UI. 58.2 Gbaud: With MU181500B, SSC with frequency of 33 kHz and deviation of 3300 ppm can be applied simultaneously with RJ with amplitude of 0.3 UI. These specifications are defined assuming the following conditions: Loopback connection to MU196040B, at a constant temperature between 20 and 30 °C. When RJ + BUJ/SJ3 is bigger than 0.5 UIp-p or SJ1 + Built-in SJ2 + RJ + BUJ/SJ3 is bigger than the standard value + 0.3 UIp-p, "Overload" is displayed on the MU181500B screen. Note that if Modulation Frequency is 33 kHz, and RJ+BUJ/SJ3 is bigger than 0.5UIp-p or SJ1 is bigger than 550 UIp-p, "Overload" is displayed on the MU181500B screen. For details on the maximum modulation jitter that depends on the bit rate, refer to "Table 1.3.2.2-2 Jitter Setting Range". 32.1 Gbaud  **Modulation frequency [Hz] / Max. modulation amplitude [UIp-p] / Specification [UIp-p]** 10 — 2 000 — 2 000 7 500 — 2 000 — 2 000 100 000 — 2 000 — 150 1 000 000 — 200 — 15 10 000 000 — 16 — 1 150 000 000 — 1 — 1

Table 1.3.2.2-14 Jitter Tolerance (Cont'd)

Item	Specifications
Jitter tolerance (Cont'd)	58.2 Gbaud



Modulation frequency [Hz]	Max. modulation amplitude [UIp-p]	Specification [UIp-p]
10	2 000	1 000
7 500	2 000	1 000
100 000	2 000	75
1 000 000	200	7.5
10 000 000	16	0.5
150 000 000	1	0.5

Table 1.3.2.2-15 Multichannel Operation*1

Item	Specifications
Multi-Module Synchronization	A function to synchronize timing of generating patterns among multiple modules*2, *3, *4, *5, *6 Baud Rate ≤ 32.1 Gbaud: Bit generation timing alignment accuracy < 1 UI Baud Rate > 32.1 Gbaud: Bit generation timing alignment accuracy < 5 UI
Inter-Module 2ch Combination	This is available only for NRZ. Generates signals of which the first bit generation timing is synchronized between modules. And, generates signals with the bit-interleaved generation bit patterns between modules. Slot1 Data 1 3 5 7 Slot2 Data 2 4 6 8
Inter-Module CH Synchronization	Generates signals of which the first bit generation timing is synchronized between modules. Slot1 Data 1 2 3 4 Slot2, 3, 4 Data 1 2 3 4

*1: With Options x30 and x50

*2: The presence or absence of the following options must be the same across synchronized modules.

Option 001
Option 002 or y12
Option 003, y13, or y23

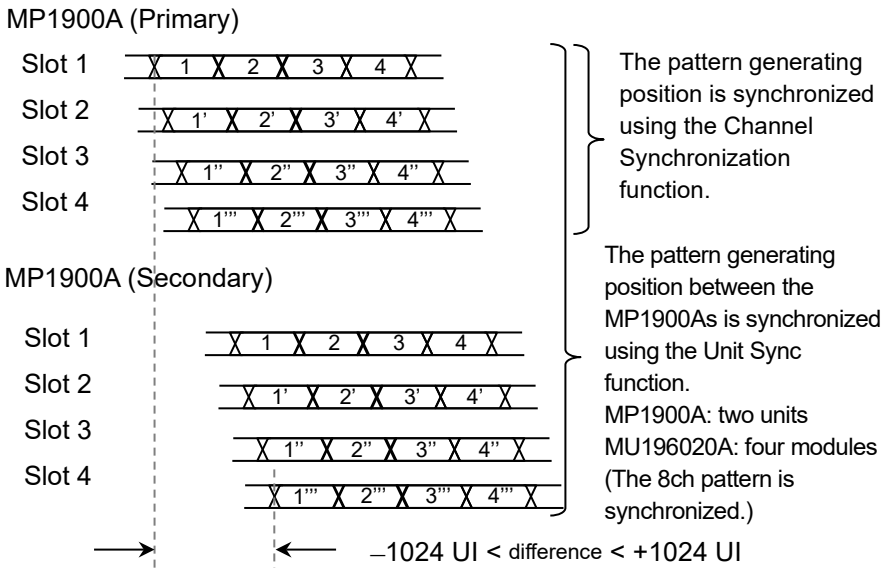
*3: Slots 1 to 2: Inter-Module 2ch Combination (only for NRZ)

*4: Slots 1 to 4: Inter-Module CH Synchronization

*5: The modules to be synchronized must be installed successively from Slot 1.

*6: In the range of ±3 °C from the temperature when performing the Multi Channel Calibration function, the bit generation timing is guaranteed.

Table 1.3.2.2-15 Multichannel Operation*1 (Cont'd)

Item	Specifications
Output Phase setting range Phase setting resolution	Only the items to be changed when Multi-Module Synchronization is set are described. –64 000 to +64 000 mUI*7 2 mUI*7
Pattern Data length	When CH Combination is set: 4 to 536 870 912 bits, in steps of 2 bits When CH Synchronization is set: same as Sync OFF
Unit Sync*8, *9, *10	ON/OFF switching available
Number of Units	Synchronous control available between up to two MP1900As. Synchronous control of up to 8 channels is available with two MP1900As each installed with four MU196020As.
Unit Sync Output*11	To output a timing signal from the Gating Out connector when **Unit Sync** is touched Provided with an inter-unit synchronization status indicator. The status indicator at Unit Sync turns orange when it requires to be timed to the other.
Unit Sync Input*11	To input a timing signal from the AUX In connector
Bit phase difference between MP1900As	Within ±1024 UI Timing difference between bit generations that occurs when **Unit Sync** is touched 

*7: Each channel can be set independently.

*8: Available in MX190000A version 3.02.00 or later.

*9: Available only when using inter-module synchronization.

*10: Cannot be set when the BERT for PCIe1-6 Forced Link is selected.

*11: Available only when **Unit Sync** is set to **ON**.

Table 1.3.2.2-16 Multichannel Operation (Sequence for Multi-Channel)*1, *2

Item	Specifications
Inter-Module Synchronization	A function that synchronizes the pattern generation timing across multiple modules*3, *4, *5 Baud Rate ≤ 32.1 Gbaud: Bit generation timing alignment accuracy < 1 UI
Inter-Module CH Synchronization	Generates signals of which the first bit generation timing is synchronized between modules. Slot1 Data 1 2 3 4 Slot2, 3, 4 Data 1 2 3 4
Sequence	
Transmit	Starts transmitting the sequence pattern. The LED lights up during transmission. Selecting **Transmit** on the operation screen of any module in Slots 1 to 4 starts sequence transmission from all modules.
Manual	Enabled when Manual Trigger is set.
Trigger Sync	Configures the synchronization setting for Manual Trigger. Manual Trigger synchronization can be performed across modules installed in any number of slots. However, External Trigger synchronization is not supported.
Output	
Delay	
Phase variable range	–64 000 to +64 000 mUI*5
Phase setting range	2 mUI*6

*1: With Options x30, x50, z51, and z52

*2: Enabled when the BERT for PCIe1-6 Forced Link application is selected. Transmission timing is synchronized only when a Sequence pattern is set. It is not synchronized for other patterns.

*3: Slots 1 to 4: Inter-Module CH Synchronization.

*4: The modules to be synchronized must be installed consecutively starting from Slot 1.

*5: The bit generation timing is guaranteed within ±3 °sC of the temperature at which the Multi Channel Calibration function was performed.

*6: Each channel can be set independently.

Table 1.3.2.2-17 General

Item	Specifications
Dimensions	21 mm (H), 234 mm (W), 175 mm (D) Excluding protrusions
Mass	2.5 kg max.
Operating Temperature	15 to 30 °C MP1900A's ambient temperature. MU196020A shall operate when installed.
Storage Temperature	–20 to 60 °C MU196020A installed to MP1900A shall comply with MIL-T-28800E Class 5.

Table 1.3.2.2-18 Extended Functions

Item	Specifications
PCIe	Supports the following PCIe tests when controlled by the MX183000A. The supported installer versions are: • MX190000A V10.00.00 or later • MX183000A V10.00.00 or later
Applicable Standards	PCI Express Base Specification Revision 4.0 Version1.0 PCI Express Base Specification Revision 5.0 Version1.0 PCI Express Base Specification Revision 6.0 Version1.0 Bit rate: PCIe1/2/3/4/5/6 Number of lanes: x1 Subjects of Testing: Root Complex, End Point
Required Options	Option x11 (Required for PCIe1 to 6) Option x60 (Required for PCIe6)
Required Software	MX183000A-PL021: Can support negotiation with the DUT and can put the DUT into Loopback state according to the LTSSM of PCIe1 to PCIe4. State transition of LTSSM can be analyzed as a log.(One MU196020A and one MU195040A/MU196040B are required.) MX183000A-PL025: Can extend the functionality of the PL021 option to PCIe5. MX183000A-PL026: Can extend the functionality of the PL021 and PL025 options to PCIe 6. (One MU196020A and one MU196040B are required.) When the MX183000A-PL001 is installed in addition to the MX183000A-PL021, MX183000A-PL025, and MX183000A-PL026, the MX183000A can control the MU196020A, MU181500B, and MU195040A/MU196040B and support Jitter Tolerance Test.

1.3.2.3 Specifications for MU196020C

Table 1.3.2.3-1 Operating Baud/Bit Rate

Item	Specifications
Operating Baud/Bit Rate	The baud rate of the PAM4/PAM3 output and the bit rate of the NRZ output share a common numerical value range. Only the baud rate is described hereafter.
Setting Range/Step	2.4 to 32.1(*1)/ 58.2(*2)/ 64.2(*3) Gbaud*5, *6
When linking with MU181000A/B*4, *5, *6	2.400 000 to 25.000 000 Gbaud, 0.000 002 Gbaud step*1, *2, *3 25.000 004 to 32.100 000 Gbaud, 0.000 004 Gbaud step*1 25.000 004 to 50.000 000 Gbaud, 0.000 004 Gbaud step*2, *3 50.000 008 to 58.200 000 Gbaud, 0.000 008 Gbaud step*2 50.000 008 to 64.200 000 Gbaud, 0.000 008 Gbaud step*3
When linking with MU181000A/B and MU181500B*4, *5, *6	2.400 000 to 3.125 000 Gbaud, 0.000 002 Gbaud step 3.200 002 to 6.250 000 Gbaud, 0.000 002 Gbaud step 6.400 002 to 12.500 000 Gbaud, 0.000 002 Gbaud step 12.800 002 to 25.000 000 Gbaud, 0.000 002 Gbaud step 25.600 004 to 32.100 000 Gbaud, 0.000 004 Gbaud step*1 25.600 004 to 50.000 000 Gbaud, 0.000 004 Gbaud step*2 51.200 008 to 58.200 000 Gbaud, 0.000 008 Gbaud step*2 51.200 008 to 64.200 000 Gbaud, 0.000 008 Gbaud step*3
When linking with MU191000A*4, *5, *6	2.400 000 to 25.600 000 Gbaud, 0.000 002 Gbaud step*1, *2, *3 25.600 004 to 32.100 000 Gbaud, 0.000 004 Gbaud step*1 25.600 004 to 51.200 000 Gbaud, 0.000 004 Gbaud step*2, *3 51.200 008 to 58.200 000 Gbaud, 0.000 008 Gbaud step*2 51.200 008 to 64.200 000 Gbaud, 0.000 008 Gbaud step*3
When linking with MU191000A and MU181500B*4, *5, *6	2.400 000 to 25.600 000 Gbaud, 0.000 002 Gbaud step 25.600 004 to 32.100 000 Gbaud, 0.000 004 Gbaud step*1 25.600 004 to 51.200 000 Gbaud, 0.000 004 Gbaud step*2 51.200 008 to 58.200 000 Gbaud, 0.000 008 Gbaud step*2 51.200 008 to 64.200 000 Gbaud, 0.000 008 Gbaud step*3

*1: With Option 001

*2: With Option 002 or y12

*3: With Option 003, y13, or y23

*4: Linking is not available when **Unit Sync** is **ON**.

*5: When the "BERT for PCIe1-7" application is selected, the operating baud rate can be set as follows:
2.4 to 32.1 Gbaud (*1, *2) / 64.2 Gbaud (*3)

*6: When the "BERT for PCIe1-6 Forced Link" application is selected, the operating bit/baud rate can be set as follows:
2.5, 5.0, 8.0, 16.0, 32.0 Gbit/s, 32.0 Gbaud

Table 1.3.2.3-1 Operating Baud/Bit Rate (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>When linking with MU181500B and using external clock
Clock Output Rate Full Rate</td><td>
<table>
<tr><th>Baud Rate Setting Range</th><th>Input Clock Frequency</th><th>Relationship Between Baud Rate and Input Clock Frequency</th></tr>
<tr><td>2.4 to 15.0 Gbaud</td><td>2.4 to 15.0 GHz</td><td>1/1 Clock Input</td></tr>
<tr><td>15.0 to 30.0 Gbaud</td><td>7.5 to 15.0 GHz</td><td>1/2 Clock Input</td></tr>
<tr><td>25.0 to 32.1 Gbaud</td><td>6.25 to 8.025 GHz</td><td>1/4 Clock Input</td></tr>
</table>
Clock Output Rate Half Rate, Quarter Rate
<table>
<tr><th>Baud Rate Setting Range</th><th>Input Clock Frequency</th><th>Relationship Between Baud Rate and Input Clock Frequency</th></tr>
<tr><td>2.4 to 30.0 Gbaud</td><td>1.2 to 15.0 GHz</td><td>1/2 Clock Input</td></tr>
<tr><td>30.0 to 32.1 Gbaud*1</td><td>7.5 to 8.025 GHz*1</td><td>1/4 Clock Input</td></tr>
<tr><td>30.0 to 58.2 Gbaud*2</td><td>7.5 to 14.55 GHz*2</td><td>1/4 Clock Input</td></tr>
<tr><td>30.0 to 60.0 Gbaud*3</td><td>7.5 to 15.0 GHz*3</td><td>1/4 Clock Input</td></tr>
<tr><td>50.0 to 58.2 Gbaud*2</td><td>6.25 to 7.275 GHz*2</td><td>1/8 Clock Input</td></tr>
<tr><td>50.0 to 64.2 Gbaud*3</td><td>6.25 to 8.025 GHz*3</td><td>1/8 Clock Input</td></tr>
</table>
</td></tr>
</table>

Table 1.3.2.3-1 Operating Baud/Bit Rate (Cont'd)

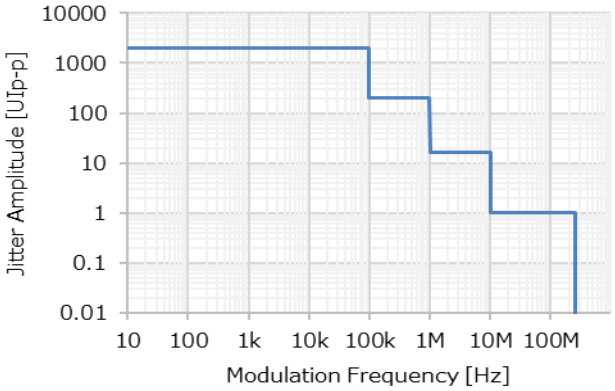
<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>External Clock
Clock Output Rate Full Rate

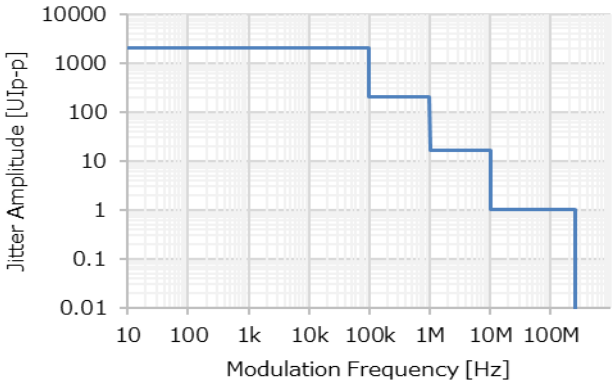
Clock Output Rate Half Rate, Quarter Rate</td><td>
<table>
<tr><th>Baud Rate Setting Range</th><th>Input Clock Frequency</th><th>Relationship Between Baud Rate and Input Clock Frequency</th></tr>
<tr><td>2.4 to 16.05 Gbaud</td><td>2.4 to 16.05 GHz</td><td>1/1 Clock Input</td></tr>
<tr><td>16.05 to 32.1 Gbaud</td><td>8.025 to 16.05 GHz</td><td>1/2 Clock Input</td></tr>
<tr><td>25.0 to 32.1 Gbaud</td><td>6.25 to 8.025 GHz</td><td>1/4 Clock Input</td></tr>
</table>
<table>
<tr><th>Baud Rate Setting Range</th><th>Input Clock Frequency</th><th>Relationship Between Baud Rate and Input Clock Frequency</th></tr>
<tr><td>2.4 to 30.0 Gbaud</td><td>1.2 to 15.0 GHz</td><td>1/2 Clock Input</td></tr>
<tr><td>30.0 to 32.1 Gbaud*1</td><td>7.5 to 8.025 GHz*1</td><td>1/4 Clock Input</td></tr>
<tr><td>30.0 to 58.2 Gbaud*2</td><td>7.5 to 14.55 GHz*2</td><td>1/4 Clock Input</td></tr>
<tr><td>30.0 to 60.0 Gbaud*3</td><td>7.5 to 15.0 GHz*3</td><td>1/4 Clock Input</td></tr>
<tr><td>50.0 to 58.2 Gbaud*2</td><td>6.25 to 7.275 GHz*2</td><td>1/8 Clock Input</td></tr>
<tr><td>50.0 to 64.2 Gbaud*3</td><td>6.25 to 8.025 GHz*3</td><td>1/8 Clock Input</td></tr>
</table>
</td></tr>
<tr><td>Offset Setting Range/Step</td><td>This is available only when linking with MU181000A/B or MU191000A.</td></tr>
<tr><td>When linking with MU181000A/B</td><td>–1000 to +1000 ppm, 1 ppm step
Note: The setting range is limited to –1000 to 0 ppm for the following bit rate settings:
Clock Output Rate Full Rate
12.500 000 Gbaud, 25.000 000 Gbaud
Clock Output Rate Half Rate, Quarter Rate
25.000 000 Gbaud, 50.000 000 Gbaud</td></tr>
<tr><td>When linking with MU191000A</td><td>–1000 to +1000 ppm, 1 ppm step
Note: The setting range is limited to –1000 to 0 ppm for the following bit rate settings:
Clock Output Rate Full Rate
12.800 000 Gbaud, 25.600 000 Gbaud
Clock Output Rate Half Rate, Quarter Rate
25.600 000 Gbaud, 51.200 000 Gbaud</td></tr>
</table>

Table 1.3.2.3-2 Jitter Setting Range

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Jitter Setting Range

SJ1 Setting Range

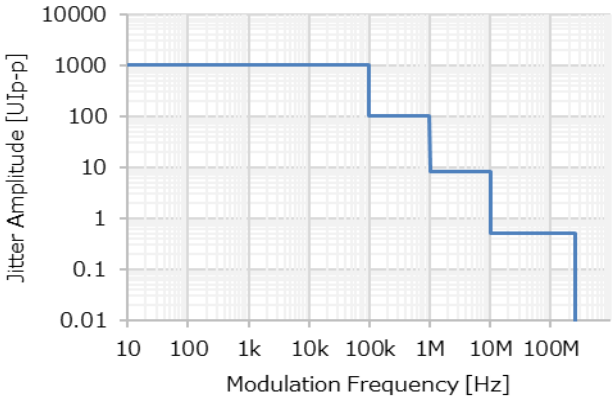
SJ1 Clock Output Rate At Full Rate</td><td>When linked (tracked) with either of the following module combinations:
・MU181000A/B and MU181500B ・MU191000A and MU181500B
When SJ2 switch is the built-in SJ2, the settable Jitter Amplitude is halved.
30 < Baud rate ≤ 32.1 Gbaud, 15 < Baud rate ≤ 17 Gbaud
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 100k</td><td>0 to 2000</td></tr>
<tr><td>100.1k to 1M</td><td>0 to 200</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 16</td></tr>
<tr><td>10.01M to 150M</td><td>0 to 1</td></tr>
</table>
17 < Baud rate ≤ 30 Gbaud
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 100k</td><td>0 to 2000</td></tr>
<tr><td>100.1k to 1M</td><td>0 to 200</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 16</td></tr>
<tr><td>10.01M to 250M</td><td>0 to 1</td></tr>
</table></td></tr>
</table>

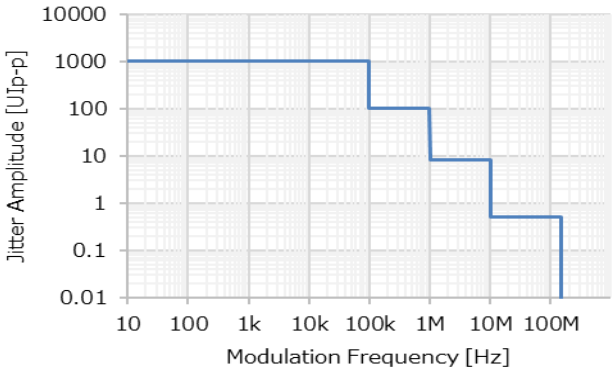
Table 1.3.2.3-2 Jitter Setting Range (Cont'd)

Item	Specifications
SJ1 Clock Output Rate At Full Rate (Cont'd)	8.5 < Baud rate ≤ 15 Gbaud



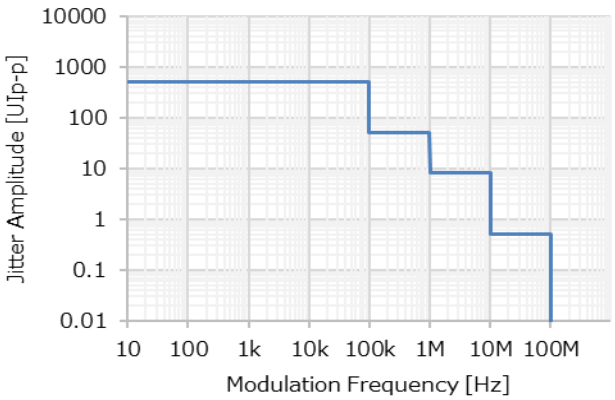
Modulation Frequency (Hz)	Jitter Amplitude (UIp-p)
10 to 100k	0 to 1000
100.1k to 1M	0 to 100
1.001M to 10M	0 to 8
10.01M to 250M	0 to 0.5

4 < Baud rate ≤ 8.5 Gbaud



Modulation Frequency (Hz)	Jitter Amplitude (UIp-p)
10 to 100k	0 to 1000
100.1k to 1M	0 to 100
1.001M to 10M	0 to 8
10.01M to 150M	0 to 0.5

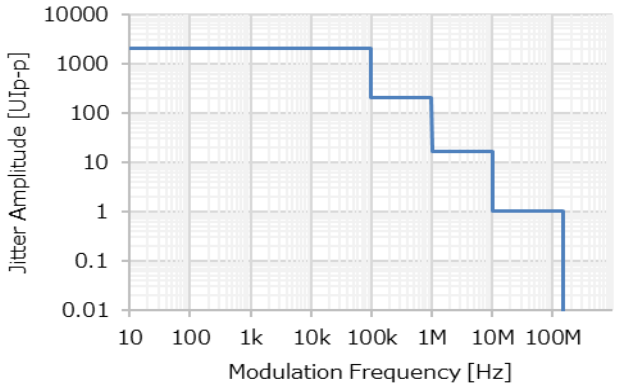
Table 1.3.2.3-2 Jitter Setting Range (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>SJ1 Clock Output Rate At Full Rate (Cont'd)</td><td>2.4 ≤ Baud rate ≤ 4 Gbaud
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 100k</td><td>0 to 500</td></tr>
<tr><td>100.1k to 1M</td><td>0 to 50</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 8</td></tr>
<tr><td>10.01M to 100M</td><td>0 to 0.5</td></tr>
</table>
</td></tr>
</table>

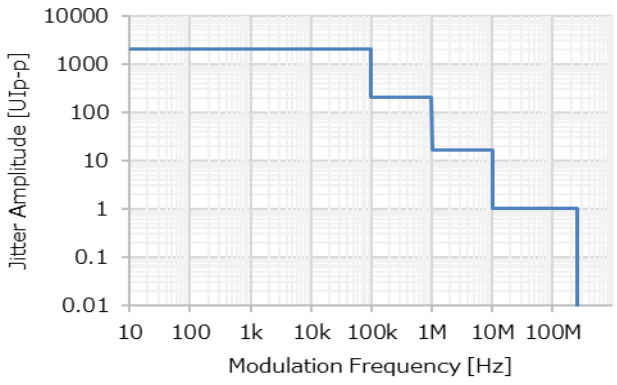
Table 1.3.2.3-2 Jitter Setting Range (Cont'd)

Item	Specifications
SJ1 Clock Output Rate At Half Rate, Quarter Rate	60 < Baud rate ≤ 64.2 Gbaud, 30 < Baud rate ≤ 34 Gbaud, 8 < Baud rate ≤ 17 Gbaud



Modulation Frequency (Hz)	Jitter Amplitude (UIp-p)
10 to 100k	0 to 2000
100.1k to 1M	0 to 200
1.001M to 10M	0 to 16
10.01M to 150M	0 to 1

34 < Baud rate ≤ 60 Gbaud*1, 17 < Baud rate ≤ 30 Gbaud



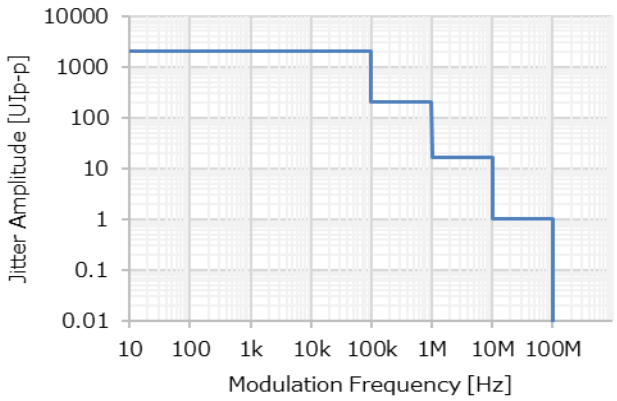
Modulation Frequency (Hz)	Jitter Amplitude (UIp-p)
10 to 100k	0 to 2000
100.1k to 1M	0 to 200
1.001M to 10M	0 to 16
10.01M to 250M*1	0 to 1

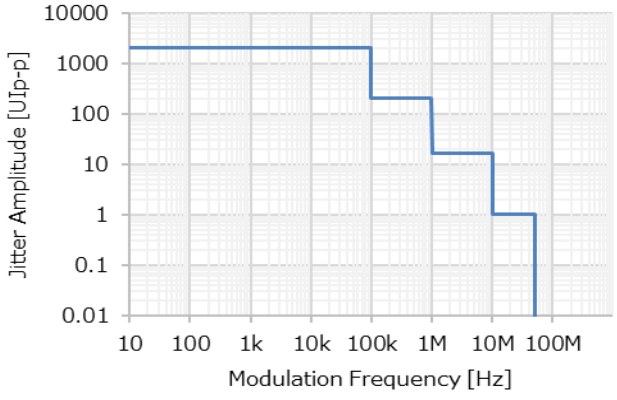
*1: The modulation frequency (Hz) is 10.01M to 150M when both of the following conditions are met:

- Operation Baud Rate is 50 ≤ Baud rate ≤ 60 Gbaud.

- Relationship between Baud Rate and Input Clock Frequency is set to 1/8 Clock Input with Clock Output Rate Half Rate and Quarter Rate in Table 1.3.2.2-1.

Table 1.3.2.3-2 Jitter Setting Range (Cont'd)

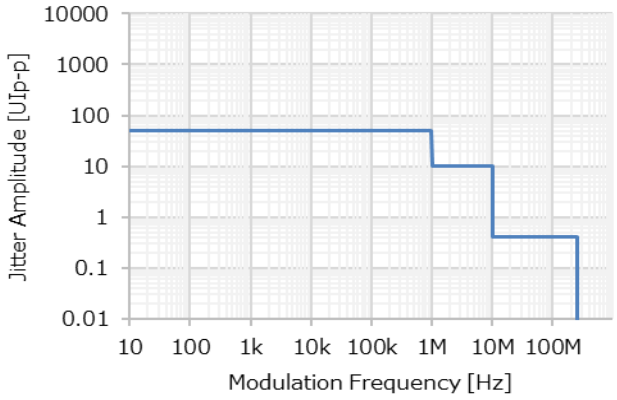
<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>SJ1 Clock Output Rate At Half Rate, Quarter Rate (Cont'd)</td><td>2.4 < Baud rate ≤ 8 Gbaud
 

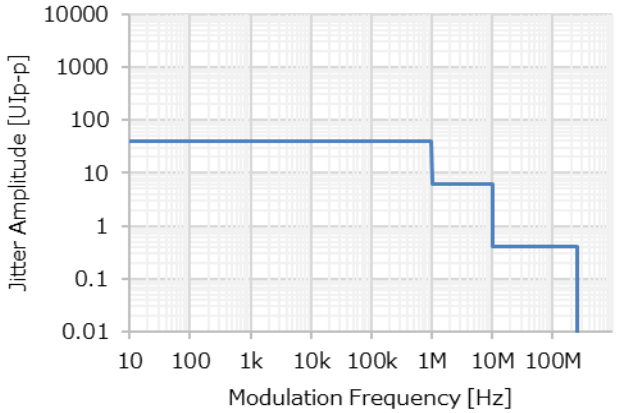
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 100k</td><td>0 to 2000</td></tr>
<tr><td>100.1k to 1M</td><td>0 to 200</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 16</td></tr>
<tr><td>10.01M to 100M</td><td>0 to 1</td></tr>
</table>
Baud rate 2.4 Gbaud
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 100k</td><td>0 to 2000</td></tr>
<tr><td>100.1k to 1M</td><td>0 to 200</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 16</td></tr>
<tr><td>10.01M to 50M</td><td>0 to 1</td></tr>
</table></td></tr>
</table>

Table 1.3.2.3-2 Jitter Setting Range (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>SJ2 Setting Range

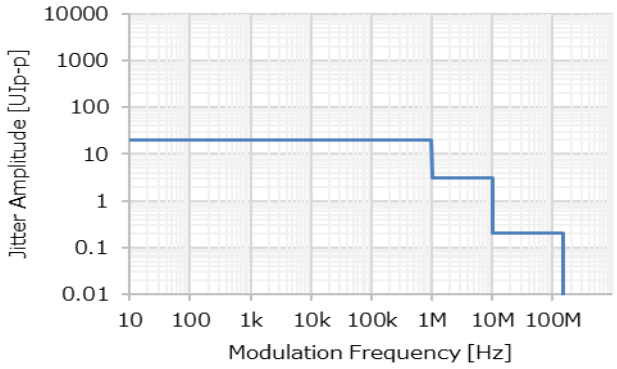
SJ2 via MU181000 Clock Output Rate
At Full Rate</td><td>When linked (tracked) with either of the following module combinations:
・MU181000A/B and MU181500B ・MU191000A and MU181500B
The SJ2 via MU181000A/B Clock (*2) and the Built-in SJ2 can be set exclusively.
15.000 001 ≤ Baud rate ≤ 32.1 Gbaud
 

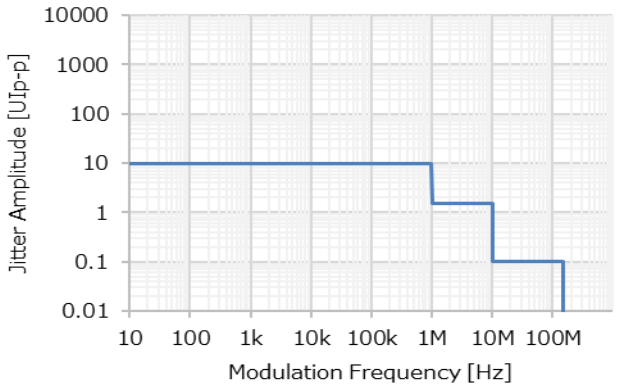
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 1M</td><td>0 to 50</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 10</td></tr>
<tr><td>10.01M to 250M</td><td>0 to 0.4</td></tr>
</table>
6.400 001 ≤ Baud rate ≤ 15 Gbaud
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 1M</td><td>0 to 40</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 6</td></tr>
<tr><td>10.01M to 250M</td><td>0 to 0.4</td></tr>
</table></td></tr>
</table>

*2: Applicable only when linked with MU181000A/B and MU181500B.

Table 1.3.2.3-2 Jitter Setting Range (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>SJ2 via MU181000 Clock Output Rate
At Full Rate (Cont'd)</td><td>3.200 001 ≤ Baud rate ≤ 6.25 Gbaud
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 1M</td><td>0 to 20</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 3</td></tr>
<tr><td>10.01M to 150M</td><td>0 to 0.2</td></tr>
</table>
2.4 ≤ Baud rate ≤ 3.125 Gbaud
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 1M</td><td>0 to 10</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 1.5</td></tr>
<tr><td>10.01M to 150M</td><td>0 to 0.1</td></tr>
</table></td></tr>
</table>

Table 1.3.2.3-2 Jitter Setting Range (Cont'd)

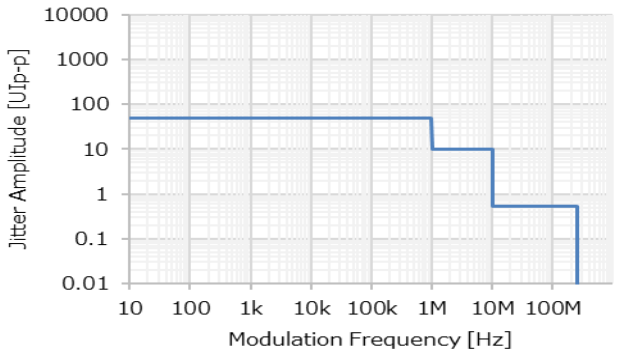
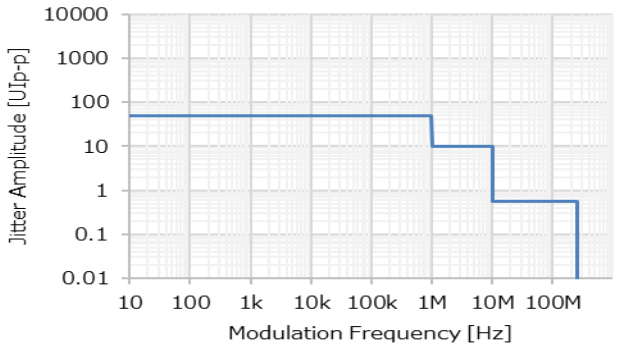
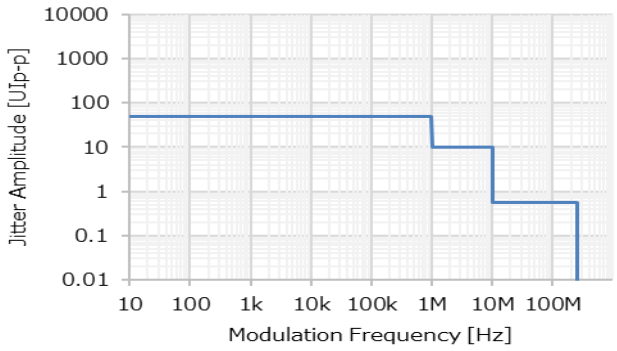
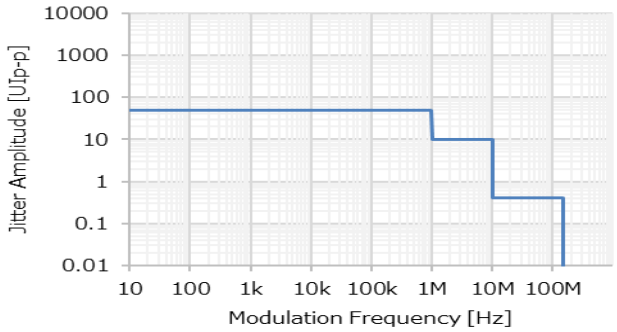
Item	Specifications
SJ2 via MU181000 Clock Output Rate: Half Rate / Quarter Rate	60.000 001 ≤ Baud rate ≤ 64.2 Gbaud  **Modulation Frequency (Hz) / Jitter Amplitude (UIp-p)** 10 to 1M: 0 to 50 1.001M to 10M: 0 to 10 10.01M to 250M: 0 to 0.544 30.000 001 ≤ Baud rate ≤ 60.0 Gbaud  **Modulation Frequency (Hz) / Jitter Amplitude (UIp-p)** 10 to 1M: 0 to 50 1.001M to 10M: 0 to 10 10.01M to 250M: 0 to 0.548

Table 1.3.2.3-2 Jitter Setting Range (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>SJ2 via MU181000 Clock Output Rate
At Half Rate, Quarter Rate (Cont'd)</td><td>12.800001 ≤ Baud rate ≤ 30.0 Gbaud
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 1M</td><td>0 to 50</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 10</td></tr>
<tr><td>10.01M to 250M</td><td>0 to 0.55</td></tr>
</table>
6.400001 ≤ Baud rate ≤ 12.5 Gbaud
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 1M</td><td>0 to 50</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 10</td></tr>
<tr><td>10.01M to 150M</td><td>0 to 0.4</td></tr>
</table></td></tr>
</table>

Table 1.3.2.3-2 Jitter Setting Range (Cont'd)

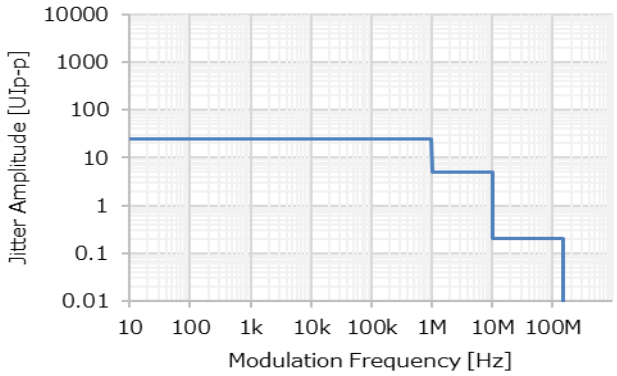
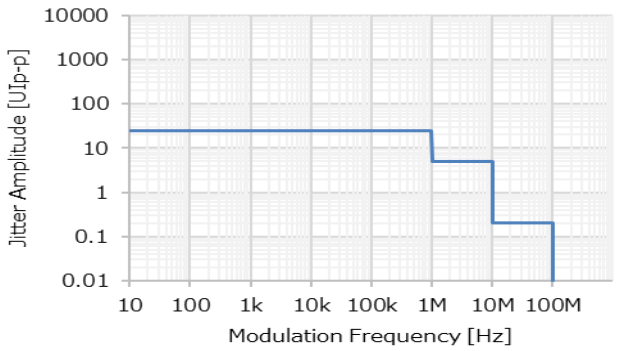
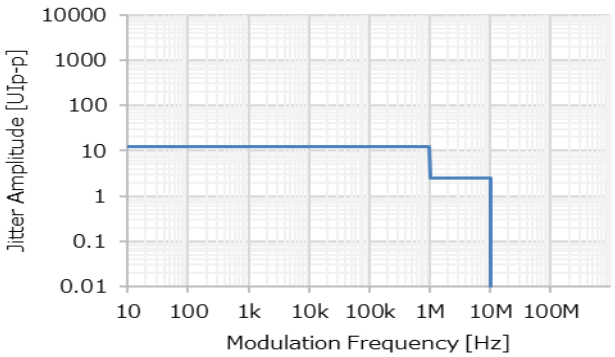
Item	Specifications
SJ2 via MU181000 Clock Output Rate At Half Rate, Quarter Rate (Cont'd)	3.600001 ≤ Baud rate ≤ 6.25 Gbaud  **Modulation Frequency (Hz) / Jitter Amplitude (UIp-p)** 10 to 1M: 0 to 25 1.001M to 10M: 0 to 5 10.01M to 150M: 0 to 0.2 3.200001 < Baud rate ≤ 3.6 Gbaud  **Modulation Frequency (Hz) / Jitter Amplitude (UIp-p)** 10 to 1M: 0 to 25 1.001M to 10M: 0 to 5 10.01M to 100M: 0 to 0.2

Table 1.3.2.3-2 Jitter Setting Range (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>SJ2 via MU181000 Clock Output Rate
At Half Rate, Quarter Rate (Cont'd)</td><td>2.4 ≤ Baud rate ≤ 3.125 Gbaud
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (UIp-p)</th></tr>
<tr><td>10 to 1M</td><td>0 to 12.4</td></tr>
<tr><td>1.001M to 10M</td><td>0 to 2.5</td></tr>
</table>
</td></tr>
</table>

Table 1.3.2.3-2 Jitter Setting Range (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Built-in SJ2 Clock Output Rate
At Full Rate</td><td>15 < Baud rate ≤ 32.1 Gbaud
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (Ulp-p)</th></tr>
<tr><td>33k</td><td>0 to 1000</td></tr>
<tr><td>87M</td><td>0 to 0.5</td></tr>
<tr><td>100M</td><td>0 to 0.5</td></tr>
<tr><td>210M</td><td>0 to 0.2</td></tr>
</table>
4 < Baud rate ≤ 15 Gbaud
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (Ulp-p)</th></tr>
<tr><td>33k</td><td>0 to 500</td></tr>
<tr><td>87M</td><td>0 to 0.25</td></tr>
<tr><td>100M</td><td>0 to 0.25</td></tr>
<tr><td>210M</td><td>0 to 0.1</td></tr>
</table>
2.4 ≤ Baud rate ≤ 4 Gbaud
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (Ulp-p)</th></tr>
<tr><td>33k</td><td>0 to 500</td></tr>
<tr><td>87M</td><td>0 to 0.25</td></tr>
<tr><td>100M</td><td>0 to 0.25</td></tr>
</table></td></tr>
<tr><td>Built-in SJ2 Clock Output Rate
At Half Rate, Quarter Rate</td><td>8 < Baud rate ≤ 64.2 Gbaud
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (Ulp-p)</th></tr>
<tr><td>33k</td><td>0 to 1000</td></tr>
<tr><td>87M</td><td>0 to 0.5</td></tr>
<tr><td>100M</td><td>0 to 0.5</td></tr>
<tr><td>210M</td><td>0 to 0.2</td></tr>
</table>
2.4 < Baud rate ≤ 8 Gbaud
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (Ulp-p)</th></tr>
<tr><td>33k</td><td>0 to 1000</td></tr>
<tr><td>87M</td><td>0 to 0.5</td></tr>
<tr><td>100M</td><td>0 to 0.5</td></tr>
</table>
Baud rate 2.4 Gbaud
<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Amplitude (Ulp-p)</th></tr>
<tr><td>33k</td><td>0 to 1000</td></tr>
</table></td></tr>
</table>

Table 1.3.2.3-3 External Clock Input

Item	Specifications
Number of Inputs	1 (Single-Ended)
Input frequency range	1.2 to 16.05 GHz
Input amplitude	0.3 to 1.0 Vp-p (–6.5 to +4.0 dBm)
Termination	50 Ω, AC Coupling
Connector	SMA connector (j.)

Table 1.3.2.3-4 AUX Input

Item	Specifications
Number of Inputs	1 (Single-Ended)
Variation	Error Injection, Burst, Unit Sync, Jitter Sync
Minimum Pulse Width	1/256 of data rate
Input level	• 0/–1 V (H: –0.25 to 0.05 V, L: –1.1 to –0.8 V) • 0/–0.5 V (H: –0.05 to 0.05 V, L: –0.55 to –0.45 V) • Vth 0 V (Input amplitude: 0.5 to 1.0 Vp-p) Select one of the above.
Termination	50 Ω, GND
Connector	SMA connector (j.)

Table 1.3.2.3-5 AUX Output

Item	Specifications
Number of Outputs	2 (Differential output)
Output control	ON/OFF switching
Variation	1/n Clock (n = 8, 12, 16, 20...1020, 1024), Pattern Sync, Burst Out2
Pattern Sync PRBS, PRGM	Position: 1 to {(Least common multiple of Pattern Length' and 256) –263}, in 8 steps When the pattern length is 1023 bits or less, Pattern Length' is the length as an integer multiple so that it becomes 1024 bits or more.
Burst Out2 Burst Trigger Delay Pulse Width	 0 to (Burst Cycle – 256) bits, in steps of 8 bits 16 to (Burst Cycle – 256) bits, in steps of 8 bits
Output level	0/–0.6 V (H: –0.25 to 0.05 V, L: –0.80 to –0.45 V)
Termination	50 Ω, GND
Connector	SMA connector (j.)

Table 1.3.2.3-6 Gating Output

Item	Specifications
Number of Outputs	1 (Single-Ended)
Output control	ON/OFF switching
Variation	Burst, Repeat
Burst	Burst Output
Burst Trigger Delay	0 to (Burst Cycle – 256) bits, in steps of 8 bits
Enable Pulse Width	16 to (Burst Cycle – 256) bits, in steps of 8 bits
Output Level	0/–1 V (H: –0.25 to 0.05 V, L: –1.25 to –0.8 V)*
Repeat	Timing Signal Output
Timing Signal Cycle	INT ($\frac{\text{Pattern length'}}{256}$) × 256
Timing Signal Delay	0 to {(Least common multiple of Pattern Length' and 256) –256} The maximum settable number is 68 719 476 480, in steps of 8 bits When the pattern length is 1023 bits or less, Pattern Length' is the length as an integer multiple so that it becomes 1024 bits or more.
Timing Signal Pulse Width	256 to {(Least common multiple of Pattern Length' and 256) –256} The maximum settable number is 68 719 476 480, in steps of 8 bits When the pattern length is 1023 bits or less, Pattern Length' is the length as an integer multiple so that it becomes 1024 bits or more.
Output Level	0/–1 V (H: –0.25 to 0.05 V, L: –1.25 to –0.8 V)*
Unit Sync Output	Outputs the timing signal when **Unit Sync** is set to **ON**.
Termination	50 Ω, GND
Connector	SMA connector (j.)

*: L: Output Enable, H: Output Disable

Table 1.3.2.3-7 Pattern Generation

Item	Specifications
PRBS	
Pattern Length	2^n–1 (n = 7, 9, 10, 11, 13, 15, 20, 23, 31)
Mark ratio	1/2 (1/2INV is supported by a logical inversion.)
PRBS generator polynomial	n = 7: $1 + X^6 + X^7$ n = 9: $1 + X^5 + X^9$ n = 10: $1 + X^7 + X^{10}$ n = 11: $1 + X^9 + X^{11}$ n = 13: $1 + X + X^2 + X^{12} + X^{13}$ n = 15: $1 + X^{14} + X^{15}$ n = 20: $1 + X^3 + X^{20}$ n = 23: $1 + X^{18} + X^{23}$ n = 31: $1 + X^{28} + X^{31}$
PRBS Inversion	This is available in PAM4 mode only. Logical inversion of PRBS can be set independently for MSB and LSB.
PRBS 1st Bit	MSB or LSB can be selected to set the 1st bit of the PRBS Generator.

Table 1.3.2.3-7 Pattern Generation (Cont'd)

Item	Specifications
Zero-Substitution	This is available in NRZ mode only.
Additional bit	0 bit, 1 bit
Pattern Length	2^n (n = 7, 9, 10, 11, 15, 20, 23) 2^n–1 (n = 7, 9, 10, 11, 15, 20, 23)
Start position	Bit after the longest run of zero bits
Length of Consecutive Zero Bits	1 to (Pattern Length – 1) bits If the bit coming after Zero-substitution is "0", then it is replaced with "1".
Data	
Data Length	NRZ: 2 to 268 435 456 bits, in steps of 1 bit PAM4/PAM3: 2 to 268 435 456 symbols, in steps of 1 symbol
Bit Shift	This is available in PAM4 mode only. Bit shift of MSBs can be controlled in the range of ±256 bits (in steps of 1 bit).
PAM4 Standard Pattern	Standard-compliant PAM4-mode patterns
CEI	QPRBS13-CEI, QPRBS31-CEI
IEEE	IEEE802.3bs/cd: PRBS13Q, PRBS31Q, SSPRQ, Square Wave IEEE802.3bj: QPRBS13, JP03A, JP03B, Transmitter Linearity
InfiniBand	PRBS13Q (InfiniBand), PRBS23Q, PRBS31Q (InfiniBand)
Fibre Channel	PRBS31Q (Fibre Channel)
RS-FEC	With Option z42 RS-FEC Scrambled Idle 50G 1Lane, RS-FEC Scrambled Idle 100G 1Lanes, RS-FEC-Int Scrambled Idle 100G 1Lanes, RS-FEC Scrambled Idle 100G 2Lanes, RS-FEC Scrambled Idle 200G 2Lanes, RS-FEC Scrambled Idle 200G 4Lanes, RS-FEC Scrambled Idle 400G 4Lanes, RS-FEC Scrambled Idle 400G 8Lanes

Table 1.3.2.3-7 Pattern Generation (Cont'd)

Item	Specifications
PCIe	CP in 1b/1b Encoding for PCIe6 MCP in 1b/1b Encoding for PCIe6 Jitter Measurement Pattern in 1b/1b Encoding for PCIe6 High Swing Toggle Pattern in 1b/1b Encoding for PCIe6 Low Swing Toggle Pattern 1b/1b Encoding for PCIe6 Jitter Calibration Pattern for PCIe6 Preset Calibration Pattern for PCIe6 CP in 1b/1b Encoding for PCIe7 MCP in 1b/1b Encoding for PCIe7 Jitter Measurement Pattern in 1b/1b Encoding for PCIe7 High Swing Toggle Pattern in 1b/1b Encoding for PCIe7 Low Swing Toggle Pattern 1b/1b Encoding for PCIe7 Jitter Calibration Pattern for PCIe7 Preset Calibration Pattern for PCIe7 With Option z43 NOP Flit Layout in a x1 Link NOP Flit Layout in a x2 Link NOP Flit Layout in a x4 Link NOP Flit Layout in a x8 Link NOP Flit Layout in a x16 Link

Table 1.3.2.3-7 Pattern Generation (Cont'd)

Item	Specifications
NRZ Standard Pattern	Standard-compliant NRZ-mode pattern
CEI	SSPR
RS-FEC	With Option z42 RS-FEC Scrambled Idle 25G 1Lane, RS-FEC Scrambled Idle 50G 2Lanes RS(544,514), RS-FEC Scrambled Idle 100G 4Lanes, RS-FEC Scrambled Idle 100G 4Lanes RS(544,514)
PCIe	CP in 8b/10b Encoding for PCIe1 MCP in 8b/10b Encoding for PCIe1 Jitter Calibration Pattern for PCIe1 Preset Calibration Pattern for PCIe1 CP in 8b/10b Encoding for PCIe2 MCP in 8b/10b Encoding for PCIe2 Jitter Calibration Pattern for PCIe2 Preset Calibration Pattern for PCIe2 CP in 128b/130b Encoding for PCIe3 MCP in 128b/130b Encoding for PCIe3 Jitter Calibration Pattern for PCIe3 Preset Calibration Pattern for PCIe3 CP in 128b/130b Encoding for PCIe4 MCP in 128b/130b Encoding for PCIe4 Jitter Calibration Pattern for PCIe4 Preset Calibration Pattern for PCIe4 CP in 128b/130b Encoding for PCIe5 MCP in 128b/130b Encoding for PCIe5 Jitter Calibration Pattern for PCIe5 Preset Calibration Pattern for PCIe5
PRTS	
PRTS Length	3^n-1 (n = 7, 19)
PRTS generator polynomial	n=7 : $1 + X^2 + 2X^7$ Over GF(3) n=19 : $1 + X^2 + 2X^{19}$ Over GF(3)

Table 1.3.2.3-7 Pattern Generation (Cont'd)

Item	Specifications
PAM3 Standard Pattern	With Option z45
USB4 Gen4	PRBS TS2.clksw USB4 Gen4 Power Management State Signal USB4 Gen4 Rx Frequency Variation Training Sequence
USB4 Gen4 Power Management State Signal	
tPeriod	20 to 80 ns, in steps of 10 ns
Duty Cycle	45%, 50%, 55 %
tPreData	80 to 120 ns, in steps of 10 ns
LFPS Diff.Amp	Displays the differential amplitude of the LFPS signal.
LFPS Repetition	50 to 150 times, in steps of 10 times
USB4 Data	PRBSn (n = 7, 9, 10, 11, 13, 15, 20, 23, 31) PRTS7, 19 Data TS2.clksw
Transmit	Starts the LFPS signal transmission.
Manual	Transitions the state from the LFPS signal to USB4 Data.
Break	Manual, Auto Manual: Transitions to the next state, triggered by clicking **Manual**. Auto: Transitions to the next state at the time set to switch.
LFPS Swing	High, Low Sets the amplitude of the LFPS. High: Outputs the amplitude of 0/2 Level. Low: Outputs the amplitude of 0/1 Level.
USB4 Gen4 Rx Frequency Variation Training Sequence	Linked with the MU181500B's SSC Clock switching function.
Transmit	Starts the Rx Frequency Variation Training Sequence signal transmission.
Manual	Changes the output pattern.
Time	Sets the output time by pattern. Pattern output time for other than the final state 10.0 to 20.0 us, in steps of 0.1 us Pattern output time for the final state 1 to 10,000 ms, in steps of 1 ms

Table 1.3.2.3-7 Pattern Generation (Cont'd)

Item	Specifications
Pattern	Sets the sequence pattern. PRBSn (n = 7, 9, 10, 11, 13, 15, 20, 23, 31) PRTS7, 19 TS2.clksw
Break	Manual, Auto Manual: Transitions to the next state, triggered by clicking **Manual**. Auto: Transitions to the next state at the time set to switch.

Table 1.3.2.3-8 Pattern Sequence

Item	Specifications
Sequence	Repeat, Burst
Repeat	Continuous Pattern
Burst	This is available only when Coding is NRZ.
Source	Internal, External-Trigger (AUX Input), External-Enable (AUX Input)
Data Sequence	Restart, Consecutive, Continuous
Enable period	Internal: 12 800 to 2 147 483 136 bits, in steps of 256 bits External-Trigger, External-Enable: 12 800 to 2 147 483 648 bits, in steps of 256 bits
Burst Cycle	25 600 to 2 147 483 648 bits, in steps of 1 024 bits

Table 1.3.2.3-9 Coding

Item	Specifications
Coding	NRZ, PAM4, PAM3
NRZ	Normal, Invert
PAM4 Gray Coding	ON, OFF
PAM4 Precoding (1/(1 + D) mod 4)*1	ON, OFF
Delay Symbol	ON, OFF
SKP	No SKP, SKPx1, SKPx2
Preset	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10
SRIS	ON, OFF
EIEOS	ON
PAM3 Precoding (1/(1+D) mod 3) *2	ON, OFF
Polarity Inverse	ON, OFF Sets the polarity of the PAM3 signal.

*1: (1/(1+D) mod 4) is a generator polynomial defined in the IEEE802.3.

*2: (1/(1+D) mod 3) is a generator polynomial defined in the USB4.

Table 1.3.2.3-10 Error Addition

Item	Specifications
Type	Bit, Error on MSB, Error on LSB, Error on LSB&MSB, RS-FEC Symbol Error*1, PCIe6 FEC Symbol Error*2
Bit	This is available only when Coding is NRZ.
Source	Internal, External-Trigger (Rising edge trigger), External-Disable (L: Disable)
Error Variation	Repeat, Single (Cannot be selected when Source is External-Trigger.)
Error Rate	*E–n (* = 1 to 9, n = 3 to 12), Upper limit: 3.0E–3
Error Route	Select 1 to 32, Scan
Bit/Burst	Switching between Bit and Burst
Burst Length	1 to 256, 1 step
RS-FEC Symbol Error	This is available whether Coding is NRZ or PAM4.*1 When Coding is PAM4, an error is inserted to make the PAM4 signal change by one level only. NRZ: An error is inserted every 10 bits. PAM4: An error is inserted every 10 or 20 PAM4 symbols.
FEC Standard	When Coding is NRZ: RS-FEC Scrambled Idle 25G 1Lane, RS-FEC Scrambled Idle 50G 2Lanes RS(544,514), RS-FEC Scrambled Idle 100G 4Lanes, RS-FEC Scrambled Idle 100G 4Lanes RS(544,514) When Coding is PAM4: RS-FEC Scrambled Idle 50G 1Lane, RS-FEC Scrambled Idle 100G 1Lanes, RS-FEC-Int Scrambled Idle 100G 1Lane, RS-FEC Scrambled Idle 100G 2Lanes, RS-FEC Scrambled Idle 200G 2Lanes, RS-FEC Scrambled Idle 200G 4Lanes, RS-FEC Scrambled Idle 400G 4Lanes, RS-FEC Scrambled Idle 400G 8Lanes
Source	Internal, External-Trigger (Rising edge trigger), External-Disable (L: Disable)
Error Variation	Repeat, Single (Cannot be selected when Source is External-Trigger.)
Symbol error per codeword	1 to 20 (When Coding is NRZ.) 1 to 20 (When Coding is PAM4.)
Total BER for All Lane	*E–n (* = 1 to 9, n = 3 to 12), Upper limit: 6.0E–3 The error addition range varies depending on the value of Symbol Error per Codeword.
BER for One Lane/ SER for One Lane	*E–n (* = 1 to 9, n = 3 to 12), Upper limit:6.0E–3 The error addition range varies depending on the value of Symbol Error per Codeword.

*1: With Option z42

*2: With Option z43

Table 1.3.2.3-10 Error Addition (Cont'd)

Item	Specifications
RS-FEC Symbol Error (Cont'd) Error Addition Method	Type1: Level 0 → Level 1, Level 1 → Level 2, Level 2 → Level 3, Level 3 → Level 2 Type2: Level 0 → Level 1, Level 1 → Level 2, Level 2 → Level 1, Level 3 → Level 2 Type3: Level 0 → Level 1, Level 1 → Level 0, Level 2 → Level 1, Level 3 → Level 2 Type4: Level 0 → Level 1, Level 1 → Level 0 or Level 2, Level 2 → Level 1 or Level 3, Level 3 → Level 2 MSB Only: Level 0 → Level 2, Level 1 → Level 3, Level 2 → Level 0, Level 3 → Level 1 LSB Only: Level 0 → Level 1, Level 1 → Level 0, Level 2 → Level 3, Level 3 → Level 2 MSB or LSB: Level 0 → Level 1 or Level 2, Level 1 → Level 0 or Level 3, Level 2 → Level 0 or Level 3, Level 3 → Level 1 or Level 2 MSB and LSB: Level 0 → Level 3, Level 1 → Level 2, Level 2 → Level 1, Level 3 → Level 0 Applicable only when Coding is PAM4.

Table 1.3.2.3-10 Error Addition (Cont'd)

Item	Specifications
Error on MSB	Adds the specified symbol error. This is available only when Coding is PAM4. The set error is added to MSB only.
Source	Internal, External-Trigger (Rising edge trigger), External-Disable (L: Disable)
Error Variation	Repeat, Single (Cannot be selected when Source is External-Trigger.)
Symbol Error Rate	*E–n (* = 1 to 9, n = 3 to 12), Upper limit: 3.0E–3
Symbol/Burst	Switching between Symbol and Burst
Burst Length	1 to 256, 1 step
Error on LSB	Adds the specified symbol error. This is available only when Coding is PAM4. The set error is added to LSB only.
Source	Internal, External-Trigger (Rising edge trigger), External-Disable (L: Disable)
Error Variation	Repeat, Single (Cannot be selected when Source is External-Trigger.)
Symbol Error Rate	*E–n (* = 1 to 9, n = 3 to 12), Upper limit: 3.0E–3
Symbol/Burst	Switching between Symbol and Burst
Burst Length	1 to 256, 1 step

Table 1.3.2.3-10 Error Addition (Cont'd)

Item	Specifications
Error on LSB&MSB	Adds the specified symbol error. This is available only when Coding is PAM4. An error is inserted to make the PAM4 signal change by one level only.
Source	Internal, External-Trigger (Rising edge trigger), External-Disable (L: Disable)
Error Variation	Repeat, Single (Cannot be selected when Source is External-Trigger.)
Symbol Error Rate	*E–n (* = 1 to 9, n = 3 to 12), Upper limit: 3.0E–3
Symbol/Burst	Switching between Symbol and Burst
Burst Length	1 to 256, 1 step
Error Addition Method	Type1: Level 0 → Level 1, Level 1 → Level 2, Level 2 → Level 3, Level 3 → Level 2 Type2: Level 0 → Level 1, Level 1 → Level 2, Level 2 → Level 1, Level 3 → Level 2 Type3: Level 0 → Level 1, Level 1 → Level 0, Level 2 → Level 1, Level 3 → Level 2 Type4: Level 0 → Level 1, Level 1 → Level 0 or Level 2, Level 2 → Level 1 or Level 3, Level 3 → Level 2 MSB Only: Level 0 → Level 2, Level 1 → Level 3, Level 2 → Level 0, Level 3 → Level 1 LSB Only: Level 0 → Level 1, Level 1 → Level 0, Level 2 → Level 3, Level 3 → Level 2 MSB or LSB: Level 0 → Level 1 or Level 2, Level 1 → Level 0 or Level 3, Level 2 → Level 0 or Level 3, Level 3 → Level 1 or Level 2 MSB and LSB: Level 0 → Level 3, Level 1 → Level 2, Level 2 → Level 1, Level 3 → Level 0

Table 1.3.2.3-10 Error Addition (Cont'd)

Item	Specifications
PCIe6 FEC Symbol Error	This is available only when Coding is PAM4.*2 An error is inserted to make the PAM4 signal change by one level only. PAM4: An error is inserted every 4 or 12 PAM4 symbols.
Source	Internal, External-Trigger (Rising edge trigger), External-Disable (L: Disable)
Error Variation	Repeat, Single (Cannot be selected when Source is External-Trigger.)
PCIe6 Standard	x1 Link Common CLK/SRNS Mode x2 Link Common CLK/SRNS Mode x4 Link Common CLK/SRNS Mode x8 Link Common CLK/SRNS Mode x16 Link Common CLK/SRNS Mode x1 Link SRIS Mode x2 Link SRIS Mode x4 Link SRIS Mode x8 Link SRIS Mode x16 Link SRIS Mode
SKP	No SKP, SKPx1, SKPx2
Flit Error Interval	Add every 8 Bits(Do not distinguish ECC groups) Add every 24 Bits(Add to only ECC Group)
PAM4 Symbol Error per Flit	1 to 8 FEC Symbols, in steps of 1 FEC Symbol The upper limit value is "4" if PCIe6 Standard is set to one of the following: x16 Link Common CLK/SRNS Mode x16 Link SRIS Mode
Flit Error per Control SKP Interval	1 to 4 Flits, in steps of 1 Flit
Total BER for All Lane	*E–n (* = 1 to 9, n = 3 to 12), Upper limit: 7.0E–3 The error addition range varies depending on the PCIe6 Standard and the values set for PAM4 Symbol Error per Flit and Flit Error per Control SKP Interval.
PAM4 Symbol Error for One Lane	*E–n (* = 1 to 9, n = 3 to 12), Upper limit: 7.0E–3 The error addition range varies depending on the PCIe6 Standard and the values set for PAM4 Symbol Error per Flit and Flit Error per Control SKP Interval.

Table 1.3.2.3-10 Error Addition (Cont'd)

Item	Specifications
PCIe6 FEC Symbol Error (Cont'd) Error Addition Method	Type1: Level 0 → Level 1, Level 1 → Level 2, Level 2 → Level 3, Level 3 → Level 2 Type2: Level 0 → Level 1, Level 1 → Level 2, Level 2 → Level 1, Level 3 → Level 2 Type3: Level 0 → Level 1, Level 1 → Level 0, Level 2 → Level 1, Level 3 → Level 2 Type4: Level 0 → Level 1, Level 1 → Level 0 or Level 2, Level 2 → Level 1 or Level 3, Level 3 → Level 2 MSB Only: Level 0 → Level 2, Level 1 → Level 3, Level 2 → Level 0, Level 3 → Level 1 LSB Only: Level 0 → Level 1, Level 1 → Level 0, Level 2 → Level 3, Level 3 → Level 2 MSB or LSB: Level 0 → Level 1 or Level 2, Level 1 → Level 0 or Level 3, Level 2 → Level 0 or Level 3, Level 3 → Level 1 or Level 2 MSB and LSB: Level 0 → Level 3, Level 1 → Level 2, Level 2 → Level 1, Level 3 → Level 0

Table 1.3.2.3-10 Error Addition (Cont'd)

Item	Specifications
PAM3 Error Addition	This is available only when Coding is PAM3.
Error on LSB&MSB	Add the specified Symbol Error.
Source	Internal, External-Trigger (Rise edge trigger), External-Disable (L: Disable)
Error Variation	Repeat, Single (Cannot be selected when Source is External-Trigger.)
Symbol Error Rate	*E–n (* = 1 to 9, n = 3 to 12). Upper limit: 3.0E–3
Symbol/Burst	Symbol, Burst switching
Burst Length	1 to 256, 1 step
Error Addition Method	Type6: Level 0 → Level 2, Level 1 → Level 0, Level 2 → Level 0

Table 1.3.2.3-11 Data Output

Item	Specifications*1
Number of Outputs	2 (Data and XData): individual configuration not supported
Coding	NRZ, PAM4, PAM3
NRZ Eye Amplitude	
Setting Range	NRZ: 70 to 800 mVp-p, 2 mV step (Single-Ended)
Accuracy	When using the J1789A: ±35 mV ±12 % (Single-Ended) *2 When using the J1790A: ±35 mV ±12 % (Single-Ended) *3, *4

*1: Unless otherwise specified, these are specified with the conditions of PRBS2^{31}–1, Mark ratio 1/2, and Cross Point 50 %.

The values shall be observed by using an optional accessory, J1790A, and a 100-GHz bandwidth sampling oscilloscope.

*2: Setting Range ≤ 700 mVp-p

*3: Setting Range ≤ 700 mVp-p (≤ 32.1 Gbit/s)

*4: Setting Range ≤ 650 mVp-p (32.1 < Bit rate ≤ 64.2 Gbit/s)

Table 1.3.2.3-11 Data Output (Cont'd)

Item	Specifications*1
PAM3/4 Eye Amplitude	
PAM4 (0/3 Level) Setting Range	PAM4(0/3 Level): 70 to 800 mVp-p, 1 mV step (Single-Ended) *5
PAM4 (0/3 Level) Accuracy	When using the J1789A: ±35 mV ±12 % of Amplitude*2, *6 When using the J1790A: ±35 mV ±12 % of Amplitude*3, *4, *6
PAM4 (0/1, 1/2, 2/3 Level) Independently variable	Provided, 20 to 50 %, in steps of 1 mV (Eye amplitude conversion) (PAM4 Amplitude 0/3 level is assumed to be 100 %.)
PAM4 (0/1, 1/2, 2/3 Level) Setting Range	PAM4(0/1 Level): 23 to 266 mVp-p, 1 mV step (Single-Ended) PAM4(1/2 Level): 24 to 268 mVp-p, 1 mV step (Single-Ended) PAM4(2/3 Level): 23 to 266 mVp-p, 1 mV step (Single-Ended)
PAM4 (0/1, 1/2, 2/3 Level) Accuracy	When using J1789A: ±35 mV ±12 % of Amplitude*7 When using J1790A: ±35 mV ±12 % of Amplitude*8, *9
PAM3 (0/2 Level) Setting Range	PAM3(0/2 Level): 48 to 532 mVp-p, 1 mV step (Single-Ended)
PAM3(0/2Level) Accuracy	When using J1789A: ±35 mV ±12 % of Amplitude*10, *13 When using J1790A: ±35 mV ±12 % of Amplitude*11, *12, *13
PAM3 (0/1, 1/2 Level) Independently variable	Available, 20.0 to 80.0 %, 0.1 % Step (PAM3 Amplitude 0/2 level is assumed to be 100%.)
PAM3 (0/1, 1/2 Level) Setting Range	PAM3(0/1 Level): 24 to 266 mVp-p, 1 mV step (Single-Ended) PAM3(1/2 Level): 24 to 266 mVp-p, 1 mV step (Single-Ended) However, when the eye ratio is set, the amplitude can be set with a resolution finer than 1 mV.
PAM3 (0/1, 1/2 Level) Accuracy	When using J1789A: ±35 mV ±12 % of Amplitude*14 When using J1790A: ±35 mV ±12 % of Amplitude*15, *16

*5: When PAM4 output signal is directly input to the ED, the lower limit for the error-free amplitude depends on the performance of the ED used.

When using MP1862A as ED, the lower limit for the error-free amplitude (reference data) is as follows:

125 mV (0/3 Level, ≤ 32.1 Gbaud)

250 mV (0/3 Level, ≤ 58.2 Gbaud)

Pattern: PRBS15, at a constant temperature between 20 and 30 °C

*6: Single-Ended, PAM4 0/3 Level, and when setting each of PAM4 Amplitude (3/2, 2/1 and 1/0) equally to 33 %

*7: Setting Range ≤ 234 mVp-p, Single-Ended, at each amplitude level (Upper, Middle, Lower)

*8: Setting Range ≤ 234 mVp-p, Single-Ended, at each amplitude level (Upper, Middle, Lower)
(≤ 32.1 Gbaud)

*9: Setting Range ≤ 217 mVp-p, Single-Ended, at each amplitude level (Upper, Middle, Lower)
(32.1 < Baud rate ≤ 64.2 Gbaud)

*10: Setting Range ≤ 466 mVp-p

*11: Setting Range ≤ 466 mVp-p (≤ 32.1 Gbaud)

*12: Setting Range ≤ 433 mVp-p (32.1 < Baud rate ≤ 64.2 Gbaud)

*13: Single-ended, with the PAM3 0/2 level and PAM3 amplitudes (2/1 and 1/0) set equally to 50%.

*14: Setting Range ≤ 234 mVp-p, Single-Ended, at each amplitude level (Upper, Lower)

*15: Setting Range ≤ 234 mVp-p, Single-Ended, at each amplitude level (Upper, Lower) (≤ 32.1 Gbaud)

*16: Setting Range ≤ 217 mVp-p, Single-Ended, at each amplitude level (Upper, Lower) (32.1 < Baud rate ≤ 64.2 Gbaud)

Table 1.3.2.3-11 Data Output (Cont'd)

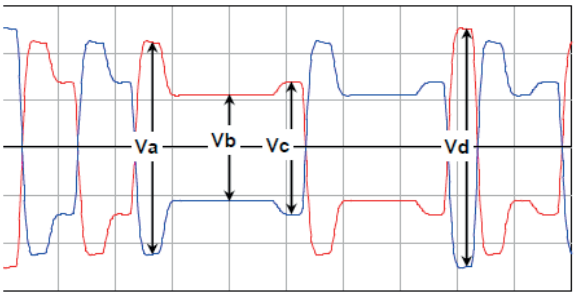
Item	Specifications*1
Offset	
Offset reference	Vth
Setting Range	–2.0–Eye Amplitude/2 to +3.3–Eye Amplitude/2 Vth, 1 mV step (Single-Ended)
Accuracy	±65 mV ±10 % of offset (Vth) ± (Total Amplitude Accuracy / 2) (Except when Emphasis is turned On with the MU196020C-x11 installed.)
Cross Point	Typ. 50 % (fixed)
Tr/Tf	Typ. 6.0 ps (20-80%) at 32,64Gbaud, When using the J1789A Typ. 7.0 ps (20-80%) at 32,64Gbaud, When using the J1790A
Half Period Jitter	
Setting Range	–20.0 to +20.0, 0.1 step
Accuracy	Typ. ±0.04 UI
Jitter	
Measurement conditions	NRZ, 32, 64 Gbit/s Clock Input: 8 GHz (using MU191000A + MU181500B or MG369xA/B/C + MU181500B)
Jitter RMS	≤ 600 fs rms (Count of measured jitters: 30)
Intrinsic RJ	≤ 108 fs rms (Repeating pattern of 1,0)*17
Peak to Peak Jitter	≤ 6 ps p-p (Count of measured jitters: 30)
Random Noise	≤ 4.75 mVrms*17
Waveform Distortion (0-peak)	±110 mV
PAM4 Level Separation Mismatch Ratio (R_{LM})	≥ 0.95 ≥ 0.975 (Adjustable.)
Signal to noise and distortion ratio (SNDR)	PAM4: typ. 35 dB*18 PAM3: typ. 41 dB*19

*17: Bit Rate 64.0 Gbit/s (with Option 003, y13, or y23)

*18: Baud Rate 64.0 Gbaud (with Option 003, y13, or y23)
PRBS13Q at 0.8 Vp-p (differential), applied using the J1793A Pick OFF Tee
For details on the calculation method, refer to the *PCIe7 specification*.

*19: Baud Rate 25.600 004 Gbaud, 1.0 Vp-p (differential), observed using a real-time oscilloscope
For details on the calculation method, refer to the *USB4 Gen4 specification*.

Table 1.3.2.3-11 Data Output (Cont'd)

Item	Specifications*1
Electrical TDECQ	0.9 dB*20
Output ON/OFF	ON/OFF switching available
Glitch-free	ON/OFF switching available Glitch-free operation without interrupting the PPG output during frequency changes.
Data / XData Skew	±1 ps Cable error not included.
Termination	AC, DC switching For DC: GND, –2V, +1.3V, +3.3V, Open (LVDS), 50 Ω
Connector	V connector (j.)
Level Guard	Amplitude, Voh and Vol can be set.
External ATT Factor	–40 to 0 dB, in steps of 0.1 dB When the fixed attenuator is connected, the amplitude and offset of the signal output via the fixed attenuator are displayed.
Emphasis	With Option x11
Emphasis Tap	4 Tap
Cursor Setting Range/Step	Coeficient: -2.0000 to +2.0000, 0.0001 step De-Emphasis: –20 to +20 dB, in steps of 0.01 dB (Post-Cursor: $20\log_{10}Va/Vb$, Pre-Cursor: $20\log_{10}Vc/Vb$) The coefficient of each tap is common to the Upper, Middle, and Lower eyes. Independent adjustment for each eye is not supported. 
Accuracy	± (35 mV + 10 % of Total Amplitude x Coeficient)
Setting Range of Emphasis Peak Voltage	• For NRZ and PAM4 modes Max. 800 mVp-p (Single-Ended) • For PAM3 mode Max. 532 mVp-p (Single-Ended)
Emphasis ON/OFF	ON/OFF switching

*20: Baud Rate 64.0 Gbaud (with Option 003, y13, or y23)

Table 1.3.2.3-11 Data Output (Cont'd)

Item	Specifications*1
Channel Emulator*21, *22	Normal: Outputs the PPG Data signal whose waveform emulates the connected transmission line with the loaded S parameter. Inverse: Outputs the PPG Data signal whose inverse characteristics emulate the transmission line with the loaded S parameter.
Response	Normal, Inverse switching
S-Parameter file	S2P file (Extension: "*.s2p"), S4P file (Extension: "*.s4p") S2P and S4P S-parameter files (from MS4640B Series vector network analyzers)
Channel Emulator ON/OFF	ON/OFF switching
Gain Adjust	Adjusts the loss to emulate and loss of the loaded S parameter at the specified frequency, when Response is Normal. 0GHz, 1GHz, Nyquist Frequency switching
Adjustable ISI*21	Sets the loss of the channel which generates ISI and outputs the PPG data signal whose waveform emulates the setting. (Output waveform amplitude is normalized to the set amplitude.)
Loss Channel	This is available for MU196020C in combination with the following. Not Specified: an external loss channel board J1800A×1 Short Channel: one J1800A (optional accessory) J1800A×2 Middle Channel: two J1800As (optional accessory) J1800A×3 Long Channel: three J1800As (optional accessory) J1758A: a J1758A (optional accessory) MU195050A Noise: an MU195050A Noise Module J1793A Pick OFF Tee: Combination with the J1793A Pick OFF Tee (optional accessory)
Frequency	Insertion Loss can be set at Nyquist or 1/2 Nyquist Frequency.

*21: With Option z40

*22: It is assumed to use for the purpose of compensating the loss of the transmission line.

The following graph shows typical limits for adjustable insertion loss. However, it does not mean that all the responses emulated from the S-Parameter file are compensated as the graph shows.

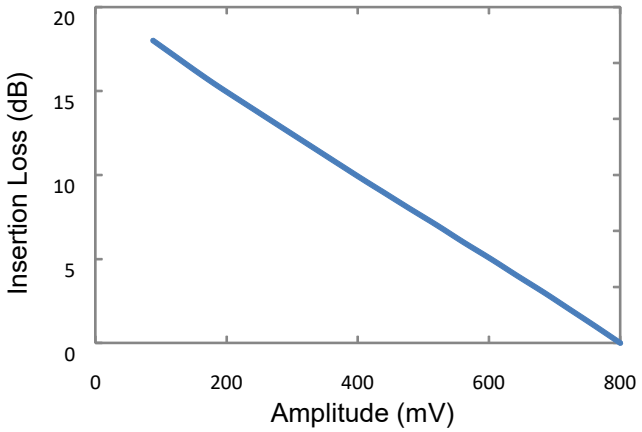


Table 1.3.2.3-11 Data Output (Cont'd)

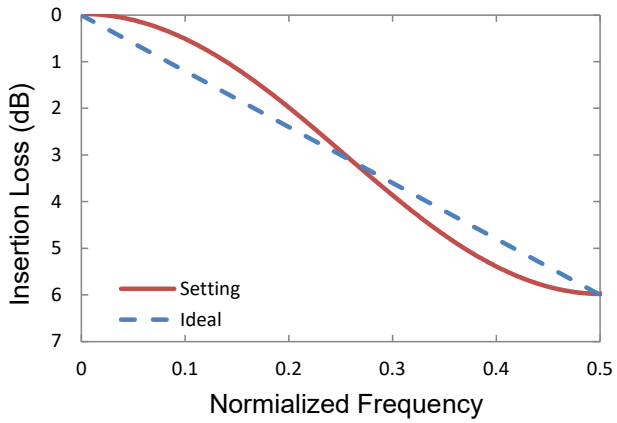
Item	Specifications*1
Insertion Loss	Displays the absolute loss that is sum of the loss selected for Loss Channel and the setting value of Tuning Insertion Loss at Nyquist Frequency and 1/2 Nyquist Frequency.
Tuning Insertion Loss	The relative loss from the loss value of Loss Channel can be set. –8.00 to 8.00 dB, in steps of 0.01 dB, Nyquist Frequency –8.00 to 8.00 dB, in steps of 0.01 dB, 1/2 Nyquist Frequency
Insertion Loss Accuracy	±1.0 dB Nominal @Nyquist Frequency 6 dB, Repeating pattern of "1,0" *23, *25, *26 ±1.5 dB Nominal @Nyquist Frequency 6 dB, Repeating pattern of "1,0" *24, *25, *26 ±1.0 dB Nominal @1/2Nyquist Frequency 3 dB, Repeating pattern of "1,1,0,0" *23, *25, *26 ±1.5 dB Nominal @1/2Nyquist Frequency 3 dB, Repeating pattern of "1,1,0,0" *24, *25, *26
Adjustable ISI ON/OFF	ON/OFF switching
Insertion Loss Compensation	With Options 11 and 45 Modulation: PAM3, Baud Rate: USB4 Gen4: Corrects the insertion loss at the Nyquist frequency by using Emphasis.
Setting Range	0.0 to 2.0 dB, in steps of 0.1 dB
Insertion Loss Accuracy	Since the BERT Insertion Loss*27 is calibrated using an oscilloscope, the accuracy of the setting value is not guaranteed, and it is set to Typ.
Insertion Loss Compensation ON/OFF	ON, OFF switching

*23: Baud Rate 26.6 Gbaud (when Options 001, 002, y12, 003, y13, and y23 installed)

*24: Baud Rate 53.1 Gbaud (when Options 002, y12, Option 003, y13, and y23 installed)

*25: Eye Amplitude 0.5 Vp-p, at each spectrum, at a constant temperature between 20 and 30 °C

*26: The frequency characteristics of Insertion Loss Accuracy when setting 6 dB@Nyquist Frequency and 3 dB@1/2 Nyquist Frequency are shown below.



*27: BERT Insertion Loss is a required specification for measuring instruments in the USB4 Version 2 GEN4 Electrical Compliance Test Specification (CTS).

Table 1.3.2.3-12 Clock Output

Item	Specifications*
Frequency Full Rate Half Rate Quarter Rate	 Operation Baud Rate = Clock Output Frequency 2.4 to 32.1 GHz (Option 001) Operation Baud Rate = (Clock Output Frequency) × 2 1.2 to 16.05 GHz (Option 001) 1.2 to 29.1 GHz (with Option 002 or y12) 1.2 to 32.1 GHz (with Option 003, y13, or y23) Operation Baud Rate = (Clock Output Frequency) × 4 0.6 to 8.025 GHz (Option 001) 0.6 to 14.55 GHz (with Option 002 or y12) 0.6 to 16.05 GHz (with Option 003, y13, or y23)
Number of Outputs	1
Amplitude	Min. 0.3 Vp-p, Max. 1.0 Vp-p (Output Frequency ≤ 16.05 GHz) Min. 0.4 Vp-p, Max. 1.0 Vp-p (Output Frequency > 16.05 GHz)
Output control	ON, OFF switching
Termination	50 Ω, AC Coupling
Connector	K connector (j.)

*: These values are monitored using an optional accessory (J1439A) at a sampling oscilloscope bandwidth of 70 GHz.

Table 1.3.2.3-13 Data Delay*1

Item	Specifications
Phase variable range	–1000 to +1000 mUI, in steps of 2 mUI
Accuracy	±50 mUIp-p*2, *3, *4 ±100 mUIp-p*2, *3, *5
mUI – ps switching	Available (internally converted into ps)
Calibration	Available (when jitter modulation is off)
Calibration indicator	This is displayed when one of the following conditions is met: ● 1/1 Clock frequency change by ±250 kHz. ● Ambient temperature change by ±5°C.

*1: With Option x30

*2: Unless otherwise specified, the following measurement conditions apply.
Using a 70 GHz bandwidth sampling oscilloscope
Eye Amplitude 0.5Vp-p (NRZ/PAM4)
Using optional accessory J1790A

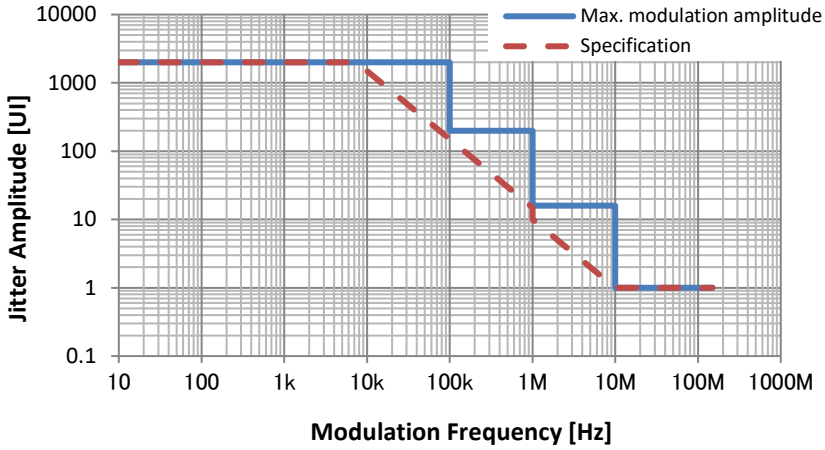
*3: Typical value

*4: Baud rate ≤ 32.1 Gbaud

*5: Baud rate > 32.1 Gbaud

Table 1.3.2.3-14 Jitter Tolerance

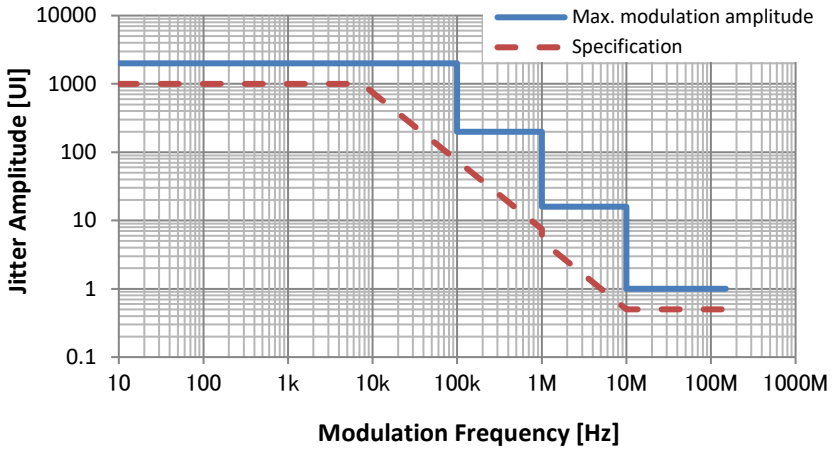
Item	Specifications
Jitter tolerance	PCIe 5/6 Baud rate 32.0 Gbaud PRBS 2^{23}–1, PAM4 When clock modulation by SSC (33 kHz, 5300 ppm, Down Spread) and RJ (500 fs rms) are applied simultaneously using MU181500B.



Modulation frequency [Hz]	Max. modulation amplitude [UIp-p]	Specification [UIp-p]
10	2 000	2 000
7 500	2 000	2 000
10 000	2 000	1 500
100 000	2 000	150
1 000 000	200	15
10 000 000	16	1
150 000 000	1	1

Table 1.3.2.3-14 Jitter Tolerance (Cont'd)

Item	Specifications
Jitter tolerance (Cont'd)	PCIe 7 Baud rate 64.0 Gbaud PRBS 2^{23}–1, PAM4 When clock modulation by SSC (33 kHz, 5300 ppm, Down Spread) and RJ (125 fs rms) are applied simultaneously using MU181500B. Defined at measurement points where the modulation frequency is ≥ 400 kHz and the BER is < 1E-12.



$\frac{1.9156 \times 10^{12}}{F^{1.9969}}$ (400 kHz ≤ F < 1 MHz)

$\frac{8.192 \times 10^{9}}{F^{1.6021}}$ (1 MHz ≤ F < 10 MHz)

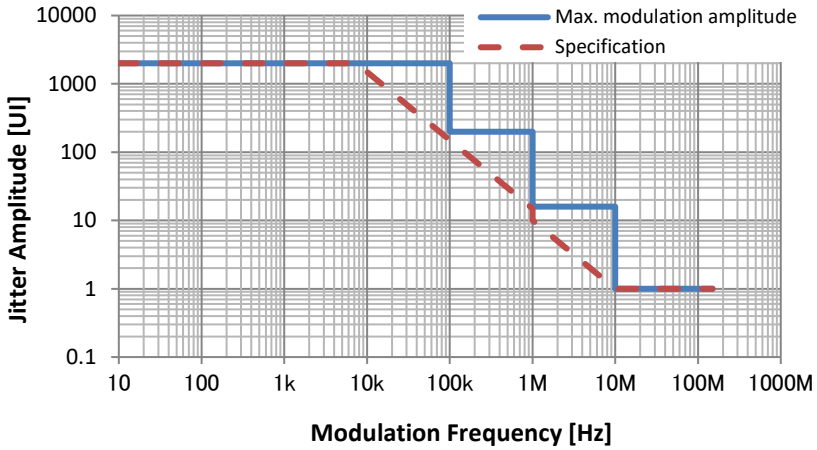
0.05 (F ≤ 10 MHz)

(The specification values are the same as those for F ≥ 400 kHz as defined in PCI Express® Base Specification Revision 7.0.)

Modulation frequency [Hz]	Max. modulation amplitude [UIp-p]	Specification [UIp-p]
10	2 000	
7 500	2 000	
10 000	2 000	
100 000	2 000	
400 000	200	12.46
1 000 000	200	2.00
10 000 000	16	0.05
150 000 000	1	0.05

Table 1.3.2.3-14 Jitter Tolerance (Cont'd)

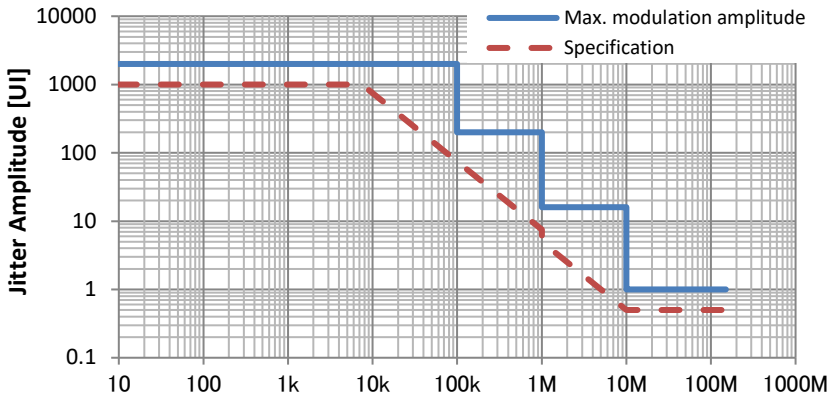
Item	Specifications
Jitter tolerance (Cont'd)	Ethernet 26G Baud rate 26.5625 Gbaud PRBS 2^{31}-1, PAM4 or NRZ



Modulation frequency [Hz]	Max. modulation amplitude [UIp-p]	Specification [UIp-p]
10	2 000	2 000
7 500	2 000	2 000
10 000	2 000	1 500
100 000	2 000	150
1 000 000	200	15
10 000 000	16	1
150 000 000	1	1

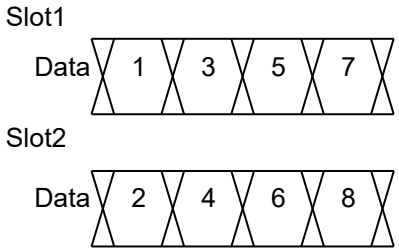
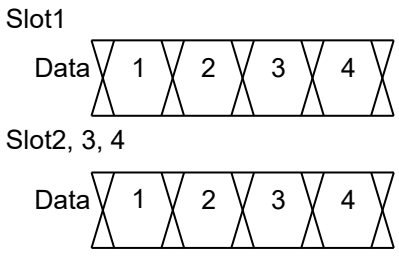
Table 1.3.2.3-14 Jitter Tolerance (Cont'd)

Item	Specifications
Jitter tolerance (Cont'd)	Ethernet 53G Baud rate 53.125 Gbaud PRBS 2^{31}-1, PAM4 or NRZ



Modulation frequency [Hz]	Max. modulation amplitude [UIp-p]	Specification [UIp-p]
10	2 000	1 000
7 500	2 000	1 000
10 000	2 000	750
100 000	2 000	75
1 000 000	200	7.5
10 000 000	16	0.5
150 000 000	1	0.5

Table 1.3.2.3-15 Multichannel Operation*1

Item	Specifications
Multi-Module Synchronization	A function to synchronize timing of generating patterns among multiple modules*2, *3, *4, *5, *6 Baud Rate ≤ 32.1 Gbaud: Capable of synchronizing bit generation timing with an accuracy of less than 1 UI. Baud Rate > 32.1 Gbaud: Capable of synchronizing bit generation timing with an accuracy of less than 5 UI
Inter-Module 2ch Combination	This is available only for NRZ. Generates signals of which the first bit generation timing is synchronized between modules. And, generates signals with the bit-interleaved generation bit patterns between modules. Supported applications include CEI-112G-NRZ (56 Gbit/s × 2ch). 
Inter-Module CH Synchronization	Generates signals of which the first bit generation timing is synchronized between modules. Supported applications include 400GbE (53.125 Gbaud x 4-ch) and CEI-112G-PAM4 (56 Gbaud x 4ch). 

*1: With Options x30 and x50

*2: The presence or absence of the following options must be the same across synchronized modules.
Option 001
Option 002 or y12
Option 003, y13, or y23

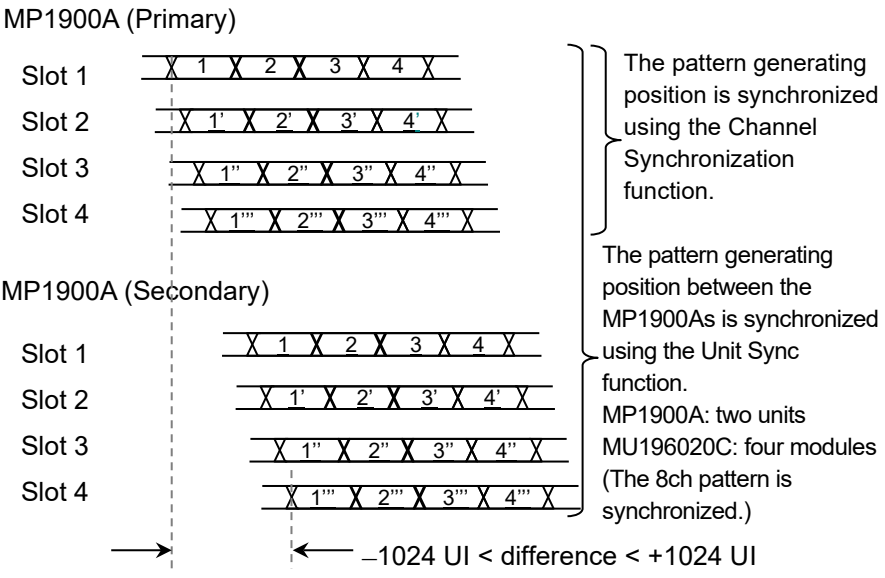
*3: Slots 1 to 2: Inter-Module 2ch Combination (only for NRZ)

*4: Slots 1 to 4: Inter-Module CH Synchronization

*5: The modules to be synchronized must be installed successively from Slot 1.

*6: In the range of ±3 °C from the temperature when performing the Multi Channel Calibration function, the bit generation timing is guaranteed.

Table 1.3.2.3-15 Multichannel Operation*1 (Cont'd)

Item	Specifications
Output Phase setting range Phase setting resolution	Only the items to be changed when Multi-Module Synchronization is set are described. –64 000 to +64 000 mUI*7 2 mUI*7
Pattern Data Length	When CH Combination is set: 4 to 536 870 912 bits, in steps of 2 bits When CH Synchronization is set: same as Sync OFF
Unit Sync*8	ON/OFF switching available
Number of Unit	Synchronous control available between up to two MP1900As. Maximum synchronous control: 8 channels (4 PAM4 PPGs per MP1900A × 2 MP1900A units)
Unit Sync Output*9	To output a timing signal from the Gating Out connector when **Unit Sync** is touched Provided with an inter-unit synchronization status indicator. The status indicator at Unit Sync turns orange when it requires to be timed to the other.
Unit Sync Input*9	To input a timing signal from the AUX In connector
Bit phase difference between MP1900As	Within ±1024 UI Timing difference between bit generations that occurs when **Unit Sync** is touched 

*7: Each channel can be set independently.

*8: Available only when using inter-module synchronization.

*9: Available only when **Unit Sync** is **ON**.

Table 1.3.2.3-16 General

Item	Specifications
Dimensions	21 mm (H), 234 mm (W), 175 mm (D) Excluding protrusions
Mass	2.5 kg max.
Operating Temperature	15 to 30 °C MP1900A's ambient temperature. MU196020A shall operate when installed.
Storage Temperature	–20 to 60 °C MU196020C installed to MP1900A shall comply with MIL-T-28800E Class 5.

1.3.3 ED

1.3.3.1 Specifications for MU195040A

Table 1.3.3.1-1 Operating Bit Rate

Item	Specifications
Operating bit rate	2.4 to 21.0 Gbit/s*1 2.4 to 32.1 Gbit/s*2

*1: Without Option x01

*2: With Option x01

Table 1.3.3.1-2 System Clock

Item	Specifications
System Clock	External, Clock Recovery, Clock and Data Recovery are optional.*

*: Available only with Option x22. If it is not installed, only External is available. Clock is recovered from the data input to the Data1 Input connector.

Table 1.3.3.1-3 Data Input

Item	Specifications
Number of inputs	2 (Data, XData) (Differential)*1 4 (Data1, XData1, Data2, XData2) (Differential)*2
Amplifier	Single-Ended 50 Ω, Differential 50 Ω, Differential 100 Ω can be set. At single-ended 50 Ω: Data and XData can be set. At differential 50/100 Ω: Tracking, Independent, Alternate can be set. When Alternate is selected: Data-XData and XData-Data can be set.*3 CTLE: ON, OFF Switching*4
Format	NRZ, PAM4
Amplitude*5	0.05 to 1.0 Vp-p (NRZ) 0.3 to 1.0 Vp-p (PAM4, ≤ 28.1 Gbaud) 0.4 to 1.0 Vp-p (PAM4, > 28.1 Gbaud)
Threshold	–3.5 to +3.3 V (1mV step) (Can be set separately.) (Absolute value of difference between Data and XData Threshold values shall be 3 V or less.)

*1: Option x10

*2: Option x20

*3: Absolute value of difference between Data and XData Threshold values shall be 1.5 V or less.

*4: Option x11 or Option x21

*5: The NRZ input amplitude is the range where the Auto Adjust function operates. The PAM4 input amplitude is the range where the PAM4 Auto Search function operates. Input sensitivity is the minimum input amplitude which becomes error-free.

Table 1.3.3.1-3 Data Input (Cont'd)

Item	Specifications
Sensitivity	NRZ*5,*6,*7 19 mVp-p*9, ≤27 mVp-p (21.0 Gbit/s) 22 mVp-p*9, ≤31 mVp-p (28.0 Gbit/s*8) PAM4*5,*7,*11 120 mVp-p*9, 40 mV/Eye (21.0 Gbaud, Eye Height 24 mV/Eye*9) 120 mVp-p*9, 40 mV/Eye (28.1 Gbaud*8, Eye Height 26 mV/Eye*9)
Eye Height (NRZ) *10	13 mV*9 (21.0 Gbit/s) 15 mV*9 (28.0 Gbit/s*8)

*6: PRBS31, Single-Ended, Mark ratio 1/2, CTLE OFF

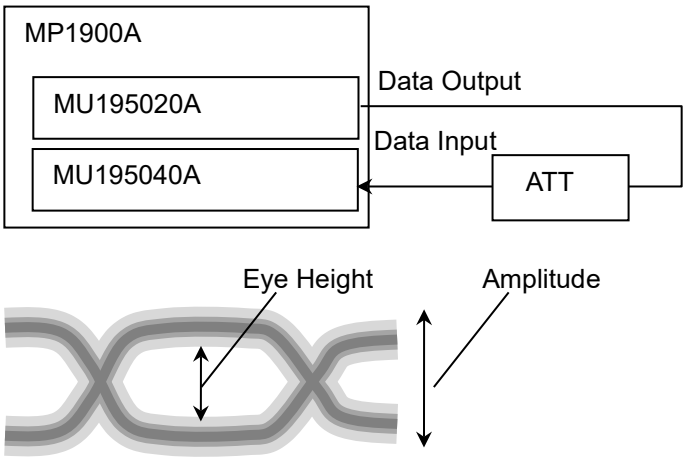
*7: Defined by one specific temperature in the range of 20 to 30 °C.

*8: Option x01

*9: Typical value

*10: Sensitivity of eye height.

Eye height is the minimum value that induces no bit error when MU195040A receives the output signal from MU195020A + ATT in the measurement system shown in the following figure (using a sampling oscilloscope of 70 GHz band or higher for measuring output amplitude).



*11: PRBS15, Single-Ended, marking rate equivalent to 1/2, CTLE OFF, MU195020A + G375A and back-to-back connection

Table 1.3.3.1-3 Data Input (Cont'd)

Item	Specifications
Phase margin	NRZ*6,*12 33 ps*9 (21.0 Gbit/s) 27 ps*9 (25.0 Gbit/s*8) 20 ps*9 (28.1 Gbit/s*8) 18 ps*9 (32.1 Gbit/s*8) PAM4 Middle*11,*13 13 ps*9 (21.0 Gbaud, Eye Width 26.5 ps*9) 8 ps*9 (25.0 Gbaud*8, Eye Width 20.0 ps*9) 5 ps*9 (28.1 Gbaud*8, Eye Width 15 ps*9) 2 ps*9 (32.1 Gbaud*8, Eye Width 13 ps*9) PAM4 Upper/Lower*11,*13 8 ps*9 (21.0 Gbaud*8, Eye Width 26.5 ps*9) 5 ps*9 (25.0 Gbaud*8, Eye Width 20.0 ps*9) 3 ps*9 (28.1 Gbaud*8, Eye Width 15.0 ps*9)
Termination	GND, 50 Ω, Variable, 50 Ω
Termination voltage	When Variable is selected for Termination: –2.5 to +3.5 V, 10 mV step
Connector	K (f.)
CTLE*4	
Band	OFF, 8-10 Gbit/s, 16-20 Gbit/s, 25-28 Gbit/s, PCIe3, PCIe4, PCIe5
CTLE Gain	
Setting range	0 to –12 dB, 0.1 dB step
Accuracy	±0.5 dB*9
Amplitude	0.05 to 0.4 Vp-p*14

*12: When using 0.5 Vp-p Input and External Clock.

*13: Emphasis ON (Best value in the range of 1Pre ≤ 3 dB/1 Post ≤ 1 dB), Based on the IEEE802.3bs measurement methods

*14: Input range that the signal is not saturated when CTLE is On.

Table 1.3.3.1-4 Clock Input

Item	Specifications
Number of inputs	1 (Single-Ended)
Frequency	1.2 to 16.05 GHz
Amplitude	0.3 to 1.0 Vp-p (–6.5 to +4.0 dBm)
Termination	AC, 50 Ω
Connector	SMA (f.)

Table 1.3.3.1-5 Aux Input, Aux Output

Item	Specifications
Aux Input	
Number of inputs	1 (Single-Ended)
Variation	External Mask, Burst, Capture External Trigger
Minimum pulse width	1/128 of Data rate
Input level	• 0/–1 V (H: –0.25 to 0.05 V / L: –1.1 to –0.8 V) • 0/–0.5 V (H: –0.05 to 0.05 V / L: –0.55 to –0.45 V) • Vth 0 V (Input amplitude 0.5 to 1.0 Vp-p) Select one of the above.
Termination	GND, 50 Ω
Connector	SMA (f.)
Aux Output	
Number of outputs	2 (Differential)
Variation	1/n Clock (n = 4, 6, 8, 10…510, 512), Pattern Sync*, Sync. Gain, Error Output
Pattern Sync	
PRBS, PRGM	Position: 1 to {(Least common multiple of Pattern Length' and 128) – 135}, in 8-bit steps Pattern Length' shall be the value obtained by multiplying Pattern Length setting until it becomes 512 or more if it is 511 or less.
Mixed Data	Block No. setting: 1 to the Block No. specified for Mixed Data, in 1-steps Row No. setting: 1 to the Row No. specified for Mixed Data, in 1-steps
Output level	0/–0.6 V (H: –0.25 to 0.05V / L: –0.80 to –0.45 V)
Termination	GND, 50 Ω
Connector	SMA (f.)

*: Cannot be selected when Test Pattern is HSSB Data.

Table 1.3.3.1-6 Pattern Detection

Item	Specifications
PRBS	
Pattern length	2^n–1 (n = 7, 9, 10, 11, 13, 15, 20, 23, 31)
Mark ratio	1/2 (1/2INV is supported by a logical inversion.)
Zero-Substitution	
Additional Bit	0 bit, 1 bit
Pattern length	2^n or 2^n–1 (n = 7, 9, 10, 11, 15, 20, 23)
Start position	Substitutes the bit coming after the maximum "0" successive bits.
Successive-zeros bit length	1 to (Pattern Length–1) bits If the bit coming after Zero-substitution is "0," then it is replaced with "1."
Data	
Data length	2 to 268435456 bits, in 1-bit steps
Mixed Pattern	
Pattern	Data
Mixed Block	To the smaller of the following values: 1 to 511 Block, in 1-Block steps $\mathrm{INT}\left(\frac{268435456}{\mathrm{ROW\,count}}\times\mathrm{Data\,length}\right)$ bits $\mathrm{INT}\left(\frac{268435456+2^{31}}{\mathrm{ROW\,length}}\times\mathrm{ROW\,count}\right)$ bits
Mixed Row Length	2048 to 268435456+2^{31} bits, in 1024-bit steps (Data + PRBS Length)
Data length	1024 to 268435456 bits, in 1-bit steps
Number of rows	1 to 16, in 1-steps
Number of blocks	1 to 511, in 1-steps
PRBS steps/Mark ratio	Same as PRBS.
PRBS Sequence	Restart, Consecutive
Descramble	Can be set per PRBS and Data for each Block (except the Data area for Block 1).
PAM4*1	
Pattern Type	Square Wave, JP03A, JP03B, PRQS10, SSPR, QPRBS13, QPRBS13-CEI, SSPRQ, Transmitter Linearity, PRBS13Q, PRBS31Q, User Define
User Define in detail	
Raw Data	PRBS, Data
PRBS Pattern Length	Same as PRBS.
PRBS Inversion	Logic Inversion/Non-Inversion of PRBS part
Data Length	Same as Data
Gray Coding	Gray Coding ON, OFF

*1: Configurable when 2ch Combination is set

Table 1.3.3.1-6 Pattern Detection (Cont'd)

Item	Specifications
HSSB Data*2	
Specification	PCIe1, PCIe2, PCIe3, PCIe4, PCIe5, USB3.0, USB3.1 Gen2
EIEOSQ	EIEOSQ Insertion: ON, OFF EIEOSQ Interval: 1 to 65536 pattern repeats, 1 step Enabled when Specification is PCIe1, PCIe2, PCIe3, PCIe4, or PCIe5 When Specification is PCIe3, PCIe4, or PCIe5, only ON is available for EIEOSQ Insertion.
SYNCOS	SYNC OS Insertion: ON, OFF SYNC OS Interval: 1 to 65536 pattern repeats, 1 step When Specification is USB3.0, only OFF is available. Enabled when Specification is USB3.1 Gen2.
Scrambler Seed	When Specification is set to PCIe1, PCIe 2, or USB3.0: FFFF When Specification is set to PCIe3, PCIe4, or PCIe5: Lane0, Lane1, Lane2, Lane3, Lane4, Lane5, Lane6, Lane7 When Specification is set to USB3.1 Gen2: 1DBFBC
Pre Coder	ON, OFF This is available only for PCIe5.
PCIe1	
Length	32 to 1024 bit, 8bit step
Coding	8b10b
PCIe2	
Length	32 to 1024 bit, 8bit step
Coding	8b10b
PCIe3	
Length	128 to 1024 bit, 128bit step
Coding	128b130b
PCIe4	
Length	128 to 1024 bit, 128bit step
Coding	128b130b
PCIe5	
Length	128 to 1024 bit, 128bit step
Coding	128b130b
USB3.0	
Length	32 to 1024 bit, 8bit step
Coding	8b10b
USB3.1 Gen2	
Length	128 to 1024 bit, 128bit step
Coding	128b132b

*2: Available only when **Module Combination** is set to **Independent** and the channel is **Data1**.

Table 1.3.3.1-6 Pattern Detection (Cont'd)

Item	Specifications
HSSB Data*2 (Cont'd)	
8b10b Pattern Editor	
Notation	Symbol, Bin, Hex
Scrambler Enable	Scrambles the selected symbols. ON, OFF
Scrambler Reset	Resets the seed value of scrambler on the selected symbols. ON, OFF
Code	K-code, D-code
K code	K28.0, K28.1, K28.2, K28.3, K28.4, K28.5, K28.6, K28.7 K23.7, K27.7, K29.7, K30.7
D code	D0.0 to D31.7
MSB First / LSB First	MSB First, LSB First
128b130b Pattern Editor	
Notation	Bin, Hex
Scrambler Enable	Scrambles the selected symbols. ON, OFF
Scrambler Reset	Resets the seed value of scrambler on the selected symbols. ON, OFF
DC Balance	Adds DC balance to the symbol 14 and 15. ON, OFF
Sync Header	Defines 2-bits Sync Header.
MSB First / LSB First	MSB First, LSB First
128b132b Pattern Editor	
Notation	Symbol Bin, Symbol Hex
Scrambler Enable	Scrambles the selected symbols. ON, OFF
Scrambler Reset	Resets the seed value of scrambler on the selected symbols. ON, OFF
DC Balance	Adds DC balance to the symbol 14 and 15. ON, OFF
Sync Header	Defines 4-bits Sync Header.
MSB First / LSB First	MSB First, LSB First

Table 1.3.3.1-7 Pattern Sequence

Item	Specifications
Sequence	Repeat, Burst
Repeat	Continuous Pattern
Burst	
Source	Internal, External-Trigger (Aux Input), External-Enable (Aux Input)
Delay	Internal: 0 to 2147483640 bits, in 8-bit steps Ext Trigger, Enable: 0 to 2147483520 bits, in 8-bit steps Adjust Method: Auto, Manual
Enable Period	Internal: 12800 to 2147482624 bits, in 256-bit steps Ext Trigger: 12800 to 2147483392 bits, in 256-bit steps
Burst Cycle	25600 to 2147483648 bits, in 1024-bit steps

Table 1.3.3.1-8 Measurement

Item	Specifications	
Measurement types	Error Rate:	0.0001E–18 to 1.0000E00
	Error Count:	0 to 9999999, 1.0000E07 to 9.9999E17
	Error Interval:	0 to 9999999, 1.0000E07 to 9.9999E17
	%Error Free Interval:	0.0000 to 100.0000
	Frequency:	2400.000 to 32100.000 MHz
	Frequency measurement accuracy:	±1 ppm ±1 kHz*1
	Clock Count:	0 to 9999999, 1.0000E07 to 9.9999E17
	Confidence Level:	0.0 to 99.9 %
	Sync Loss Interval:	0 to 9999999, 1.0000E07 to 9.9999E17
	Clock Loss Interval:	0 to 9999999, 1.0000E07 to 9.9999E17
Gating	Time, Clock Count, Error Count, Block Count	
Unit, Cycle setting	Time:	1 second to 99 days 23 hours 59 minute 59 seconds
	Clock Count:	> E+4 to > E+16
	Error Count:	> E+4 to > E+16
	Block Count:	> E+2 to > E+14
Gating Cycle	Single, Repeat, Untimed, Single (Target CL)	
Confidence Level	Available on MX190000A version 10.07.00 or later.	
	Target CL:	0 to 99.9 %
	Target ER:	1E-15 to 9E-3
	Target EC:	0 to 10
	Target Bitrate:	2.4 to 21.0 Gbit/s*2, *4 2.4 to 32.1 Gbit/s*3, *4
	PPG Target Bitrate Tracking:	Tracks the operating bit rate of the PPG that is selected from the PPGs installed in the same MP1900A.
Current	On, Off can be set.	
	Calculation:	Progressive, Immediate
	Interval:	100 ms, 200 ms, 500 ms

*1: When Gating is selected and the MP1900A reference clock 10 MHz is calibrated.

*2: Without Option x01

*3: With Option x01

*4: When **2ch Combination** is selected for Combination Setting, the bitrate used for Confidence Level calculation is twice the normal bitrate.

Table 1.3.3.1-8 Measurement (Cont'd)

Item	Specifications
Auto Sync	On, Off can be set. Synchronization threshold: INT, E–2 to E–8
Sync Control	PRBS: Automatic Synchronization Data: Frame On, Quick Mixed-Data: Frame On HSSB Data: Automatic Synchronization
Frame length	4 to 64 bits, in 4-bit steps
Frame mask	Available
Frame Position	1 to (Pattern Length – Frame Length +1) bits, in 1-bit steps
Error/Alarm conditions	
Error detection mode	• Total, Insertion, Omission • Transition, Non Transition
EI/EFI interval	1 ms, 10 ms, 100 ms, 1 s
SKP OS Filtering	Filters the SKP OS that are compliant with the following standards: • PCIe: Gen1, Gen2, Gen3, Gen4, Gen5 • USB: USB3.0, USB3.1 Gen2 This function is available only at the bit rate of each standard. When Test pattern is HSSB Data, only ON is enabled.

Table 1.3.3.1-9 Error Analysis

Item	Specifications
Block Window	Excludes the specified data pattern bit from the measurement target according to the settings. Invalid when "Mixed" pattern or "HSSB Data" is selected for Test Pattern.
Setting resolution	Pattern length (bits) / Step [bits] 2 to 2097152 / 1 2097153 to 4194304 / 2 4194305 to 8388608 / 4 8388609 to 16777216 / 8 16777217 to 33554432 / 16 33554433 to 67108864 / 32 67108865 to 134217728 / 64 134217729 to 268435456 / 128
Bit window*1	Excludes any channels among internal 32 channels from the measurement target.
External mask*1	H: Measurement L: Mask
Capture function*1	
Number of blocks	1, 2, 4, 8, 16, 32, 64, 128
Length of block	$\frac{8\,\text{Mbits}}{n}$ (n is Number of blocks.)
Trigger	Error Detect, Match Pattern, Manual Trigger, External Trigger (Rising Edge)
Trigger position	Top, Middle, Bottom
Matching pattern	4 to 64, in 4-bit steps
Automatic measurement function	Eye margin*1,*2, Bathtub*1,*2, Eye Contour*1,*2, PAM4 BER measurement Auto Adjust*3,*4,*5, Auto Search*3, Auto Search PAM4 mode*6

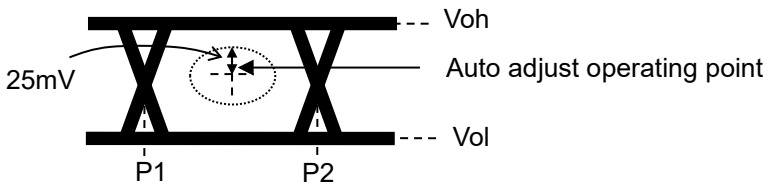
*1: Not available when "HSSB Data" is selected for Test Pattern.

*2: Unavailable when the system clock is set to Clock and Data Recovery.

*3: The input pattern must be an NRZ PRBS pattern with a mark ratio of 1/2.

*4: The Auto Adjust function obtains a point in the vicinity of the following as an optimum point:
- (Voh + Vol) / 2 in voltage direction
- (P1 + P2) / 2 in phase direction

The Auto Adjust function works properly when there are no mask-hits which are observed by the oscilloscope vertically within ±25 mV area from the Auto Adjust operating point.



*5: If eye diagram of input signal is not symmetric, the Auto Adjust may not adjust input signals to the optimum value. The Auto Search Fine is recommended to measure asymmetric input signals.

*6: Each of PAM4 waveform levels is equal. PRBS pattern with a mark ratio of 1/2.

Table 1.3.3.1-10 PAM4 BER Measurement

Item	Specifications
PAM4 BER Measurement	Available patterns • GrayPRBS7, 9, 10, 11, 13Q-IEEE200G_400G[Draft2], 15,20 • GrayPrePRBS20 • GrayPreQPRBS13-CEI • GrayPreQPRBS13-IEEE100GBASE-KP4_Lane0, 1, 2, 3 • GrayPRQS10 • GrayQPRBS13-CEI • GrayQPRBS13-IEEE100GBASE-KP4_Lane0, 1, 2, 3 • GraySSPR • PRBS7, 9, 10, 11, 13Q-IEEE200G_400G[Draft2], 15, 20 • PrePRBS20 • PreQPRBS13-CEI • PRQS10 • QPRBS13-CEI • QPRBS13-IEEE100GBASE-KP4_Lane0, 1, 2, 3 • Squarewave • SSPR • SSPRQ • Transmitter_Linearity

Table 1.3.3.1-11 Variable Clock Delay

Item	Specifications
Phase variable range	–1000 to +1000 mUI, 2 mUI step
Accuracy	±50 mUIp-p*1,*2
mUI – ps switching	Available
Calibration	Available
Calibration indicator	This indicator is on when Calibration is required due to: • Change in 1/1Clock frequency by ±250 kHz. • Change in the ambient temperature by ±5 °C.

*1: Using oscilloscope with residual jitter of less than 200 fs (RMS).

*2: Typical value

Table 1.3.3.1-12 Clock Recovery

Item	Specifications	
Clock source options	Clock Recovery, Clock and Data Recovery Clock*1	
Operating bit rate	**NRZ**	**PAM4**
	2.4 to 21.0 Gbit/s*2 2.4 to 32.1 Gbit/s*3	2.4 to 21.0 Gbaud*2 2.4 to 28.1 Gbaud*3 28.100 001 to 32.1 Gbaud*3,*4
Setting range	2.400000 to 21.000000 Gbit/s, 0.000001 Gbit/s step*2 2.400000 to 32.100000 Gbit/s, 0.000001 Gbit/s step*3	

*1: The system clock can be selected only with Option x22. Clock is recovered from the data input to the Data1 Input connector. The input pattern must be an NRZ PRBS pattern with a mark ratio of 1/2.
When PAM4 is set, clock recovery is performed with PRBS15, Data1 and Middle. Upper, Middle, Lower are measured with Data2.
At the back-to-back connection with MU195020A + J1741A + G0375A + J1728A, the target loop band is defined at the maximum bit rate of each Bit rate range.

*2: With Option x22

*3: With Option x01

*4: Typical value, BER 1.0E–7

Table 1.3.3.1-12 Clock Recovery (Cont'd)

Item	Specifications
Supported standard and bit rate	

Standard	Bit rate [Gbit/s]
100G ULH	32.100000*3
PCI Express Gen5	32.000000*3
32GFC	28.050000*3
100G OTU4	27.952496*3
100GbE(25.78x4)	25.781250*3
InfiniBand EDR	25.781250*3
SAS	24.000000*3
SAS4	22.500000*3
Thunderbolt2	20.625000
DisplayPort UHBR 20	20.000000
USB4 Gen3	20.000000
PCI Express Gen4	16.000000
InfiniBand FDR	14.062500
16G FC	14.025000
DisplayPort UHBR 13.5	13.500000
10G FC Over FEC	11.316800
10GbE Over FEC	11.095700
OTU2	10.709225
G975 FEC	10.664228
10G FC	10.518750
10GbE	10.312500
Thunderbolt1	10.312500
DisplayPort UHBR 10	10.000000
USB4 Gen2	10.000000
InfiniBand QDR	10.000000
USB3.1	10.000000
OC-192/STM-64	9.953280
8G FC	8.500000
DisplayPort HBR3	8.100000
PCI Express Gen3	8.000000
HSBI	6.250000
SATA 6Gb/s	6.000000
DisplayPort HBR2	5.400000
PCI Express Gen2	5.000000
USB3.0	5.000000
InfiniBand DDR	5.000000
4G FC	4.250000

Table 1.3.3.1-12 Clock Recovery (Cont'd)

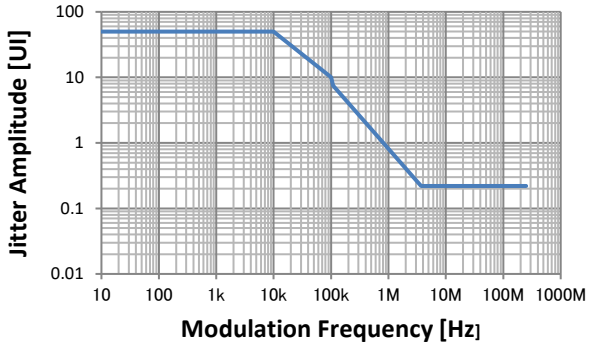
<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Supported standard and bit rate (Cont'd)</td><td>
<table>
<tr><th>Standard</th><th>Bit rate [Gbit/s]</th></tr>
<tr><td>XAUI</td><td>3.125000</td></tr>
<tr><td>SATA 3Gb/s</td><td>3.000000</td></tr>
<tr><td>DisplayPort HBR</td><td>2.700000</td></tr>
<tr><td>OTU1</td><td>2.666060</td></tr>
<tr><td>InfiniBand SDR</td><td>2.500000</td></tr>
<tr><td>PCI Express Gen1</td><td>2.500000</td></tr>
<tr><td>OC-48/STM-16</td><td>2.488320</td></tr>
</table>
</td></tr>
<tr><td>Operating bit rate tracking</td><td>Supported.
Tracking target: The operating bit rate of the PPG mounted to the same mainframe</td></tr>
<tr><td>Maximum number of consecutive zeros*5</td><td>72 bit (Zero Substitution 2^{15})</td></tr>
<tr><td>Lock range*5</td><td>±200 ppm</td></tr>
<tr><td>Target loop band</td><td>Available options are $\frac{\text{Bit rate}}{1667}$ MHz, $\frac{\text{Bit rate}}{2578}$ MHz, Jitter Tolerance*6 and Variable.
If the Variable option is selected, the following settings are available:
<table>
<tr><th>Bit rate [Gbit/s]</th><th>Setting Range [MHz]</th><th>Step [MHz]</th></tr>
<tr><td>2.400000 to 5.500000</td><td>3</td><td>-</td></tr>
<tr><td>5.500001 to 7.500000</td><td>3 to 4</td><td>1</td></tr>
<tr><td>7.500001 to 9.500000</td><td>3 to 5</td><td>1</td></tr>
<tr><td>9.500001 to 10.500000</td><td>3 to 6</td><td>1</td></tr>
<tr><td>10.500001 to 12.500000</td><td>3 to 7</td><td>1</td></tr>
<tr><td>12.500001 to 14.500000</td><td>3 to 8</td><td>1</td></tr>
<tr><td>14.500001 to 15.500000</td><td>3 to 9</td><td>1</td></tr>
<tr><td>15.500001 to 17.500000</td><td>3 to 10</td><td>1</td></tr>
<tr><td>17.500001 to 19.500000</td><td>3 to 11</td><td>1</td></tr>
<tr><td>19.500001 to 20.500000</td><td>3 to 12</td><td>1</td></tr>
<tr><td>20.500001 to 22.500000</td><td>3 to 13</td><td>1</td></tr>
<tr><td>22.500001 to 24.500000</td><td>3 to 14</td><td>1</td></tr>
<tr><td>24.500001 to 25.500000</td><td>3 to 15</td><td>1</td></tr>
<tr><td>25.500001 to 27.500000</td><td>3 to 16</td><td>1</td></tr>
<tr><td>27.500001 to 29.500000</td><td>3 to 17</td><td>1</td></tr>
<tr><td>29.500001 to 30.500000</td><td>11 to 18</td><td>1</td></tr>
<tr><td>30.500001 to 32.100000</td><td>11 to 19</td><td>1</td></tr>
</table>
</td></tr>
</table>

*5: With Option x22:
The target loop band is specified by the maximum setting value of each bit rate.

*6: The Jitter Tolerance option makes the loop band wider than the other options and enables the Jitter Tolerance measurement.

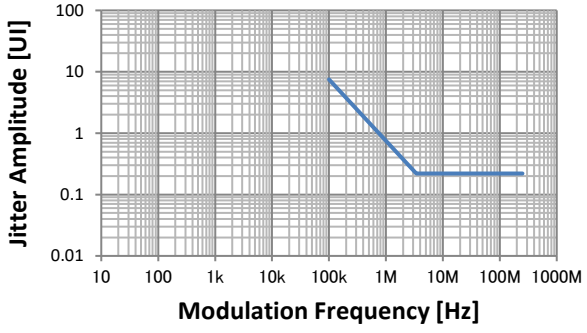
Table 1.3.3.1-12 Clock Recovery (Cont'd)

Item	Specifications
Jitter Tolerance Clock Recovery*7,*8	At the bit rate of 28.05 Gbit/s, conforming to Jitter Tolerance Mask defined by the "32G FC standard"



Modulation Frequency (Hz)	Jitter Tolerance Mask (UIp-p)
10	50
10,000	50
100,000	10
108,805	7.5
3,709,271	0.22
250,000,000	0.22

At the bit rate of 25.78125 Gbit/s, conforming to Jitter Tolerance Mask defined by the "100GbE (25.78 × 4) standard"

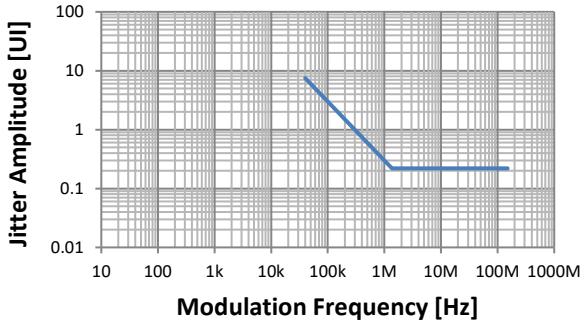


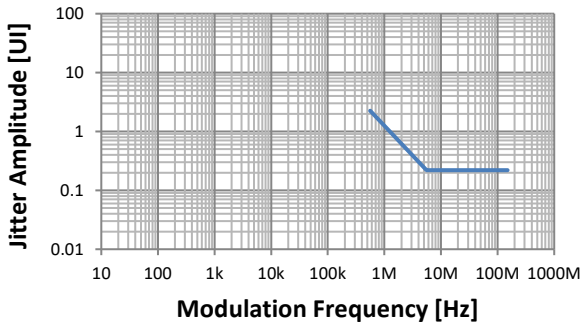
Modulation Frequency (Hz)	Jitter Tolerance Mask (UIp-p)
100,000	7.5
3,409,256	0.22
250,000,000	0.22

*7: Defined assuming the following conditions:
- Loop-back connection to MU195020A
- Test Pattern (Length): PRBS (2^31–1)
- Data input amplitude: 0.05 Vp-p

*8: Typical value, specified at 20 to 30 °C

Table 1.3.3.1-12 Clock Recovery (Cont'd)

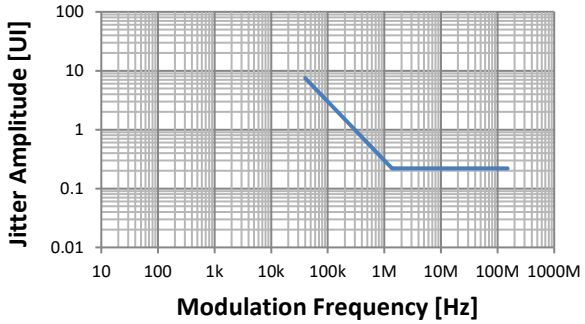
<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Jitter Tolerance
Clock Recovery (Cont'd)</td><td>At the bit rate of 14.0625 Gbit/s, conforming to Jitter Tolerance Mask defined by the "Infiniband FDR standard"
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Tolerance Mask (UIp-p)</th></tr>
<tr><td>40,000</td><td>7.5</td></tr>
<tr><td>1,363,636</td><td>0.22</td></tr>
<tr><td>150,000,000</td><td>0.22</td></tr>
</table>
At the bit rate of 14.025 Gbit/s, conforming to Jitter Tolerance Mask defined by the "16G FC standard"
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Tolerance Mask (UIp-p)</th></tr>
<tr><td>561,000</td><td>2.25</td></tr>
<tr><td>5,535,929</td><td>0.22</td></tr>
<tr><td>150,000,000</td><td>0.22</td></tr>
</table></td></tr>
</table>

Table 1.3.3.1-12 Clock Recovery (Cont'd)

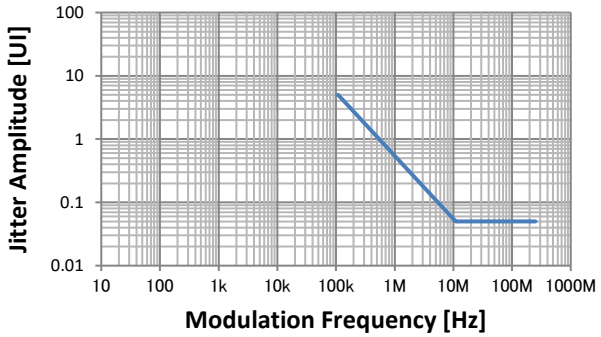
Item	Specifications
Jitter Tolerance Clock Recovery (Cont'd)	At the bit rate of 10.3125 Gbit/s, conforming to Jitter Tolerance Mask defined by the "10GbE standard"

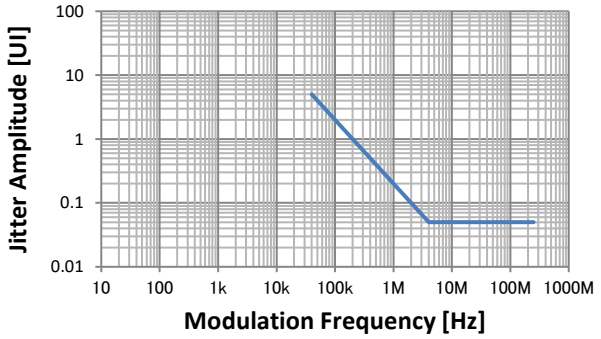


Modulation Frequency (Hz)	Jitter Tolerance Mask (UIp-p)
40,000	7.5
1,363,636	0.22
150,000,000	0.22

Table 1.3.3.1-12 Clock Recovery (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Jitter Tolerance

Data Clock Recovery</td><td>SSC with 5300 ppm amplitude can be simultaneously applied by using MU181500B.
At the bit rate of 28.05 Gbit/s
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Tolerance Mask (UIp-p)</th></tr>
<tr><td>108,805</td><td>5</td></tr>
<tr><td>10,880,528</td><td>0.05</td></tr>
<tr><td>250,000,000</td><td>0.05</td></tr>
</table>
At the bit rate of 25.78125 Gbit/s
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Tolerance Mask (UIp-p)</th></tr>
<tr><td>40,000</td><td>5</td></tr>
<tr><td>4,000,000</td><td>0.05</td></tr>
<tr><td>250,000,000</td><td>0.05</td></tr>
</table></td></tr>
</table>

Table 1.3.3.1-12 Clock Recovery (Cont'd)

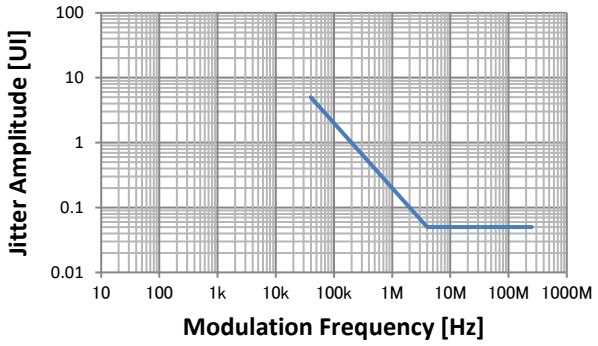
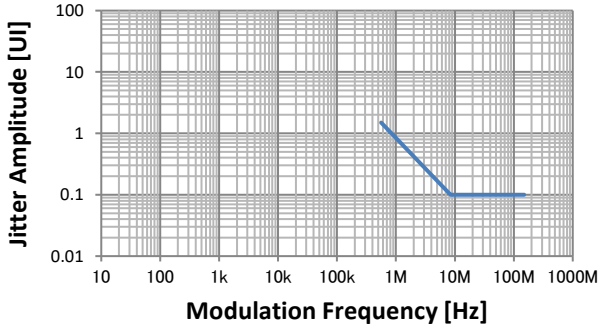
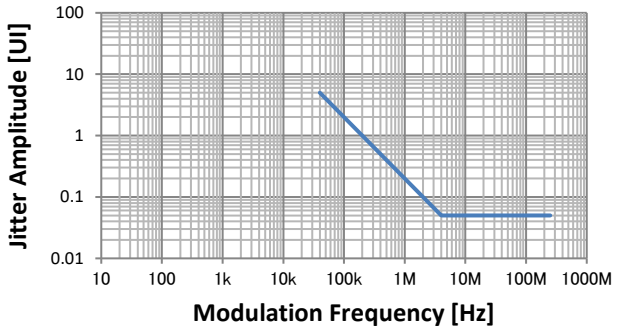
Item	Specifications
Jitter Tolerance Data Clock Recovery (Cont'd)	At the bit rate of 14.0625 Gbit/s  **Modulation Frequency (Hz) / Jitter Tolerance Mask (UIp-p)** 40,000 — 5 4,000,000 — 0.05 150,000,000 — 0.05 At the bit rate of 14.025 Gbit/s  **Modulation Frequency (Hz) / Jitter Tolerance Mask (UIp-p)** 561,000 — 1.5 8,413,317 — 0.1 150,000,000 — 0.1

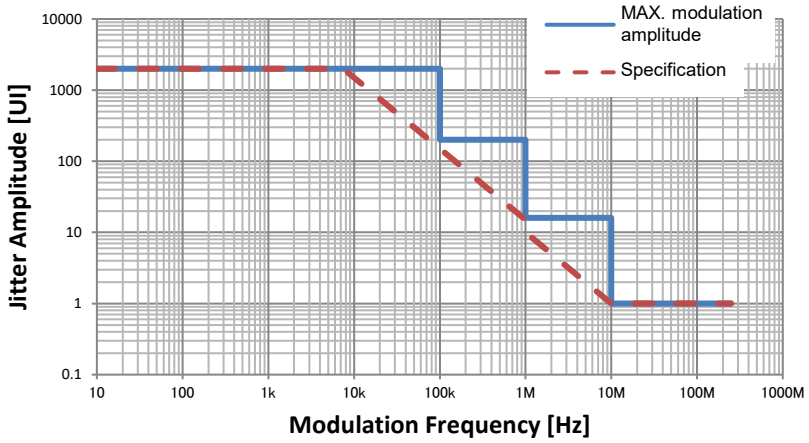
Table 1.3.3.1-12 Clock Recovery (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Jitter Tolerance
Clock Recovery (Cont'd)</td><td>At the bit rate of 10.3125 Gbit/s
 

<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Tolerance Mask (UIp-p)</th></tr>
<tr><td>40,000</td><td>5</td></tr>
<tr><td>4,000,000</td><td>0.05</td></tr>
<tr><td>250,000,000</td><td>0.05</td></tr>
</table></td></tr>
<tr><td>SSC tolerance</td><td>PCI Express Gen 5.0 compliant</td></tr>
</table>

Table 1.3.3.1-13 Jitter Tolerance

Item	Specifications
Jitter tolerance When using external clock	Bit rate: 16 Gbit/s, 28.1 Gbit/s*, 32.1 Gbit/s* Pattern: PRBS2^{31}–1 SSC with a 5300 ppm amplitude and RJ of 0.3 UI can be simultaneously applied by using MU181500B. These specifications are defined assuming the following conditions: Loopback connection to the MU195020A, defined by one specific temperature in the range of 20 to 30 °C. When RJ+BUJ/SJ3 is bigger than 0.5 UIp-p or SJ + RJ + BUJ/SJ3 is bigger than the standard value + 0.3 UIp-p, "Overload" is displayed on the MU181500B screen. Note that if Modulation Frequency is 33 kHz, and RJ+BUJ/SJ3 is bigger than 0.5UIp-p or SJ1 is bigger than 550 UIp-p, "Overload" is displayed on the MU181500B screen.



Modulation frequency [Hz]	MAX. modulation amplitude [UIp-p]	Specification [UIp-p]
10	2,000	2,000
7,500	2,000	2,000
100,000	2,000	150
1,000000	200	15
10,000,000	16	1
250,000,000	1	1

*: With Option x01

Table 1.3.3.1-14 Multichannel Operation*1

Item	Specifications
Combination*2	
Number of channels	2
Pattern	At Combination n = 2 below (2ch Combination)
Data	
Data Length	2 × n to 268435456 × n bits, in n-bit steps*3
Mixed	
Row Length	2048 × n to (268435456+2^{31}) × n bits, in 1024 × n bit steps*3
Data Length	1024 × n to 268435456 × n bits, in n-bit steps*3
HSSB Data	Not available for combination.
Block Window	Excludes the specified data pattern bit from the measurement target according to the settings. (Mask measurement function) Invalid when "Mixed" is selected for Test Pattern. Invalid when Zero-substitution is set to "2^n–1". n = 2 (2ch Combination) is considered in the following:
Setting resolution	Pattern length (bits) → Step [bits] 2 to 2 097 152 × n → 1 × n 2 097 153 to 4 194 304 × n → 2 × n 4 194 305 to 8 388 608 × n → 4 × n 8 388 609 to 16 777 216 × n → 8 × n 16 777 217 to 33 554 432 × n → 16 × n 33 554 433 to 67 108 864 × n → 32 × n 67 108 865 to 134 217 728 × n → 64 × n 134 217 729 to 268 435 456 × n → 128 × n
Burst	
Burst Cycle	25600 × n to 2147483648 × n bits, in 1024 × n bit steps*3
Enable Period	Internal: 12800 × n to 2147482624 × n bits, in 256 × n bit steps*3 Ext Trigger: 12800 × n to 2147483392× n bits, in 256 × n bit steps*3
Delay	Internal: 0 to 2147483640 × n bits, in 8 × n bit steps*3 Ext Trigger, Enable: 0 to 2147483520 × n bits, in 8 × n bit steps*3
Measurement	
Sync Control	
Frame length	4 × n to 64 × n bits, in 4 × n bit steps*3
Frame Position	1 to (Pattern Length' – Frame Length + n) bits, in n-bit steps

*1: Cannot be set when Test Pattern is HSSB Data.

*2: Combination extending over multiple slots cannot be set.

*3: Common to every channel specified by Combination Setting.

Table 1.3.3.1-14 Multichannel Operation*1 (Cont'd)

Item	Specifications
Error detection mode	Total, Insertion, and Omission
Eye Contour	
Measurement target	Data 1 to Data n*4
Eye Margin	
Measurement target	Data 1 to Data n*4
Bathtub	
Measurement target	Data 1 to Data n*4
Capture	2 ch Combination is available*3

*4: Separately specified for each channel.

Table 1.3.3.1-15 General

Item	Specifications
Dimensions	21 mm (H), 234 mm (W), 175 mm (D), Excluding protrusions
Mass	2.5 kg max.
Operating temperature	15 to 35 °C
Storage temperature	–20 to 60 °C

Table 1.3.3.1-16 Extension Function

Item	Specifications
PCIe	
Supported standards	PCI Express Base Specification Revision 4.0 Version 0.5, 0.7, 1.0 PCI Express Base Specification Revision 5.0 Version 1.0 Bitrate: PCIe Gen1, Gen2, Gen3, Gen4, Gen5 Lane number: ×1 Test target: Root Complex, End Point
Required option	Option x10/x11/x22 or x20/x21/x22
Required software	MX183000A-PL011: Follows the PCIe LTSSM to generate the training sequence required to transition the DUT to Loopback state. MX183000A-PL021: Follows the PCIe LTSSM to support negotiation with the DUT and provides LTSSM state transition logging and analysis. (One MU195020A and one MU195040A are required.) MX183000A-PL025: Extends the functionality of PL021 to support PCIe 5.0. Adding MX183000A-PL001 to each software option enables control of MU195020A, MU181500B, and MU195040A and supports Jitter Tolerance Test.

Table 1.3.3.1-16 Extension Function (Cont'd)

Item	Specifications
Loopback Through	Configuration, Recovery
Test Pattern	Modified Compliance Pattern Insert Delay Symbol: Enable, Disable (Available for Gen1 and Gen2) Insert SRIS: Enable, Disable (Available for Gen3, Gen4, and PCIe5) Compliance Pattern Insert Delay Symbol: Enable, Disable (Available for Gen1 and Gen2) User PRBS, Data
SKP Ordered Set Insertion	Enable, Disable
SKP Length/Insertion	For Gen1, Gen2 Length: COM+1, COM+2, COM+3, COM+4, COM+5 Interval: 768 to 3076, in 1-steps For Gen3, Gen4, Gen5 Length: 8, 12, 16, 20, 24 Interval: 187 to 750, in 1-steps
Dynamic Link Training	Available only when using MX183000A-PL021.
Counter	Tx SKP Count, Rx SKP Count (when using MX183000A-PL021) Error Rate, Error Count (when using MX183000A-PL021)
LTSSM Log	
Log Item	LTSSM State, Link Speed, Time[ns]
Log Size	16384 times
Termination condition	Memory full
USB	Supports the following USB tests when controlled by MX183000A.
Supported standards	USB3.0/3.1/3.2
Required option	For USB3.2x1*1: Option 10 or 20 For USB3.2x2*1: Option 20*2
Required software	MX183000A-PL022: Follows the USB LTSSM to support negotiation with the DUT and provides LTSSM state transition logging and analysis. One MU195020A and one MU195040A are required. Adding MX183000A-PL001 to MX183000A-PL022 enables control of MU195020A, MU181500B, and MU195040A and supports Jitter Tolerance Test. Adding MX183000A-PL023 to MX183000A-PL022 enables control of MU195020A and MU195040A and supports USB3.2x2 Link Training.

*1: With Option 22

*2: With MX183000A-PL023

1.3.3.2 Specifications for MU196040A

Table 1.3.3.2-1 Operating Baud Rate

Item	Specifications
Operating Baud Rate	With Option 001 PAM4 input: 2.4 to 32.1 Gbaud NRZ input: 2.4 to 32.1 Gbit/s

Table 1.3.3.2-2 System Clock

Item	Specifications
System Clock	External, Recovered Clock (with Option 022) External: Clock input from the Ext Clock Input connector Recovered Clock: Clock recovered from the data input from the Data Input connector

Table 1.3.3.2-3 Data Input

Item	Specifications
Number of inputs	2 (Data, XData) (Differential)
Input Condition	Single-Ended, Differential 50 Ohm, Differential 100 Ohm When set to Differential 50 Ohm or Differential 100 Ohm: Independent, Tracking, Alternate*1 When set to Alternate: Data-XData, XData-Data*2 When set to Single-Ended: Data, XData*3
Signal Type LSB/MSB Diagnostics	NRZ, PAM4 When set to PAM4, the PAM4 mode can be switched between as follows: Diagnostics Mode OFF: Treats signals as symbols by receiving LSB and MSB while synchronizing them with each other. Diagnostics Mode ON: Asynchronously receives LSB and MSB.
Amplitude	NRZ: The range in which the Auto Adjust function operates. PAM4: The range in which the Auto Search PAM4 Fine function operates. NRZ: 0.05 to 1.0 Vp-p*4 PAM4: 0.3 to 1.0 Vp-p*5
Threshold	NRZ, PAM4 Middle Eye Threshold: –3.5 to +3.3 V, in steps of 1 mV*2, *6 PAM4 Upper Eye Threshold: –3.9 to +3.7 V, in steps of 1 mV*7 PAM4 Lower Eye Threshold: –3.9 to +3.7 V, in steps of 1 mV*7

*1: Tracking is available only for NRZ.

*2: The absolute value of the difference between Data and XData Threshold values shall be 1.5 V or less.

*3: PAM4 Upper Eye and Lower Eye can be set by relative values to Middle Eye in the range of –0.4 V to +0.4 V.

*4: Single-Ended, Differential

*5: 0/3 Level, PRBS31, Single-Ended, Differential, when connecting directly to the MU196020A.

*6: Data and XData can be set independently.

*7: Data and XData cannot be set independently, and can be set in the range of ±0.4 V from Middle Eye Threshold.

Table 1.3.3.2-3 Data Input (Cont'd)

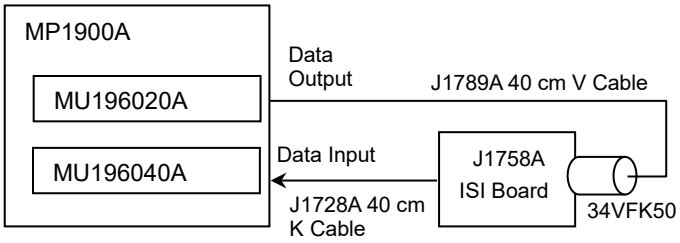
Item	Specifications
Sensitivity	Single-Ended , Mark Ratio1/2, when connecting directly to the MU196020A with J1789A. With Option 001, 34VKF50A shall be included. At a constant temperature between 20 and 30 °C
Eye Amplitude	NRZ, PRBS31 Typ. 32 mVp-p, ≤ 50 mVp-p*8 (26.5625 Gbit/s, 32.1 Gbit/s)
Eye Height	NRZ, PRBS31 Typ. 23 mV*8 (26.5625 Gbit/s, 32.1 Gbit/s) PAM4 0/1 1/2 2/3 Level, PRBS31, Eye Height where BER is 1E–06, when using External Clock Typ. 23 mV, ≤ 50 mV*8 (26.5625 Gbaud, 32.1 Gbaud)
Phase Margin	When connecting directly to the MU196020A with J1789A. With Option 001, 34VKF50A shall be included. At a constant temperature between 20 and 30 °C, when using External Clock NRZ, PRBS31, Differential, Mark Ratio 1/2, when inputting 1.0 Vp-p Typ. 25.8 ps*8 (26.5625 Gbit/s) Typ. 18.0 ps*8 (32.1 Gbit/s) PAM4 0/3 Level, Eye Width where BER is 1E–06, PRBS31, Single-Ended, Mark Ratio1/2, when inputting 0.5 Vp-p, Emphasis ON (Best values in the range of 1Pre ≤ 5 dB and 1Post ≤ 5 dB) Typ. 5.3 ps*8 (26.5625 Gbaud) Typ. 4.5 ps*8 (32.1 Gbaud)

*8: With Option 001

Table 1.3.3.2-3 Data Input (Cont'd)

Item	Specifications
Stressed Margin*9	
Stressed Eye Height	PAM4 0/1 1/2 2/3 Level, QPRBS13-CEI, Eye Height where BER is 1E–06, when using External Clock ≥ 32 mV*10
Stressed Eye Width	PAM4 0/1 1/2 2/3 Level, QPRBS13-CEI, Eye Width where BER is 1E–06, when using External Clock ≥ 7.15 ps*10
Termination	50 Ω, GND, Variable
Termination Voltage	When set to Variable: –2.5 to +3.5 V, in steps of 10 mV
Connector	K connector (f.) (with Option 001)

*9: Differential, Mark Ratio1/2, when connecting J1758A and MU196020A by using J1789A, 34VKF50A and J1728A.



At a constant temperature between 20 and 30 °C, measure with a 70-GHz bandwidth sampling oscilloscope with residual jitter of less than 200 fs (RMS).

Adjust De-Emphasis (2 Pre Cursors and 1 Post Cursor) of MU196020A so that the product of Eye Height (1E–06) and Eye Width (1E–06) can be maximized in the differential waveform.

Calculate the 4th-order Bessel Filter (Cutoff Frequency 50 GHz) + CTLE (+1 dB Peaking at 14 GHz) and calibrate it to a PAM4 waveform with Eye Amplitude of 0.88 Vp-p (Diff) or less and Eye Linearity RLM 0.85 or more.

*10: 28 Gbaud, with Option 001, BER 1E–12

Table 1.3.3.2-4 Clock Input

Item	Specifications
External Clock Input	Operation Baud Rate = Clock Input Frequency (with Option 001)
Number of inputs	1 (Single-Ended)
Frequency range	With Option 001 2.4 to 32.1 GHz
Amplitude	0.3 to 1.0 Vp-p (–6.5 to +4.0 dBm) (Input Frequency ≤ 16.05 GHz) 0.4 to 1.0 Vp-p (–3.9 to +4.0 dBm) (Input Frequency > 16.05 GHz)
Termination	50 Ω, AC Coupling
Connector	K connector (f.)

Table 1.3.3.2-5 AUX Input

Item	Specifications
Number of inputs	1 (Single-Ended)
Variation	External Mask, Burst
Minimum pulse width	1/256 of Data rate
Input level	• 0/–1 V (H: –0.25 to 0.05 V, L: –1.1 to –0.8 V) • 0/–0.5 V (H: –0.05 to 0.05 V, L: –0.55 to –0.45 V) • Vth 0 V (Input amplitude 0.5 to 1.0 Vp-p) Select one of the above.
Termination	50 Ω, GND
Connector	SMA connector (f.)

Table 1.3.3.2-6 AUX Output

Item	Specifications
Number of outputs	2 (Differential)
Variation	1/n Clock (n = 8, 12, 16, 20…1020, 1024), Pattern Sync, Sync Gain, Error Output
Pattern Sync PRBS, PRGM	Position: 1 to {(Least common multiple of Pattern Length' and 128) – 135}, in steps of 8 (with Option 001) Pattern Length' shall be the value obtained by multiplying Pattern Length setting until it becomes 1024 or more if it is 1023 or less.
Output level	0/–0.6 V (H: –0.25 to 0.05V, L: –0.80 to –0.45 V)
Termination	50 Ω, GND
Connector	SMA connector (f.)

Table 1.3.3.2-7 Pattern Detection

Item	Specifications
PRBS	
Pattern length	2^n–1 (n = 7, 9, 10, 11, 13, 15, 20, 23, 31)
Mark ratio	1/2, 1/2inv
PRBS generator polynomial	n=7: $1 + X^6 + X^7$ n=9: $1 + X^5 + X^9$ n=10: $1 + X^7 + X^{10}$ n=11: $1 + X^9 + X^{11}$ n=13: $1 + X + X^2 + X^{12} + X^{13}$ n=15: $1 + X^{14} + X^{15}$ n=20: $1 + X^3 + X^{20}$ n=23: $1 + X^{18} + X^{23}$ n=31: $1 + X^{28} + X^{31}$
PRBS Inversion	This is available in PAM4 mode only. Logically inverted PRBS can be set independently for MSB and LSB.
Zero-Substitution	This is available in NRZ mode only.
Additional Bit	0 bit, 1 bit
Pattern length	2^n or 2^n–1 (n = 7, 9, 10, 11, 15, 20, 23)
Start position	Substitutes the bit coming after the maximum “0” successive bits.
Zero-Length	1 to (Pattern Length – 1) bits If the bit coming after Zero-substitution is “0,” then it is replaced with “1.”
Data	
Data length	NRZ: 2 to 268 435 456 bits, in steps of 1 bit PAM4: 2 to 268 435 456 symbols, in steps of 1 symbol
Coding	NRZ, PAM4
NRZ	Normal, Invert
PAM4 Gray Coding	ON, OFF
PAM4 Precoding (1/(1 + D) mod 4)*	ON, OFF
PAM4 Standard Pattern	Standard-compliant PAM4-mode patterns
CEI	QPRBS13-CEI, QPRBS31-CEI
IEEE	IEEE802.3bs/cd: PRBS13Q, PRBS31Q, SSPRQ, Square Wave IEEE802.3bj: QPRBS13, JP03A, JP03B, Transmitter Linearity
InfiniBand	PRBS13Q (InfiniBand), PRBS23Q, PRBS31Q (InfiniBand)
Fibre Channel	PRBS31Q (Fibre Channel)
NRZ Standard Pattern	Standard-compliant NRZ-mode pattern
CEI	SSPR

*: (1/(1+D) mod 4) is a generator polynomial defined in the IEEE802.3.

Table 1.3.3.2-8 Pattern Sequence

Item	Specifications
Sequence	Repeat, Burst
Repeat	Continuous Pattern
Burst	This is available only when **Coding** is set to **NRZ**.
Source	Internal, External-Enable (AUX Input), External-Trigger (AUX Input)
Delay	Internal: 0 to 2 147 483 640 bits, in steps of 8 bits External-Trigger, External-Enable: 0 to 2 147 483 520 bits, in steps of 8 bits Adjust Method: Auto, Manual
Enable Period	Internal: 12 800 to 2 147 482 624 bits, in steps of 256 bits External-Trigger: 12 800 to 2 147 483 136 bits, in steps of 256 bits
Burst Cycle	25 600 to 2 147 483 648 bits, in steps of 1 024 bits

Table 1.3.3.2-9 Measurement

Item	Specifications
Counter	Error Rate (ER) Total: 0.000 1E–18 to 1.000 0E00 Error Count (EC) Total: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Error Interval: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 %Error Free Interval: 0.000 0 to 100.000 0 Error Rate (ER) Insertion (INS): 0.000 1E–18 to 1.000 0E00 Error Count (EC) Insertion (INS): 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Error Rate (ER) Omission (OMI): 0.000 1E–18 to 1.000 0E00 Error Count (EC) Omission (OMI): 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Frequency: 2 400.000 to 58 200.000 MHz Frequency measurement accuracy: ±1 ppm ±1 kHz* Clock Count: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Sync Loss Interval: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Clock Loss Interval: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Expressions enclosed in parentheses are abbreviations.
	The following are available only for PAM4 (Diagnostics Mode ON) measurement. MSB Error Rate (ER) Total: 0.000 1E–18 to 1.000 0E00 MSB Error Count (EC) Total: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 MSB Error Interval: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 MSB %Error Free Interval: 0.000 0 to 100.000 0 MSB Error Rate (ER) Insertion (INS): 0.000 1E–18 to 1.000 0E00 MSB Error Count (EC) Insertion (INS): 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 MSB Error Rate (ER) Omission (OMI): 0.000 1E–18 to 1.000 0E00 MSB Error Count (EC) Omission (OMI): 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 LSB Error Rate (ER) Total: 0.000 1E–18 to 1.000 0E00 LSB Error Count (EC) Total: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 LSB Error Interval: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 LSB %Error Free Interval: 0.000 0 to 100.000 0 LSB Error Rate (ER) Insertion (INS): 0.000 1E–18 to 1.000 0E00 LSB Error Count (EC) Insertion (INS): 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 LSB Error Rate (ER) Omission (OMI): 0.000 1E–18 to 1.000 0E00 LSB Error Count (EC) Omission (OMI): 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Expressions enclosed in parentheses are abbreviations.

*: With a gating system and with MP1900A's reference clock (10 MHz) calibrated

Table 1.3.3.2-9 Measurement (Cont'd)

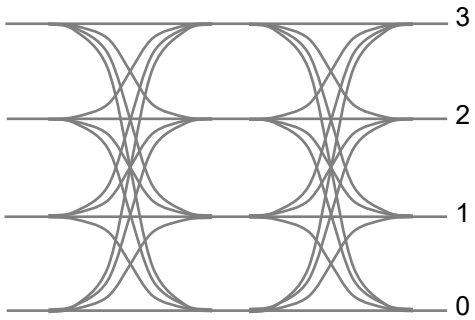
Item	Specifications
Counter (Cont'd)	The following are available only with the Option x41 SER Measurement. The following are available only for PAM4 (Diagnostics Mode OFF) measurement.  Symbol Error Rate (SER): 0.000 1E–18 to 1.000 0E00 Symbol Error Count (SEC): 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Symbol Error Interval: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Symbol %Error Free Interval: 0.000 0 to 100.000 0 Level 0 → 3 EC: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 0 → 2 EC: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 0 → 1 EC: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 0 → 3 ER: 0.000 1E–18 to 1.000 0E00 Level 0 → 2 ER: 0.000 1E–18 to 1.000 0E00 Level 0 → 1 ER: 0.000 1E–18 to 1.000 0E00 Level 0 EC Total: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 0 ER Total: 0.000 1E–18 to 1.000 0E00 Level 1 → 3 EC: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 1 → 2 EC: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 1 → 0 EC: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 1 → 3 ER: 0.000 1E–18 to 1.000 0E00 Level 1 → 2 ER: 0.000 1E–18 to 1.000 0E00 Level 1 → 0 ER: 0.000 1E–18 to 1.000 0E00 Level 1 EC Total: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 1 ER Total: 0.000 1E–18 to 1.000 0E00

Table 1.3.3.2-9 Measurement (Cont'd)

Item	Specifications	
Counter (Cont'd)	Level 2 → 3 EC:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Level 2 → 1 EC:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Level 2 → 0 EC:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Level 2 → 3 ER:	0.000 1E–18 to 1.000 0E00
	Level 2 → 1 ER:	0.000 1E–18 to 1.000 0E00
	Level 2 → 0 ER:	0.000 1E–18 to 1.000 0E00
	Level 2 EC Total:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Level 2 ER Total:	0.0001E–18 to 1.000 0E00
	Level 3 → 2 EC:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Level 3 → 1 EC:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Level 3 → 0 EC:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Level 3 → 2 ER:	0.000 1E–18 to 1.000 0E00
	Level 3 → 1 ER:	0.000 1E–18 to 1.000 0E00
	Level 3 → 0 ER:	0.000 1E–18 to 1.000 0E00
	Level 3 EC Total:	0 to 9 999 999, 1.000 0E07 to 9.999 9E17
	Level 3 ER Total:	0.000 1E–18 to 1.000 0E00
	Expressions enclosed in parentheses are abbreviations.	
Gating	Time, Clock Count, Error Count	
Gating Unit	Time:	1 second to 99 days 23 hours 59 minute 59 seconds
	Clock Count:	>E+4 to >E+16
	Error Count:	>E+4 to >E+16
Cycle	Single, Repeat, Untimed	
Current	On, Off can be set.	
	Calculation:	Progressive, Immediate
	Interval:	100 ms, 200 ms
Auto Sync	On, Off can be set.	
	Synchronization threshold:	INT, E–2 to E–8
Sync Control	PRBS:	Automatic Synchronization
	Data:	Frame On
Frame Length	NRZ:	4 to 64 bits, in steps of 4 bits
	PAM4:	4 to 64 symbols, in steps of 4 symbols
Frame Mask	Available	
Frame Position	NRZ:	1 to (Pattern Length – Frame Length +1) bits, in steps of 1 bit
	PAM4:	1 to (Pattern Length – Frame Length +1) symbols, in steps of 1 symbol
Error/Alarm Conditions		
Error Detection	NRZ:	Insertion/Omission, Transition/Non Transition
	PAM4:	Not available
EI/EFI Interval	1 ms, 10 ms, 100 ms, 1 s	

Table 1.3.3.2-10 Error Analysis

Item	Specifications
Block Window Setting resolution	Excludes the specified data pattern from measurement. Pattern length (bits) — Step (bits) 2 to 2 097 152 — 1 2 097 153 to 4 194 304 — 2 4 194 305 to 8 388 608 — 4 8 388 609 to 16 777 216 — 8 16 777 217 to 33 554 432 — 16 33 554 433 to 67 108 864 — 32 67 108 865 to 134 217 728 — 64 134 217 729 to 268 435 456 — 128
Bit Window	Excludes any channels among internal 32 channels from measurement. (Available only in NRZ mode.)
External Mask	H: Measurement L: Mask

Table 1.3.3.2-11 Auto Measurement

Item	Specifications
Auto Adjust	NRZ: Vth direction only (Phase direction not supported.)*1 PAM4: MSB Vth direction only (Phase direction not supported.)*1, *2
Auto Search	NRZ: Available*1 PAM4 (LSB/MSB Diagnostics OFF/ON): Available*1, *2

*1: PRBS Pattern, Mark Ratio 1/2

*2: Each of amplitudes shall be equal.

Table 1.3.3.2-12 Variable Clock Delay

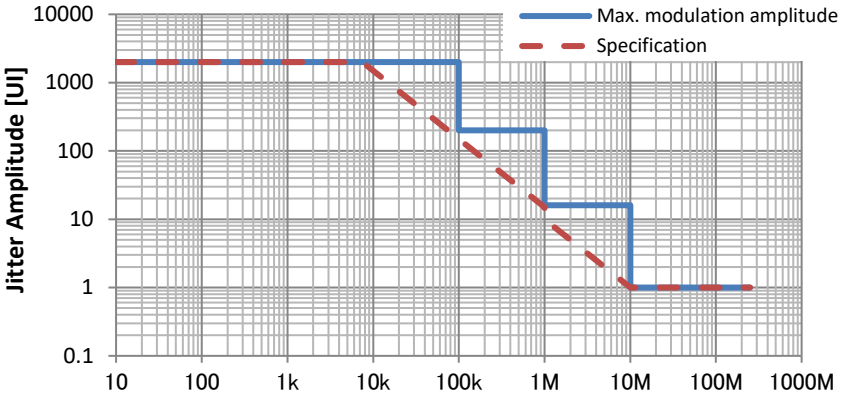
Item	Specifications
Phase variable range	–1000 to +1000 mUI, in steps of 2 mUI
Accuracy	±50 mUIp-p*1, *2
mUI – ps switching	Available (internally converted into ps)
Calibration	Available (when jitter modulation is off)
Calibration indicator	This indicator is on when Calibration is required due to: • Change in 1/1Clock frequency by ±250 kHz. • Change in the ambient temperature by ±5°C.

*1: Measure using an oscilloscope with residual jitter of less than 200 fs (RMS).

*2: Typical value

Table 1.3.3.2-13 Jitter Tolerance

Item	Specifications
Jitter tolerance	For NRZ output Bit rate: 32.1 Gbit/s Pattern: PRBS2^{31}–1 With MU181500B, SSC with frequency of 33 kHz and deviation of 5300 ppm can be applied simultaneously with RJ with amplitude of 0.3 UI. These specifications are defined assuming the following conditions: Loopback connection to the MU196020A, at a constant temperature between 20 and 30 °C. When RJ+BUJ is bigger than 0.5 UIp-p or SJ + RJ + BUJ is bigger than the standard value + 0.3 UIp-p, “Overload” is displayed on the MU181500B screen.



Modulation frequency [Hz]	Max. modulation amplitude [UIp-p]	Specification [UIp-p]
10	2 000	2 000
7 500	2 000	2 000
100 000	2 000	150
1 000 000	200	15
10 000 000	16	1
250 000 000	1	1

Table 1.3.3.2-14 Clock Recovery

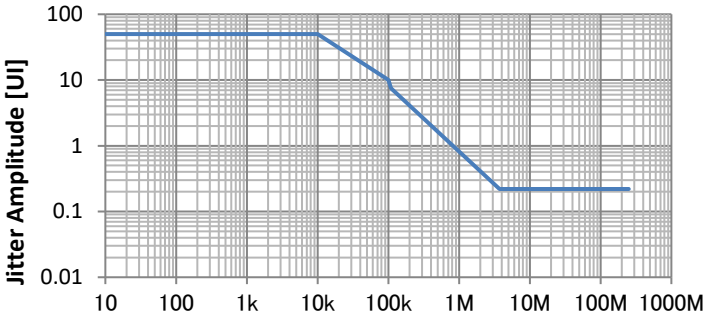
<table>
<tr><th>Item</th><th>Specifications*1</th></tr>
<tr><td>Operating bit rate</td><td>NRZ: 25.5 to 32.1 Gbit/s
PAM4: 25.5 to 32.1 Gbaud</td></tr>
<tr><td>Setting range</td><td>25.500 000 to 32.100 000 Gbaud, in steps of 0.000 001 Gbaud</td></tr>
<tr><td>Supported standard and baud rate</td><td>For NRZ mode
<table>
<tr><th>Standard</th><th>Bit Rate [Gbit/s]</th><th>Remarks</th></tr>
<tr><td>100G ULH</td><td>32.100 000</td><td></td></tr>
<tr><td>32G FC</td><td>28.050 000</td><td></td></tr>
<tr><td>CEI-28G</td><td>28.000 000</td><td></td></tr>
<tr><td>100G OTU4</td><td>27.952 496</td><td></td></tr>
<tr><td>100GbE(25.78 × 4)</td><td>25.781 250</td><td></td></tr>
<tr><td>InfiniBand EDR</td><td>25.781 250</td><td></td></tr>
</table>
For PAM4 mode
<table>
<tr><th>Standard</th><th>Baud Rate [Gbaud]</th><th>Remarks</th></tr>
<tr><td>64G FC</td><td>28.900 000</td><td></td></tr>
<tr><td>CEI-56G</td><td>28.000 000</td><td></td></tr>
<tr><td>200GbE(26.6 × 4)</td><td>26.562 500</td><td></td></tr>
<tr><td>InfiniBand HDR</td><td>26.562 500</td><td></td></tr>
</table></td></tr>
<tr><td>Operating bit rate tracking</td><td>Tracks the operating bit rate of the PPG selected from the PPGs installed in the same MP1900A.</td></tr>
<tr><td>Maximum number of consecutive zeros*2</td><td>72 bits (Zero Substitution 2^{15})</td></tr>
<tr><td>Lock range*2</td><td>±100 ppm</td></tr>
<tr><td>Target loop band*3</td><td>Baud rate / 1667, Baud rate / 2578, Baud rate / 6640, Jitter Tolerance</td></tr>
</table>

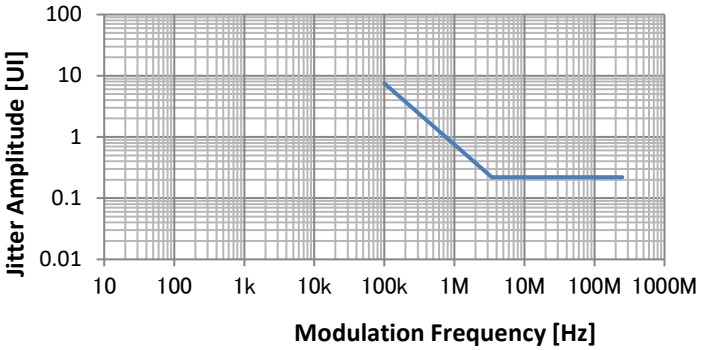
*1: With Option x22, these are specified with the conditions of PRBS Pattern and Mark Ratio 1/2 (in PAM4 mode, MSB Mark Ratio 1/2) unless otherwise specified.

*2: The target loop band is specified by 1/1667, 1/2578, 1/6640.

*3: The SSPRQ pattern supports Baud rate / 6640 only. When set to Jitter Tolerance, Baud rate / 1667 or higher.

Table 1.3.3.2-14 Clock Recovery (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Jitter Tolerance
Clock Recovery*4,*5</td><td>
At the bit rate of 28.05 Gbaud, conforming to Jitter Tolerance Mask defined by the "32G FC standard". The following masks are taken as typical values:


<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Tolerance Mask (UIp-p)</th></tr>
<tr><td>10</td><td>50</td></tr>
<tr><td>10 000</td><td>50</td></tr>
<tr><td>100 000</td><td>10</td></tr>
<tr><td>108 805</td><td>7.5</td></tr>
<tr><td>3 709 271</td><td>0.22</td></tr>
<tr><td>250 000 000</td><td>0.22</td></tr>
</table>
At the bit rate of 25.78125 Gbaud, conforming to Jitter Tolerance Mask defined by the "100GbE (25.78G × 4) standard". The following masks are taken as typical values:


<table>
<tr><th>Modulation Frequency (Hz)</th><th>Jitter Tolerance Mask (UIp-p)</th></tr>
<tr><td>100 000</td><td>7.5</td></tr>
<tr><td>3 409 256</td><td>0.22</td></tr>
<tr><td>250 000 000</td><td>0.22</td></tr>
</table>
</td></tr>
</table>

*4: Defined assuming the following conditions:

- Loop-back connection to MU196020A
- NRZ input
- Test Pattern (Length): PRBS2^{31}–1
- Data input amplitude: 0.1 Vp-p

*5: Typical value, specified at a constant temperature between 20 and 30 °C.

Table 1.3.3.2-15 General

Item	Specifications
Dimensions	21 mm (H), 234 mm (W), 175 mm (D), Excluding protrusions
Mass	2.5 kg max.
Operating temperature	15 to 30 °C MP1900A's ambient temperature. MU196040A shall operate when installed.
Storage temperature	–20 to 60 °C MU196040A installed to MP1900A shall comply with MIL-T-28800E Class 5.

1.3.3.3 Specifications for MU196040B

Table 1.3.3.3-1 Operating Baud Rate

Item	Specifications
Operating Baud Rate	With Option 001 PAM4 input: 2.4 to 32.1 Gbaud NRZ input: 2.4 to 32.1 Gbit/s With Option 002 or y12 PAM4 input: 2.4 to 58.2 Gbaud* NRZ input: 2.4 to 64.2 Gbit/s* With Option 005, 115, or 125 PAM4 input: 2.4 to 64.2 Gbaud* NRZ input: 2.4 to 64.2 Gbit/s*

*: Available only when the BERT for PCIe1-7, BERT for PCIe1-6 Forced Link, or BERT for PCIe1-5 and PCIe6 Base application is selected:

PAM4 input: 2.4 to 32.1 Gbaud

NRZ input: 2.4 to 32.1 Gbit/s

When the "BERT for PCIe1-7" application is selected:

PAM4 input: 2.4 to 64.2 Gbaud

NRZ input: 2.4 to 64.2 Gbit/s

Table 1.3.3.3-2 System Clock

Item	Specifications
System Clock	External, Recovered Clock (with Option x21, x22, x23, or y24) External: Clock input from the Ext Clock Input connector PAM4: 2.4 to 32.1 Gbaud, 32.1 to 58.2 Gbaud, 64.2 Gbaud (with Option 005, 115, or 125), Auto NRZ: 2.4 to 32.1 Gbit/s, 32.1 to 64.2 Gbit/s, Auto Recovered Clock: Clock recovered from the data input from the Data Input connector

Table 1.3.3.3-3 Data Input

Item	Specifications
Number of inputs	2 (Data, XData) (Differential)
Input Condition	Single-Ended, Differential 50 Ohm, Differential 100 Ohm When set to Differential 50 Ohm or Differential 100 Ohm: Independent, Tracking, Alternate*1 When set to Alternate: Data-XData, XData-Data*2 When set to Single-Ended: Data, XData*3
Signal Type LSB/MSB Diagnostics	NRZ, PAM4 When set to PAM4, the PAM4 mode can be switched between as follows: Diagnostics Mode OFF: Treats signals as symbols by receiving LSB and MSB while synchronizing them with each other. Diagnostics Mode ON: Asynchronously receives LSB and MSB.
Amplitude	NRZ: The range in which the Auto Adjust function and the Auto Search function operate. 0.05 to 1.0 Vp-p*4, *5 0.1 to 1.0 Vp-p*4, *6 PAM4: The range in which the Auto Search PAM4 Fine function operates. 0.3 to 1.0 Vp-p*7, *8 0.4 to 1.0 Vp-p*7, *9
Threshold	NRZ, PAM4 Middle Eye Threshold: –3.5 to +3.3 V, in steps of 1 mV*2, *10 PAM4 Upper Eye Threshold: –3.9 to +3.7 V, in steps of 1 mV*11 PAM4 Lower Eye Threshold: –3.9 to +3.7 V, in steps of 1 mV*11

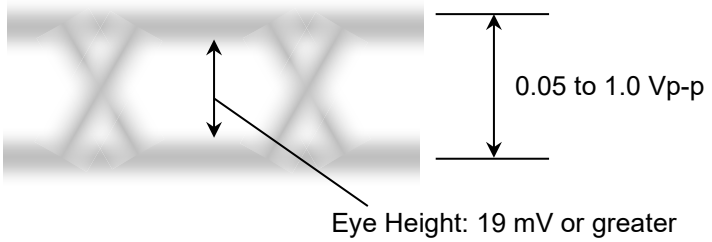
*1: Tracking is available only for NRZ.

*2: The absolute value of the difference between Data and XData Threshold values shall be 1.5 V or less.

*3: PAM4 Upper Eye and Lower Eye can be set by relative values to Middle Eye in the range of –0.4 V to +0.4 V.

*4: Single-Ended, Differential, Mark Ratio1/2, the Eye Height shall meet the specification.

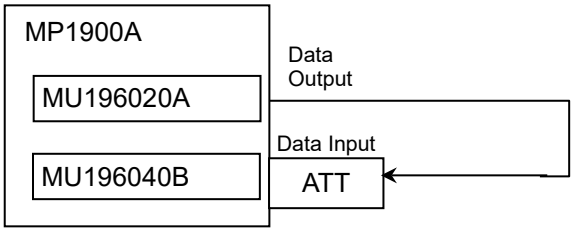
Example of waveform input to MU196040B when bit rate is 32.1 Gbit/s



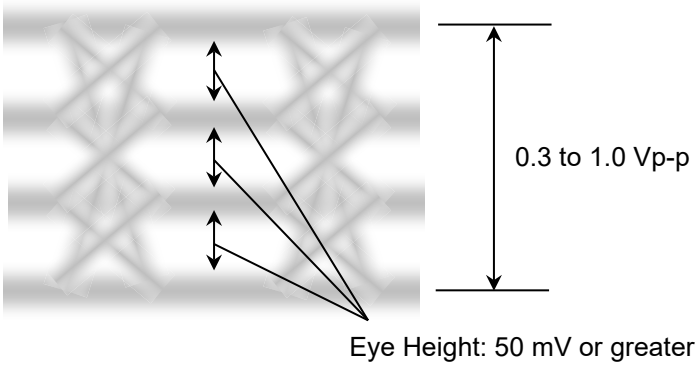
*5: Bit rate ≤32.1 Gbit/s

*6: Bit rate >32.1 Gbit/s

*7: 0/3 Level, PRBS31, Mark Ratio1/2, with connected to the MU196020A using an attenuator, with Emphasis adjusted so that the Eye Height meets the specification



Example of waveform input to MU196040B when baud rate is 32.1 Gbaud



*8: Single-Ended, Differential, Baud rate ≤32.1 Gbaud

*9: Differential, Baud rate >32.1 Gbaud

*10: Data and XData can be set independently.

*11: Data and XData cannot be set independently, and can be set in the range of ±0.4 V from Middle Eye Threshold.

Table 1.3.3.3-3 Data Input (Cont'd)

Item	Specifications
Sensitivity	Single-Ended , Mark Ratio1/2, PRBS31, when connecting directly to the MU196020A using J1789A and an attenuator, Emphasis ON, unused connectors on the MU196020A and MU196040B are terminated, At a constant temperature between 20 and 30 °C
Eye Amplitude	NRZ Typ. 25 mVp-p, ≤ 50 mVp-p*12 (26.5625 Gbit/s, 32.1 Gbit/s) Typ. 31 mVp-p, ≤ 55 mVp-p*15 (53.125 Gbit/s) Typ. 43 mVp-p, ≤ 60 mVp-p*15 (64.2 Gbit/s)
Eye Height	NRZ Typ. 19 mV*12 (26.5625 Gbit/s, 32.1 Gbit/s) Typ. 21 mV*15 (53.125 Gbit/s) Typ. 32 mV*15 (64.2 Gbit/s) PAM4 0/1 1/2 2/3 Level, PRBS31, when using External Clock Typ. 23 mV, ≤ 50 mV*12 (26.5625 Gbaud, 32.1 Gbaud) Typ. 36 mV, ≤ 60 mV*15 (53.125 Gbaud) Typ. 49 mV, ≤ 70 mV*13 (58.2 Gbaud) Typ. 49 mV, ≤ 70 mV*16 (64.2 Gbaud) Note that 53.125 Gbaud, 58.2 Gbaud, and 64.2 Gbaud are defined by the Eye Height value that results in a differential waveform having BER of 1E-06 by changing the test pattern to QPRBS13-CEI after setting the test pattern to PRBS31 and setting the amplitude value.
Phase Margin	Differential, Mark Ratio 1/2, PRBS31, when inputting 0.5 Vp-p, when connecting directly to the MU196020A using J1789A and an attenuator. At a constant temperature between 20 and 30 °C, when using External Clock NRZ*14 Typ. 25.8 ps*12 (26.5625 Gbit/s) Typ. 18.0 ps*12 (32.1 Gbit/s) Typ. 10.5 ps*15 (53.125 Gbit/s) Typ. 8.7 ps*15 (64.2 Gbit/s) PAM4 Typ. 5.3 ps*12 (26.5625 Gbaud) Typ. 4.5 ps*12 (32.1 Gbaud) Typ. 4.1 ps*14, *15 (53.125 Gbaud) Typ. 2.5 ps*14, *15 (58.2 Gbaud) Typ. 0.7 ps*16 (64.2 Gbaud)

*12: When Option 001, 002, 005, y12, 115, or 125 is installed.

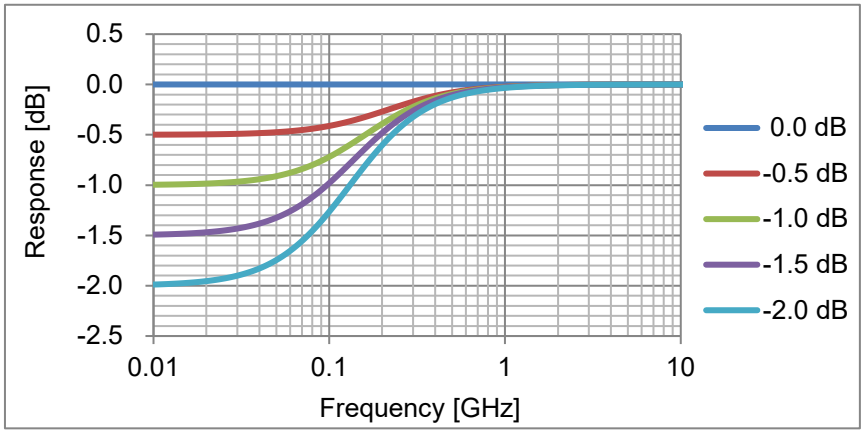
*13: With Option 002 or y12

*14: Value including RJ equivalent to BER 1E–12 of input signal

*15: When Option 002, 005, y12, 115, or 125 is installed.

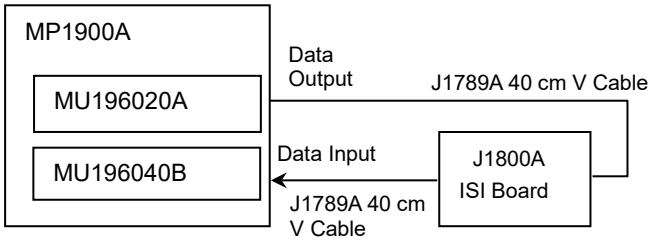
*16: With Option 005, 115, or 125

Table 1.3.3.3-3 Data Input (Cont'd)

Item	Specifications
Stressed Margin	
Stressed Eye Height	PAM4 0/1 1/2 2/3 Level, QPRBS13-CEI, Eye Height where BER is 1E–06, when using External Clock ≥ 32 mV*17, *18 ≥ 37 mV*19, *20
Stressed Eye Width	PAM4 0/1 1/2 2/3 Level, QPRBS13-CEI, Eye Width where BER is 1E–06, when using External Clock ≥ 7.53 ps*17, *18 ≥ 3.76 ps*19, *20
Termination	50 Ω, GND, Variable
Termination Voltage	When set to Variable: –2.5 to +3.5 V, in steps of 10 mV
Connector	V connector (f.)
Decision Feedback Equalizer	With a built-in Decision Feedback Equalizer (DFE)*19
Tap	1
Coefficient	
Setting Range	0 to 30, in steps of 1
Loss Compensation	Nom. 1.4 dB*22
Low Frequency Equalizer	With a built-in Low Frequency Equalizer*21
Gain	
Setting Range	–2.0 to 0 dB, in steps of 0.5 dB
Accuracy	Typ. ±1.0 dB
Ideal Frequency Response	

*17: 26.5625 Gbaud, when Option 001, 002, 005, y12, 115, or 125 is installed and Option x11 is installed.

*18: 26.5625 Gbaud, Differential, Mark Ratio1/2, when J1789A is used to connect J1800A (1 pc) and MU196020A



At a constant temperature between 20 and 30 °C, measure with a 70-GHz bandwidth sampling oscilloscope with residual jitter of less than 200 fs (RMS).

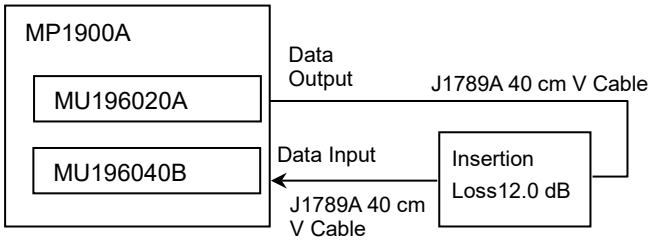
Adjust De-Emphasis (2 Pre Cursors and 1 Post Cursor) of MU196020A so that the product of Eye Height (1E–06) and Eye Width (1E–06) can be maximized in the differential waveform.

Calculate the 4th-order Bessel Filter (Cutoff Frequency 40 GHz) + CTLE (+1 dB Peaking at 14 GHz) and calibrate it to a PAM4 waveform with Eye Amplitude of 0.88 Vp-p (Diff) or less and Eye Linearity R_{LM} 0.85 or more.

Activate the DFE and Low Frequency Equalizer in the MU196040B and perform adjustment.

*19: Nominal value at a BER of 1E-8 for operation at 53.125 Gbaud when the configuration includes any of Options 002, 005, y12, 115, 125, and x11.

*20: Condition applicable when operating at 53.125 Gbaud with a configuration that includes any of Options 002, 005, y12, 115, 125, and x11, and when a connection setup using a measurement system with differential signaling, a mark ratio of 1/2, an insertion loss of 12.0 dB, and MU196020A is used.



At a constant temperature between 20 and 30 °C, measure with a 70-GHz bandwidth sampling oscilloscope with residual jitter of less than 200 fs (RMS).

Adjust De-Emphasis (2 Pre Cursors and 1 Post Cursor) of MU196020A so that the product of Eye Height (1E–06) and Eye Width (1E–06) can be maximized in the differential waveform.

Calculate the 4th-order Bessel Filter (Cutoff Frequency 43 GHz) + CTLE (+1 dB Peaking at 28 GHz) and calibrate it to a PAM4

waveform with Eye Amplitude of 0.88 Vp-p (Diff) or less and Eye Linearity R_{LM} 0.85 or more.

Activate the DFE and Low Frequency Equalizer in the MU196040B and perform adjustment.

*21: With Option x11

*22: 53.125 Gbaud, Calculated from the following three:

- The BER result obtained when DFE is OFF under the condition of *20.
- The BER result obtained when DFE is OFF under the condition of *20 and 1.8 dB additional loss.
- The best BER result obtained when DFE is ON under the condition of *20 and 1.8 dB additional loss.

Table 1.3.3.3-4 Clock Input

Item	Specifications
External Clock Input	Operation Baud Rate = Clock Input Frequency × 2
Number of inputs	1 (Single-Ended)
Frequency range	1.2 to 32.1 GHz
Amplitude	0.3 to 1.0 Vp-p (–6.5 to +4.0 dBm) (Input Frequency ≤ 16.05 GHz) 0.4 to 1.0 Vp-p (–3.9 to +4.0 dBm) (Input Frequency > 16.05 GHz)
Termination	50 Ω, AC Coupling
Connector	K connector (f.)

Table 1.3.3.3-5 AUX Input

Item	Specifications
Number of inputs	1 (Single-Ended)
Variation	External Mask, Burst, Capture External Trigger
Minimum pulse width	1/256 of Data rate
Input level	• 0/–1 V (H: –0.25 to 0.05 V, L: –1.1 to –0.8 V) • 0/–0.5 V (H: –0.05 to 0.05 V, L: –0.55 to –0.45 V) • Vth 0 V (Input amplitude 0.5 to 1.0 Vp-p) Select one of the above.
Termination	50 Ω, GND
Connector	SMA connector (f.)

Table 1.3.3.3-6 AUX Output

Item	Specifications
Number of outputs	2 (Differential)
Variation*	1/n Clock (n = 8, 12, 16, 20…1020, 1024), Pattern Sync, Sync Gain, Error Output, Capture Trigger
Pattern Sync PRBS, PRGM	 Position: 1 to {(Least common multiple of Pattern Length' and 256) – 263}, 8 steps (with Option 001) Pattern Length' shall be the value obtained by multiplying Pattern Length setting until it becomes 1024 or more if it is 1023 or less.
Output level	0/–0.6 V (H: –0.25 to 0.05V, L: –0.80 to –0.45 V)
Termination	50 Ω, GND
Connector	SMA connector (f.)

*: Pattern Sync cannot be selected when an HSSB Data pattern is selected.

Table 1.3.3.3-7 Pattern Detection

Item	Specifications
PRBS Pattern length Mark ratio PRBS generator polynomial PRBS Inversion PRBS 1st Bit	 2^n–1 (n = 7, 9, 10, 11, 13, 15, 20, 23, 31) 1/2, 1/2inv n=7: $1 + X^6 + X^7$ n=9: $1 + X^5 + X^9$ n=10: $1 + X^7 + X^{10}$ n=11: $1 + X^9 + X^{11}$ n=13: $1 + X + X^2 + X^{12} + X^{13}$ n=15: $1 + X^{14} + X^{15}$ n=20: $1 + X^3 + X^{20}$ n=23: $1 + X^{18} + X^{23}$ n=31: $1 + X^{28} + X^{31}$ This is available in PAM4 mode only. Logically inverted PRBS can be set independently for MSB and LSB. MSB or LSB can be selected to set the 1st bit of the PRBS Generator.
Zero-Substitution Additional Bit Pattern length Start position Zero-Length	This is available in NRZ mode only. 0 bit, 1 bit 2^n or 2^n–1 (n = 7, 9, 10, 11, 15, 20, 23) Substitutes the bit coming after the maximum "0" successive bits. 1 to (Pattern Length – 1) bits If the bit coming after Zero-substitution is "0," then it is replaced with "1."
Data Data length	 NRZ: 2 to 268 435 456 bits, in steps of 1 bit PAM4: 2 to 268 435 456 symbols, in steps of 1 symbol

Table 1.3.3.3-7 Pattern Detection (Cont'd)

Item	Specifications
Coding	NRZ, PAM4
NRZ	Normal, Invert
PAM4 Gray Coding	ON, OFF*3
PAM4 Precoding (1/(1 + D) mod 4)*1	ON, OFF*3
PAM4 Inverse Gray Coder	ON, OFF*4
PAM4 Pre Code Remover*2	ON, OFF*4
Input Signal Decoder	ON, OFF Fixed to OFF when PAM4 Standard Pattern is one of the following specific patterns: PRBS13Q, QPRBS13-CEI, PRBS13Q(InfiniBand), PRBS23Q, PRBS31Q, QPRBS-CEI, PRBS31Q(InfiniBand), PRBS31Q(Fiber Channel), SSPRQ, QPRBS13, JP03A, JP03B, Transmitter Linearity, Square Wave
Delay Symbol	ON, OFF
SKP	No SKP, SKPx1, SKPx2
Preset	P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10
SRIS	ON, OFF
EIEOS	ON
SKP OS Filter	ON, OFF

*1: (1/(1+D) mod 4) is a generator polynomial defined in the IEEE802.3.

*2: Uses the generator polynomial *(1+D) mod 4* defined in the IEEE 802.3.

*3: Available only when **Input Signal Decoder** is set to **OFF**. Not available when it is set to **ON**.

*4: Available only when **Input Signal Decoder** is set to **ON**. Not available when it is set to **OFF**.

Table 1.3.3.3-7 Pattern Detection (Cont'd)

Item	Specifications
PAM4 Standard Pattern	Standard-compliant PAM4-mode patterns
CEI	QPRBS13-CEI, QPRBS31-CEI
IEEE	IEEE802.3bs/cd: PRBS13Q, PRBS31Q, SSPRQ, Square Wave IEEE802.3bj: QPRBS13, JP03A, JP03B, Transmitter Linearity
InfiniBand	PRBS13Q (InfiniBand), PRBS23Q, PRBS31Q (InfiniBand)
Fibre Channel	PRBS31Q (Fibre Channel)
RS-FEC	RS-FEC Scrambled Idle 50G 1Lane*5, RS FEC Scrambled Idle 100G 1Lane*5, RS FEC-Int Scrambled Idle 100G 1Lane*5, RS FEC Scrambled Idle 100G 2Lanes*5, RS-FEC Scrambled Idle 200G 2Lanes*5, RS-FEC Scrambled Idle 200G 4Lanes*5, RS-FEC Scrambled Idle 400G 4Lanes*5, RS-FEC Scrambled Idle 400G 8Lanes*5
PCIe	CP in 1b/1b Encoding for PCIe6 MCP in 1b/1b Encoding for PCIe6 CP in 1b/1b Encoding for PCIe7*7 MCP in 1b/1b Encoding for PCIe7*7 NOP Flit Layout in a x1 Link*6 NOP Flit Layout in a x2 Link*6 NOP Flit Layout in a x4 Link*6 NOP Flit Layout in a x8 Link*6 NOP Flit Layout in a x16 Link*6

*5: With Option w42

*6: With Option w43

*7: When Option 005, 115, or 125 is installed.

Table 1.3.3.3-7 Pattern Detection (Cont'd)

Item	Specifications
NRZ Standard Pattern	Standard-compliant NRZ-mode pattern
CEI	SSPR
RS-FEC	RS-FEC Scrambled Idle 25G 1Lane*5, RS-FEC Scrambled Idle 50G 2Lanes RS(544,514)*5, RS-FEC Scrambled Idle 100G 4Lanes*5, RS-FEC Scrambled Idle 100G 4Lanes RS(544,514)*5
PCIe	CP in 8b/10b Encoding for PCIe1 MCP in 8b/10b Encoding for PCIe1 CP in 8b/10b Encoding for PCIe2 MCP in 8b/10b Encoding for PCIe2 CP in 128b/130b Encoding for PCIe3 MCP in 128b/130b Encoding for PCIe3 CP in 128b/130b Encoding for PCIe4 MCP in 128b/130b Encoding for PCIe4 CP in 128b/130b Encoding for PCIe5 MCP in 128b/130b Encoding for PCIe5

Table 1.3.3.3-7 Pattern Detection (Cont'd)

Item	Specifications
HSSB Data	Compatible with MX190000A version 10.05.00 or later.*8 When the BERT for PCIe1-6 Forced Link application is executed.
Specification	NRZ: PCIe1, PCIe2, PCIe3/CXL1-2, PCIe4/CXL1-2, PCIe5/CXL1-2 PAM4: PCIe6/CXL3
Pattern Length	PCIe1, PCIe2: 32 to 1024 bits, in steps of 8 bits PCIe3/CXL1-2, PCIe4/CXL1-2, PCIe5/CXL1-2: 128 to 1024 bits, in steps of 128 bits PCIe6/CXL3: 128 to 2048 bits, in steps of 128 bits
Coding	PCIe1, PCIe2: 8b10b PCIe3/CXL1-2, PCIe4/CXL1-2, PCIe5/CXL1-2: 128b130b PCIe6/CXL3: 1b1b
EIEOSQ	
EIEOSQ Insertion	ON, OFF*9
EIEOSQ Interval	1 to 65536 pattern repeats, in steps of 1
EIEOS Count	Sets the number of EIEOS in the EIEOSQ. 2.5G, 5.0G, 8.0G, 16.0G: 1 32.0G: 2 64.0G: 1, 4
Coding	
Scrambler Seed	PCIe1, PCIe2: FFFF PCIe3/CXL1-2, PCIe4/CXL1-2, PCIe5/CXL1-2, PCIe6/CXL3: Lane0, Lane1, Lane2, Lane3, Lane4, Lane5, Lane6, Lane7
Scrambler Mode	PCIe1, PCIe2, PCIe3/CXL1-2, PCIe4/CXL1-2, PCIe5/CXL1-2: NRZ PCIe6/CXL3: NRZ, PAM4
Pre Coder	PCIe1, PCIe2, PCIe3/CXL1-2, PCIe4/CXL1-2: OFF PCIe5/CXL1-2, PCIe6/CXL3: ON, OFF
Gray Coder	PCIe1, PCIe2, PCIe3/CXL1-2, PCIe4/CXL1-2, PCIe5/CXL1-2: OFF PCIe6/CXL3: ON, OFF
Input Signal Decoder	OFF
128b130b Encoder*10	Inserts the Sync Header for CP and MCP patterns in 128b130b encoding. PCIe1, PCIe2, PCIe6/CXL3: OFF PCIe3/CXL1-2, PCIe4/CXL1-2, PCIe5/CXL1-2: ON, OFF

*8: With Option z51

*9: Fixed to ON when PCIe3, PCIe4, PCIe5, or PCIe6 is selected.

*10: Available in MX190000A version 10.08.00 or later.

Table 1.3.3.3-7 Pattern Detection (Cont'd)

Item	Specifications
PCIe Encoding Pattern	
8b10b Pattern Editor	
Notation	Symbol(8b10b), Bin, Hex
Scrambler Enable	Scrambles the selected symbols. ON, OFF
Scrambler Reset	Resets the scrambler seed value for the selected symbols. ON, OFF
Code	K-code, D-code
K code	K28.0, K28.1, K28.2, K28.3, K28.4, K28.5, K28.6, K28.7, K23.7, K27.7, K29.7, K30.7
D code	D0.0 to D31.7
MSB/LSB First	MSB First, LSB First
128b130b Pattern Editor	
Notation	Bin, Hex
Scrambler Enable	Scrambles the selected symbols. ON, OFF
Scrambler Reset	Resets the scrambler seed value for the selected symbols. ON, OFF
DC Balance	Adds DC balance to Symbols 14 and 15. ON, OFF
Sync Header	Defines a 2-bit Sync Header.
MSB/LSB First	MSB First, LSB First
1b1b Pattern Editor	
Notation	Symbol (PAM4), Bin, Hex
Scrambler Enable	Scrambles the selected symbols. ON, OFF
Scrambler Reset	Resets the scrambler seed value for the selected symbols. ON, OFF
DC Balance	Adds DC balance to Symbols 7 and 15. ON, OFF
MSB/LSB First	MSB First, LSB First

Table 1.3.3.3-8 Pattern Sequence

Item	Specifications
Sequence	Repeat, Burst
Repeat	Continuous Pattern
Burst	This is available only when **Coding** is set to **NRZ**.
Source	Internal, External-Enable (AUX Input), External-Trigger (AUX Input)
Delay	Internal: 0 to 2 147 483 640 bits, in steps of 8 bits External-Trigger, External-Enable: 0 to 2 147 483 520 bits, in steps of 8 bits Adjust Method: Auto, Manual
Enable Period	Internal: 12 800 to 2 147 482 624 bits, in steps of 256 bits External-Trigger: 12 800 to 2 147 483 136 bits, in steps of 256 bits
Burst Cycle	25 600 to 2 147 483 648 bits, in steps of 1 024 bits

Table 1.3.3.3-9 Measurement

Item	Specifications
Counter	Error Rate (ER) Total: 0.000 1E–18 to 1.000 0E00 Error Count (EC) Total: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Error Interval: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 %Error Free Interval: 0.000 0 to 100.000 0 Error Rate (ER) Insertion (INS): 0.000 1E–18 to 1.000 0E00 Error Count (EC) Insertion (INS): 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Error Rate (ER) Omission (OMI): 0.000 1E–18 to 1.000 0E00 Error Count (EC) Omission (OMI): 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Frequency: 2 400.000 to 58 200.000 MHz Frequency measurement accuracy: ±1 ppm ±1 kHz*1 Clock Count: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Confidence Level: 0.0 to 99.9 % Sync Loss Interval: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Clock Loss Interval: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Expressions enclosed in parentheses are abbreviations.

*1: With a gating system and with MP1900A's reference clock (10 MHz) calibrated

Table 1.3.3.3-9 Measurement (Cont'd)

Item	Specifications
Counter (Cont'd)	MSB Error Rate (ER) Total: 0.000 1E–18 to 1.000 0E00 MSB Error Count (EC) Total: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 MSB Error Interval*2: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 MSB %Error Free Interval*2: 0.000 0 to 100.000 0 MSB Error Rate (ER) Insertion (INS): 0.000 1E–18 to 1.000 0E00 MSB Error Count (EC) Insertion (INS): 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 MSB Error Rate (ER) Omission (OMI): 0.000 1E–18 to 1.000 0E00 MSB Error Count (EC) Omission (OMI): 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 LSB Error Rate (ER) Total: 0.000 1E–18 to 1.000 0E00 LSB Error Count (EC) Total: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 LSB Error Interval*2: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 LSB %Error Free Interval*2: 0.000 0 to 100.000 0 LSB Error Rate (ER) Insertion (INS): 0.000 1E–18 to 1.000 0E00 LSB Error Count (EC) Insertion (INS): 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 LSB Error Rate (ER) Omission (OMI): 0.000 1E–18 to 1.000 0E00 LSB Error Count (EC) Omission (OMI): 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 The following are available only for PAM4 (Diagnostics Mode ON) measurement. MSB Bit Count: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 MSB Clock Count: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 MSB Sync. Loss Interval: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 LSB Bit Count: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 LSB Clock Count: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 LSB Sync. Loss Interval: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Expressions enclosed in parentheses are abbreviations.

*2: Can be obtained only with remote commands.

Table 1.3.3.3-9 Measurement (Cont'd)

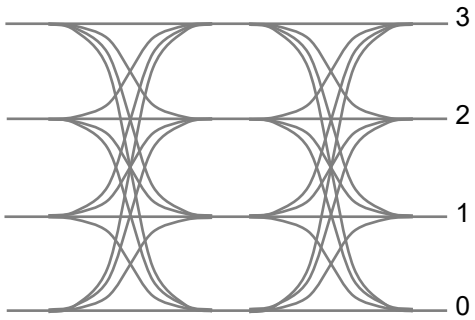
Item	Specifications
Counter (Cont'd)	The following are available only with the Option z41 SER Measurement. The following are available only for PAM4 (Diagnostics Mode OFF) measurement.  Symbol Error Rate (SER): 0.000 1E–18 to 1.000 0E00 Symbol Error Count (SEC): 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Symbol Error Interval: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Symbol %Error Free Interval: 0.000 0 to 100.000 0 PAM4 Symbol Count: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 3 PAM4 Count: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 2 PAM4 Count: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 1 PAM4 Count: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 0 PAM4 Count: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Details-Result PAM4- Transition Level 0 → 3 EC: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 0 → 2 EC: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 0 → 1 EC: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 0 EC Total: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 0 ER Total: 0.000 1E–18 to 1.000 0E00 Level 1 → 3 EC: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 1 → 2 EC: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 1 → 0 EC: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 1 EC Total: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 1 ER Total: 0.000 1E–18 to 1.000 0E00

Table 1.3.3.3-9 Measurement (Cont'd)

Item	Specifications
Counter (Cont'd)	Level 2 → 3 EC: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 2 → 1 EC: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 2 → 0 EC: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 2 EC Total: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 2 ER Total: 0.0001E–18 to 1.000 0E00 Level 3 → 2 EC: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 3 → 1 EC: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 3 → 0 EC: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 3 EC Total: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 3 ER Total: 0.000 1E–18 to 1.000 0E00 Details-Result PAM4- Eye*3 Transition 1level Level 0 → 1 and Level 1 → 0 SEC: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 1 → 2 and Level 2 → 1 SEC: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 2 → 3 and Level 3 → 2 SEC: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Transition 2level Level 0 → 2 and Level 2 → 0 SEC: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Level 1 → 3 and Level 3 → 1 SEC: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Transition 3level Level 0 → 3 and Level 3 → 0 SEC: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Upper Eye Total SEC: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Middle Eye Total SEC: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Lower Eye Total SEC: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Upper Eye Total SER: 0.000 1E–18 to 1.000 0E00 Middle Eye Total SER: 0.000 1E–18 to 1.000 0E00 Lower Eye Total SER: 0.000 1E–18 to 1.000 0E00

*3: Available only when **Input Signal Decoder** is set to **OFF**.

Table 1.3.3.3-9 Measurement (Cont'd)

Item	Specifications
Counter (Cont'd)	The following items are available only with the Option w42 FEC Analysis. Uncorrectable Codeword Error Rate (UCWER): 0.000 1E–18 to 1.000 0E00 Uncorrectable Codeword Error Count (UCWEC): 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Uncorrectable Codeword Error Interval: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Uncorrectable Codeword %Error Free Interval: 0.000 0 to 100.000 0 FEC Symbol Error Rate (ER): 0.000 1E–18 to 1.000 0E00 FEC Symbol Error Count (EC): 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 FEC Symbol Error Interval: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 FEC Symbol %Error Free Interval: 0.000 0 to 100.000 0 Total Codeword Count: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Details-Result RS-FEC MSB FEC Symbol Error Rate (ER) Total: 0.000 1E–18 to 1.000 0E00 MSB FEC Symbol Error Count (EC) Total: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 LSB FEC Symbol Error Rate (ER) Total: 0.000 1E–18 to 1.000 0E00 LSB FEC Symbol Error Count (EC) Total: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 FEC Symbol Error Count N = 0 to 31 Codeword Rate: 0.000 1E–18 to 1.000 0E00 N = 0 to 31 Codeword Count: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Uncorrectable Codeword Rate (UCWR): 0.000 1E–18 to 1.000 0E00 Uncorrectable Codeword Count (UCWC): 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Expressions enclosed in parentheses are abbreviations.

Table 1.3.3.3-9 Measurement (Cont'd)

Item	Specifications
Counter (Cont'd)	The following are available only when the "BERT for PCIe1-7", "BERT for PCIe1-6 Forced Link", or "BERT for PCIe1-5 and PCIe6 Base" application is selected. First Bit Error Rate (ER): 0.000 1E–18 to 1.000 0E00 First Bit Error Count (EC): 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 First Bit Error Interval: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 First Bit %Error Free Interval: 0.000 0 to 100.000 0 Details-Result PAM4 MSB First Bit Error Rate (ER) Total: 0.000 1E–18 to 1.000 0E00 MSB First Bit Error Count (EC) Total: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 LSB First Bit Error Rate (ER) Total: 0.000 1E–18 to 1.000 0E00 LSB First Bit Error Count (EC) Total: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 The following are available only when the "BERT for PCIe1-7", "BERT for PCIe1-6 Forced Link", or "BERT for PCIe1-5 and PCIe6 Base" application is selected with the Option w43 FEC Analysis for PCIe6. Flit Error Rate (FER): 0.000 1E–18 to 1.000 0E00 Flit Error Count (FEC): 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Flit Error Interval: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Flit %Error Free Interval: 0.000 0 to 100.000 0 FEC Symbol Error Rate (ER): 0.000 1E–18 to 1.000 0E00 FEC Symbol Error Count (EC): 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 FEC Symbol Error Interval: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 FEC Symbol %Error Free Interval: 0.000 0 to 100.000 0 Total Flit Count: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17

Table 1.3.3.3-9 Measurement (Cont'd)

Item	Specifications
Counter (Cont'd)	Details-Result FEC FEC Symbol Error Count N = 0 to Over8 Flit Rate: 0.000 1E–18 to 1.000 0E00 N = 0 to Over8 Flit Count: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 N = 0 to Over8 ECC Group Rate: 0.000 1E–18 to 1.000 0E00 N = 0 to Over8 ECC Group Count: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Flit Error Rate (FER): 0.000 1E–18 to 1.000 0E00 Flit Error Count (FEC): 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Consecutive Flit Error Rate (ER) Total: 0.000 1E–18 to 1.000 0E00 Consecutive Flit Error Count (EC) Total: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Consecutive FEC Symbol Error Rate (ER) Total: 0.000 1E–18 to 1.000 0E00 Consecutive FEC Symbol Error Count (EC) Total: 0 to 9 999 999, 1.000 0E07 to 9.999 9E17 Expressions enclosed in parentheses are abbreviations.
RS-FEC Error Distribution	Available only with the Option w42 FEC Analysis. The number of codewords is displayed in a graph by FEC symbol error count per codeword.
PCIe6 FEC Error Distribution	Available only when the "BERT for PCIe1-7", "BERT for PCIe1-6 Forced Link", or "BERT for PCIe1-5 and PCIe6 Base" application is selected with the Option w43 FEC Analysis for PCIe6. The number of flits is displayed in a graph by FEC symbol error count per flit.

Table 1.3.3.3-9 Measurement (Cont'd)

Item	Specifications
Input Signal Decoder Indicator	Displays the coding status during PAM4 mode error measurement. Raw Signal: Displays error measurement results of input data without decoding it. Decoded Signal: Displays error measurement results of decoded input data.
Gating	Time, Clock Count, Error Count
Gating Unit	Time: 1 second to 99 days 23 hours 59 minute 59 seconds Clock Count: >E+4 to >E+16 Error Count: >E+4 to >E+16
Cycle	Single, Repeat, Untimed, Single(Target CL)
Current	On, Off can be set. Calculation: Progressive, Immediate Interval: 100 ms, 200 ms
Auto Sync	On, Off can be set. Synchronization threshold: INT, E–2 to E–8

Table 1.3.3.3-9 Measurement (Cont'd)

Item	Specifications		
Sync Control	PRBS:	Automatic Synchronization	
	Data:	Frame On	
	HSSB Data:	Automatic Synchronization	
Frame Length	NRZ:	4 to 64 bits, in steps of 4 bits	
	PAM4:	4 to 64 symbols, in steps of 4 symbols	
Frame Mask	Available		
Frame Position	NRZ:	1 to (Pattern Length – Frame Length +1) bits, in steps of 1 bit	
	PAM4:	1 to (Pattern Length – Frame Length +1) symbols, in steps of 1 symbol	
Error/Alarm Conditions			
Error Detection	NRZ:	Insertion/Omission, Transition/Non Transition	
	PAM4:	Not available	
EI/EFI Interval	1 ms, 10 ms, 100 ms, 1 s		
Confidence Level	Compatible with MX190000A version 10.07.00 or later.		
	Target CL:	0 to 99.9 %	
	Target ER:	1E-15 to 9E-3	
	Target EC:	0 to 10	
	Target Unit:	NRZ:	Bit, Codeword*4
		PAM4:	Bit, PAM4 Symbol*5, Codeword*4
		When the "BERT for PCIe1-6", "BERT for PCIe1-6 Forced Link", or "BERT for PCIe1-5 and PCIe6 Base" application is running:	
		NRZ:	Bit
		PAM4:	Bit, First Bit, PAM4 Symbol*5, Flit*6
	Target Baud Rate/Bitrate:	NRZ:	2.4 to 64.2 Gbit/s
		PAM4:	2.4 to 58.2 Gbaud
		When the "BERT for PCIe1-6", "BERT for PCIe1-6 Forced Link", or "BERT for PCIe1-5 and PCIe6 Base" application is running:	
		NRZ:	2.4 to 32.1 Gbit/s
		PAM4:	2.4 to 32.1 Gbaud
	PPG Target Baud Rate/Bitrate Tracking:	Tracks the operating baud rate or bit rate of the PPG that is selected from the PPGs installed in the same MP1900A.	

*4: With Option w42

*5: With Option z41

*6: With Options z41 and w43

Table 1.3.3.3-10 Error Analysis

Item	Specifications
Bit Mask (Block Window)	Excludes the specified data pattern from measurement.*1 Available only when **Modulation** is set to **PAM4** in the BERT for PCIe1-7, BERT for PCIe1-6 Forced Link, or BERT for PCIe1-5 and PCIe6 Base application.
Setting resolution	The resolution is set depending on the pattern length as follows: Pattern length (bits) — Setting resolution (bits) 2 to 2 097 152 — 1 2 097 153 to 4 194 304 — 2 4 194 305 to 8 388 608 — 4 8 388 609 to 16 777 216 — 8 16 777 217 to 33 554 432 — 16 33 554 433 to 67 108 864 — 32 67 108 865 to 134 217 728 — 64 134 217 729 to 268 435 456 — 128
Lane Mask (Bit Window)	Excludes any channels among internal 32 channels from measurement.*1 (Available only in NRZ mode.)
External Mask*2	H: Measurement L: Mask

*1: RS-FEC and HSSB Data patterns are excluded.

*2: Not available when HSSB Data is selected.

Table 1.3.3.3-10 Error Analysis (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Capture*2

Capture Mode</td><td>NRZ, PAM4 (Only FEC Symbol Capture is available when LSB/MSB Diagnostics is set to ON.)
PAM4 is available only with the Option z41 SER Measurement.
Sync Mode Capture
Performs error judgment. Input data must be synchronized to the set pattern.
Raw Data Capture
Does not perform error judgment. Input data do not need to be synchronized to the set pattern.
FEC Symbol Capture*3, *4
Performs IEEE802.3 FEC symbol error judgment. Input data must be synchronized to the set pattern.
Judgement is made on whether the number of FEC Symbol errors exceeds the threshold.
PCIe6 FEC Symbol Capture*4, *5
Performs PCIe6 FEC symbol error judgment. Input data must be synchronized to the set pattern.
Judgement is made on whether the number of FEC symbol errors exceeds the threshold.

Refer to the table below for Capture Mode that can be executed according to the Input Signal Decoder setting.
<table>
<tr><th rowspan="3">Capture Mode</th><th colspan="4">Input Signal Decoder</th></tr>
<tr><th colspan="2">(Diagnostics Mode = OFF)</th><th colspan="2">(Diagnostics Mode = ON)</th></tr>
<tr><th>OFF</th><th>ON</th><th>OFF</th><th>ON</th></tr>
<tr><td>Raw Data Capture</td><td>✓*6</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>Sync Mode Capture</td><td>✓</td><td>✓</td><td>–</td><td>–</td></tr>
<tr><td>FEC Symbol Capture</td><td>✓</td><td>✓</td><td>✓</td><td>✓</td></tr>
<tr><td>PCIe6 FEC Symbol Capture</td><td>✓</td><td>✓</td><td>–</td><td>–</td></tr>
</table>
</td></tr>
</table>

*3: Each FEC Symbol consists of data of 10 or 20 bits.

*4: Occurrence of one or more bit errors in one FEC Symbol is counted as one FEC Symbol error.

*5: Each PCIe6 FEC symbol consists of 8-bit data.

*6: This is available only when SKP OS Filter = OFF.

Table 1.3.3.3-10 Error Analysis (Cont'd)

<table>
<tr><th>Item</th><th>Specifications</th></tr>
<tr><td>Capture (Cont'd)
Auto Launch</td><td>Select the result screen you want to display automatically when data is captured.
● Capture Data
Displays the captured pattern data numerically or by a string (Bin, Hex, Symbol).
● Error Mapping
Displays the captured error data as a map.
This cannot be selected when Capture Mode is Raw Data Capture or FEC Symbol Capture.
● Disable
Does not automatically display the result screen.</td></tr>
<tr><td>Number of Blocks</td><td>1, 2, 4, 8, 16, 32, 64, 128</td></tr>
<tr><td>Block Length</td><td>NRZ: 8 Mbits / n (n=Number of blocks)
PAM4: 4 Msymbols / n (n=Number of blocks)</td></tr>
<tr><td>Trigger</td><td>Error Detect, Match Pattern, Manual Trigger, External Trigger (Rising Edge), Consecutive Error Detect, Intermittent Error Detect
Error Detect cannot be selected when Capture Mode is Raw Data Capture.
For the relationship between Capture Modes and selectable Triggers, refer to the table below.
<table>
<tr><th>Trigger</th><th>Sync Mode Capture</th><th>Raw Data Capture</th><th>FEC Symbol Capture</th><th>PCIe6 FEC Symbol Capture</th></tr>
<tr><td>Error Detect</td><td>✓</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>Match Pattern</td><td>✓</td><td>✓</td><td>–</td><td>–</td></tr>
<tr><td>Manual Trigger</td><td>✓</td><td>✓</td><td>✓</td><td>✓</td></tr>
<tr><td>External Trigger</td><td>✓</td><td>✓</td><td>–</td><td>–</td></tr>
<tr><td>Consecutive FEC Symbol Error Detect*7</td><td>–</td><td>–</td><td>✓</td><td>✓</td></tr>
<tr><td>Intermittent FEC Symbol Error Detect*8</td><td>–</td><td>–</td><td>✓</td><td>✓</td></tr>
<tr><td>Consecutive Flit Error Detect*9</td><td>–</td><td>–</td><td>–</td><td>✓</td></tr>
<tr><td>Pattern Sync</td><td>✓</td><td>–</td><td>–</td><td>✓</td></tr>
</table></td></tr>
</table>

*7: Consecutive Error Detect: Starts capturing when the number of consecutive FEC symbol errors equals to or exceeds the threshold regardless of codeword or flit.

*8: Intermittent Error Detect: Starts capturing when the number of FEC symbol errors per codeword or flit exceeds the threshold.

*9: Consecutive Flit Error Detect: Starts capturing when the number of consecutive flit errors equals to or exceeds the threshold.

Table 1.3.3.3-10 Error Analysis (Cont'd)

Item	Specifications
Capture (Cont'd)	
Capture Area	After the Trigger, Around the Trigger, Before the Trigger After the Trigger and Before the Trigger cannot be selected when Capture Mode is FEC Symbol Capture or PCIe6 FEC Symbol Capture.
Match Pattern Length	NRZ: 4 to 64 bits, in steps of 1 bit PAM4: 4 to 64 symbols, in steps of 1 symbol
Match Pattern Mask	NRZ: 4 to 64 bits, in steps of 1 bit PAM4: 4 to 64 symbols, in steps of 1 symbol
FEC Symbol Capture Setting	
Preset	For NRZ: Variable,RS-FEC 25G 1Lane, RS-FEC 50G 2Lanes RS(544,514), RS-FEC 100G 4Lanes, RS-FEC 100G 4Lanes RS(544,514) For PAM4: Variable, RS-FEC 50G 1Lane, RS-FEC 100G 1Lane, RS-FEC-Int 100G 1Lane, RS-FEC 100G 2Lanes, RS-FEC 200G 2Lanes, RS-FEC 200G 4Lanes, RS-FEC 400G 4Lanes, RS-FEC 400G 8Lanes
Number of FEC Symbols per Lane in a Codeword	68, 132, 136, 272, 528, 544 FEC Symbols, in steps of 1 FEC Symbol
Bit Length in a FEC Symbol	10, 20 bits
FEC Symbol Errors in a Codeword	When Trigger is Consecutive Error Detect: 1 to 32 FEC Symbols, in steps of 1 FEC Symbol When Trigger is Intermittent Error Detect: 1 to 32 FEC Symbols, in steps of 1 FEC Symbol
Comparison	Greater than or equal to, Equal to

Table 1.3.3.3-10 Error Analysis (Cont'd)

Item	Specifications
Capture (Cont'd)	
PCIe6 FEC Symbol Capture Setting	
PCIe6 Standard	x1 Link Common CLK/SRNS Mode x2 Link Common CLK/SRNS Mode x4 Link Common CLK/SRNS Mode x8 Link Common CLK/SRNS Mode x16 Link Common CLK/SRNS Mode x1 Link SRIS Mode x2 Link SRIS Mode x4 Link SRIS Mode x8 Link SRIS Mode x16 Link SRIS Mode
SKP	No SKP, SKPx1, SKPx2
Flit Length	16, 32, 64, 128, 256 FEC Symbols
SKP Interval	4, 9, 18, 37, 46, 74, 93, 187, 374, 748 Flits
FEC Symbol Error Threshold in One ECC Group	1 to 8 FEC Symbols, in steps of 1 FEC Symbol The upper limit value is "4" if PCIe6 Standard is set to one of the following: ● x16 Link Common CLK/SRNS Mode ● x16 Link SRIS Mode
FEC Symbol Error Threshold in One ECC Group Comparison	Greater than or equal to
FEC Symbol Error Threshold	1 to 8 FEC Symbols, in steps of 1 FEC Symbol
FEC Symbol Error Threshold Comparison	Greater than or equal to, Equal to
Errored Flit Threshold	1 to 4 Flits, in steps of 1 Flit
Errored Flit Threshold Comparison	Greater than or equal to, Equal to
Capture Result	
Capture Data	Displays captured results by bit or symbol sequence in NRZ or PAM4 mode. When Capture Mode is Sync Mode Capture, FEC Symbol Capture, or PCIe6 FEC Symbol Capture, error bits and symbols are displayed with background color.
Trigger Position	Displays the trigger position by block and the total number of flits by block.
Viewer Mode	Sets the view mode of the captured result pattern. NRZ: BIN, HEX PAM4: Symbol, BIN(MSB/LSB) Waveform display can be turned on and off. ECC Group display can be turned on and off.*10

*10: This is available in PCIe6 FEC Symbol Capture mode only.

Table 1.3.3.3-10 Error Analysis (Cont'd)

Item	Specifications
Capture (Cont'd) Capture Result (Cont'd) Capture Data (Cont'd) Error display	NRZ: Insertion Error, Omission Error When the input signal decoder is **OFF**: PAM4(Symbol): Lower Eye Error, Middle Eye Error, Upper Eye Error, Middle/Lower Eye Error, Upper/Middle Eye Error, Upper/Middle/Lower Eye Error When the input signal decoder is **ON**: PAM4(Symbol): MSB, LSB, MSB+LSB PAM4(MSB/LSB): Insertion Error, Omission Error
Error Search	Available only when **Capture Mode** is set to **Sync Mode Capture**, **FEC Symbol Capture**, or **PCIe6 FEC Symbol Capture**. First: Fist error Pre: Previous error Next: Next error Last: Last error In PAM4 mode only, a search target can be selected from All, Upper Eye, Middle Eye and Lower Eye.
Continuous Error	Available only when **Capture Mode** is set to **Sync Mode Capture**, **FEC Symbol Capture**, or **PCIe6 FEC Symbol Capture**. Searches for continuous error bits/symbols. NRZ: 1 to 256 bits PAM4(Symbol): 1 to 256 symbols PAM4(MSB/LSB) : 1 to 256 bits FEC Symbol: 1 to 256 FEC symbols 1b/1b Encoding: 1 to 256 1b/1b symbols
Codeword Head Position Jump	Available only when **Capture Mode** is set to **Sync Mode Capture**, **FEC Symbol Capture**, or **PCIe6 FEC Symbol Capture**. Searches for the First bit/symbol of a codeword. First: First bit/symbol of the first codeword Pre: First bit/symbol of the previous codeword Next: First bit/symbol of the next codeword Last: First bit/symbol of the last codeword
Flit Jump	Available only when **Capture Mode** is set to **FEC Symbol Capture**. Searches for the First bit/symbol of a Filt. First Flit: First bit/symbol of the first Filt Pre Flit Interval: First bit/symbol of the previous Flit block Pre Flit: First bit/symbol of the previous Filt Next Flit: First bit/symbol of the next Filt Next Flit Interval: First bit/symbol of the next Flit block Last Flit: First bit/symbol of the last Filt Available only when **Capture Mode** is set to **PCIe6 FEC Symbol Capture**.

Table 1.3.3.3-10 Error Analysis (Cont'd)

Item	Specifications
Capture (Cont'd)	
File Save	Saves the captured results and pattern to a file. NRZ: BIN/HEX Text: Captured result file (It can be opened in the Capture Data screen.) BIN/HEX Text(export): Pattern file including error information (It can be opened in Pattern Editor.) PAM4: Symbol Text: Captured result file (It can be opened in the Capture Data screen.) Symbol Text(export): Pattern file including error information (It can be opened in Pattern Editor.)
File Open	Redisplays the captured results. NRZ: BIN/HEX Text: Captured result file PAM4: Symbol Text: Captured result file
Error Mapping	Visually maps errors using bits with colored-background in NRZ or PAM4 mode. This is available only when **Capture Mode** is set to **Sync Mode Capture**.
Error display	NRZ: Insertion Error, Omission Error When the input signal decoder is **OFF**: PAM4: Lower Eye Error, Middle Eye Error, Upper Eye Error, Middle/Lower Eye Error, Upper/Middle Eye Error, Upper/Middle/Lower Eye Error When the input signal decoder is **ON**: PAM4: MSB, LSB, MSB+LSB
File Open	Remaps the captured results (errors). NRZ: BIN/HEX Text: Captured result file PAM4: Symbol Text: Captured result file

Table 1.3.3.3-11 Auto Measurement

Item	Specifications
Bath-Tub	NRZ/PAM4: Available*1, *2, *3, *4
Eye Contour	NRZ/PAM4: Available*2, *3, *4, *5, *6
Auto Adjust	NRZ: Vth direction only*7 PAM4: MSB Vth direction only*7, *8
Auto Search	NRZ: Available*7 PAM4 (LSB/MSB Diagnostics OFF/ON): Available*7, *9
Advanced Search	Supports adjustment of PRBS Inv, Logic (MSB, LSB), Gray Coder, Inverse Gray Coder, Eye Threshold (Middle, Upper, Lower), Delay, DFE and LFEQ.*10 NRZ: Available*7 PAM4: Available*7, *9, *11
BER/SER Logging	NRZ: With BER Logging PAM4: With SER Logging

*1: When PAM4 is selected, measurement can be performed by selecting one from Upper, Middle, and Lower Eyes, and SER.

*2: Not available under the following conditions:

- There is a swap between MSB and LSB patterns in RS-FEC Scrambled Idle Pattern. (Swap lamp: On)
- The measured value of MSB/LSB Diff is other than 0.

*3: With Option z41

*4: Not available when HSSB Data is selected.

*5: When PAM4 is selected, measurement can be performed by selecting one from Upper, Middle, and Lower Eyes.

*6: PAM4 waveform display (Phase delay of each of Upper, Middle, and Lower eyes inside the measuring instrument is optimized and simultaneously displayed.)

*7: PRBS Pattern, Mark Ratio 1/2

*8: Each of amplitudes shall be equal.

*9: Each of 0/1, 1/2, and 2/3 levels is equal.

*10: Option x11 is required for adjustment of DEF and LFEQ.

*11: PRBS Inv, Logic (MSB, LSB), Gray Coder, Inverse Gray Coder, and Eye Threshold (Middle, Upper, Lower) are available only when Modulation Type is set to PAM4.

Table 1.3.3.3-12 Variable Clock Delay

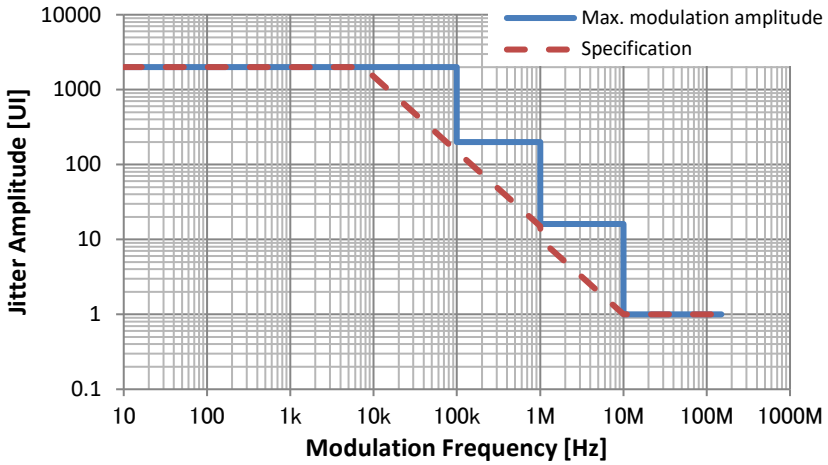
Item	Specifications
Phase variable range	–1000 to +1000 mUI, in steps of 2 mUI
Accuracy	±50 mUIp-p*1, *2 (Baud rate ≤32.1 Gbaud) ±100 mUIp-p*1, *2 (Baud rate >32.1 Gbaud)
mUI – ps switching	Available (internally converted into ps)
Calibration	Available (when jitter modulation is off)
Calibration indicator	This indicator is on when Calibration is required due to: ● Change in 1/1Clock frequency by ±250 kHz. ● Change in the ambient temperature by ±5 °C.
Delay Stabilizer	Provided*3 Automatically enabled when performing Auto Search including Phase Search.

*1: Measure using an oscilloscope with residual jitter of less than 200 fs (RMS).

*2: Typical value

*3: Available only when **PAM4** is selected and Baud rate is between 26.0 and 32.1 Gbaud.

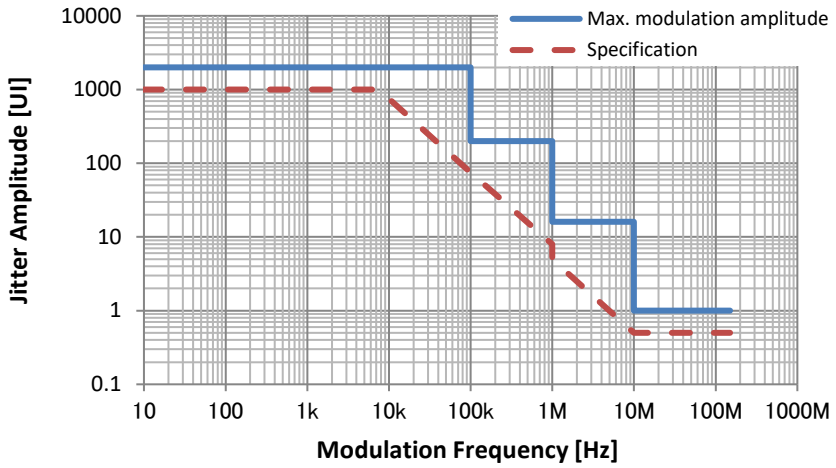
Table 1.3.3.3-13 Jitter Tolerance

Item	Specifications
For NRZ input	Bit rate: 32.1 Gbit/s, 64.2 Gbit/s*1 Pattern:PRBS2^{31}–1 32.1 Gbits: With MU181500B, SSC with frequency of 33 kHz and deviation of 5300 ppm can be applied simultaneously with RJ with amplitude of 0.3 UI. 64.2 Gbits: With MU181500B, SSC with frequency of 33 kHz and deviation of 3300 ppm can be applied simultaneously with RJ with amplitude of 0.3 UI. These specifications are defined assuming the following conditions: Loopback connection to the MU196020A, at a constant temperature between 20 and 30 °C. When RJ+BUJ/SJ3 is bigger than 0.5 UIp-p or SJ + RJ + BUJ/SJ3 is bigger than the standard value + 0.3 UIp-p, “Overload” is displayed on the MU181500B screen. Note that if Modulation Frequency is 33 kHHz, and RJ+BUJ/SJ3 is bigger than 0.5UIp-p or SJ1 is bigger than 550 UIp-p, “Overload” is displayed on the MU181500B screen. 32.1 Gbit/s  **Modulation frequency [Hz] / Max. modulation amplitude [UIp-p] / Specification [UIp-p]** 10 / 2 000 / 2 000 7 500 / 2 000 / 2 000 100 000 / 2 000 / 150 1 000 000 / 200 / 15 10 000 000 / 16 / 1 150 000 000 / 1 / 1

*1: When Option 002, 005, y12, 115, or 125 is installed.

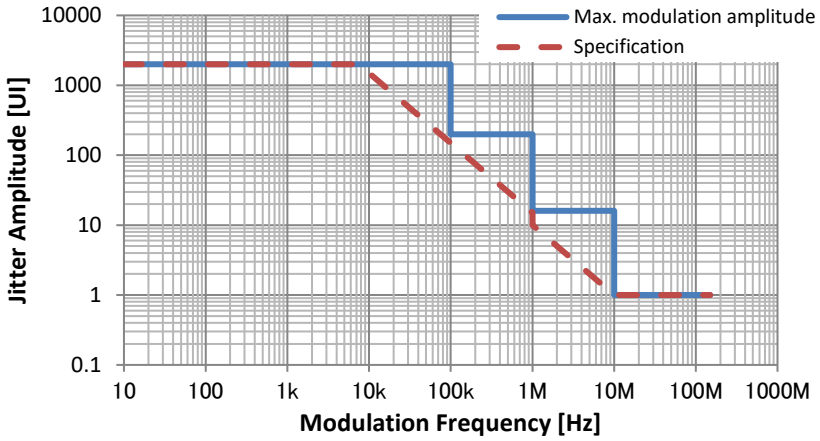
Table 1.3.3.3-13 Jitter Tolerance (Cont'd)

Item	Specifications
For NRZ input (Cont'd)	64.2 Gbit/s



Modulation frequency [Hz]	Max. modulation amplitude [UIp-p]	Specification [UIp-p]
10	2 000	1 000
7 500	2 000	1 000
100 000	2 000	75
1 000 000	200	8
10 000 000	16	0.5
150 000 000	1	0.5

Table 1.3.3.3-13 Jitter Tolerance (Cont'd)

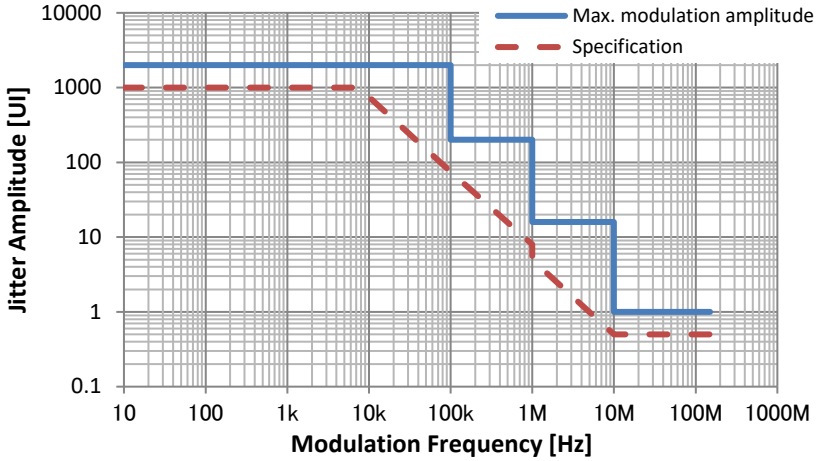
Item	Specifications
For PAM4 input	Baud rate: 32.1 Gbaud*2, 58.2 Gbaud*1 Pattern:PRBS31Q 32.1 Gbaud: With MU181500B, SSC with frequency of 33 kHz and deviation of 5300 ppm can be applied simultaneously with RJ with amplitude of 0.3 UI. 58.2 Gbaud: With MU181500B, SSC with frequency of 33 kHz and deviation of 3300 ppm can be applied simultaneously with RJ with amplitude of 0.3 UI. These specifications are defined assuming the following conditions: Loopback connection to the MU196020A, at a constant temperature between 20 and 30 °C. When RJ+BUJ/SJ3 is bigger than 0.5 UIp-p or SJ + RJ + BUJ/SJ3 is bigger than the standard value + 0.3 UIp-p, "Overload" is displayed on the MU181500B screen. When the modulation frequency is 33 kHz, an Overload message is displayed on the MU181500B screen if RJ+BUJ/SJ3 >0.5 UIp-p or SJ1 >550UIp-p. 32.1 Gbaud 

Modulation frequency [Hz]	Max. modulation amplitude [UIp-p]	Specification [UIp-p]
10	2 000	2 000
7 500	2 000	2 000
100 000	2 000	150
1 000 000	200	15
10 000 000	16	1
150 000 000	1	1

*2: With Option 001

Table 1.3.3.3-13 Jitter Tolerance (Cont'd)

Item	Specifications
For PAM4 input (Cont'd)	58.2 Gbaud



Modulation frequency [Hz]	Max. modulation amplitude [UIp-p]	Specification [UIp-p]
10	2 000	1 000
7 500	2 000	1 000
100 000	2 000	75
1 000 000	200	8
10 000 000	16	0.5
150 000 000	1	0.5

Table 1.3.3.3-14 Clock Recovery

Item	Specifications*1
Operating Baud rate	With Option x21 NRZ: 2.4 to 29.0 Gbit/s PAM4: 2.4 to 29.0 Gbaud When Option x22, or x21 + y24 is installed. NRZ: 2.4 to 32.1 Gbit/s PAM4: 2.4 to 32.1 Gbaud With Option x23 NRZ: 51.0 to 58.2 Gbit/s PAM4: 51.0 to 58.2 Gbaud
Setting range*2	With Option x21 NRZ: 2.400 000 to 29.000 000 Gbit/s, in steps of 0.000 001 Gbit/s PAM4: 2.400 000 to 29.000 000 Gbaud, in steps of 0.000 001 Gbaud When Option x22, or x21 + y24 is installed. NRZ: 2.400 000 to 32.100 000 Gbit/s, in steps of 0.000 001 Gbit/s PAM4: 2.400 000 to 32.100 000 Gbaud, in steps of 0.000 001 Gbaud With Option x23 NRZ: 51.000 000 to 58.200 000 Gbit/s, in steps of 0.000 001 Gbit/s*3 PAM4: 51.000 000 to 58.200 000 Gbaud, in steps of 0.000 001 Gbaud*3

*1: With Option x21, x22, x23, or y24
Options x22 and x23 can be installed together.
Option x23 requires one of the following options: x21, x22, 002, 005, y12, 115, and 125.
Options x21 and x22 cannot be installed together.
Options x21 and x23 can be installed together.
Option y24 requires Option x21.
These are specified with the conditions of PRBS Pattern and Mark Ratio 1/2 (in PAM4 mode, MSB Mark Ratio 1/2) unless otherwise specified.

*2: When the ED is tracking the PPG linked with MU181000A/B and MU181500B, it operates in the same ranges of bit rate and baud rate as the PPG if a recovered clock is used as a system clock.

*3: Available only when neither the BERT for PCIe1-7, BERT for PCIe1-6 Forced Link, nor BERT for PCIe1-5 and PCIe6 Base application is selected.

Table 1.3.3.3-14 Clock Recovery (Cont'd)

<table>
<tr><th>Item</th><th>Specifications*1</th></tr>
<tr><td>Supported standard and baud rate</td><td>For NRZ mode
<table>
<tr><th>Standard</th><th>Bit Rate [Gbit/s]</th><th>Remarks</th></tr>
<tr><td>CEI-56G</td><td>56.000 000</td><td>*4</td></tr>
<tr><td>100G ULH</td><td>32.100 000</td><td>*5</td></tr>
<tr><td>PCIe5</td><td>32.000 000</td><td>*5</td></tr>
<tr><td>32G FC</td><td>28.050 000</td><td>*6</td></tr>
<tr><td>CEI-28G</td><td>28.000 000</td><td>*6</td></tr>
<tr><td>100G OTU4</td><td>27.952 496</td><td>*6</td></tr>
<tr><td>100GAUI-4</td><td>26.562 500</td><td>*6</td></tr>
<tr><td>50GAUI-2</td><td>26.562 500</td><td>*6</td></tr>
<tr><td>LAUI-2</td><td>25.781 250</td><td>*6</td></tr>
<tr><td>25GAUI</td><td>25.781 250</td><td>*6</td></tr>
<tr><td>CAUI-4 (100GbE (25.78 × 4))</td><td>25.781 250</td><td>*6</td></tr>
<tr><td>InfiniBand EDR</td><td>25.781 250</td><td>*6</td></tr>
<tr><td>SAS4</td><td>22.500 000</td><td>*6</td></tr>
<tr><td>Thunderbolt2</td><td>20.625 000</td><td>*6</td></tr>
<tr><td>DisplayPort UHBR 20</td><td>20.000 000</td><td>*6</td></tr>
<tr><td>USB4 Gen3</td><td>20.000 000</td><td>*6</td></tr>
<tr><td>PCIe4</td><td>16.000 000</td><td>*6</td></tr>
<tr><td>InfiniBand FDR</td><td>14.062 500</td><td>*6</td></tr>
<tr><td>16G FC</td><td>14.025 000</td><td>*6</td></tr>
<tr><td>DisplayPort UHBR 13.5</td><td>13.500 000</td><td>*6</td></tr>
<tr><td>SAS3</td><td>12.000 000</td><td>*6</td></tr>
<tr><td>10G FC Over FEC</td><td>11.316 800</td><td>*6</td></tr>
<tr><td>10GbE Over FEC</td><td>11.095 700</td><td>*6</td></tr>
<tr><td>OTU2</td><td>10.709 225</td><td>*6</td></tr>
<tr><td>G975 FEC</td><td>10.664 228</td><td>*6</td></tr>
<tr><td>10G FC</td><td>10.518 750</td><td>*6</td></tr>
<tr><td>CAUI-10 (10GbE)</td><td>10.312 500</td><td>*6</td></tr>
<tr><td>Thunderbolt1</td><td>10.312 500</td><td>*6</td></tr>
<tr><td>DisplayPort UHBR 10</td><td>10.000 000</td><td>*6</td></tr>
</table></td></tr>
</table>

*4: With Option x23

*5: When Option x22, or x21 + y24 is installed.

*6: When Option x21, x22, or x21 + y24 is installed.

Table 1.3.3.3-14 Clock Recovery (Cont'd)

Item	Specifications*1
Supported standard and baud rate	For NRZ mode

Standard	Bit Rate [Gbit/s]	Remarks
USB4 Gen2	10.000 000	*6
InfiniBand QDR	10.000 000	*6
USB3.1 Gen2	10.000 000	*6
OC-192/STM-64	9.953 280	*6
8G FC	8.500 000	*6
DisplayPort HBR3	8.100 000	*6
PCIe3	8.000 000	*6
HSBI	6.250 000	*6
SATA 6Gb/s	6.000 000	*6
DisplayPort HBR2	5.400 000	*6
PCIe2	5.000 000	*6
InfiniBand DDR	5.000 000	*6
USB3.0	5.000 000	*6
4G FC	4.250 000	*6
XAUI	3.125 000	*6
OTU1	2.666 060	*6
InfiniBand SDR	2.500 000	*6
PCIe1	2.500 000	*6
OC-48/STM-16	2.488 320	*6

Table 1.3.3.3-14 Clock Recovery (Cont'd)

<table>
<tr><th>Item</th><th>Specifications*1</th></tr>
<tr><td>Supported standard and baud rate (Cont'd)</td><td>For PAM4 mode
<table>
<tr><th>Standard</th><th>Baud Rate [Gbaud]</th><th>Remarks</th></tr>
<tr><td>CEI 112G</td><td>56.000 000</td><td>*4</td></tr>
<tr><td>400GAUI-4 (400GbE (53.1 × 4))</td><td>53.125 000</td><td>*4</td></tr>
<tr><td>200GAUI-2</td><td>53.125 000</td><td>*4</td></tr>
<tr><td>100GAUI-1</td><td>53.125 000</td><td>*4</td></tr>
<tr><td>PCIe6</td><td>32.000 000</td><td>*5</td></tr>
<tr><td>64G FC</td><td>28.900 000</td><td>*6</td></tr>
<tr><td>CEI 56G</td><td>28.000 000</td><td>*6</td></tr>
<tr><td>400GAUI-8</td><td>26.562 500</td><td>*6</td></tr>
<tr><td>200GAUI-4 (200GbE (26.6 × 4))</td><td>26.562 500</td><td>*6</td></tr>
<tr><td>100GAUI-2</td><td>26.562 500</td><td>*6</td></tr>
<tr><td>50GAUI-1</td><td>26.562 500</td><td>*6</td></tr>
<tr><td>InfiniBand HDR</td><td>26.562 500</td><td>*6</td></tr>
</table>
PPG Operating baud rate tracking
Tracks the operating baud rate of the PPG selected from the PPGs installed in the same MP1900A. It is provided with an indicator that turns on when the PPG's operating baud rate is out of the tracking range.</td></tr>
<tr><td>Maximum number of consecutive zeros</td><td>When Option x21, x22, or x21 + y24 is installed.
72 bits
Zero Substitution 2^{15},
Target loop band: 1/1667, 1/2578 at 2.4 to 25.499 999 G,
1/1667, 1/2578, 1/6640 at 25.5 to 32.1 G
With Option x23
72 bits
Zero Substitution 2^{15},
Target loop band: 1/6640, 1/13280 at 51.0 to 58.2G</td></tr>
<tr><td>Lock range</td><td>When Option x21, x22, or x21 + y24 is installed.
±200 ppm
2.4 to 25.499 999 G, The target loop band is specified by 1/1667, 1/2578.
±100 ppm
25.5 to 32.1 G, The target loop band is specified by 1/1667, 1/2578, 1/6640.
With Option x23
±100 ppm
51.0 to 58.2 G, The target loop band is specified by 1/6640, 1/13280.</td></tr>
</table>

Table 1.3.3.3-14 Clock Recovery (Cont'd)

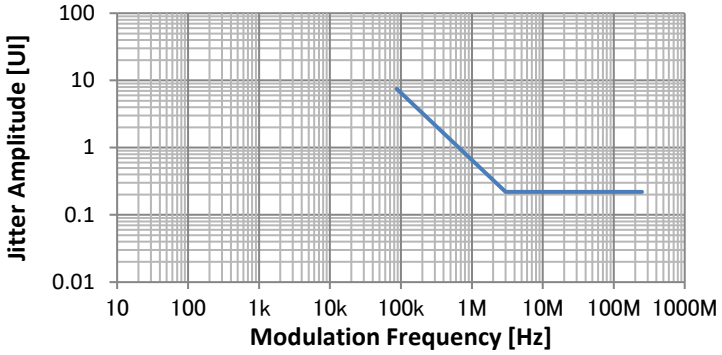
Item	Specifications*1
Target loop band	When Option x21, x22, or x21 + y24 is installed. 25.5 to 32.1 G*7 Baud rate / 1667 Baud rate / 2578 Baud rate / 6640 Jitter Tolerance 2.4 to 25.499 999 G Baud rate / 1667 Baud rate / 2578 Jitter Tolerance Variable When Variable is selected, the ranges are as follows: Baud rate [Gbaud] / Range [MHz] / Step [MHz] 2.400 000 to 5.500 000 / 3 / - 5.500 001 to 7.500 000 / 3 to 4 / 1 7.500 001 to 9.500 000 / 3 to 5 / 1 9.500 001 to 10.500 000 / 3 to 6 / 1 10.500 001 to 12.500 000 / 3 to 7 / 1 12.500 001 to 14.500 000 / 3 to 8 / 1 14.500 001 to 15.500 000 / 3 to 9 / 1 15.500 001 to 17.500 000 / 3 to 10 / 1 17.500 001 to 19.500 000 / 3 to 11 / 1 19.500 001 to 20.500 000 / 3 to 12 / 1 20.500 001 to 22.500 000 / 3 to 13 / 1 22.500 001 to 24.500 000 / 3 to 14 / 1 24.500 001 to 25.499 999 / 3 to 15 / 1 With Option x23 51.0 to 58.2 G*8 Baud rate / 6640 Baud rate / 13280 Jitter Tolerance

*7: The SSPRQ pattern supports Baud rate / 6640 only. When set to Jitter Tolerance, Baud rate / 1667 or higher.

*8: The SSPRQ pattern supports Baud rate / 6640 only. When set to Jitter Tolerance, Baud rate / 6640 or higher.

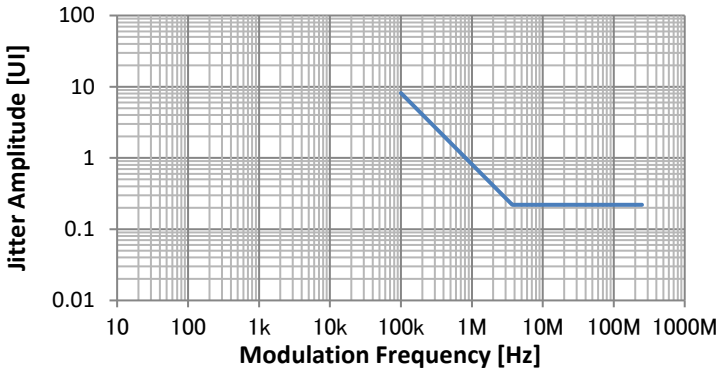
Table 1.3.3.3-14 Clock Recovery (Cont'd)

Item	Specifications
Jitter Tolerance NRZ input*9	At the bit rate of 58.0 Gbit/s, conforming to Jitter Tolerance Mask defined by the "CEI 56G Jitter Tolerance Mask". The following masks are taken as nominal values:



Modulation Frequency (Hz)	Jitter Tolerance Mask (UIp-p)
87 349	7.5
2 977 820	0.22
250 000 000	0.22

At the bit rate of 28.05 Gbit/s, conforming to Jitter Tolerance Mask defined by the "32G FC Jitter Tolerance Mask". The following masks are taken as typical values:

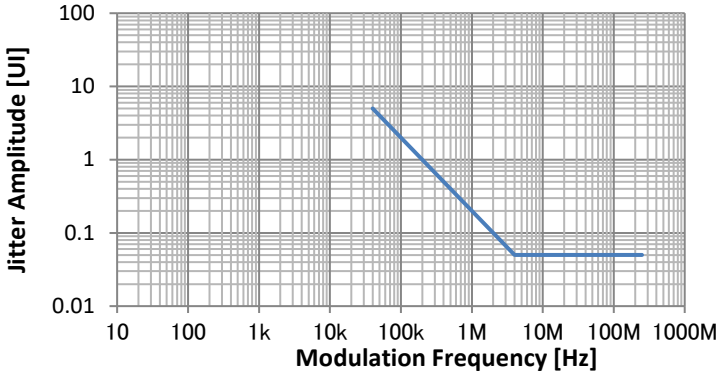


Modulation Frequency (Hz)	Jitter Tolerance Mask (UIp-p)
100 000	8.16
3 709 271	0.22
250 000 000	0.22

*9: Loopback connection to the MU196020A, PRBS $2^{31}-1$, specified at a constant temperature between 20 and 30 °C.

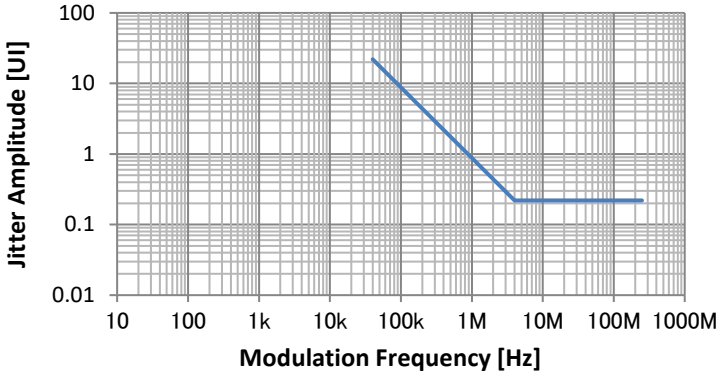
Table 1.3.3.3-14 Clock Recovery (Cont'd)

Item	Specifications
Jitter Tolerance (Cont'd) PAM4 input*10	At the bit rate of 53.125 Gbaud, conforming to Jitter Tolerance Mask defined by the "CEI-112G-VSR Jitter Tolerance Mask". The following masks are taken as nominal values:



Modulation Frequency (Hz)	Jitter Tolerance Mask (UIp-p)
40 004	5
4 000 377	0.05
250 000 000	0.05

At the bit rate of 26.5625 Gbaud, conforming to Jitter Tolerance Mask defined by the "IEEE802.3bs Jitter Tolerance Mask". The following masks are taken as typical values:



Modulation Frequency (Hz)	Jitter Tolerance Mask (UIp-p)
40 000	22
4 000 000	0.22
250 000 000	0.22

*10: Loopback connection to the MU196020A, PRBS31Q, specified at a constant temperature between 20 and 30 °C.

Table 1.3.3.3-15 General

Item	Specifications
Dimensions	21 mm (H), 234 mm (W), 175 mm (D), Excluding protrusions
Mass	2.5 kg max.
Operating temperature	15 to 30 °C MP1900A's ambient temperature. MU196040B shall operate when installed.
Storage temperature	–20 to 60 °C MU196040B installed to MP1900A shall comply with MIL-T-28800E Class 5.

Table 1.3.3.3-16 Extended Functions

Item	Specifications
PCIe	Supports the following PCIe tests when controlled by the MX183000A. The supported installer versions are: ● MX190000A V10.00.00 or later ● MX183000A V10.00.00 or later
Applicable Standards	PCI Express Base Specification Revision 4.0 Version1.0 PCI Express Base Specification Revision 5.0 Version1.0 PCI Express Base Specification Revision 6.0 Version1.0 Bit rate: PCIe1/2/3/4/5/6 Number of lanes: x1 Subjects of Testing: Root Complex, End Point
Required Options	Option x41 (Required for PCIe6)
Required Software	MX183000A-PL021: Can support negotiation with the DUT and can put the DUT into Loopback state according to the LTSSM of PCIe1 to PCIe4. State transition of LTSSM can be analyzed as a log.(One MU196020A and one MU195040A/MU196040B are required.) MX183000A-PL025: Can extend the functionality of the PL021 option to PCIe5. MX183000A-PL026: Can extend the functionality of the PL021 and PL025 options to PCIe 6. (One MU196020A and one MU196040B are required.) When the MX183000A-PL001 is installed in addition to the MX183000A-PL021, MX183000A-PL025, and MX183000A-PL026, the MX183000A can control the MU196020A, MU181500B, and MU195040A/MU196040B and support Jitter Tolerance Test.

1.3.4 Noise Generator

1.3.4.1 Specifications for MU195050A

Table 1.3.4.1-1 Operating Bit Rate

Item	Specifications
Operating bit rate	2.4 to 32.1 Gbit/s

Table 1.3.4.1-2 Data Input

Item	Specifications
Number of channels	2
Number of inputs per channel	2 (Data, XData) (Differential)
Amplitude	1.5 Vp-p max. (Single-ended) 3.0 Vp-p max. (Differential)
Offset	–2.0 to 3.3 V
Termination	50 Ω
Connector	K (f.)

Table 1.3.4.1-3 Data Output*1

Item	Specifications
Number of channels	2
Number of outputs per channel	2 (Data, XData) (Differential)
Insertion loss	–3 dB +1/–2.5 dB*2
Termination	50 Ω
Connector	K (f.)

*1: The signal that is output from the noise source is AC-coupled.

*2: Defined for 12.890625 GHz and sine wave.

Table 1.3.4.1-4 External Input*1

Item	Specifications
Number of channels	1*2
Number of inputs per channel	2 (Differential)
Amplitude	1.5 Vp-p max. (Single-ended) 3.0 Vp-p max. (Differential)
Output control	Only Data Input 1 Channel can be turned On and Off. Either "DMI/CMI", "White noise", or "External Input" is selectable for Data Input 1 Channel. Either "DMI/CMI" or "White noise" can be selected for Data Input 2 Channel.
Termination	50 Ω, AC coupling
Connector	SMA Connector (f.)

*1: For connecting to the Gating Output signal of MU195020A.

*2: Data Input 1 Channel only

Table 1.3.4.1-5 Differential Mode Interference (DMI)*1

Item	Specifications
Amplitude	0 to 200 mVp-p (Differential)*2
Amplitude setting step	0.1 mV
Amplitude accuracy	±20 %±10mV*3
Frequency	2 to 10 GHz
Frequency setting step	10 MHz
Waveform	Sine wave
Presets	PCIe3, PCIe4, PCIe5, PCIe6
Output control	Capability of switching ON/OFF of Data Input 1 Channel and Data Input 2 Channel simultaneously. Either "DMI/CMI", "White noise", or "External Input" is selectable for Data Input 1 Channel. Either "DMI/CMI" or "White noise" can be selected for Data Input 2 Channel. DMI and CMI can be added simultaneously.

*1: The setting is common for Data Input 1 and Data Input 2.

*2: The setting range is available from 0 mVp-p, but accuracy is guaranteed from 4 mVp-p.

*3: Defined at certain temperature between 20 to 30 °C for 2.1 GHz, 4.2 GHz, 10 GHz.

Table 1.3.4.1-6 Common Mode Interference (CMI)*1

Item	Specifications
Amplitude	0 to 250 mVp-p (Single-ended)*2
Amplitude setting step	2 mV
Amplitude accuracy	±20 %±25mV*3
Frequency	Low Band: 100 MHz to 1 GHz High Band: 1 to 6 GHz
Frequency setting step	Low Band: 1 MHz High Band: 10 MHz
Waveform	Sine wave
Presets	TBT3, PCIe4, PCIe5, PCIe6
Output control	Capability of switching ON/OFF of Data Input 1 Channel and Data Input 2 Channel simultaneously. Either “DMI/CMI”, “White noise”, or “External Input” is selectable for Data Input 1 Channel. Either “DMI/CMI” or “White noise” can be selected for Data Input 2 Channel. DMI and CMI can be added simultaneously.

*1: The setting is common for Data Input 1 and Data Input 2.

*2: The setting range is available from 0 mVp-p, but accuracy is guaranteed from 10 mVp-p.

*3: Defined at certain temperature between 20 to 30 °C for 120 MHz, 400 MHz, 1 GHz, 6 GHz.

Table 1.3.4.1-7 White Noise*1

Item	Specifications
Flatness	±5 dB (10 MHz to 10 GHz)
Crest factor	> 5 (p-p/rms)
Amplitude	0.2 to 25 mV rms
Amplitude setting step	0.2 mV rms
Amplitude accuracy	±20 %±2.5 mV rms*2
Output control	Capability of switching ON/OFF of Data Input 1 Channel and Data Input 2 Channel simultaneously. Either "DMI/CMI", "White noise", or "External Input" is selectable for Data Input 1 Channel. Either "DMI/CMI" or "White noise" can be selected for Data Input 2 Channel.

*1: The setting is common for Data Input 1 and Data Input 2.

*2: Defined at one specific temperature between 20 to 30 °C, subtracting the residual noise value from the data by sampling oscilloscope with 50 GHz bandwidth.

Table 1.3.4.1-8 General

Item	Specifications
Dimensions	21 mm (H), 234 mm (W), 175 mm (D), Excluding protrusions
Mass	1.2 kg max.
Operating temperature	15 to 35 °C*
Storage temperature	–20 to 60 °C

*: Ambient temperature around equipment when installed in MP1900A.

1.3.4.2 Specifications for MU196050B

Table 1.3.4.2-1 Noise Output

Item	Specifications
Number of channels	1
Number of outputs per channel	2 (Differential)
Termination	50 Ω, AC coupled
Connector	SMA connector (J.)

Table 1.3.4.2-2 External Input*

Item	Specifications
Number of channels	1
Number of inputs per channel	2 (Differential)
Input amplitude	1.5 Vp-p max. (Single-ended) 3.0 Vp-p max. (Differential)
Output control	ON/OFF switching supported (DMI/CMI and External Input are mutually exclusive.)
Termination	50 Ω, AC coupling
Connector	SMA Connector (J.)

*: For USB LFPS signal input

Table 1.3.4.2-3 Differential Mode Interference (DMI)*1

Item	Specifications
Amplitude	0 to 200 mVp-p (Differential)*2
Amplitude setting step	0.1 mV
Amplitude accuracy	±20 %±10 mV*3
Frequency	2 to 10 GHz
Frequency setting step	10 MHz
Waveform	Sine wave
Presets	PCIe3, PCIe 4, PCIe5, PCIe6, PCIe7
Output control	ON/OFF switching supported (DMI/CMI and External Input are mutually exclusive.) (DMI and CMI can be added simultaneously.)

*1: The measurement point is defined at the end of the connection where a J1948A coaxial cable (0.4 m, SMA connector) and a J1793A Pick-Off Tee (pick-off path) are connected to the Noise Output, and the OUT port of the J1793A is connected to a 34VKF50A and a J1821A coaxial cable (0.8 m, K connector).

*2: Defined with CMI set to ON, 0 mV, and 120 MHz.

*3: Defined at amplitudes of 200 mV, 100 mV, 4 mV, and 0 mV, at a single temperature between 20 and 30 °C.

Table 1.3.4.2-4 Common Mode Interference (CMI)*1

Item	Specifications
Amplitude	0 to 250 mVp-p (Single-ended) *2
Amplitude setting step	2 mV
Amplitude accuracy	±20 %±25 mV*3
Frequency	Low Band: 100 MHz to 1 GHz High Band: 1 to 6 GHz
Frequency setting step	Low Band: 1 MHz High Band: 10 MHz
Waveform	Sine wave
Presets	TBT3, PCIe4, PCIe5, PCIe6, PCIe7
Output control	ON/OFF switching supported (DMI/CMI and External Input are mutually exclusive.) (DMI and CMI can be added simultaneously.)

*1: The measurement point is defined at the end of the connection where a J1948A coaxial cable (0.4 m, SMA connector) and a J1793A Pick-Off Tee (pick-off path) are connected to the Noise Output, and the OUT port of the J1793A is connected to a 34VKF50A and a J1821A coaxial cable (0.8 m, K connector).

*2: Defined with DMI set to ON, 0 mV, and 2.1 GHz.

*3: Defined at amplitudes of 250 mV, 120 mV, 10 mV, and 0 mV, at a single temperature between 20 and 30 °C.

Table 1.3.4.2-5 General

Item	Specifications
Dimensions	21 mm (H), 234 mm (W), 175 mm (D), Excluding protrusions
Mass	1.0 kg max.
Operating temperature	15 to 35 °C*
Storage temperature	–20 to 60 °C

*: Ambient temperature around equipment when installed in MP1900A.

1.3.5 Re-Driver

1.3.5.1 Specifications for MU196060A

Target Applications

PCIe 1.0 to 6.0 Link Training
PCIe 4.0: 16.0 Gbit/s, NRZ
PCIe 5.0: 32.0 Gbit/s, NRZ
PCIe 6.0: 32.0 Gbaud, PAM4
IEEE802.3bs 400GAUI-8 C2M: 26.5625 Gbaud, PAM4

Supported Plug-in Modules

MU196040B PAM4 ED
MU195040A 21G/32G bit/s SI ED

Table 1.3.5.1-1 Data Input

Item	Specifications
Number of inputs	2 (Data, XData) (Differential)
Operating Baud Rate	Same baud rate range as target application
Amplitude*1	
Absolute maximum input amplitude	Max. 1.4 Vp-p/Differential Max. 1.0 Vp-p/Single-ended ±1.0 VDC / Single-ended
Recommended Loopback Input amplitude	
PAM4 BERT	PAM4: 0.40 to 0.8 Vp-p / Differential*2, *3 Typ. BER 1E-12 BER < 1E-8 NRZ: 0.18 to 0.8 Vp-p / Differential*3 BER < 1E-12 At a given temperature between 20 and 30°C
SI BERT	NRZ: 0.18 to 0.8 Vp-p / Differential*4 BER < 1E-12 At a given temperature between 20 and 30°C
Termination	50 Ω, AC Coupling with DC termination
Connector	V connector (f.)

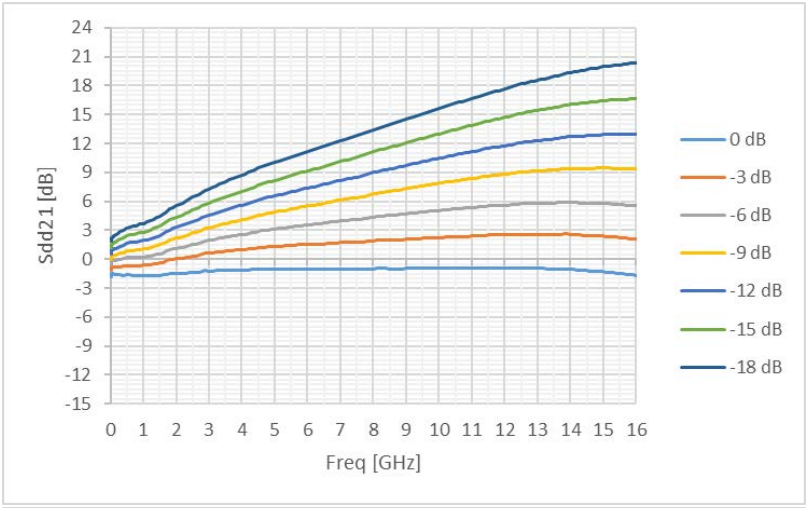
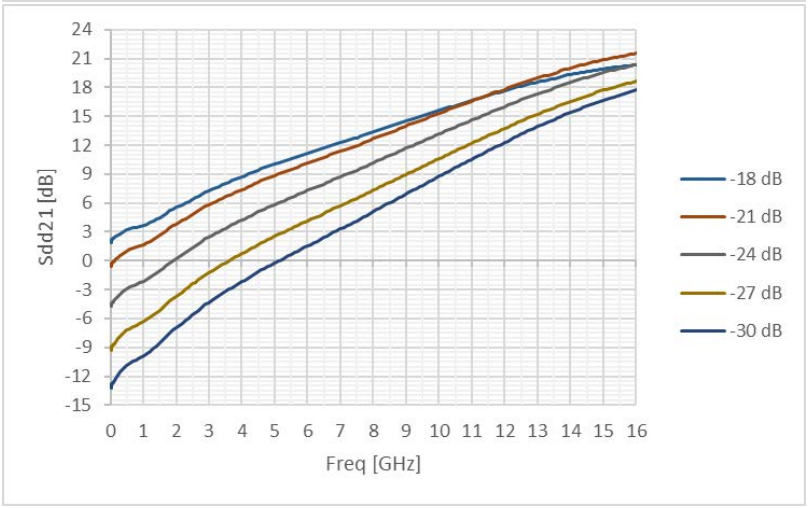
*1: Defined within the Operating Baud Rate range under the conditions that No Stress waveform is input and Equalizer is turned OFF.

*2: 32.0 Gbaud PAM4, 16.0, 32.0 Gbit/s NRZ, Differential, Modified Compliance Pattern, MU196020A + MU195050A + J1790A, MU196060A Clock Recovery, SSC 5300 ppm Down spread

*3: 19.0 to 32.1 Gbaud PAM4/NRZ, Differential, PRBS31, MU196020A + MU195050A + J1790A, MU196060A Clock Recovery, SSC OFF

*4: 16.0, 32.0 Gbit/s, Differential, Modified Compliance Pattern, MU196020A + MU195050A + J1790A, MU196060A Clock Recovery, SSC 5300 ppm Down spread, Loss Channel Emulator ON

Table 1.3.5.1-2 Equalizer

Item	Specifications
Ideal frequency response	 
Loss Compensation	(Design value) NRZ: 30 dB at 16 GHz*1 Compensation value satisfying BER < 1E–12 with respect to PCIe 5.0-compliant loss PAM4: 14 dB at 16 GHz*2 Compensation value satisfying BER < 1E-6 (Typ. BER 1E-9) with respect to PCIe 5.0-compliant loss 10 dB at 13.3 GHz *3 Compensation value satisfying BER < 1E-9 (Typ. BER 1E-11) with respect to loss in PRBS31 pattern

*1: 32.0 Gbit/s, 0.8 Vp-p Differential, Modified Compliance Pattern, 33 kHz 5300 ppm Down spread SSC

*2: 32.0 Gbaud, 0.8 Vp-p Differential, Modified Compliance Pattern, 33 kHz 5300 ppm Down spread SSC

*3: 26.5625 Gbaud 0.8 Vp-p Differential, PRBS31, SSC OFF

Table 1.3.5.1-2 Equalizer (Cont'd)

Item	Specifications
Setting Range	–30.0 to 0.0 dB
Setting Step	0.1 dB
Accuracy	±2.5 dB*4
CTLE ON/OFF	ON/OFF switching available

*4: EQ = Set value. Defined by the difference between 16 GHz and 10 MHz and in the range of –29.0 to 0.0 dB. Temperature fluctuation after setting is defined to be within ±2.5 °C.

Table 1.3.5.1-3 Data Output

Item	Specifications
Number of Outputs	2 (Data, XData) (Differential)
Operating Baud Rate	Same as the input data baud rate
Amplitude	Max 0.7 Vp-p/Single-Ended*1 Max 1.4 Vp-p/Differential*1
ON/OFF	ON/OFF switching available*3
Termination	50 Ω, AC Coupling
Connector	V connector (f.)
System skew	Typ. ±3 ps*2

*1: It shall not exceed the absolute rated input amplitude of the MU196040B PAM4 ED or MU195040A 21G/32G bit/s SI ED.

*2: J1932A included.

*3: Synchronized to Clock Output.

Table 1.3.5.1-4 Clock Output

Item	Specifications
Number of Outputs	1 (Single-Ended)
Frequency	1.25 GHz, 2.5 GHz, 4 GHz (MX183000A PCIe Link Training only) 8 GHz, 9.5 to 16.05 GHz (Half rate clock) *1
Amplitude	0.3 to 1.0 Vp-p (Fixed)*2
ON/OFF	ON/OFF switching available*5
Jitter	Typ. 700 fs rms (16.0 Gbit/s, NRZ)*3, *4 Typ. 600 fs rms (32.0 Gbit/s, NRZ)*3, *4 Typ. 650 fs rms (32.0 Gbaud, PAM4)*3, *4
Termination	50 Ω, GND
Connector	SMA connector (f.)

*1: Only 16 GHz is supported when connected with the MU195040A 21G/32G bit/s SI ED.

*2: Defined assuming that J1917A is used with a sampling oscilloscope band of 40 GHz.

*3: Input conditions:
PRBS31, Mark Ratio 1/2 (in PAM4 mode, MSB Mark Ratio),
MU196020A + MU195050A + J1790A
0.8 Vp-p/Differential Input

*4: Measurement conditions:
Measure for 10 s with a 40-GHz bandwidth sampling oscilloscope with residual jitter of less than 200 fs (RMS).

*5: Synchronized to Data Output.

Table 1.3.5.1-5 Clock Recovery

Item	Specifications*1
Operating Baud Rate	2.5 Gbit/s, 5 Gbit/s, 8 Gbit/s for NRZ (MX183000A PCIe Link Training only) 16 Gbaud, 19.0 Gbaud to 32.1 Gbaud for NRZ and PAM4
Setting Range	Same as the operating baud rate
Setting Step	1 kbaud step or 1 kbit/s step
PPG Operating baud rate tracking	Tracks the operating baud rate of the PPG selected from the PPGs installed in the same MP1900A. It is provided with an indicator that turns on when the PPG's operating baud rate is out of the tracking range.
Data pattern	PRBS pattern, Mark ratio 1/2 (in PAM4 mode, MSB Mark Ratio) Only PCIe specification data rates support PCIe Training Sequence Pattern, PCIe Compliance Pattern, and PCIe Modified Compliance Pattern.

*1: With Option x01

Table 1.3.5.1-5 Clock Recovery (Cont'd)

<table>
<tr><th>Item</th><th>Specifications*1</th></tr>
<tr><td>Maximum number of consecutive zeros

Lock range
SSC tolerance
Jitter tolerance
NRZ input</td><td>72 bits
Defined under the conditions that Coding is NRZ and Zero-Substitution is 2^{15}.
±300 ppm*2
PCI Express Gen 4.0, 5.0, and 6.0 compliant *3
When loopback-connected to MU196020A + MU196040B:

32.0 Gbit/s
SSC 33 kHz, 5300 ppm, conforming to Jitter Tolerance Mask defined by the “PCIe 5.0 Jitter Tolerance Mask”. The following masks are taken as typical values:
<table>
<tr><th>Modulation frequency (Hz)</th><th>JTOL Mask (UIp-p)</th></tr>
<tr><td>400 000</td><td>15.77</td></tr>
<tr><td>1 000 000</td><td>3.00</td></tr>
<tr><td>20 000 000</td><td>0.10</td></tr>
<tr><td>100 000 000</td><td>0.10</td></tr>
</table>
16.0 Gbit/s
SSC 33 kHz, 5300 ppm, conforming to Jitter Tolerance Mask defined by the “PCIe 4.0 Jitter Tolerance Mask”. The following masks are taken as typical values:
<table>
<tr><th>Modulation frequency (Hz)</th><th>JTOL Mask (UIp-p)</th></tr>
<tr><td>400 000</td><td>3.54</td></tr>
<tr><td>1 000 000</td><td>1.00</td></tr>
<tr><td>20 000 000</td><td>0.10</td></tr>
<tr><td>100 000 000</td><td>0.10</td></tr>
</table></td></tr>
</table>

*2: PRBS pattern, Mark ratio 1/2 (in PAM4 mode, MSB Mark Ratio), PCIe Compliance Pattern, Modified Compliance Pattern, and Training Sequence Pattern

*3: 16 Gbit/s, 32 Gbit/s, 32 Gbaud

When loopback-connected to MU196020A and MU196040B, and Data pattern (PCIe Compliance Pattern, Modified Compliance Pattern, or Training Sequence Pattern)

Table 1.3.5.1-5 Clock Recovery (Cont'd)

<table>
<tr><th>Item</th><th>Specifications*1</th></tr>
<tr><td>Jitter tolerance (Cont'd)
PAM4 input</td><td>32.0 Gbaud
SSC 33 kHz, 5300 ppm, conforming to Jitter Tolerance Mask defined by the "PCIe 6.0 Jitter Tolerance Mask". The following masks are taken as typical values:
<table>
<tr><th>Modulation frequency (Hz)</th><th>JTOL Mask (UIp-p)</th></tr>
<tr><td>400 000</td><td>12.47</td></tr>
<tr><td>1 000 000</td><td>2.00</td></tr>
<tr><td>10 000 000</td><td>0.05</td></tr>
<tr><td>100 000 000</td><td>0.05</td></tr>
</table>
26.5625 Gbaud
conforming to Jitter Tolerance Mask defined by the "IEEE802.3bs Jitter Tolerance Mask". The following masks are taken as typical values:
<table>
<tr><th>Modulation frequency (Hz)</th><th>JTOL Mask (UIp-p)</th></tr>
<tr><td>40 000</td><td>22.00</td></tr>
<tr><td>4 000 000</td><td>0.22</td></tr>
<tr><td>100 000 000</td><td>0.22</td></tr>
</table></td></tr>
</table>

Table 1.3.5.1-6 General

Item	Specifications
Dimensions	21 mm (H), 234 mm (W), 175 mm (D) For one Compact-PCI slot, excluding protrusions
Mass	1.0 kg max.
Operating Temperature	15 to 35 °C MP1900A's ambient temperature.
Storage Temperature	–20 to 60 °C

Chapter 2 Before Use

This chapter describes preparations required before using the MP1900A modules.

2.1 Installation to MP1900A 2-2
2.2 How to Operate Application 2-2
2.3 Preventing Damage 2-3

2.1 Installation to MP1900A

For information on how to install the MP1900A modules to the MP1900A and how to turn on the power, refer to Chapter 3 “Preparation before Use” in the *MP1900A Signal Quality Analyzer-R Operation Manual*.

2.2 How to Operate Application

The modules connected to the MP1900A are controlled by operating the MX190000A Signal Quality Analyzer-R Control Software (hereinafter, referred to as “MX190000A”).

For information on how to start up, shut down, and operate the MX190000A, refer to the *MX190000A Signal Quality Analyzer-R Control Software Operation Manual.*

2.3 Preventing Damage

Always observe the ratings when connecting to the input and output connectors of the MP1900A modules. If an out-of-range signal is input, the MP1900A modules may be damaged.

⚠ CAUTION

- **When signals are input to the MP1900A modules, avoid excessive voltage beyond the rating. Otherwise, the circuit may be damaged.**
- **When output is used at the 50 Ω GND terminator, never feed any current or input signals to the output.**
- **As a countermeasure against static electricity, ground other devices to be connected (including experimental circuits) with ground wires before connecting the I/O connector.**
- **The outer conductor and core of the coaxial cable may become charged as a capacitor. Use any metal to discharge the outer conductor and core before use.**
- **Never open the MP1900A modules. If you open it and MP1900A modules have failed or sufficient performance cannot be obtained, we may decline to repair the MP1900A modules.**
- **The MP1900A modules have many important circuits and parts including hybrid ICs. These parts are extremely sensitive to static electric charges, so never open the case of the MP1900A modules.**
- **The hybrid ICs used in the MP1900A modules are sealed in airtight containers; never open them. If you open it and the MP1900A modules have failed or sufficient performance cannot be obtained, we may decline to repair the MP1900A.**

⚠ CAUTION

- **To protect the MP1900A modules from electrostatic discharge failure, a conductive sheet should be placed onto the workbench, and the operator should wear an electrostatic discharge wrist strap. Always ground the wrist strap to the workbench antistatic mat or the frame ground of the MP1900A modules.**

- **When connecting an external device such as a Bias-T to the output connectors of MP1900A modules, if the output signal includes any DC voltage, variations in the output of the DC power supply or load may change the level of the output signal, risking damage to the internal circuits.**

  - **Do not connect or disconnect any external devices while DC voltage is impressed.**

  - **Only switch DC power sources ON and OFF when all equipment connections have been completed.**

  <Recommended procedure>

  Measurement Preparation 1:

  1. **Connect all equipment.**
  2. **Set the DC power supply output to ON.**
  3. **Set the MP1900A modules output to ON and complete measurement.**

  Measurement Preparation 2

  1. **Set the equipment output to OFF.**
  2. **Set the DC power supply output to OFF.**
  3. **Disconnect the MP1900A modules, or change the DUT connections.**

  Since even unforeseen fluctuations in DC voltage and load (open or short circuits at the MP1900A modules output side and changes caused by using a high-frequency probe, etc.,) can damage the DUT and equipment, we recommend connecting a 50–ohm resistance in series with the DC terminal of the Bias-T to prevent risk of damage.

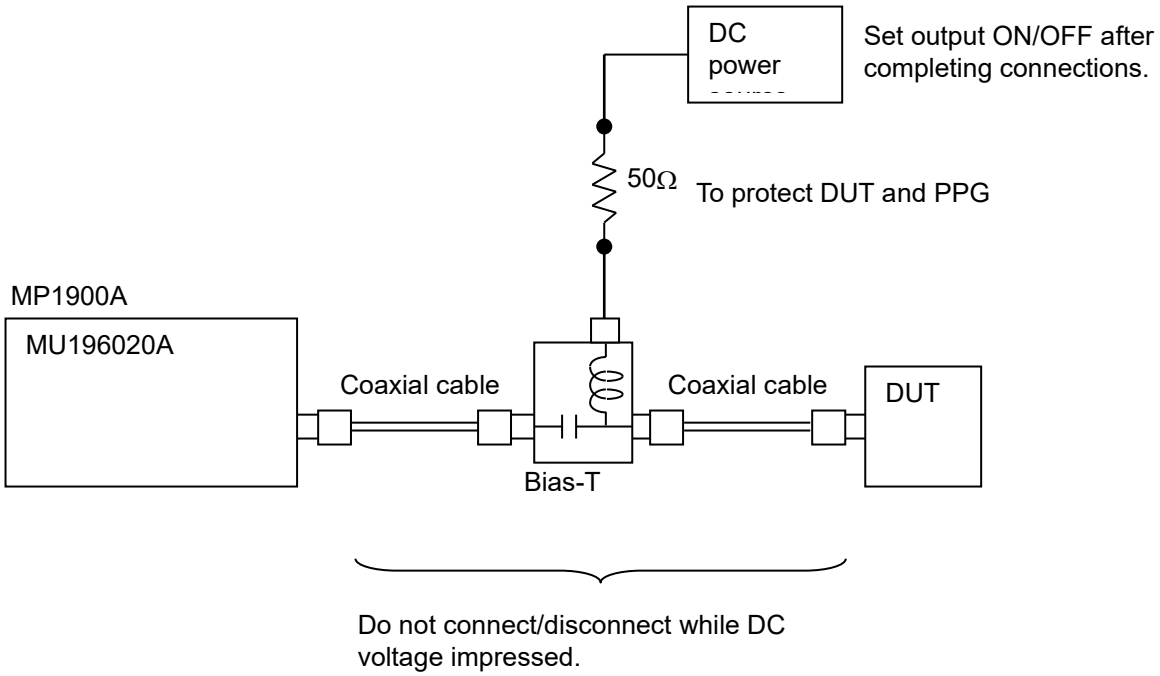


Figure 2.3-1 Bias-T Connection Example

Chapter 3 Panel Layout and Connectors

This chapter describes the panel and connectors of the MP1900A modules.

3.1 Panel Layout 3-2
3.1.1 Synthesizer 3-2
3.1.2 PPG 3-3
3.1.3 ED 3-6
3.1.4 Noise Generator 3-9
3.1.5 Re-Driver 3-11
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3.1 Panel Layout

3.1.1 Synthesizer

3.1.1.1 MU191000A

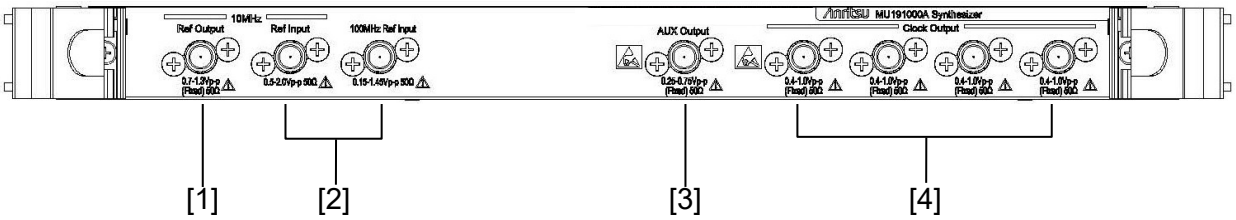


Figure 3.1.1.1-1 Panel Layout (MU191000A)

Table 3.1.1.1-1 Connectors on Panel

No.	Name	Description
[1]	10 MHz Ref. Output	Connector to output 10 MHz reference clock.
[2]	10 MHz Ref. Input, 100 MHz Ref. Input	Connector to input 10 MHz/100 MHz reference clock. Clock output of the MU191000A is synchronized with the clock input from this connector.
[3]	AUX Output	Outputs auxiliary signals. Connector to output a clock signal generated within the MU191000A.
[4]	Clock Output (100 MHz to 16.05 GHz)	Connector to output a clock signal generated within the MU191000A.

3.1.2 PPG

3.1.2.1 MU195020A

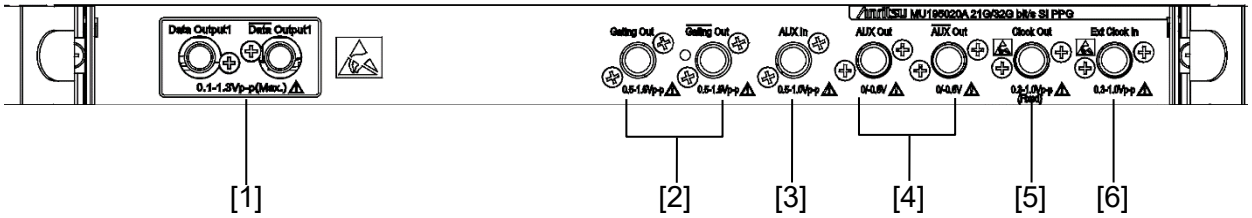


Figure 3.1.2.1-1 Panel Layout (MU195020A-x10)

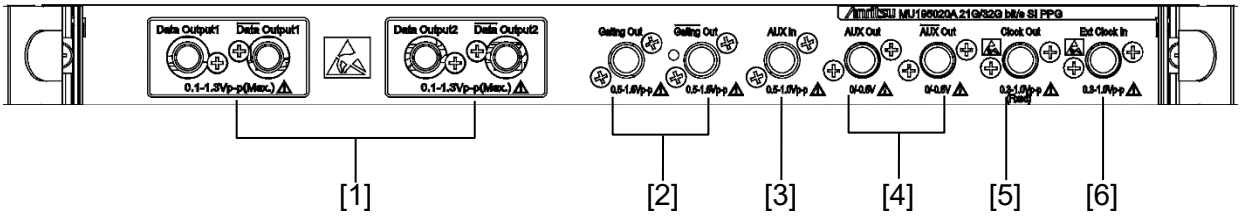


Figure 3.1.2.1-2 Panel Layout (MU195020A-x20)

Table 3.1.2.1-1 Connectors on Panel

No.	Name	Description
[1]	Data Output, $\overline{\text{Data}}$ Output	Outputs the differential data signals. Various interface signals can be output, depending on the installed option (s).
[2]	Gating Out, $\overline{\text{Gating}}$ Out	In case of Repeat: Outputs the timing signals. In case of Burst: Outputs the timing signals for Burst.
[3]	AUX In	Inputs auxiliary signals. Error Injection, and Burst can be selected.
[4]	AUX Out, $\overline{\text{AUX}}$ Out	Outputs auxiliary signals. 1/N clock, Pattern Sync, and Burst2 signals can be output according to the setting. Because of differential output, be sure to terminate the unused connector with the coaxial terminator (J1632A).
[5]	Clock Out	Outputs clock signals.
[6]	Ext Clock In	Inputs clock signals from these units: MU181000A 12.5GHz Synthesizer MU181000B 12.5GHz 4 Port Synthesizer MU191000A Synthesizer MU181500B Jitter Modulation Source External Synthesizer*

*: We recommend using the MG3690C series as an external synthesizer.

For details about the MG3690C series, contact Anritsu or our sales representative.

3.1.2.2 MU196020A

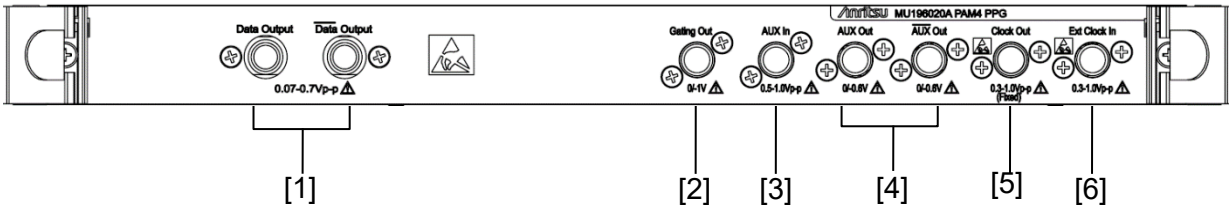


Figure 3.1.2.2-1 Panel Layout (MU196020A)

Table 3.1.2.2-1 Connectors on Panel

No.	Name	Description
[1]	Data Output, $\overline{\text{Data}}$ Output	Outputs differential Data and $\overline{\text{Data}}$ signals. Various interface signals can be output, depending on the installed option (s). Because of differential output, be sure to terminate the unused connector with the coaxial terminator.
[2]	Gating Out	In case of Repeat: Outputs the timing signals. In case of Burst: Outputs the timing signals for Burst.
[3]	AUX In	Inputs auxiliary signals. Variation: Error Injection, Burst
[4]	AUX Out, $\overline{\text{AUX}}$ Out	Outputs auxiliary signals. Variation: 1/N Clock, Pattern Sync, Burst Output2 Because of differential output, be sure to terminate the unused connector with the coaxial terminator (J1632A).
[5]	Clock Out	Outputs clock signals.
[6]	Ext Clock In	Inputs clock signals from these units: MU181000A 12.5GHz Synthesizer MU181000B 12.5GHz 4 Port Synthesizer MU191000A Synthesizer MU181500B Jitter Modulation Source External Synthesizer*

*: We recommend using the MG3690C series as an external synthesizer.

For details about the MG3690C series, contact Anritsu or our sales representative.

3.1.2.3 MU196020C

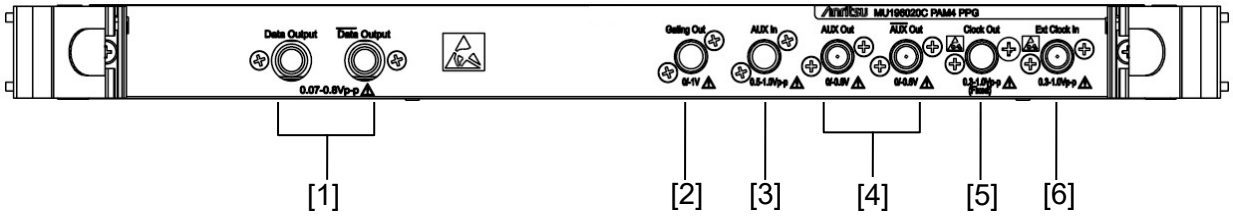


Figure 3.1.2.3-1 Panel Layout (MU196020C)

Table 3.1.2.3-1 Connectors on Panel

No.	Name	Description
[1]	Data Output, $\overline{\text{Data}}$ Output	Outputs differential Data and $\overline{\text{Data}}$ signals. Various interface signals can be output, depending on the installed option (s). Because of differential output, be sure to terminate the unused connector with the coaxial terminator.
[2]	Gating Out	In case of Repeat: Outputs the timing signals. In case of Burst: Outputs the timing signals for Burst.
[3]	AUX In	Inputs auxiliary signals. Variation: Error Injection, Burst
[4]	AUX Out, $\overline{\text{AUX}}$ Out	Outputs auxiliary signals. Variation: 1/N Clock, Pattern Sync, Burst Output2 Because of differential output, be sure to terminate the unused connector with the coaxial terminator (J1632A).
[5]	Clock Out	Outputs clock signals.
[6]	Ext Clock In	Inputs clock signals from these units: MU181000A 12.5GHz Synthesizer MU181000B 12.5GHz 4 Port Synthesizer MU191000A Synthesizer MU181500B Jitter Modulation Source External Synthesizer*

*: We recommend using the MG3690C series as an external synthesizer.

For details about the MG3690C series, contact Anritsu or our sales representative.

3.1.3 ED

3.1.3.1 MU195040A

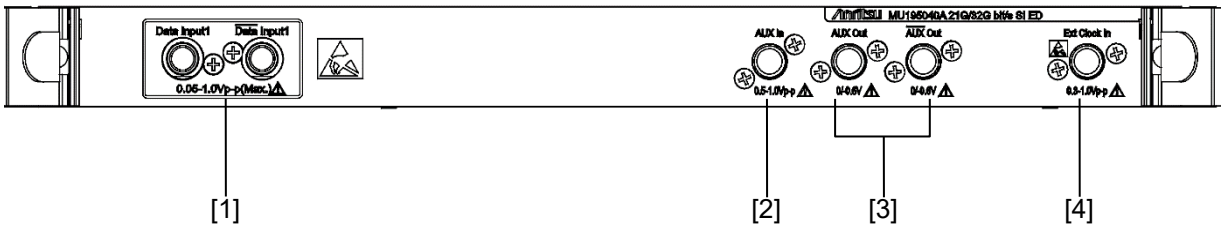


Figure 3.1.3.1-1 Panel Layout (MU195040A-x10)

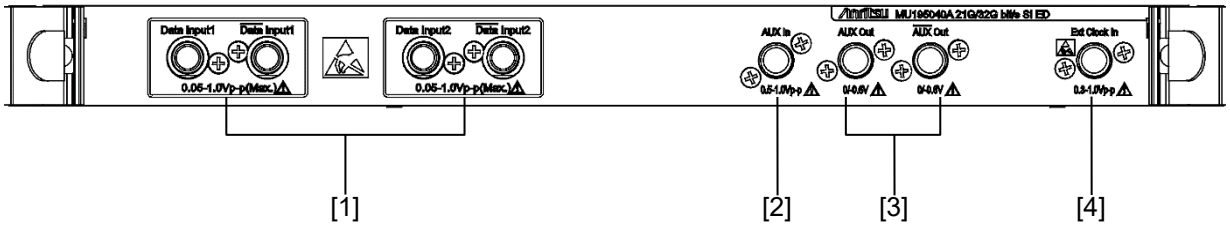


Figure 3.1.3.1-2 Panel Layout (MU195040A-x20)

Table 3.1.3.1-1 Connectors on Panel

No.	Name	Description
[1]	Data Input, $\overline{\text{Data}}$ Input	Input Data, $\overline{\text{Data}}$ data signals. Support both differential and single-ended input signals. When the MU195040A-x22 Clock Recovery is installed, the clock is recovered from the signal input to the Data Input1 connector.
[2]	AUX In	Inputs auxiliary signals. External Mask, Burst, or Capture External Trigger can be selected.
[3]	AUX Out, $\overline{\text{AUX}}$ Out	Outputs auxiliary signals. 1/N Clock, Pattern Sync, Error, and Sync Gain output signals can be selected. Because of differential output, be sure to connect the coaxial terminator (J1632A) to unused side connector.
[4]	Ext Clock In	Inputs clock signals.

3.1.3.2 MU196040A

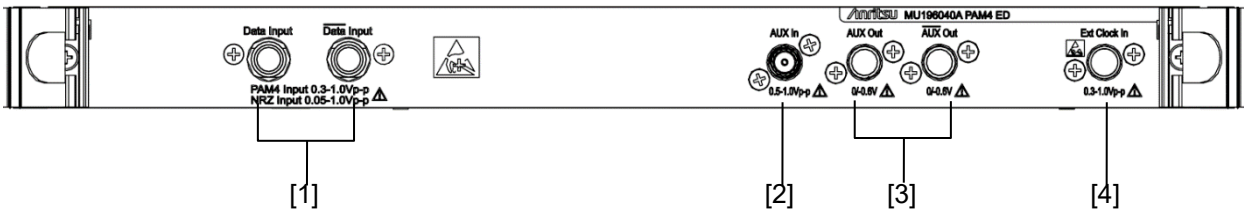


Figure 3.1.3.2-1 Panel Layout (MU196040A)

Table 3.1.3.2-1 Connectors on Panel

No.	Name	Description
[1]	Data Input, $\overline{\text{Data}}$ Input	Input Data, $\overline{\text{Data}}$ data signals. Support both differential and single-ended input signals.
[2]	AUX In	Inputs auxiliary signals. Variation: External Mask, Burst
[3]	AUX Out, $\overline{\text{AUX}}$ Out	Outputs auxiliary signals. Variation: 1/N Clock, Pattern Sync, Sync Gain, Error Output Because of differential output, be sure to connect the coaxial terminator (J1632A) to unused side connector.
[4]	Ext Clock In	Inputs clock signals. Mainly connected to the Clock Out connector on the PAM4 PPG.

3.1.3.3 MU196040B

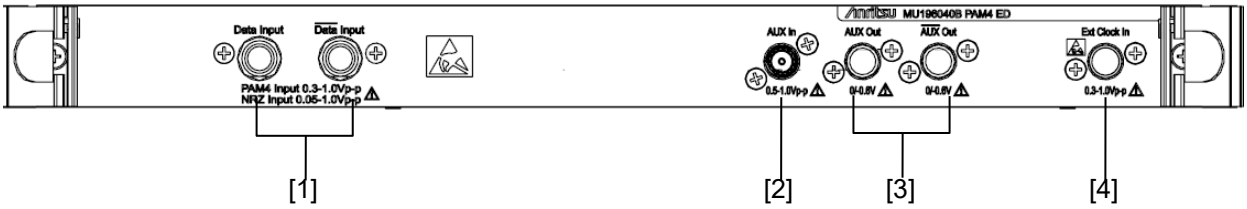


Figure 3.1.3.3-1 Panel Layout (MU196040B)

Table 3.1.3.3-1 Connectors on Panel

No.	Name	Description
[1]	Data Input, $\overline{\text{Data}}$ Input	Input Data, $\overline{\text{Data}}$ data signals. Support both differential and single-ended input signals. Be sure to terminate the unused connector with the coaxial terminator.
[2]	AUX In	Inputs auxiliary signals. Variation: External Mask, Burst, Capture External Trigger
[3]	AUX Out, $\overline{\text{AUX}}$ Out	Outputs auxiliary signals. Variation: 1/N Clock, Pattern Sync, Sync Gain, Error Output Because of differential output, be sure to connect the coaxial terminator (J1632A) to unused side connector.
[4]	Ext Clock In	Inputs clock signals. Mainly connected to the Clock Out connector on the PAM4 PPG.

3.1.4 Noise Generator

3.1.4.1 MU195050A

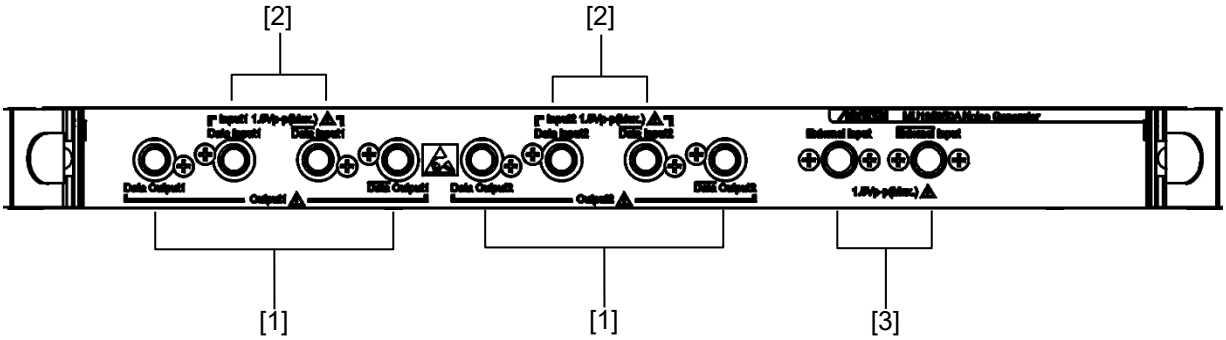


Figure 3.1.4.1-1 Panel Layout (MU195050A)

Table 3.1.4.1-1 Connectors on Panel

No.	Name	Description
[1]	Data Output, $\overline{\text{Data}}$ Output	Connectors to output differential Data and $\overline{\text{Data}}$ signals to which noise is added.
[2]	Data Input, $\overline{\text{Data}}$ Input	Connectors to input Data and $\overline{\text{Data}}$ signals to add noise. Support both differential and single-ended input signals.
[3]	External Input, $\overline{\text{External}}$ Input	Inputs auxiliary signals. They are used in connection with MU195020A Gating Output signal.

3.1.4.2 MU196050B

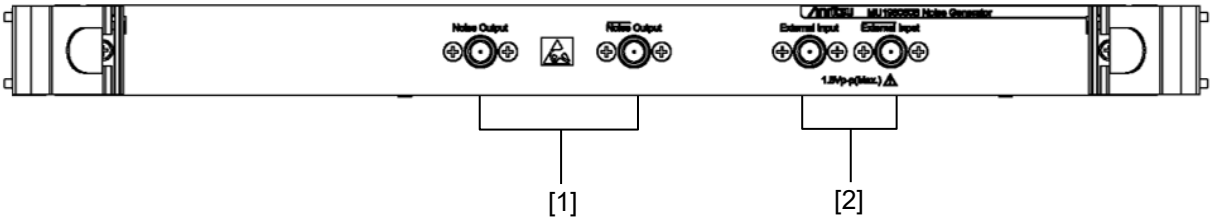


Figure 3.1.4.2-1 Panel Layout (MU196050B)

Table 3.1.4.2-1 Connectors on Panel

No.	Name	Description
[1]	Noise Output, Noise Output	These connectors output differential Noise and Noise signals for noise addition. Use these connectors with the Pick OFF Tee (J1793A) to add noise to the data signal.
[2]	External Input, External Input	Inputs auxiliary signals. They are used in connection with MU196020A/C Gating Output signal.

3.1.5 Re-Driver

3.1.5.1 MU196060A

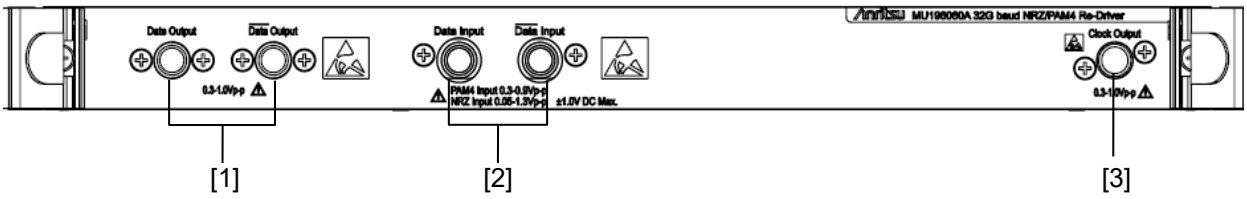


Figure 3.1.5.1-1 Panel Layout (MU196060A)

Table 3.1.5.1-1 Connectors on Panel

No.	Name	Description
[1]	Data Output, $\overline{\text{Data}}$ Output	Connectors for outputting Data and $\overline{\text{Data}}$ signals compensated by the built-in Equalizer. Be sure to use the J1932A included as standard for differentially connect to the Data Input and $\overline{\text{Data}}$ Input connectors of the MU195040A or MU196040B. Use the J1932A as well as the 34VKF50A when connecting the connectors to the MU195040A.
[2]	Data Input, $\overline{\text{Data}}$ Input	Input Data, $\overline{\text{Data}}$ data signals. Connect to the DUT differentially.
[3]	Clock Output	Connector for outputting clock signals recovered from the data signals input to the Data Input and $\overline{\text{Data}}$ Input. Be sure to use the J1917A included as standard to connect this connector to Ext Clock In of the MU196040B. Clock Output is available only when the MU196060A-x01 is installed. When the connector is not used, protect it by connecting the Open (J1341A) included as standard to it.

3.2 Inter-Module Connection

Avoid static electricity when handling the devices.

⚠ WARNING

- **When signals are input to this MP1900A modules, avoid excessive voltage beyond the rating. Otherwise, the circuit may be damaged.**
- **As a countermeasure against static electricity, ground other devices to be connected (including experimental circuits) with ground wires before connecting the I/O connector.**
- **The outer conductor and core of the coaxial cable may become charged as a capacitor. Use any metal to discharge the outer conductor and core before use.**
- **The power supply voltage rating for the MP1900A is shown on the rear panel. Be sure to operate the MP1900A within the rated voltage range. The MP1900A may be damaged if a voltage out of the rating range is applied.**
- **To protect the MP1900A modules from electrostatic discharge failure, a conductive sheet should be placed onto the workbench, and the operator should wear an electrostatic discharge wrist strap. Always ground the wrist strap to the workbench antistatic mat or the frame ground of the MP1900A.**
- **When removing a cable from a connector on the front panel of the MP1900A modules, be careful not to add excessive stress to the connector.**
  Addition of excessive stress to a connector may result in characteristic degradation or a failure. Use a torque wrench (recommended torque: 0.9 N-M) when attaching or removing a cable.

⚠ CAUTION

Note that the maximum output level of the Data Output connector of MU195020A-x10/x20 is "1.30 Vp-p" (1.50 Vp-p when Option x11/x21 is installed). Also, the data output level of MU195050A is decided by the data input level, and it is at maximum 1.50 Vp-p. The maximum data input level of MU195040A is 1.00 V.

When connecting the Data Output connector of MU195020A/MU195050A directly to the Data Input connector of MU195040A to verify operation, make sure that the data output level of MU195020A/MU195050A is 1 V or under.

Avoid inputting the signal exceeding the maximum input level to the Data Input connector of MU195040A. Failure to do so can cause damage.

⚠ CAUTION

The maximum data input level of MU196040A/B and MU196060A is 1.00 Vp-p.

When connecting the Data Output connector of MU195020A/MU183020A directly to the Data Input connector of MU196040A/B to verify operation,
make sure that the data output level of MU195020A and MU183020A is 1.00 Vp-p or under.

Avoid inputting the signal exceeding the maximum input level to the Data Input connector of MU196040A/B and MU196060A. Failure to do so can cause damage.

3.2.1 Measuring errors

3.2.1.1 Using the MU195020A/MU195040A

To perform error measurement, use the following modules:

- One of the following synthesizers: MU181000A (12.5GHz Synthesizer), MU181000B (12.5GHz 4port Synthesizer), MU191000A
- MU195020A
- MU195040A

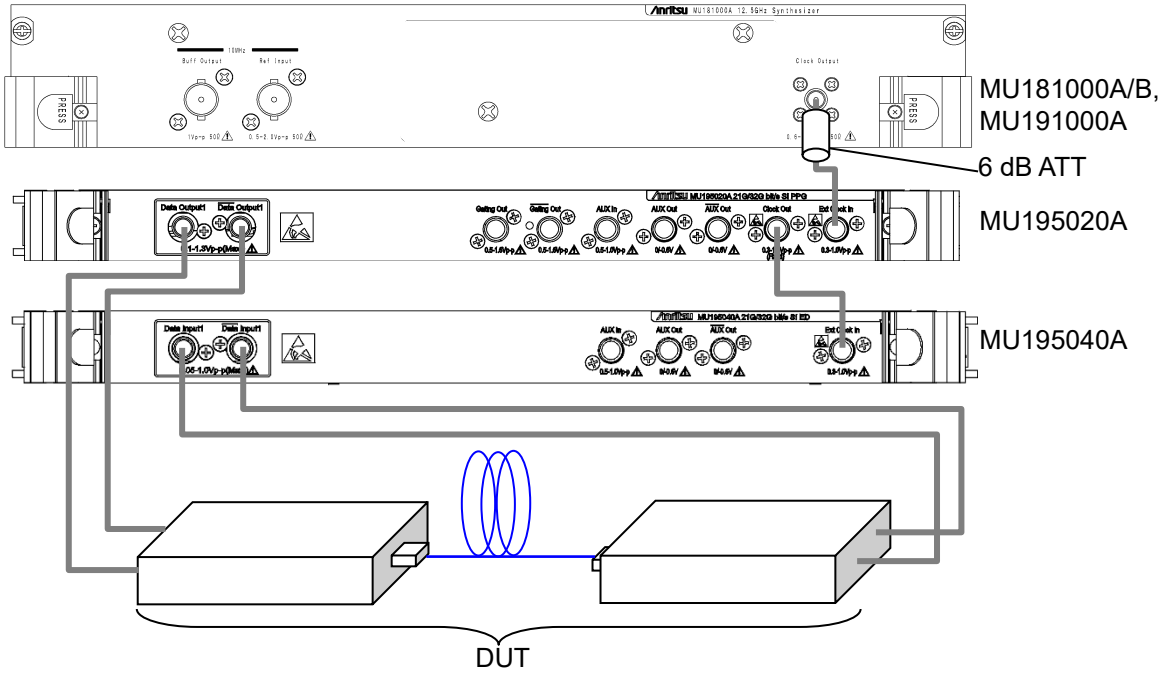


Figure 3.2.1.1-1 Inter-Module Connection Example

1. When using the MU181000A, attach the 6 dB fixed attenuator (ATT) to the Clock Output connector.
   The following module and options do not require the 6 dB fixed attenuator: MU181000A-x01, MU181000B, MU181000B-x01, MU191000A
2. Use a coaxial cable to connect the Clock Output connector on the MU181000B or MU191000A (or the ATT connector on the MU181000A) to the Ext Clock Input connector on the MU195020A (Clock Output/ATT → Ext Clock Input).
3. Use a coaxial cable to connect the Clock Output connector on the MU195020A to the Ext. Clock Input connector on the MU195040A.
4. Use a coaxial cable to connect the Data Output connector on the MU195020A to the Data Input connector on the device under test

(DUT). Also use a coaxial cable to connect the $\overline{\text{Data}}$ Output connector on the MU195020A to the $\overline{\text{Data}}$ Input connector on the DUT.

5. Use a coaxial cable to connect the Data Output connector on the DUT to the Data Input connector on the MU195040A. Also use a coaxial cable to connect the $\overline{\text{Data}}$ Output connector on the DUT to the $\overline{\text{Data}}$ Input connector on the MU195040A.
6. Start MX190000A and select **Initialize** from the **Menu** to initialize the entire system.
   Note that all the settings are initialized to the factory default settings by initialization. If necessary, select **Save** from the **Menu** to save the settings before initialization.

3.2.1.2 When MU196020A/C and MU196040A/B are used

To perform error measurement, use the following modules:

- One of the following synthesizers: MU181000A, MU181000B, MU191000A
- MU196020A/C
- MU196040A/B

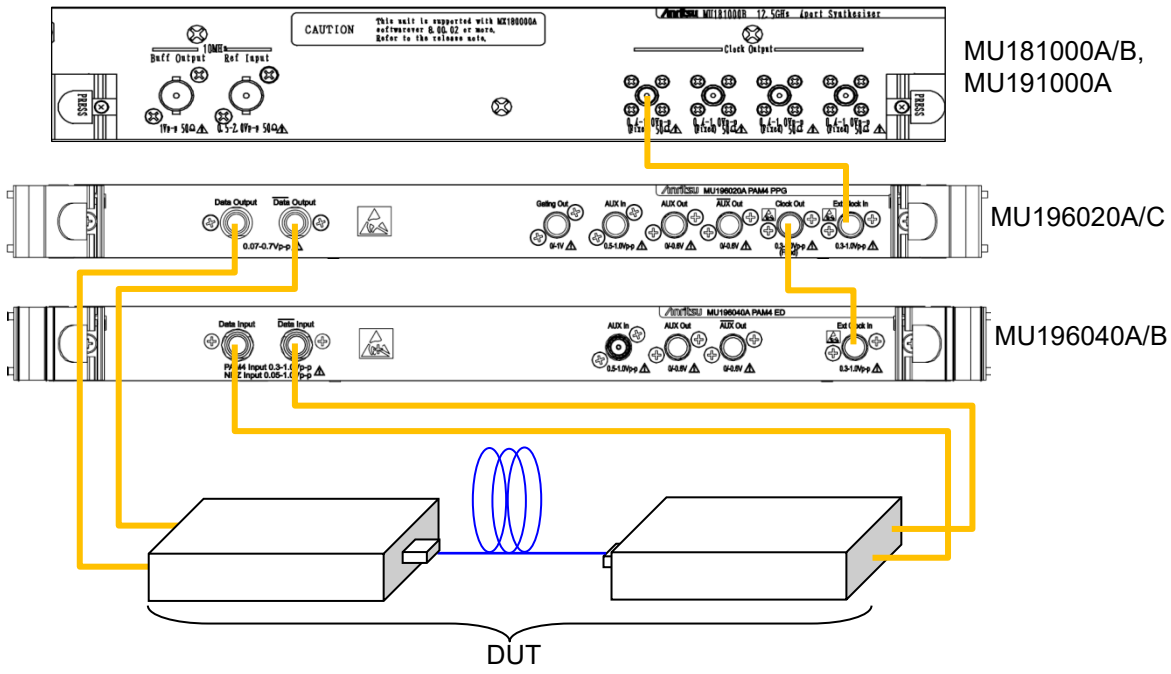


Figure 3.2.1.2-1 Inter-Module Connection Example

1. For the case of the MU181000A, attach the 6 dB fixed attenuator (ATT) to the Clock Output connector.
   The following module and options do not require the 6 dB fixed attenuator:

   MU181000A-x01, MU181000B, MU181000B-x01, MU191000A
2. Use a coaxial cable to connect the Clock Output connector on the MU181000B or MU191000A (or the ATT connector on the MU181000A) to the Ext Clock Input connector on the MU196020A/C (Clock Output/ATT → Ext Clock Input).
3. Use a coaxial cable to connect the Clock Output connector on the MU196020A to the Ext Clock Input connector on the MU196040A/B.
4. Use a coaxial cable to connect the Data Output connector on the MU196020A/C to the Data Input connector on the device under test (DUT). Also use a coaxial cable to connect the $\overline{\text{Data}}$ Output

connector on the MU196020A/C to the $\overline{\text{Data}}$ Input connector on the DUT.

5. Use a coaxial cable to connect the Data Output connector on the DUT to the Data Input connector on the MU196040A/B. Also use a coaxial cable to connect the $\overline{\text{Data}}$ Output connector on the DUT to the $\overline{\text{Data}}$ Input connector on the MU196040A/B.
6. Launch MX190000A, and touch **Standard BERT for PAM4** in the Application Selector screen.
   Configure the module settings including bit rate, pattern and amplitude.

3.2.2 Measuring errors with noise added

3.2.2.1 When MU195050A is used

When MU195020A and MU195040A are used

To perform error measurement while adding noise, use the following modules:

- One of the following synthesizers: MU181000A, MU181000B, MU191000A
- MU195020A
- MU195050A
- MU195040A

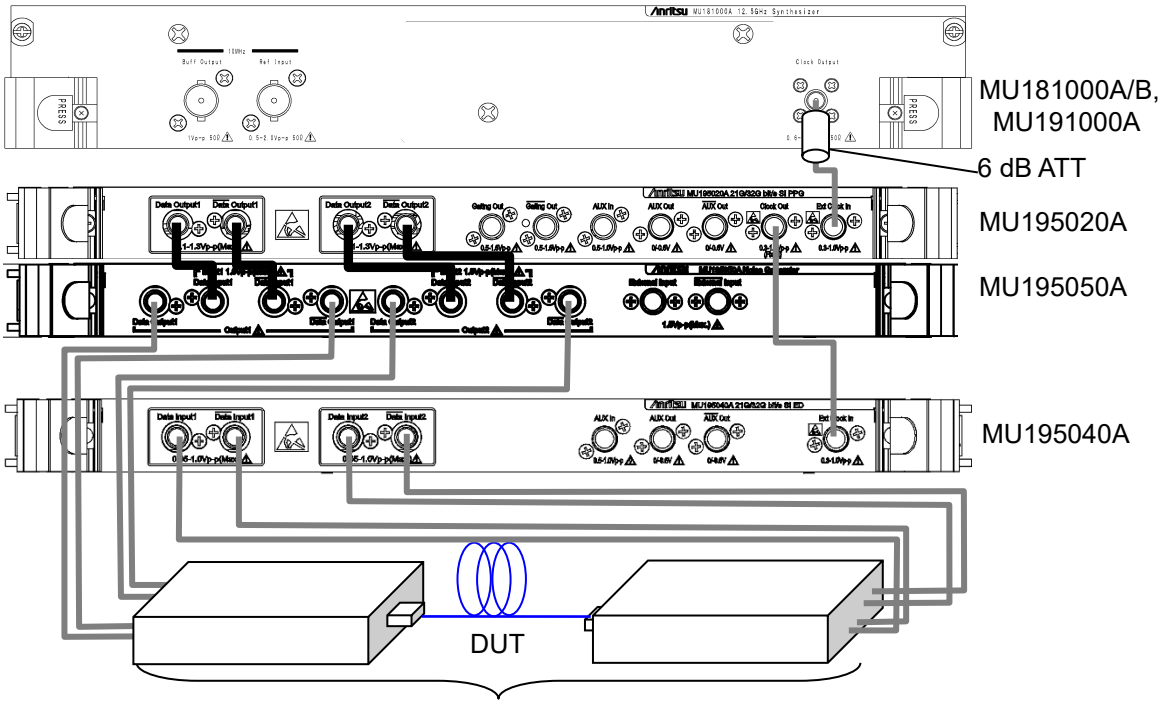


Figure 3.2.2.1-1 Inter-Module Connection Example

1. For the case of the MU181000A, attach the 6 dB fixed attenuator (ATT) to the Clock Output connector.
   The following module and options do not require the 6 dB fixed attenuator:

   MU181000A-x01, MU181000B, MU181000B-x01, MU191000A
2. Use a coaxial cable to connect the Clock Output connector on the MU181000B or MU191000A (or the ATT connector on the MU181000A) to the Ext Clock Input connector on the MU195020A (Clock Output/ATT → Ext Clock Input).
3. Connect the Data Output connector on the MU195020A to the Data Input connector on the MU195050A using a coaxial cable supplied

with MU195050A. Also use a coaxial cable (J1746A, J1747A) supplied with the MU195050A to connect the $\overline{\text{Data}}$ Output connector on the MU195020A to the $\overline{\text{Data}}$ Input connector on the MU195050A.

4. Use a coaxial cable to connect the Clock Output connector on the MU195020A to the Ext Clock Input connector on the MU195040A.
5. Use a coaxial cable to connect the Data Output connector on the MU195050A to the Data Input connector on the device under test (DUT). Also use a coaxial cable to connect the $\overline{\text{Data}}$ Output connector on the MU195050A to the $\overline{\text{Data}}$ Input connector on the DUT.
6. Use a coaxial cable to connect the Data Output connector on the DUT to the Data Input connector on the MU195040A. Also use a coaxial cable to connect the $\overline{\text{Data}}$ Output connector on the DUT to the $\overline{\text{Data}}$ Input connector on the MU195040A.
7. Start MX190000A and select **Initialize** from the **Menu** to initialize the entire system.
   Note that all the settings are initialized to the factory default settings by initialization. If necessary, select **Save** from the **Menu** to save the settings before initialization.

When MU196020A/C and MU196040A/B are used

To perform error measurement while adding noise, use the following modules:

- One of the following synthesizers: MU181000A, MU181000B, MU191000A
- MU181500B (Jitter Modulation Source)
- MU195050A
- MU196040A/B

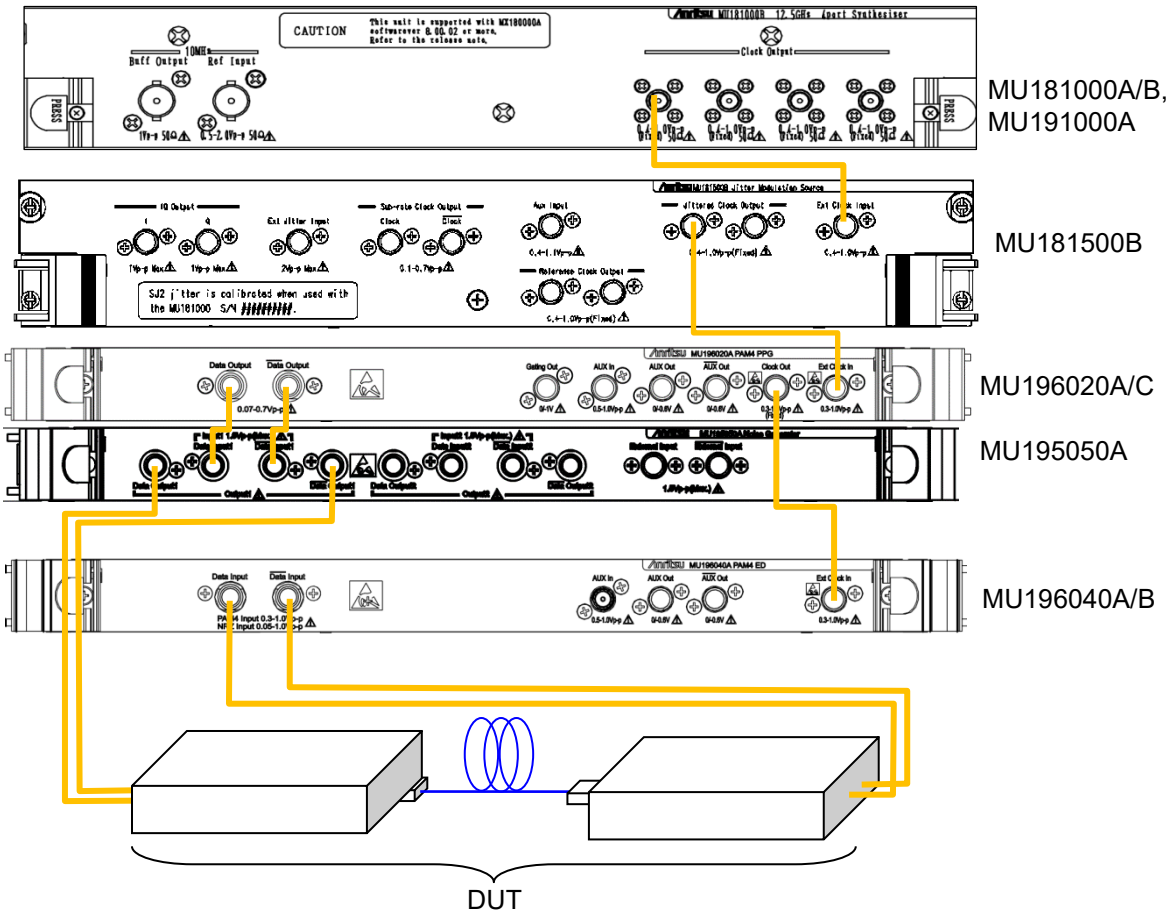


Figure 3.2.2.1-2 Inter-Module Connection Example

1. For the case of the MU181000A, attach the 6 dB fixed attenuator (ATT) to the Clock Output connector.
   The following module and options do not require the 6 dB fixed attenuator:

   MU181000A-x01, MU181000B, MU181000B-x01, MU191000A
2. Use a coaxial cable to connect the Clock Output connector on the MU181000B or MU191000A (or the ATT connector on the MU181000A) to the Ext Clock Input connector on the MU181500B (Clock Output/ATT → Ext Clock Input).
3. Use a coaxial cable to connect the Jittered Clock Output connector on the MU181500B to the Ext. Clock Input connector on the MU196020A/C.
4. Use the J1792A skew match pair semirigid cables (V-K connector, Data Input1) to connect the Data Output and $\overline{\text{Data}}$ $\overline{\text{Output}}$ connectors on the MU196020A/C to the Data Input and $\overline{\text{Data}}$ Input connectors on the MU195050A.
5. Use a coaxial cable to connect the Clock Output connector on the MU196020A/C to the Ext Clock In connector on the MU196040A/B.

6. Use a coaxial cable to connect the Data Output connector on the MU195050A to the Data Input connector on the device under test (DUT). Also use a coaxial cable to connect the $\overline{\text{Data}}$ Output connector on the MU195050A to the $\overline{\text{Data}}$ Input connector on the DUT.
7. Use a coaxial cable to connect the Data Output connector on the DUT to the Data Input connector on the MU196040A/B. Also use a coaxial cable to connect the $\overline{\text{Data}}$ Output connector on the DUT to the $\overline{\text{Data}}$ Input connector on the MU196040A/B.
8. Launch MX190000A, and touch **Standard BERT for PAM4** in the Application Selector screen.
   Configure the module settings including bit rate, pattern and amplitude.
9. On the **Output** tab of the MU196020A, set **Ext ATT Factor** to 3.3 dB (typ.) as the loss of the MU195050A.

3.2.2.2 When MU196050B is used

When MU196020A/C and MU196040A/B are used

To perform error measurement while adding noise, use the following modules:

- One of the following synthesizers: MU181000A, MU181000B, MU191000A
- MU196020A/C
- MU181500B
- MU196050B
- MU196040A/B

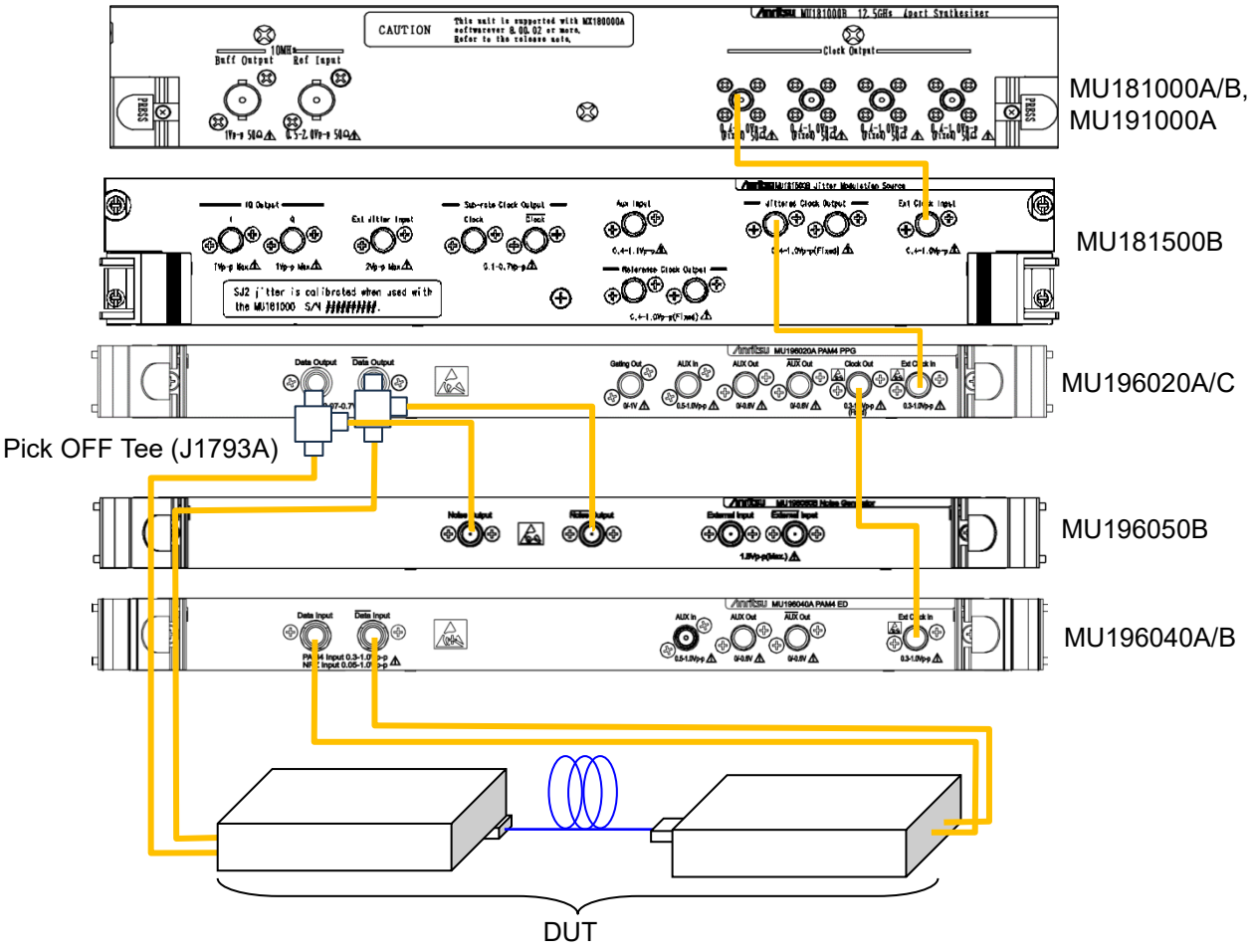


Figure 3.2.2.2-1 Inter-Module Connection Example

1. For the case of the MU181000A, attach the 6 dB fixed attenuator (ATT) to the Clock Output connector.
   The following module and options do not require the 6 dB fixed attenuator:
   MU181000A-x01, MU181000B, MU181000B-x01, MU191000A

2. Use a coaxial cable to connect the Clock Output connector on the MU181000B or MU191000A (or the ATT connector on the MU181000A) to the Ext Clock Input connector on the MU181500B (Clock Output/ATT → Ext Clock Input).
3. Use a coaxial cable to connect the Jittered Clock Output connector on the MU181500B to the Ext Clock Input connector on the MU196020A/C.
4. Attach the Pick OFF Tee (J1793A) to the Data Output and $\overline{\text{Data}}$ Output connectors on the MU196020A/C.
5. Use electrical-length-specified coaxial cables (J1948A) to connect the Pick OFF route from the Noise Output and $\overline{\text{Noise}}$ Output connectors on the MU196050B to the Pick OFF Tee (J1793A). Connect the straight connectors of J1948A to the MU196050B connectors and the right-angle connectors to J1793A.
6. Use coaxial cables to connect the output connectors on the Pick OFF Tee (J1793A) to the input connectors on the DUT, respectively.
7. Use a coaxial cable to connect the Data Output connector on the DUT to the Data Input connector on the MU196040A/B. Also use a coaxial cable to connect the $\overline{\text{Data}}$ Output connector on the DUT to the $\overline{\text{Data}}$ Input connector on the MU196040A/B.
8. Launch MX190000A, and touch **Standard BERT for PAM4** in the Application Selector screen.
   Configure the module settings including bit rate, pattern and amplitude.
9. On the Output tab of the MU196020A/C, set Ext ATT Factor to 3.3 dB (typ.) as the loss of the Pick OFF Tee (J1793A).

3.2.3 Adding jitter to output signal

3.2.3.1 Using the MU195020A/MU195040A

MU181000A or MU181000B (hereafter MU181000A/B) and MU181500B jitter modulation source (hereafter MU181500B) are used to add jitter to signal that is outputted from PPG.
Figure 3.2.3.1-1 shows a connection example of MU181000A, MU181500B, MU195020A, and MU195040A.

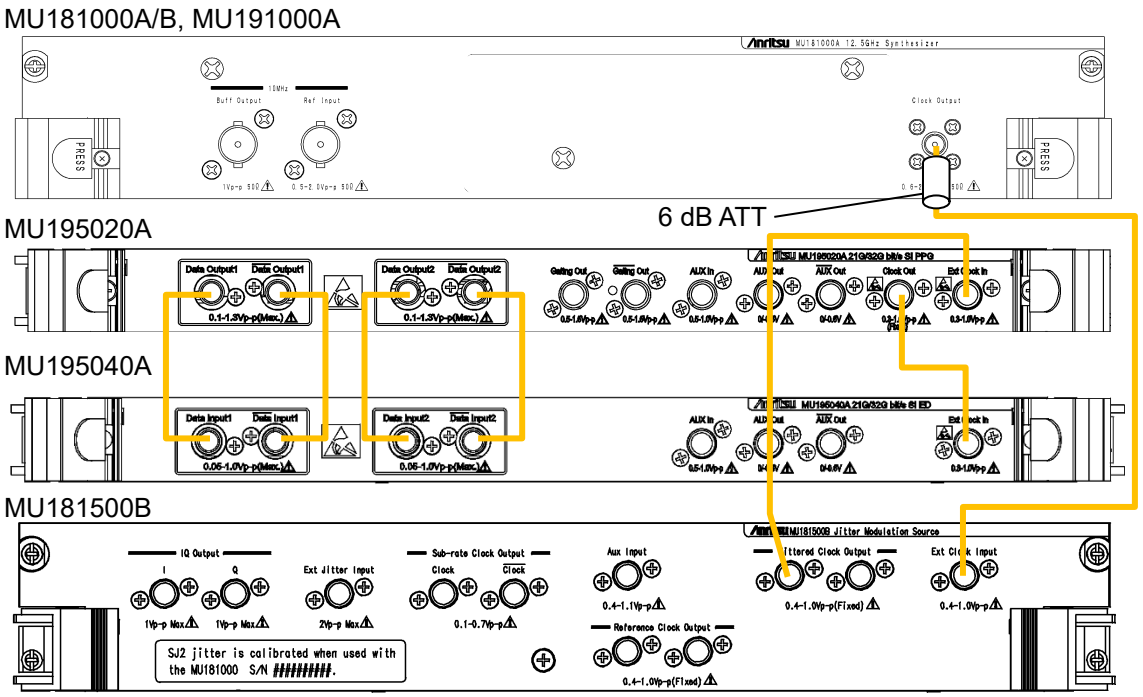


Figure 3.2.3.1-1 Connection Example When Adding Jitter to Output Signal

1. For the case of the MU181000A, attach the 6 dB fixed attenuator (ATT) to the Clock Output connector.
   The following module and options do not require the 6 dB fixed attenuator:
   MU181000A-x01, MU181000B, MU181000B-x01, MU191000A
2. Use a coaxial cable to connect the Clock Output connector on the MU181000B or MU191000A (or the ATT connector on the MU181000A) to the Ext Clock Input connector on the MU181500B (Clock Output/ATT → Ext Clock Input).
3. Use a coaxial cable to connect the Jittered Clock Output connector on the MU181500B to the Ext Clock Input connector on the MU195020A.
4. Use a coaxial cable to connect the Clock Output connector on the MU195020A to the Ext Clock Input connector on the MU195040A.

5. Use coaxial cables to connect Data Output and $\overline{\text{Data}}$ Output connectors of the MU195020A with Data Input and $\overline{\text{Data}}$ Input connectors of the MU195040A (2 connections).
6. Start MX190000A and select **Initialize** from the **Menu** to initialize the entire system.
   Note that all the settings are initialized to the factory default settings by initialization. If necessary, select **Save** from the **Menu** to save the settings before initialization.

3.2.3.2 When MU196020A/C and MU196040A/B are used

To add jitter to the PAM4 PPG output signal, use the following modules:

- One of the following synthesizers: MU181000A, MU181000B, MU191000A
- MU181500B
- MU196020A/C
- MU196040A/B

MU196040A/B-001 supports up to 32.1 Gbit/s and 32.1 Gbaud.

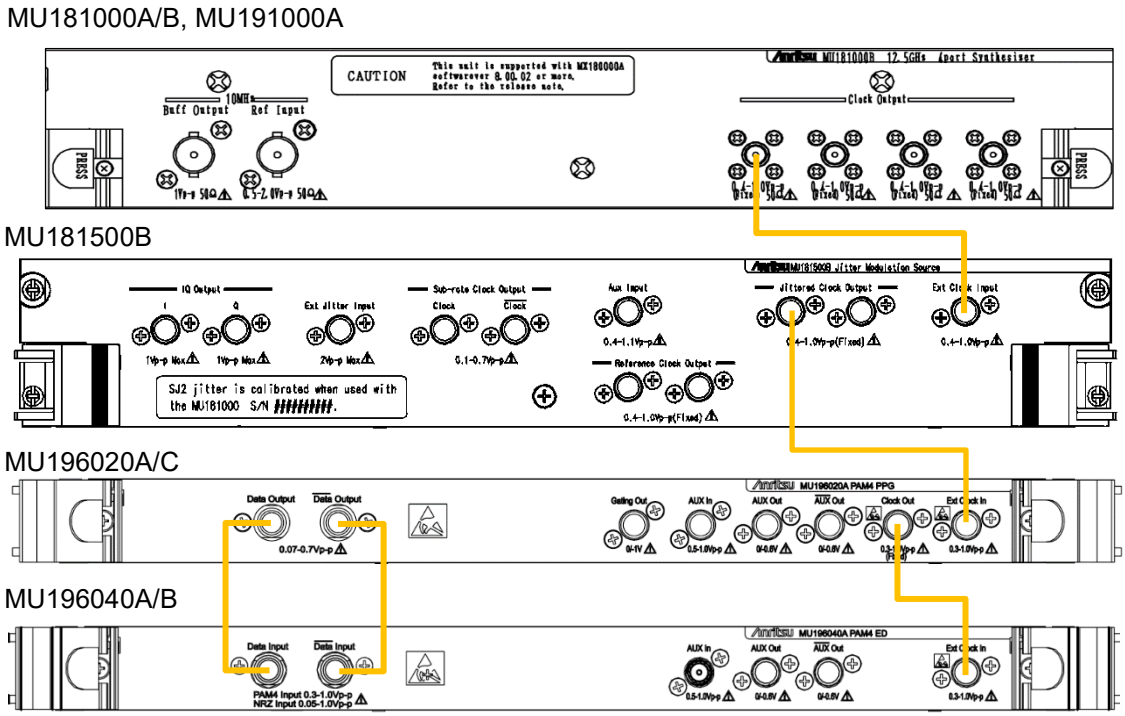


Figure 3.2.3.2-1 Connection Example When Adding Jitter to Output Signal

1. For the case of the MU181000A, attach the 6 dB fixed attenuator (ATT) to the Clock Output connector.

The following module and options do not require the 6 dB fixed attenuator:

MU181000A-x01, MU181000B, MU181000B-x01, MU191000A

2. Use a coaxial cable to connect the Clock Output connector on the MU181000B or MU191000A (or the ATT connector on the MU181000A) to the Ext Clock Input connector on the MU181500B (Clock Output/ATT → Ext Clock Input).
3. Use a coaxial cable to connect the Jittered Clock Output connector on the MU181500B to the Ext Clock Input connector on the MU196020A/C.
4. Use a coaxial cable to connect the Clock Output connector on the MU196020A/C to the Ext Clock Input connector on the MU196040A/B.
5. Use coaxial cables to connect the Data Output and $\overline{\text{Data}}$ Output connectors on the MU196020A/C to the Data Input and $\overline{\text{Data}}$ Input connectors on the MU196040A/B (2 connections).
6. Launch MX190000A, and touch **Standard BERT for PAM4** in the Application Selector screen.

   Configure the module settings including bit rate, pattern and amplitude.

3.2.4 Synchronizing multiple channels of PPG

3.2.4.1 When MU195020A is used

To synchronize multiple MU195020A modules installed in the same MP1900A, use MU181000A, MU181000B, MU191000A, or an external clock source as the clock source.

The following example shows the connection setup for synchronizing two MU195020A modules using MU181000A/B, MU191000A, or an external clock source.

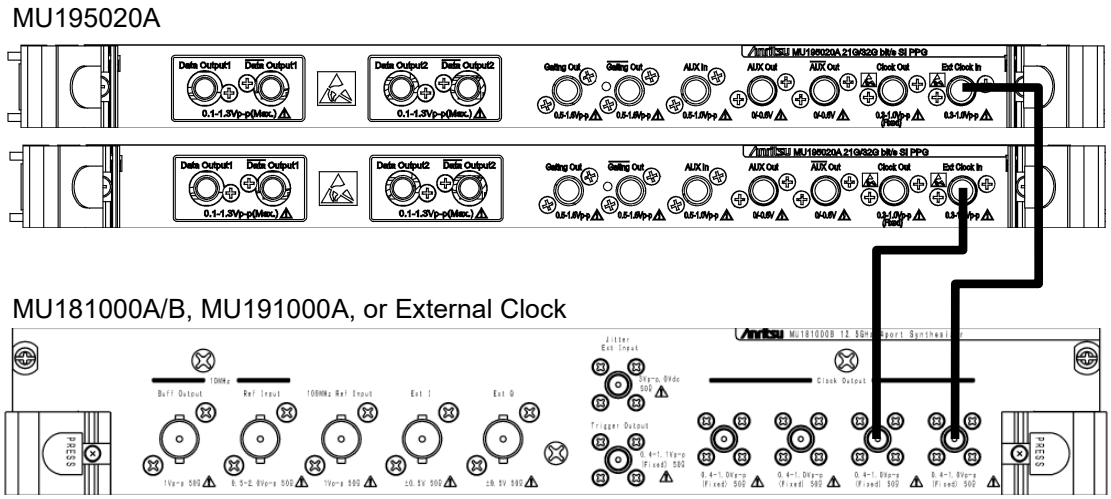


Figure 3.2.4.1-1 Connection Example for PPG Multi-Channel Synchronization

1. Use coaxial cables to connect the Clock Output connectors on the MU181000A/B, MU191000A, or an external clock source to the Ext Clock Input connector on each MU195020A module.
2. Start MX190000A and select **Menu** → **Combination Setting** on the menu bar. Set **Sync ON/OFF** of **Inter module Combination** to **Channel Synchronization**.

Notes:

- Insert units of MU195020A into slots in order from Slot 1.
- Make sure that the cable phase difference is 10 ps or under.

3.2.4.2 When MU196020A/C is used

To synchronize multiple MU196020A/C modules installed in the same MP1900A, use MU181000A, MU181000B, MU191000A, or an external clock source as the clock source.

The following example shows the connection setup for synchronizing two MU196020A/C modules using MU181000A/B, MU191000A, or an external clock source.

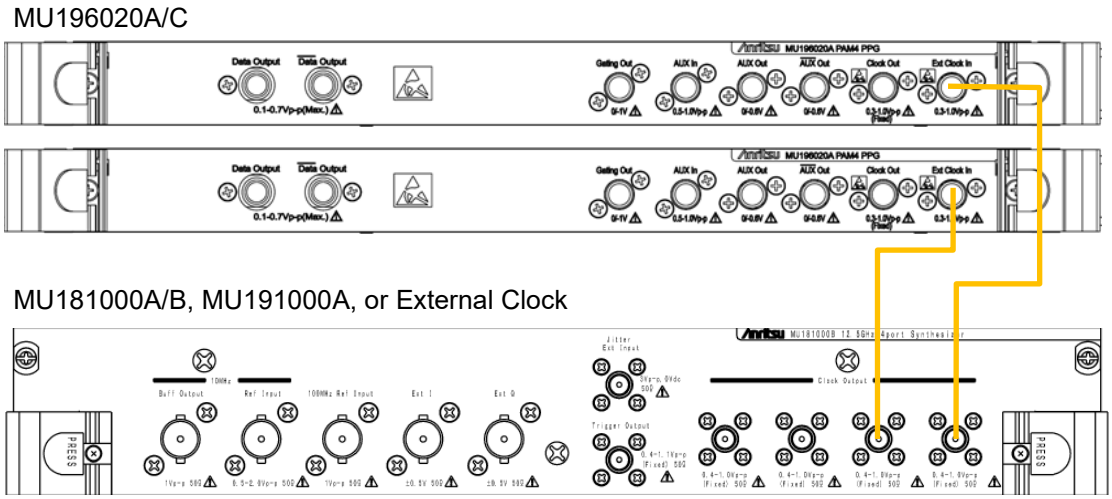


Figure 3.2.4.2-1 Connection Example When Synchronizing Two Units of PPGs

1. Use coaxial cables to connect the Clock Output connectors on the MU181000A/B, MU191000A, or an external clock source to the Ext Clock Input connector on each MU196020A/C module.
2. Start MX190000A and select **Menu** → **Combination Setting** on the menu bar. Set Sync ON/OFF of Inter module Combination to **Channel Synchronization**.

Notes:

- Insert units of MU196020A/C into slots in order from Slot 1.
- Ensure that the delay difference between the coaxial cables connecting to the MU196020A/C modules does not exceed 10 ps.

The following example shows the connection setup for synchronizing four MU196020A/C modules using MU181500B and one of the following external clock sources: MU181000A/B, MU191000A, or an external clock source.

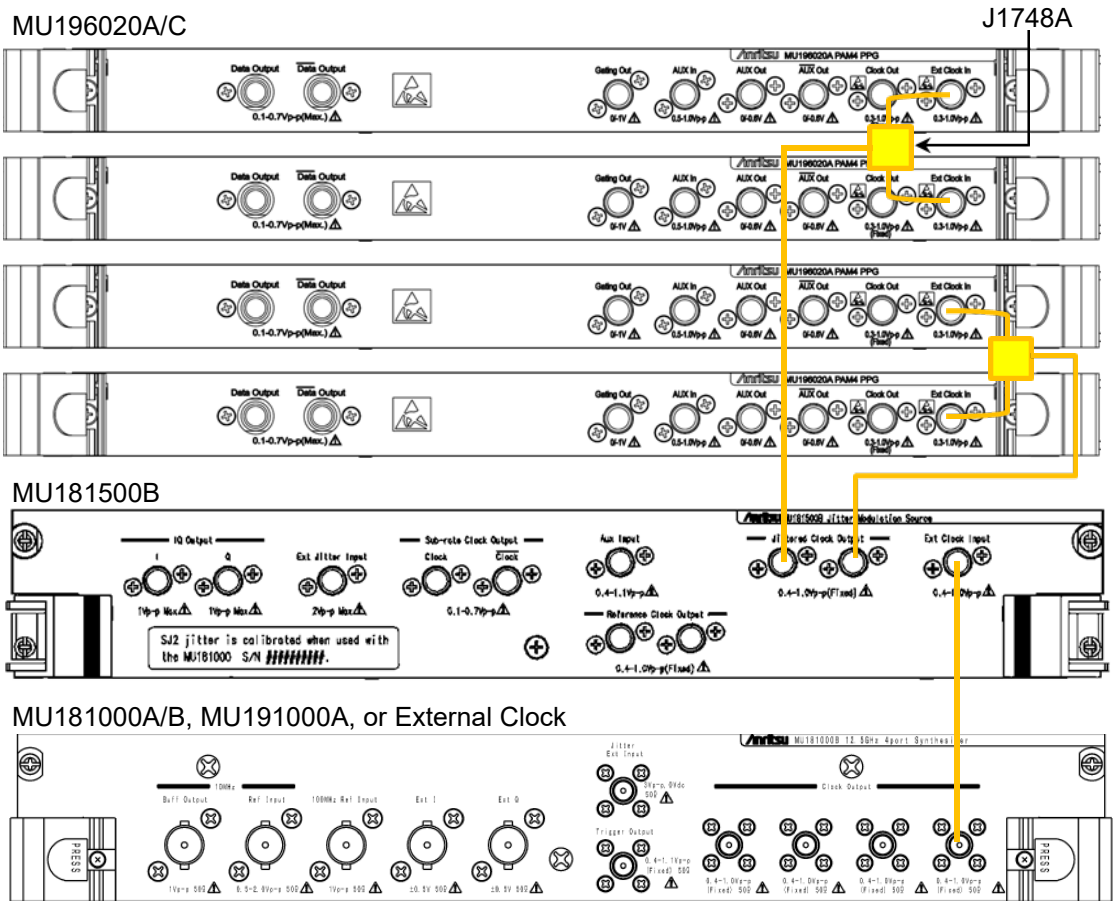


Figure 3.2.4.2-2 Connection Example When Synchronizing Four Units of PPGs

1. Use coaxial cables to connect the Clock Output connectors on the MU181000A/B, MU191000A, or an external clock source to the Ext Clock Input connector on each MU196020A/C module.
2. Use two coaxial cables to connect one Jittered Clock Output connecter on the MU181500B to the J1748A Power Splitter (1.5G-18GHz), which is an optional accessory, and the other Jittered Clock Output connector on the MU181500B to other J1748A.
3. Use four coaxial cables to connect two J1748As to the Ext Clock In connector on four MU196020A/Cs.
4. Start MX190000A and select **Menu** → **Combination Setting** on the menu bar. Set Sync ON/OFF of Inter module Combination to **Channel Synchronization**.

Notes:

- Insert units of MU196020A/C into slots in order from Slot 1.
- Ensure that the delay difference between the coaxial cables connecting the MU181500B to the MU196020A/C modules does not exceed 10 ps.

3.2.5 Measuring while compensating loss with Re-Driver

To perform error measurement while compensating loss using the Re-Driver, use the following modules:

- One of the following synthesizers: MU181000A, MU181000B, MU191000A
- MU196020A/C
- MU181500B
- MU195050A/MU196050B
- MU196040A/B
- MU196060A

Refer to 3.2.2 “Measuring errors with noise added” for details on how to connect the following modules:

- One of the following synthesizers: MU181000A, MU181000B, or MU191000A
- MU181500B
- MU196020A/C
- MU195050A

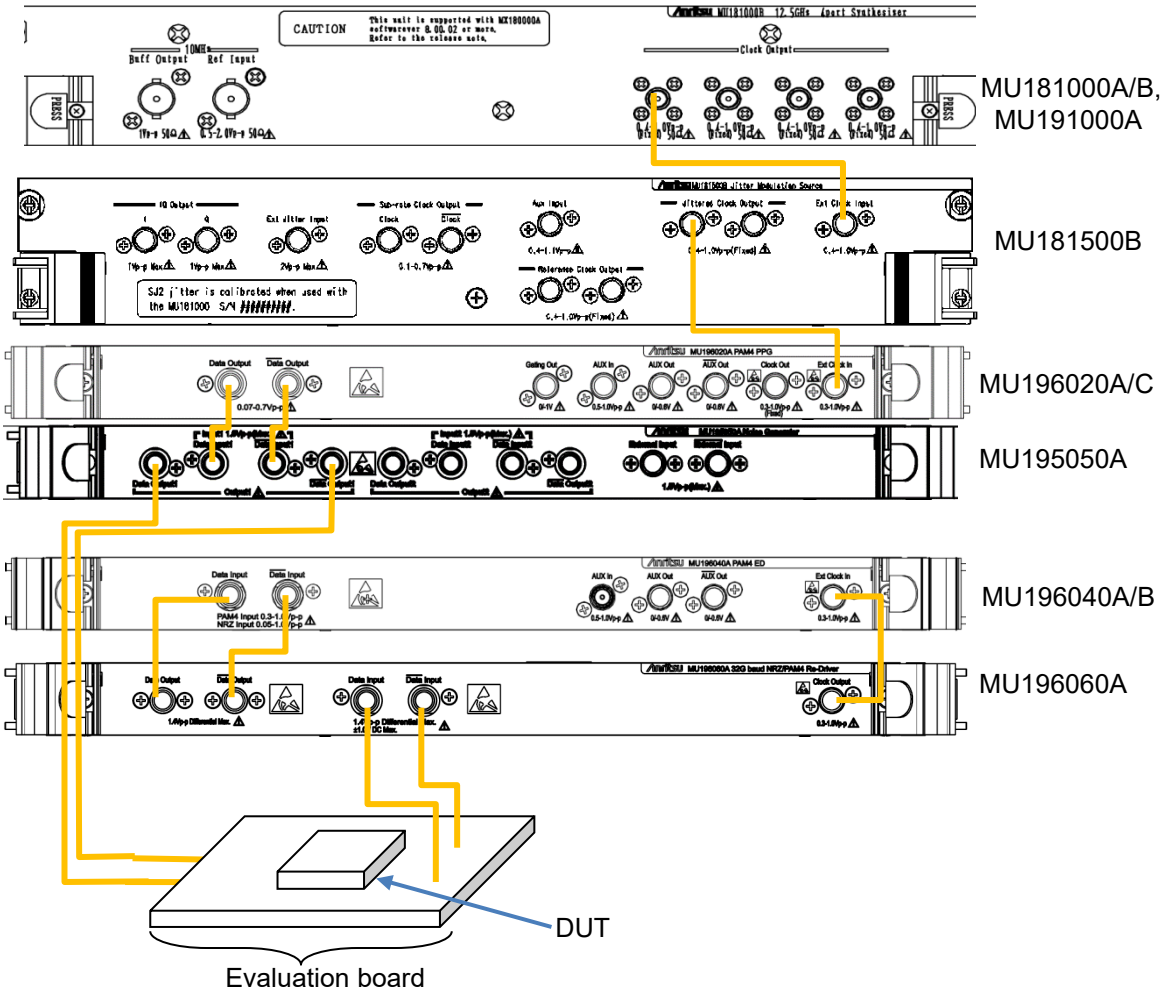


Figure 3.2.5-1 Inter-Module Connection Example (Noise Generator: MU195050A)

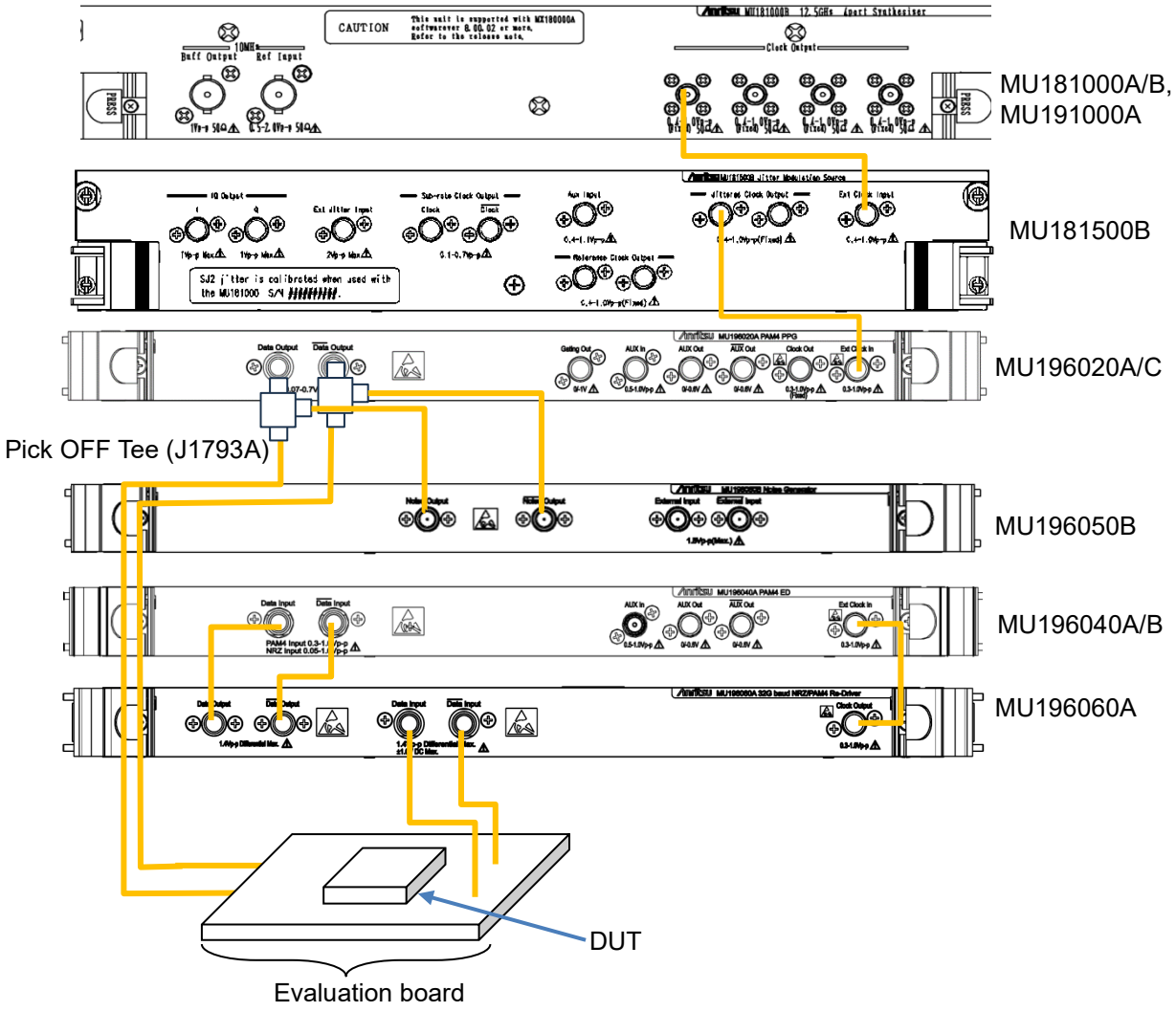


Figure 3.2.5-2 Inter-Module Connection Example (Noise Generator: MU196050B)

1. If the MU195050AMU195050A is used,
   use coaxial cables to connect the Data Output and $\overline{\text{Data}}$ Output connectors to the input connectors on the DUT.
2. If the MU196050B is used,
   2-1. Use electrical-length-specified coaxial cables (J1948A) to connect the Pick OFF route from the Noise Output and $\overline{\text{Noise}}$ Output connectors on the MU196050B to the Pick OFF Tee (J1793A). Connect the straight connectors of J1948A to the MU196050B connectors and the right-angle connectors to J1793A.
   2-2. Use coaxial cables to connect the output connectors on the Pick OFF Tee (J1793A) to the input connectors on the DUT, respectively.

3. Use the J1932A electrical length specified coaxial cables (0.8 m, V connector) to connect the Data Output and $\overline{\text{Data}}$ Output connectors on the MU196060A to the Data Input and $\overline{\text{Data}}$ Input connectors on the MU196040B.
4. Use the J1917A Coaxial Semi-rigid Cable to connect the Clock Output connector on the MU196060A to the Ext Clock In connector on the MU196040B.
5. Use a coaxial cable to connect the Data Output connector on the DUT to the Data Input connector on the MU196060A. Also use a coaxial cable to connect the $\overline{\text{Data}}$ Output connector on the DUT to the $\overline{\text{Data}}$ Input connector on the MU196040B.
6. Launch MX190000A, and touch **BERT for PCIe1-7** in the Application Selector screen.
   Configure the module settings including bit rate, pattern and amplitude.

Chapter 4 Usage Examples

This chapter describes usage examples of measurement using the MP1900A modules.

4.1 Measuring Optical Transceiver Module 4-2
4.2 Generating 56 Gbit/s DQPSK Signals 4-5
4.3 Evaluating Optical Components in 400GbE Transceiver 4-7
4.4 Evaluating Devices Such As SERDES for 400GbE Transceivers 4-10
4.5 Evaluating PCIe 6 Devices 4-13

4.1 Measuring Optical Transceiver Module

This section describes how to test the electrical interface input sensitivity of a CFP2 optical transceiver module by using MU195020A and MU195040A.

In the following test example, the MU195020A and MU195040A are installed into the MP1900A. The options configuring the test system are as follows:

- MP1900A
- MU181000B or MU191000A
- MU195020A-x20
- MU195040A-x20

Measurement

1. Connect the MP1900A and DUT to GND.
2. Use a coaxial cable to connect the Clock Output connector on the MU181000B or MU191000A to the Ext. Clock In connector on the MU195020A.
3. Use a coaxial connector to connect the Clock Out connector on the MU195020A to the Ext. Clock In connector on the MU195040A.

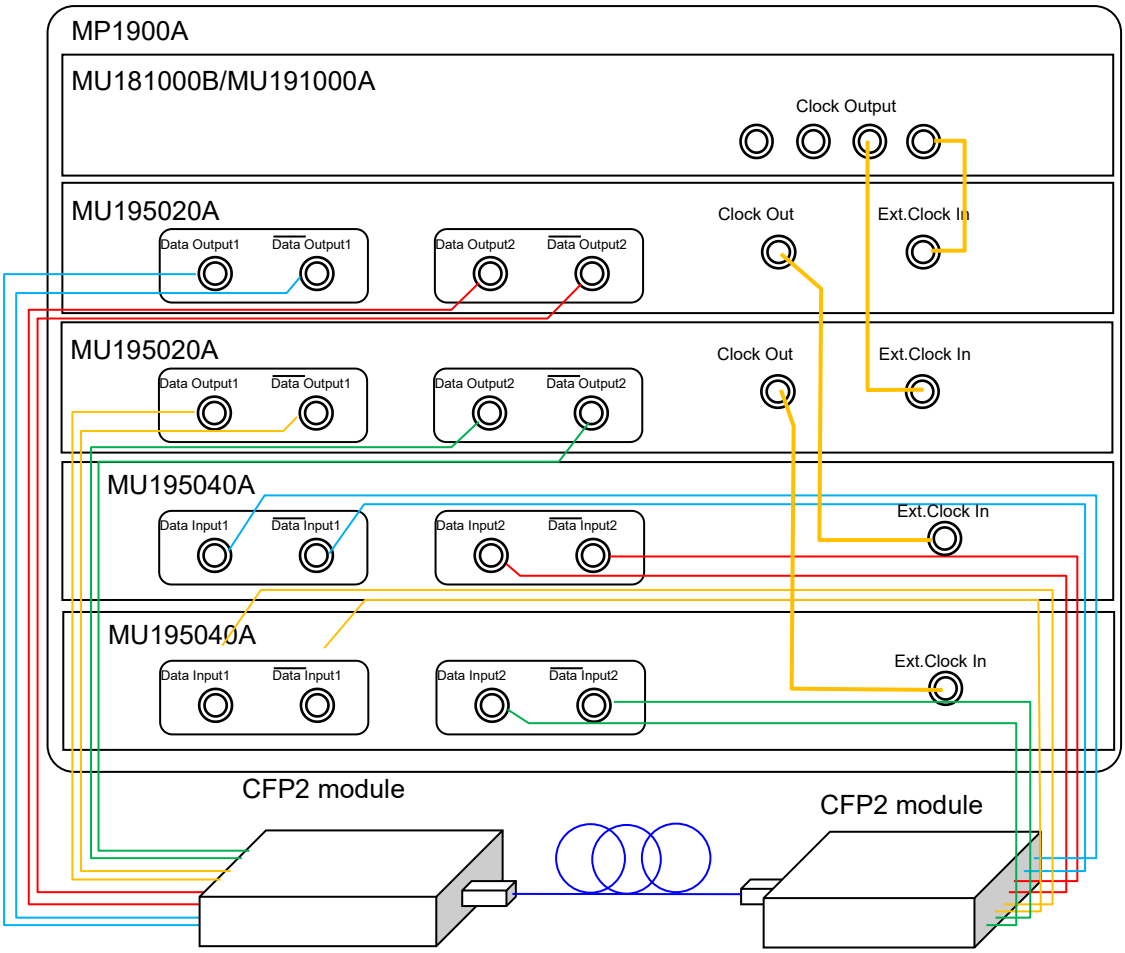


Figure 4.1-1 Connection Diagram for CFP2 Module Evaluation

4. Use coaxial cables to connect the Data Output 1-2 connectors and $\overline{\text{Data}}$ Output 1-2 connectors on the MU195020A to the Data Input connectors on the CFP2 module (8 connections).
5. Use coaxial cables to connect the Data Input 1-2 connectors and $\overline{\text{Data}}$ Input 1-2 connectors on the MU195040A to the Data Output connectors on the CFP2 module (8 connections).

Test method

1. Connect the power cord of the MP1900A.
2. Turn on the MP1900A.
3. Turn **OFF** data output. Match MU195020A data output interface to DUT's input by adjusting the amplitude and offset in the **Output** tab.
4. Set the pattern by selecting a test pattern in the **Pattern** tab of the MU195020A and MU195040A.
5. Set the operation bit rate in the **Output** tab of the MU195020A.
6. Adjust the data input interface of the MU195040A to the output interface of the DUT.

Select a terminal condition at the Input Condition in the **Input** tab of the MU195040A. Since the CFP2 module is connected by the differential interface, select **Differential 100 Ohm**, and then "Tracking".

7. Turn on the CFP2 module.
   Be sure to turn on the MP1900A first, and then the CFP2 module.

⚠ CAUTION

The DUT may be damaged if a signal line is connected or disconnected while the output is ON. Be sure to turn off the MP1900A before changing the cable connection.

8. Set Data/XData to **ON** in the **Output** tab of the MU195020A, and then touch the Output button on the top of the screen to turn it from grey to green (

).
9. Adjust the threshold voltage of the MU195040A.
   Select the **Auto Adjust** module function button.
10. Start the measurement on the **Result** tab of the MU195040A, and check the BER measurement result.
11. After checking that the DUT is operating normally, the CFP2 module data input (TD+ and TD–) sensitivity can be measured by decreasing the output level of the MU195020A.

4.2 Generating 56 Gbit/s DQPSK Signals

This section describes how to generate 56G band DQPSK signals by using the MU195020A-x20 and the DQPSK modulator.

In the following test example, the MU195020A is installed into the MP1900A. The options configuring the test system are as follows:

- MU181000A or MU191000A
- MU195020A-x20

Measurement

1. Connect the MP1900A and DUT to GND.
2. Use a coaxial cable to connect the Clock Output connector on the MU181000A or MU191000A to the Ext. Clock In connector on the MU195020A.
3. Use coaxial cables to connect the Data Output 1 and 2 and $\overline{\text{Data}}$ Output 1 and 2 connectors on the MU195020A to the DQPSK modulator (four connections).

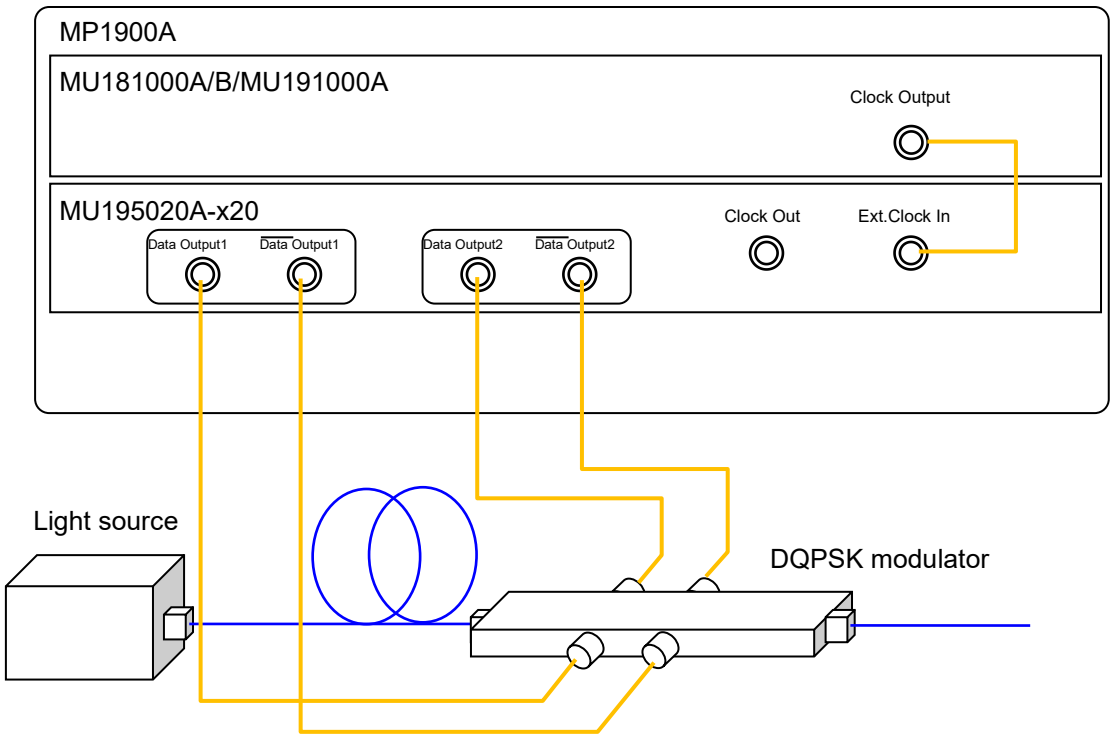
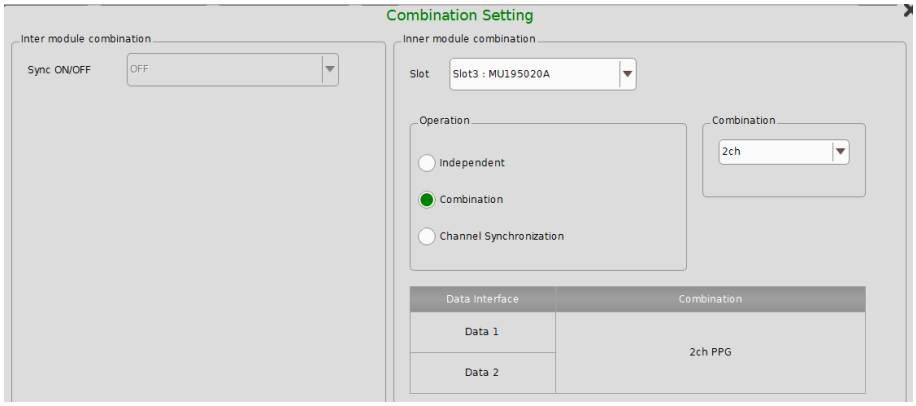


Figure 4.2-1 Connection Diagram for Generating 56 Gbit/s DQPSK Signals

Test method

1. Connect the power cord of the MP1900A.
2. Turn on the MP1900A.
3. Turn **OFF** data output. Match MU195020A data output interface to DUT's input by adjusting the amplitude and offset in the **Output** tab.
4. Set the operation bit rate to 28 Gbit/s in the **Output** tab of the MU195020A.
5. Select a test pattern in the **Pattern** tab of the MU195020A.
6. Touch 

to open the **Combination Setting** window. Select **Combination** for operation and select **2ch** for combination.



7. In the **Pre-Code** tab of the MU195020A, set Pre-Code to **ON**, select **DQPSK** in the Type dropdown list.
8. Set Data Output to **ON** in the **Output** tab of the MU195020A, and then touch the Output button on the top of the screen to turn it from grey to green (

).

By adding MU195020A signals to the DQPSK modulator, optical signals modulated to 56 Gbit/s are outputted.

4.3 Evaluating Optical Components in 400GbE Transceiver

This section explains how to evaluate optical components used in a 400GbE optical transceiver by using MU196020A/C and MU196040A/B. The optical components are as follows:

- TOSA (transmitter optical subassembly) consisting of a laser diode, driver amp, EML and other parts
- ROSA (receiver optical subassembly) consisting of a photodiode, TIA (transimpedance amplifier) and other parts

The following figure shows the block diagram for this measurement. Evaluate optical components in 400GbE transceivers using the MP1900A with the following modules installed:

- MU181000B or MU191000A
- MU196020A/C
- MU196040A/B

If a DUT has four optical channels (lanes) as shown below, the lanes are evaluated one by one.
If four MU196020A/C units or MU196040A/B units are used, the four lanes can be evaluated at a time. Up to four MU196020A/C units or MU196040A/B units can be installed on an MP1900A. For details on the connections, refer to 3.2.4 “Synchronizing multiple channels of PPG”.

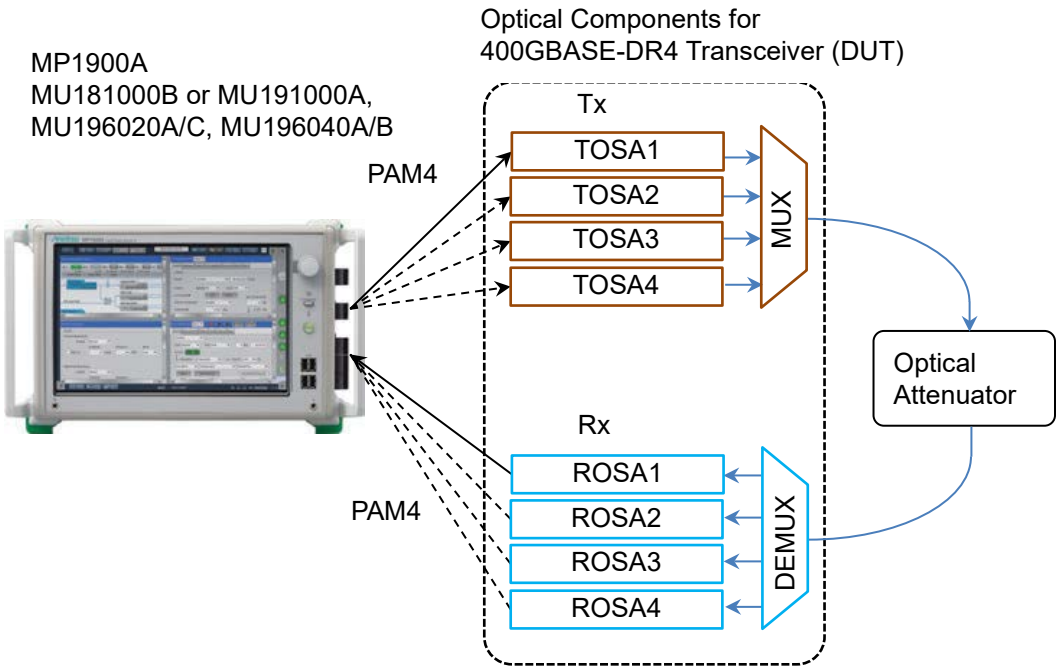


Figure 4.3-1 Block Diagram for Optical Component Evaluation

Measurement

1. Connect the MP1900A and DUT to GND.
2. Use a coaxial cable to connect the Clock Output connector on the MU181000B or MU191000A to the Ext. Clock In connector on the MU196020A/C.
3. Use a coaxial connector to connect the Clock Out connector on the MU196020A/C to the Ext. Clock In connector on the MU196040A/B.
4. Use coaxial cables to connect the Data Output connector and $\overline{\text{Data}}$ Output connector on the MU196020A/C to the Data Input connectors on the DUT (TOSA) (two connections).

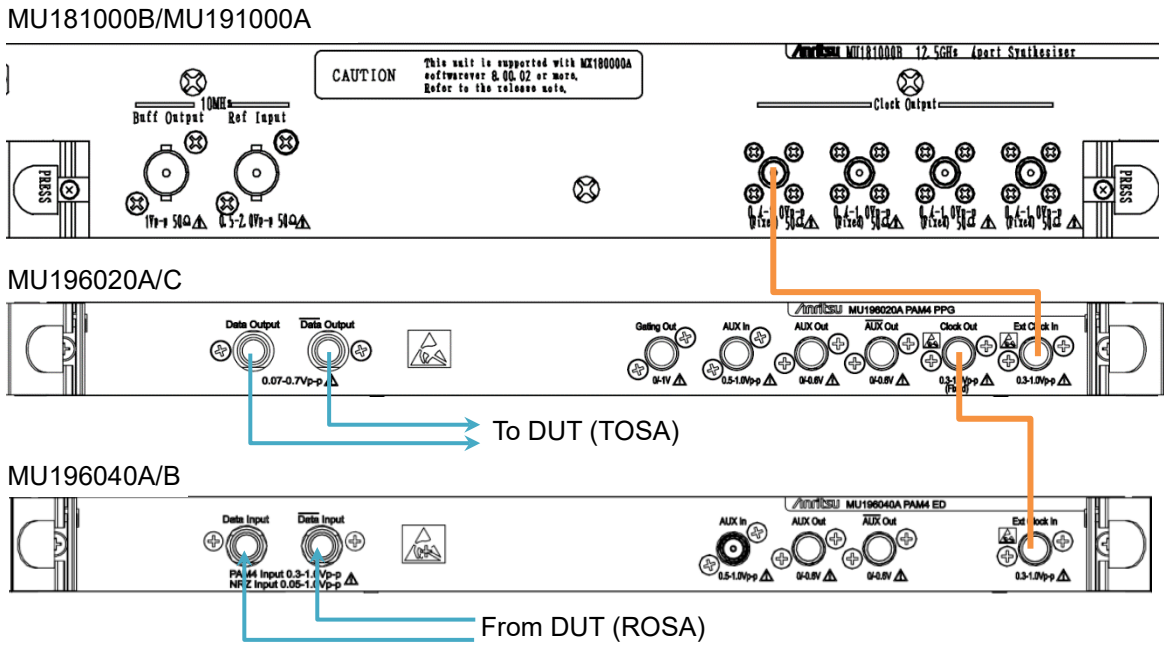


Figure 4.3-2 Module Connection Diagram

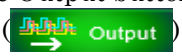
5. Use coaxial cables to connect the Data Input connector and $\overline{\text{Data}}$ Input connector on the MU196040A/B to the Data Output connectors on the DUT (ROSA) (two connections).
6. Connect the DUT and the optical attenuator. Minimize the attenuation.

Test method

1. Connect the power cord of the MP1900A.
2. Turn on the MP1900A.
3. Turn **OFF** data output. Match MU196020A/C data output interface to DUT's input by adjusting the amplitude and offset on the **Output** tab.
4. On the **Pattern** tab of the MU196020A/C and MP196040A/B, set the pattern by selecting a test pattern.
5. On the **Output** tab of the MU196020A/C, set the operation bit rate.
6. Adjust the data input interface of the MU196040A/B to the output interface of the DUT.
   On the **Input** tab of the MU196040A/B, select a terminal condition at the Input Condition. Since the DUT is connected by the differential interface, select **Differential 100 Ohm**, and then **Tracking**.
7. Turn on the DUT.
   Be sure to turn on the MP1900A first, and then the DUT.

CAUTION

The DUT may be damaged if a signal line is connected or disconnected while the output is ON. Be sure to turn off the MP1900A before changing the cable connection.

8. On the **Output** tab of the MU196020A/C, set Data to **ON**, and then touch the Output button at the top of the screen to turn it from grey to green (

).
9. Adjust the threshold voltage of the MU196040A/B.
   Touch the **Auto Search** module function button. Select the module and mode, and start. If the input level is low, manually adjust it.
10. On the **Result** tab of the MU196040A/B, start the measurement and check the BER measurement result.
11. Check that the DUT is operating normally, and then adjust the attenuation of the optical attenuator to measure the sensitivity of the DUT (ROSA).
12. Change the connection of TOSA and ROSA, and then repeat steps 3 to 11.

4.4 Evaluating Devices Such As SERDES for 400GbE Transceivers

In the evaluation of SERDES for 400GbE transceiver, the jitter tolerance of the CDR (Clock Data Recovery) is measured. This test requires the emphasis settings to be configured in order to compensate the frequency characteristics of the transmission channel and devices.
This section provides a test example with the configuration where MU196020A/C is installed to MP1900A.

If four MU196020A/C units or MU196040A/B units are used, the four lanes can be evaluated at a time. Up to four MU196020A/C units or MU196040A/B units can be installed on an MP1900A. For details on the connections, refer to 3.2.4 “Synchronizing multiple channels of PPG”.

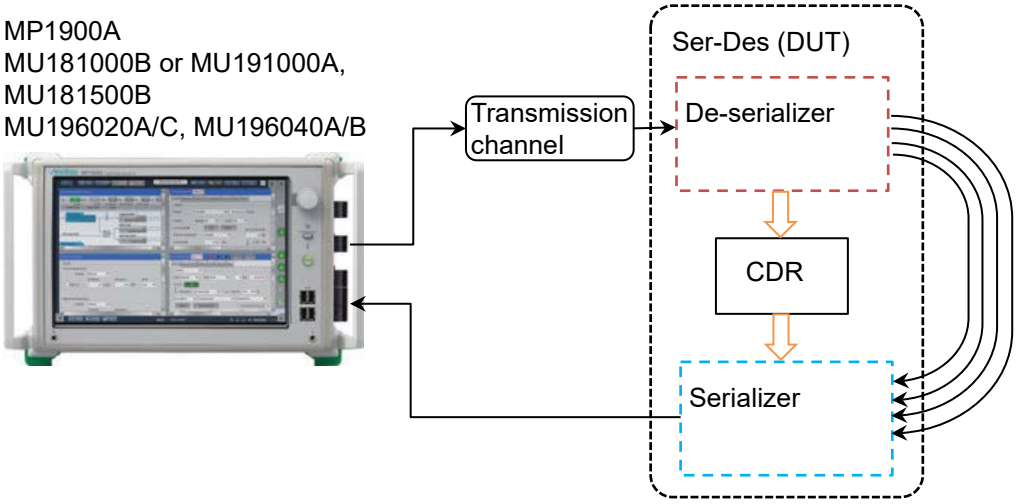


Figure 4.4-1 Block Diagram of SERDES Evaluation

Measurement

1. Connect the MP1900A and DUT to GND.
2. Use a coaxial cable to connect the Clock Output connector on the MU181000B or MU191000A to the Ext. Clock Input connector on the MU181500B.
3. Use a coaxial connector to connect the Jittered Clock Output connector on the MU181500B to the Ext. Clock In connector on the MU196020A/C.
4. Use coaxial cables to connect the Clock Out connector on the MU196020A/C to the Ext. Clock In connectors on the MU196040A/B.

5. Use coaxial cables to connect the Data Output connector and $\overline{\text{Data}}$ Output connector on the MU196020A/C to the Data Input connectors on the DUT (two connections).
6. Use coaxial cables to connect the Data Input connector and $\overline{\text{Data}}$ Input connector on the MU196040A/B to the Data Output connectors on the DUT (two connections).
7. To input the reference clock to the DUT, use a coaxial cable to connect the Sub-rate Clock Output connector on the MU181500B to the Clock Input connector on the DUT.

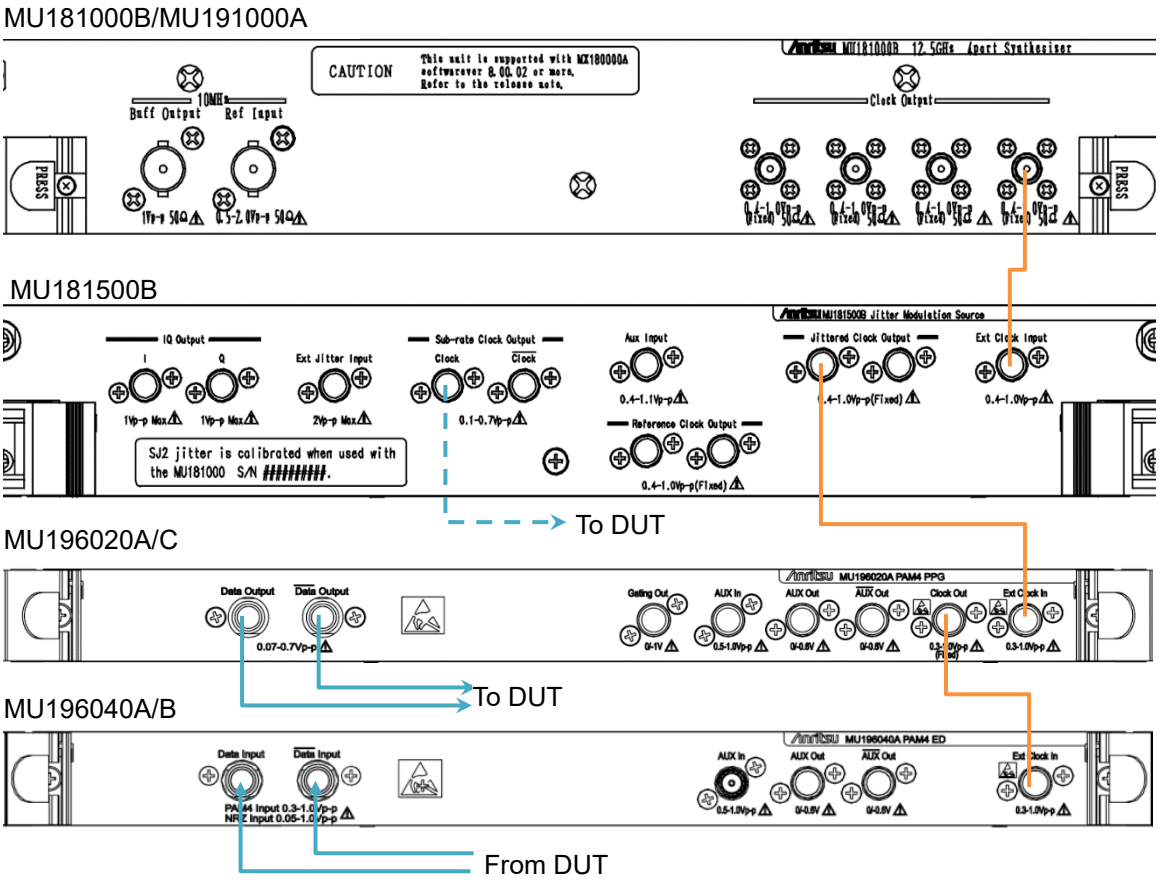


Figure 4.4-2 Module Connection Diagram

Test method

1. Connect the power cord of the MP1900A.
2. Turn on the MP1900A.
3. Set the frequency and amplitude of the jitter to be added by MU181500B.
   To input the reference clock to the DUT, set the amplitude and division ratio of the Sub-rate Clock Output.

4. Turn **OFF** data output. Match MU196020A/C data output interface to DUT's input by adjusting the amplitude and offset on the **Output** tab.
5. On the **Output** tab of the MU196020A/C, set the operation bit rate to **28 Gbit/s.**
6. On the **Pattern** tab of the MU196020A/C, select a test pattern.
7. On the **Output** tab of the MU196020A/C, set Data Output to **ON**, and then touch the Output button on the top of the screen to turn it from grey to green (

).
8. Adjust the threshold voltage of the MU196040A/B.
   Touch the **Auto Search** module function button. Select the module and mode, and start. If the input level is low, manually adjust it.
9. On the **Result** tab of the MU196040A/B, start the measurement, and check the BER measurement result.
10. On the **Emphasis** tab of the MU196020A/C, configure the emphasis settings.
11. While checking the BER measurement results of the MU196040A/B, edit the emphasis settings for the MU196020A/C so that the BER can be optimal.
12. While checking the BER measurement results of the MU196040A/B, adjust the frequency and amplitude of the jitter to be added by MU181500B so that the BER can be optimal.

4.5 Evaluating PCIe 6 Devices

In the evaluation of PCIe-6 compliant DUTs, the BER and jitter tolerance of Base spec, and the RxLEQ of CEM spec are measured. This measurement requires the Re-Driver that compensates the return path loss of DUTs.
This section provides a PCIe6 Base test example with the configuration where MU196060A is installed to MP1900A.

Evaluate PCIe 6-compliant DUTs using the MP1900A with the following modules installed:

- MU181000B or MU191000A
- MU181500B
- MU196020A/C
- MU196040B
- MU195050A or MU196050B
- MU196060A

For details on the connections, refer to 3.2.5 “Measuring while compensating loss with Re-Driver”.

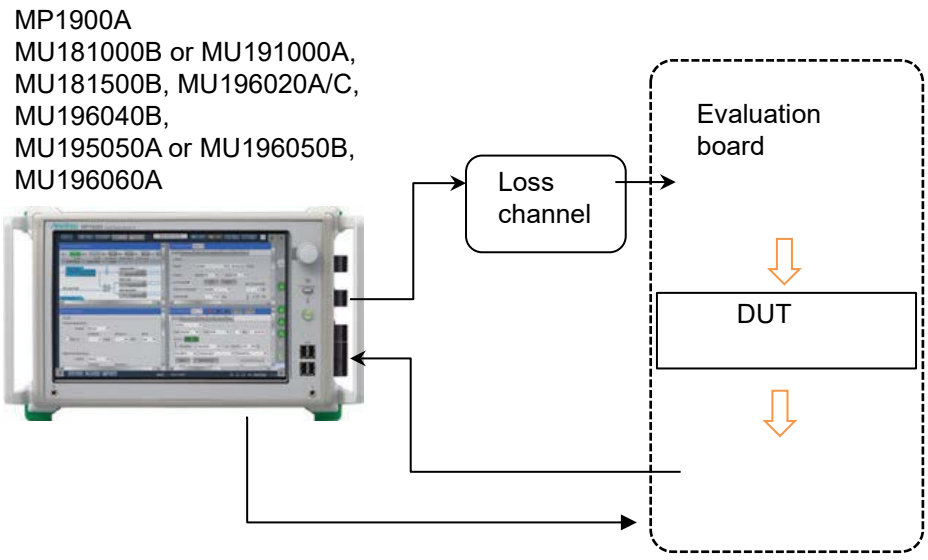


Figure 4.5-1 Block Diagram of PCIe6 DUT Evaluation

Measurement

1. Connect the MP1900A and DUT to GND.
2. If the MU195050A is used, use coaxial cables to connect the Data Output and $\overline{\text{Data}}$ Output connectors to the input connectors on the DUT (Loss channels in this example), respectively.

3. If the MU196050B is used:

   3-1. Use electrical-length-specified coaxial cables (J1948A) to connect the Pick OFF route from the Noise Output and $\overline{\text{Noise}}$ Output connectors on the MU196050B to the Pick OFF Tee (J1793A). Connect the straight connectors of J1948A to the MU196050B connectors and the right-angle connectors to J1793A.

   3-2. Use coaxial cables to connect the output connectors on the Pick OFF Tee (J1793A) to the input connectors on the DUT, respectively.

4. Use coaxial cables to connect the Data Input and $\overline{\text{Data}}$ Input connectors on the MU196060A to the Data Output and $\overline{\text{Data}}$ Output connectors on the DUT.

5. To input the reference clock to the DUT, use a coaxial cable to connect the Sub-rate Clock Output connector on the MU181500B to the Clock Input connector on the DUT.

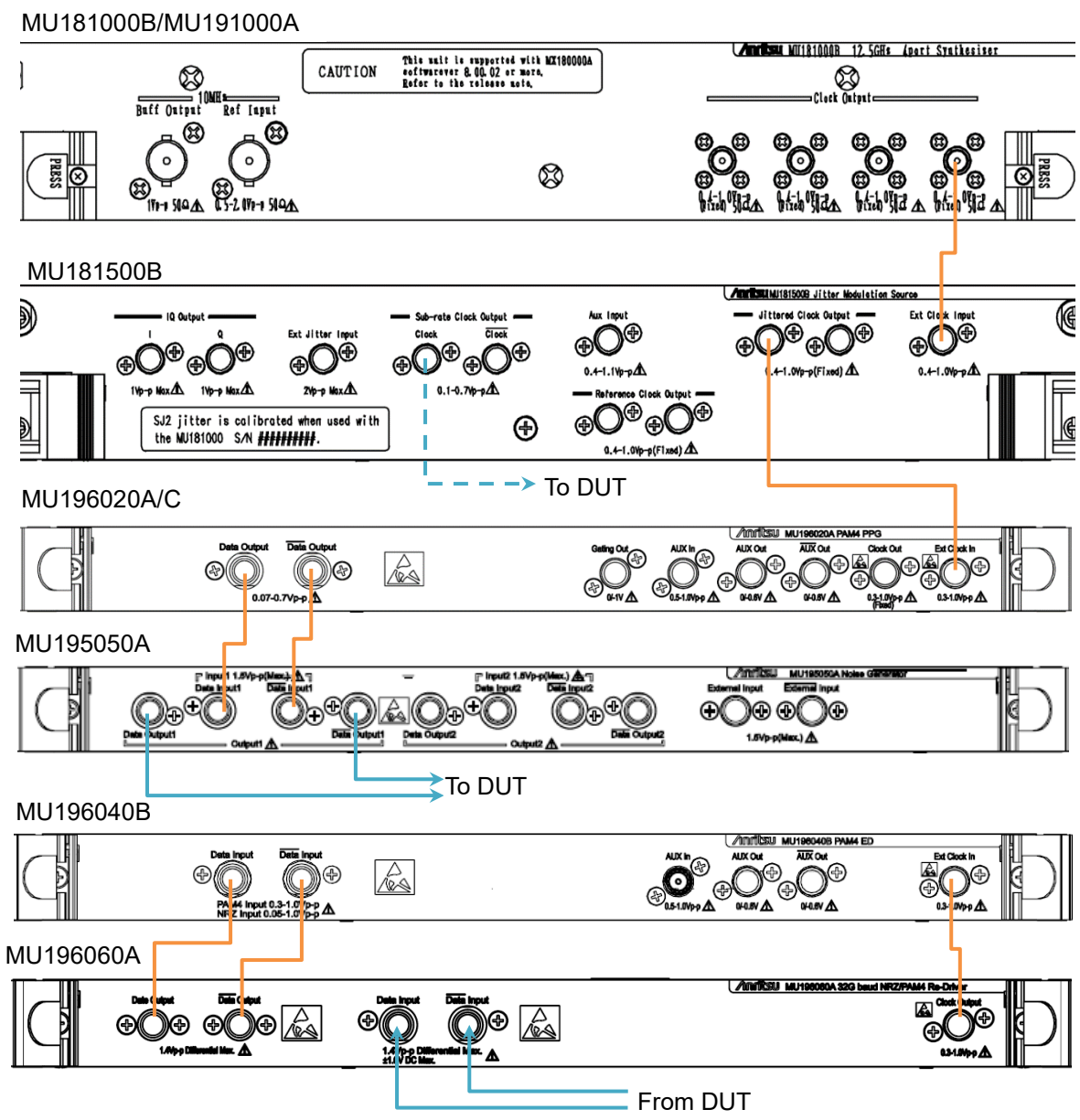


Figure 4.5-2 Module Connection Diagram (for MU195050A)

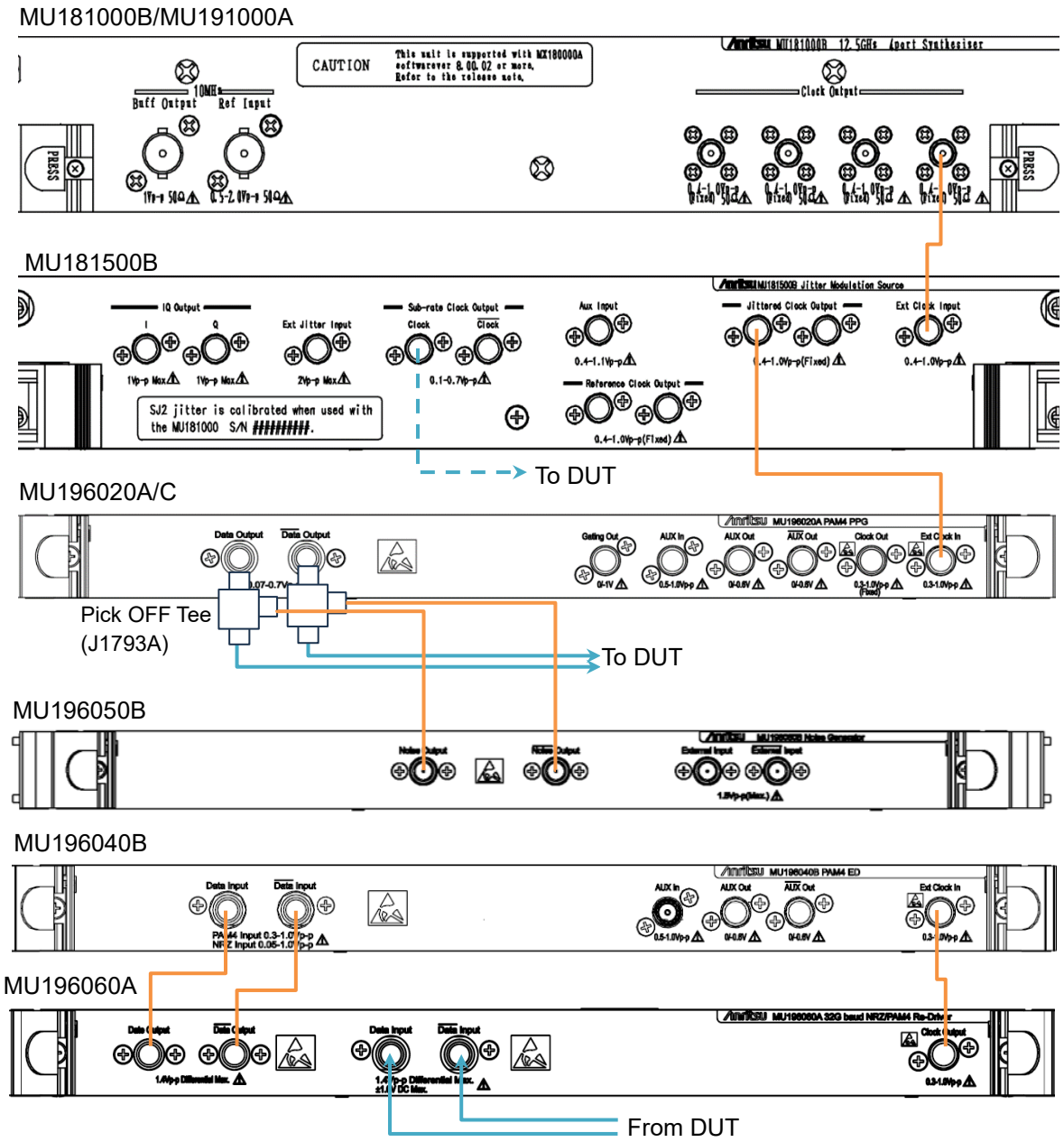


Figure 4.5-3 Module Connection Diagram (Noise Generator: MU196050B)

Measurement

1. Plug the power cord of the MP1900A to a power outlet.
2. Turn on the MP1900A.
3. Launch MX190000A, and touch **BERT for PCIe1-7** in the Application Selector screen.
4. To input the reference clock to the DUT, set the Sub-rate Clock Output amplitude and division ratio of the MU181500B.

5. Turn **OFF** data output. Match MU196020A/C data output interface to DUT's input by adjusting the amplitude and offset on the **Output** tab.
6. On the **Output** tab of the MU196020A/C, set the operation baud rate to **PCIe6.**
7. On the **Pattern** tab of the MU196020A/C, select a test pattern.
8. On the **Output** tab of the MU196020A/C, set Data Output to **ON**, and then touch the Output button on the top of the screen to turn it from grey to green (

). Set CTLE of the MU196060A.
9. Adjust the threshold voltage of the MU196040B.
   Touch the **Auto Search** module function button. Select the module and mode, and start. If the input level is low, manually adjust it.
10. On the **Result** tab of the MU196040B, start the measurement, and check the BER measurement result.
11. On the **Emphasis** tab of the MU196020A/C, configure the emphasis settings.
12. While checking the BER measurement results of the MU196040B, edit the emphasis settings for the MU196020A/C and the CTLE settings for the MU196060A so that the BER can be optimal.
13. While checking the BER measurement results of the MU196040B, adjust the following settings to obtain values to achieve the optimal BER.
    - Delay and Threshold of the MU196040B
    - Emphasis on the **Emphasis** tab of the MU196020A/C
    - CTLE of the MU196060A

Chapter 5 Performance Test

This chapter describes the performance testing of the MP1900A modules.

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5.1 Timing of Performance Tests

Performance tests verify that the MP1900A modules meet the specified performance requirements.
Run the tests at acceptance inspection, after repair, and at six-month intervals.

5.2 Devices Required for Performance Tests

5.2.1 Synthesizer

5.2.1.1 MU191000A

Before starting performance test, warm up the MU191000A and the measuring instruments for at least 30 minutes. Table 5.2.1.1-1 shows the required devices for performance test.

Table 5.2.1.1-1 Devices Required for Performance Tests

Device Name	Performance Requirements
Sampling oscilloscope	Bandwidth: 40 GHz or more
Spectrum Analyzer	Bandwidth: 40 GHz or more

Note:

Before starting the performance test, warm up the device under test and the measuring instruments for at least 30 minutes, and wait until they become sufficiently stabilized unless otherwise specified.

Maximum measurement accuracy is assured under the following conditions:

- Measurement is performed at room temperature.
- Fluctuations of AC power supply voltage are small.
- Noise, vibration, dust, and humidity are insignificant.

5.2.2 PPG/ED

Before starting performance test, warm up the MP1900A and the measuring instruments for at least 30 minutes. Table 5.2.2.1-1 shows the required devices for performance test.

5.2.2.1 MU195020A/MU195040A

Table 5.2.2.1-1 Devices Required for Performance Tests

Device Name	Model	Performance Requirements
Error detector	MP1900A + MU195040A-001	Operating frequency: 2.4 to 32.1 GHz Data input sensitivity: 300 mVp-p or more
Sampling oscilloscope		Electrical interface: 70 GHz or more band
Signal generator	MP1900A + MU195020A + MU181000A/B or MU191000A or MG3690 series	When using Ext Clock: Operating frequency: 1.2 to 16.05 GHz Output level: 300 to 1000 mVp-p Waveform: Rectangular wave or sine wave
coaxial cables (0.8 m, K connector)	J1439A	Bandwidth: 40 GHz
Coaxial Attenuator	J0541E	Attenuation: 6 dB
Power Meter	ML2437A or ML2438A	
Power Sensor + cable	MA2444D	

5.2.2.2 MU196020A/MU196040A/B

Table 5.2.2.2-1 Devices Required for Performance Tests

Device Name	Model	Performance Requirements
Error detector	MP1900A + MU196040A-001 or MP1900A + MU196040B-001*2	Operating bit rate: 2.4 to 32.1 Gbit/s Operating baud rate: 2.4 to 32.1 Gbaud
	MP1900A + MU196040B-002*2	Operating bit rate: 2.4 to 64.2 Gbit/s Operating baud rate: 2.4 to 58.2 Gbaud
	MP1900A + MU195040A-001	Operating bit rate: 16 to 32.1 Gbit/s*1
Sampling oscilloscope		Electrical channel: 70 GHz or more band
Signal generator	MP1900A + MU196020A + MU181000A/B or MU191000A or MG3690 series	When using Ext Clock: Operating frequency: 1.2 to 16.05 GHz Output level: 300 to 1000 mVp-p Waveform: Rectangular wave or sine wave
	MP1900A + MU195020A-001 + MU181000B or MU191000A	Operating bit rate: 16 to 32.1 Gbit/s*1
Re-Driver	MP1900A + MU196060A-001	Operating baud rate: 16 Gbaud, 19 to 32 Gbaud
Jitter Signal Source	MP1900A + MU181500B	SSC: 33kHz, 5300ppm*1
Electrical Length Specified Coaxial Cable (0.4m, V connector)	J1789A	Bandwidth: 65 GHz, For connecting data signals
Electrical Length Specified Coaxial Cable (0.8m, V connector)	J1790A	Bandwidth: 65 GHz, For connecting data signals
Coaxial Cable 0.3 m (SMA connector)	J1624A	Bandwidth: 18 GHz, For connecting clock signals
Coaxial cable 1 m	J1625A	Bandwidth: 18 GHz, For connecting trigger signals
Coaxial Attenuator	J0541E	Attenuation: 6 dB
Precision Fixed Attenuator 20 dB	41VA-20	Attenuation: 20 dB

*1: Used in self-loopback test. The MU195020A-001 and MU195040A-001 are required.

*2: For MP1900A with MU196040B-005, refer to Table 5.2.2.3-1 for the performance requirements.

Table 5.2.2.2-1 Devices Required for Performance Tests (Cont'd)

Device Name	Model	Performance Requirements
Precision Adaptor	34VFK50A	For the Data Input connector of MU196040A-001
Coaxial Cable Set for MU196060A	J1898A	For connecting MU196060A and ED *1 A set of J1932A and J1917A
Coaxial Skew Matched Cable Pair (0.8m, V Connector)	J1932A	V-P, V-P, a pair of 0.8 m, for Data Output and XData Output *1 Equivalent of J1790A
Coaxial Semi-rigid Cable	J1917A	SMA-P, SMA-P x 1, for Clock Output *1
Power Meter	ML2437A or L2438A	
Power Sensor + cable	MA2444D	

5.2.2.3 MU196020C/MU196040B

Table 5.2.2.3-1 Devices Required for Performance Tests

Device Name	Model	Performance Requirements
Error detector	MP1900A + MU196040B-005*2	Operating bit rate: 2.4 to 64.2 Gbit/s Operating baud rate: 2.4 to 64.2 Gbaud
	MP1900A + MU195040A-001	Operating bit rate: 16 to 32.1 Gbit/s*1
Sampling oscilloscope		Electrical channel: 70 GHz or more band
Signal generator	MP1900A + MU196020C + MU181000A/B, or MU191000A, or MG3690 series	When using Ext Clock: Operating frequency: 1.2 to 16.05 GHz Output level: 300 to 1000 mVp-p Waveform: Rectangular wave or sine wave
	MP1900A + MU195020A-001 + MU181000A/B or MU191000A	Operating bit rate: 16 to 32.1 Gbit/s*1
Re-Driver	MP1900A + MU196060A-001	Operating baud rate: 16 Gbaud, 19 to 32 Gbaud
Jitter Signal Source	MP1900A + MU181500B	SSC: 33 kHz, 5300 ppm*1
Electrical Length Specified Coaxial Cable (0.4m, V connector)	J1789A	Bandwidth: 65 GHz, For connecting data signals
Electrical Length Specified Coaxial Cable (0.8m, V connector)	J1790A	Bandwidth: 65 GHz, For connecting data signals
Coaxial Cable 0.3 m (SMA connector)	J1624A	Bandwidth: 18 GHz, For connecting clock signals
Coaxial cable 1 m	J1625A	Bandwidth: 18 GHz, For connecting trigger signals
Coaxial Attenuator	J0541E	Attenuation: 6 dB
Precision Fixed Attenuator 20 dB	41VA-20	Attenuation: 20 dB
Precision Adaptor	34VFK50A	For the Data Input connector of MU196040A-001
Coaxial Cable Set for MU196060A	J1898A	For connecting MU196060A and ED *1 A set of J1932A and J1917A
Coaxial Skew Matched Cable Pair (0.8m, V Connector)	J1932A	V-P, V-P, a pair of 0.8 m, for Data Output and XData Output *1 Equivalent of J1790A
Coaxial Semi-rigid Cable	J1917A	SMA-P, SMA-P x 1, for Clock Output *1
Power Meter	ML2437A or L2438A	
Power Sensor + cable	MA2444D	

*1: Used in self-loopback test. The MU195020A-001 and MU195040A-001 are required.

*2: For MP1900A with the following options, refer to Table 5.2.2.2-1 for the performance requirements:
– MU196040A-001
– MU196040B-001
– MU196040B-002

Note:

Before starting the performance test, warm up the device under test and the measuring instruments for at least 30 minutes, and wait until they become sufficiently stabilized unless otherwise specified.

Maximum measurement accuracy is assured under the following conditions:

- Measurement is performed at room temperature.
- Fluctuations of AC power supply voltage are small.
- Noise, vibration, dust, and humidity are insignificant.

5.3 Performance Test Items

5.3.1 Synthesizer

5.3.1.1 MU191000A

This section describes the following test items.

- Measuring waveform
- Measuring phase noise
- Measuring triangular wave modulation
- Measuring AUX output waveform

5.3.1.1.1 Measuring waveform

Measure the waveform at the Clock Output connector. Connection with the measuring instruments is shown in Figure 5.3.1.1.1-1.

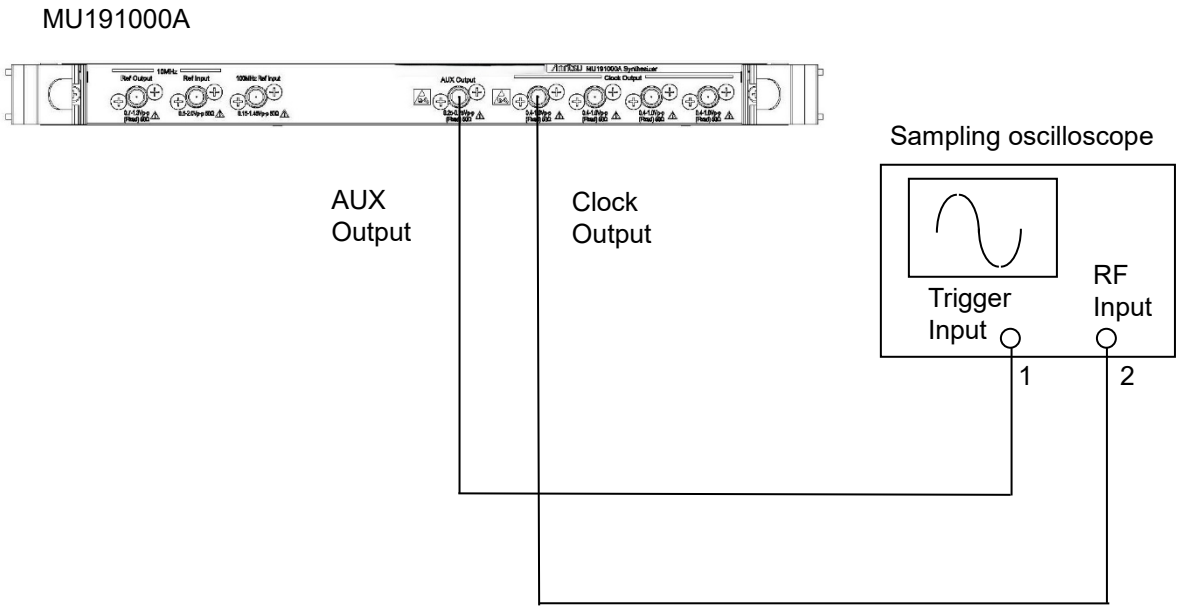


Figure 5.3.1.1.1-1 Connection diagram for waveform measurement

1. Connect the signal output from the AUX Output connector to the Trigger Input connector of the sampling oscilloscope.
2. Connect the clock signal output from the Clock Output connector to the RF Input connector of the sampling oscilloscope.

⚠ CAUTION

Use an appropriate attenuator for each input connector when connecting to the input connector of the sampling oscilloscope. Improper connection may damage the sampling oscilloscope.

3. Set as follows in the MU191000A operation window:

   Center Frequency: 16050 MHz

   Offset: 0 ppm

   Reference Clock Source: Internal

4. Use the sampling oscilloscope to measure the waveform, and then check that the level of the measured waveform falls within the range shown in Figure 5.3.1.1.1-2.

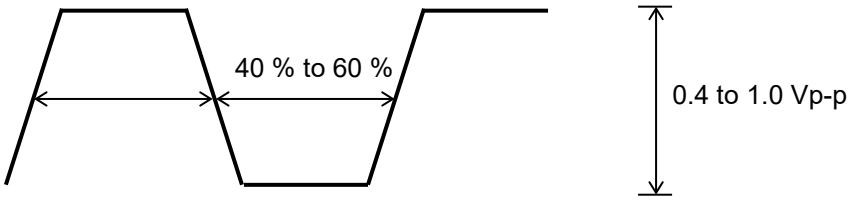


Figure 5.3.1.1.1-2 Example of waveform measured by sampling oscilloscope

5. Change the Center Frequency value in the MU191000A operation window as shown below, and perform measurement in the same way. Verify that both the waveform level and duty ratio are within the ranges specified in Figure 5.3.1.1.1-2.

   Center Frequency: 12000 MHz, 8000 MHz, 5000 MHz, 2500 MHz, 1250 MHz, 100 MHz

5.3.1.1.2 Measuring phase noise

Measure the phase noise at the Clock Output connector. Connection with the measuring instruments is shown in Figure 5.3.1.1.2-1.

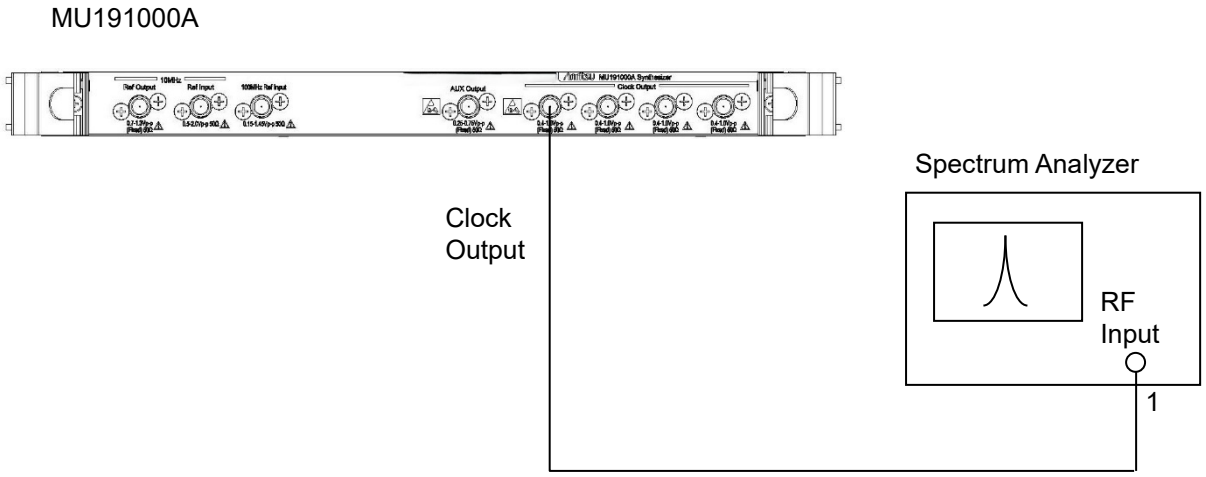


Figure 5.3.1.1.2-1 Connection diagram for phase noise measurement

1. Connect the clock signal output from the Clock Output connector to the RF Input connector of the spectrum analyzer.
2. Set as follows in the MU191000A operation window:

   Center Frequency: 16050 MHz

   Offset: 0 ppm

   Reference Clock Source: Internal
3. Verify that the phase noise measured with the spectrum analyzer does not exceed the limits listed below. Non-harmonic spurious components are excluded from the phase-noise evaluation.

   At a 10 kHz offset: ≤ −110 dBc/Hz

   At a 100 kHz offset: ≤ −111 dBc/Hz

   At a 1 MHz offset: ≤ −110 dBc/Hz
4. Repeat the measurement while changing the Center Frequency value as shown below in the MU191000A operation window. Verify that the measured phase noise does not exceed the limits in step 3.

   Center Frequency: 12000 MHz, 8000 MHz, 5000 MHz, 2500 MHz, 1250 MHz, 100 MHz

⚠ CAUTION

Use an appropriate attenuator for each input connector when connecting to the input connector of the spectrum

analyzer. Improper connection may damage the spectrum analyzer.

5.3.1.1.3 Measuring triangular wave modulation

Measure the phase deviation at the Clock Output connector. Connection with the measuring instruments is shown in Figure 5.3.1.1.3-1.

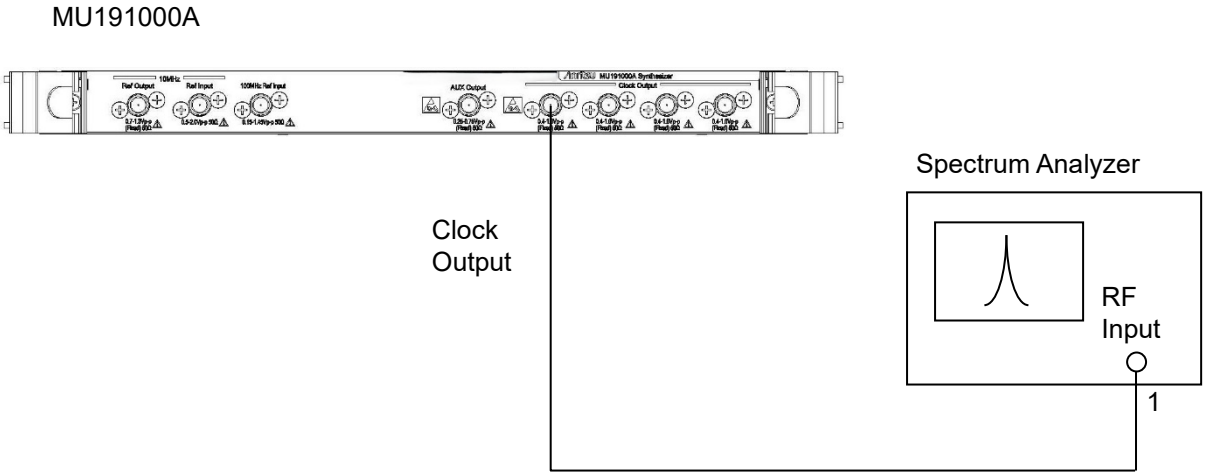


Figure 5.3.1.1.3-1 Connection diagram for triangular wave modulation measurement

1. Connect the clock signal from the Clock Output connector to the spectrum analyzer RF Input connector.
2. Set as follows in the MU191000A operation window.

   Operation: PCIe-Gen 3/4/5/6/7 (8GHz)

   Offset: 0 ppm

   Reference Clock Source: Internal

   Spectrum Spread: SSC ON (Int Ref)

   Spread Method: Center

   Deviation: 5000 ppm
3. On the trapezoid-shaped spectrum shown in Figure 5.3.1.1.3-2, measure the frequency difference between the two points where the trace is 3 dB below the level at 8 GHz Measure the frequency separation between these points, and verify that it is 40 MHz (5000 ppm at 8 GHz). If the displayed spectrum trace is not trapezoid-shaped, adjust the spectrum analyzer RBW or VBW to obtain a trapezoid-shaped spectrum.

CAUTION

Use an appropriate attenuator for each input connector when connecting to the input connector of the spectrum analyzer. Improper connection may damage the spectrum analyzer.

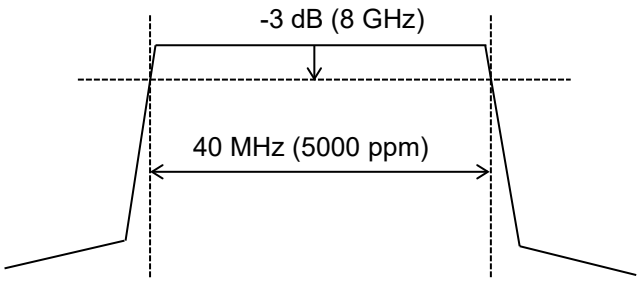


Figure 5.3.1.1.3-3 Example of Trapezoid-Shaped Spectrum Trace Measured With Spectrum Analyzer

5.3.1.1.4 Measuring AUX output waveform

Measure the AUX output waveform. Connection with the measuring instrument is shown in Figure 5.3.1.1.4-1.

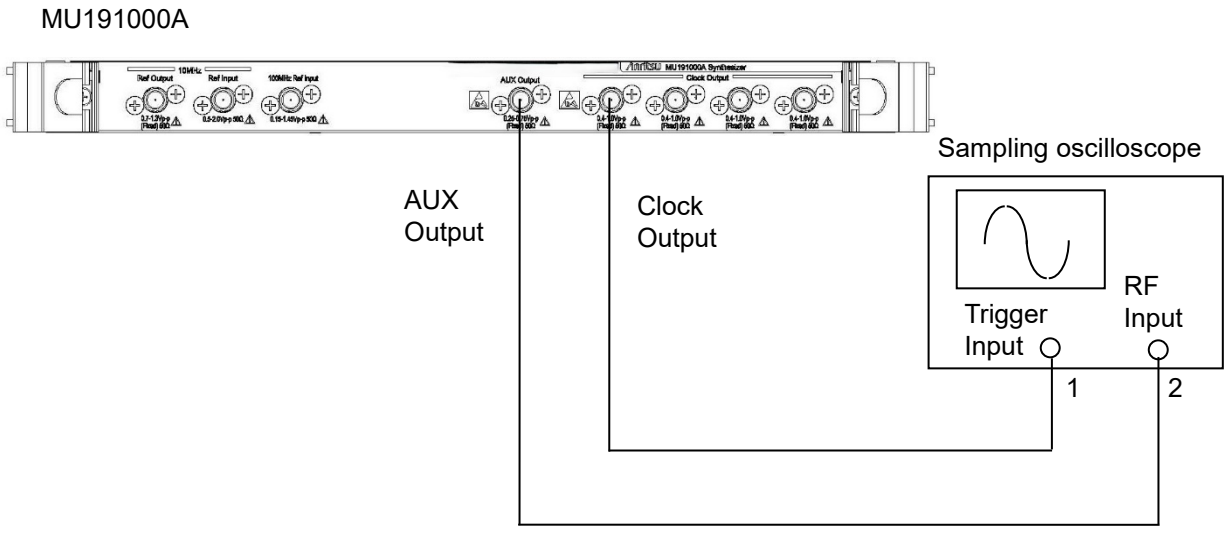


Figure 5.3.1.1.4-1 Connection diagram for AUX output waveform measurement

1. Connect the Clock Output signal to the Trigger Input connector of the sampling oscilloscope.
2. Connect the AUX Output signal to the RF Input connector of the sampling oscilloscope.

⚠ CAUTION

Use an appropriate attenuator for each input connector when connecting to the input connector of the sampling oscilloscope. Improper connection may damage the sampling oscilloscope.

3. Set as follows in the MU191000A operation window

   Center Frequency: 16050 MHz

   Offset: 0 ppm

   Reference Clock Source: Internal

4. Use the sampling oscilloscope, and then check that the level of the measured waveform falls within the range shown in Figure 5.3.1.1.4-2.

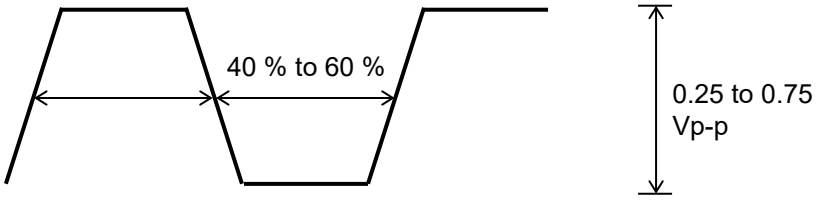


Figure 5.3.1.1.4-2 Example of waveform measured by sampling oscilloscope

5. Change the Center Frequency value in the MU191000A operation window as shown below, and perform measurement in the same way. Verify that both the waveform level and duty ratio are within the ranges specified in Figure 5.3.1.1.4-2.

   Center Frequency: 12000 MHz, 8000 MHz, 5000 MHz, 2500 MHz, 1250 MHz, 100 MHz

5.3.2 PPG/ED

5.3.2.1 MU195020A/MU195040A

This section describes the following test items.

- Operating frequency range
- Waveform evaluation test
- Input level
- Pattern
- Error detection
- Noise evaluation test

5.3.2.1.1 Operating frequency range

(1) Specifications

Table 5.3.2.1.1-1 Specifications

Option	Specifications
MU195020A	2.4 to 21.0 Gbit/s
MU195020A-001	2.4 to 32.1 Gbit/s
MU195040A	2.4 to 21.0 Gbit/s
MU195040A-001	2.4 to 32.1 Gbit/s

(2) Device connection

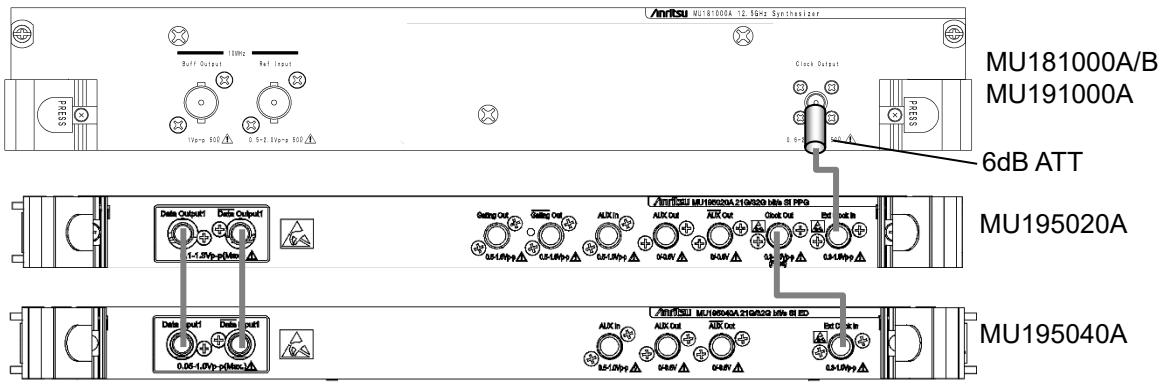


Figure 5.3.2.1.1-1 Connection Diagram for Operating Frequency Range Test

Note:

When using the MU181000A, connect the 6 dB Coaxial Attenuator to the Clock Output connector before connecting the measuring instrument cables.

(3) Test procedure

1. Mount the MU195020A onto the MP1900A, and turn on the MP1900A with the cables unconnected.
2. Set the Data signal output amplitude of the MU195020A to 500 mVp-p, offset (Vth) to 0 V, test pattern to PRBS31, and mark ratio to 1/2.
3. Turn off the MP1900A when setting the parameters completely.
4. Connect the measuring instrument cables as shown in Figure 5.3.2.2.1-1.
5. Turn on the MP1900A and the measuring instruments, and warm them up.
6. After warming up the instruments, enable the MP1900A signal output (ON) to output signals from the MU195020A. There is a warm-up status indicator for the MU195020A. The indicator is turned on after the signals are output, and is turned off when the instruments are warmed up.



7. Adjust the phase and threshold voltage of the MU195040A to the optimum values.
8. Check that no error is detected by the MU195040A.
9. Change the operating frequency and check if no error occurs within the rated operating frequency range.

5.3.2.1.2 Waveform evaluation test

(1) Specifications

Table 5.3.2.1.2-1 Specifications for MU195020A

Item	Specification
	MU195020A-x10/x20
Amplitude	0.1 to 1.3 Vp-p
Offset (Vth)	$-2.0-\frac{\text{Amp.}}{2}$ to $+3.3-\frac{\text{Amp.}}{2}$ V
Cross point	Amplitude: 1.0 Vp-p 50 %
Tr/Tf	14 ps (20 to 80 %)*1,*2
Jitter	8 ps p-p*1,*2,*3

*1: If MU195020A-001 is not available, then this is at 21.0 Gbit/s. If MU195020A-001 is available, then this is at 32.1 Gbit/s.

*2: Typical value

*3: The jitter specification value is defined assuming that the oscilloscope with residual jitter less than 200 fs (RMS) is used.

(2) Device connection

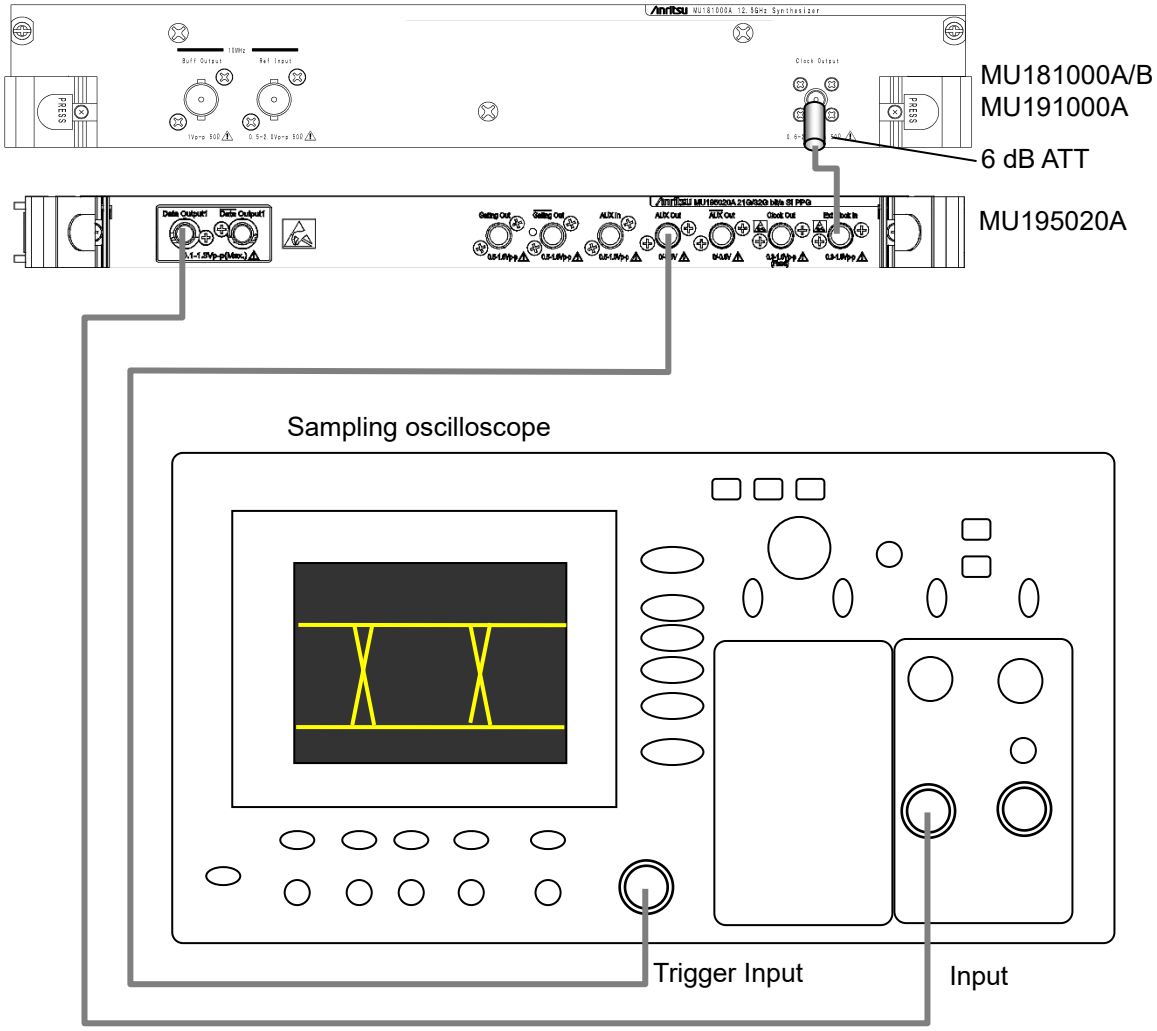


Figure 5.3.2.1.2-1 Connection Diagram for Waveform Test

Note:

When using the MU181000A, connect the 6 dB Coaxial Attenuator to the Clock Output connector before connecting the measuring instrument cables.

(3) Test procedure

1. Mount the MU195020A onto the MP1900A, and turn on the MP1900A with the cables unconnected.
2. Set the Data output amplitude, offset, and cross point to be tested in the MU195020A **Output** tab window.
3. Set the test pattern in the **Pattern** tab of the MU195020A.

   Since the specification parameters are evaluated by the eye pattern observation, set the test pattern to PRBS31, and the mark ratio to 1/2.

4. Select a trigger signal to input to the oscilloscope. Select **1/N Clock** in the AUX Output dropdown list in the **Misc1** tab of the MU195020A, and set the division ratio according to the sampling oscilloscope used.
5. Turn off the MP1900A when setting the parameters completely.
6. Connect the measuring instrument cables as shown in Figure 5.3.2.2.2-1.
7. Turn on the MP1900A and the measuring instruments, and warm them up.
8. After warming up the instruments, enable the MP1900A signal output (ON) and output signals.
9. Observe the output waveform on the sampling oscilloscope, and check that all the items meet the specifications.
10. Use a coaxial cable to connect the XData Output connector of the MU195020A and the Input connector of the sampling oscilloscope. Repeat the observation in Step 9.
11. If there are multiple channels, repeat the observation in Step 9 for all Data Output and XData Output.

5.3.2.1.3 Input level

(1) Specifications

Table 5.3.2.1.3-1 Specifications

Option	Specifications
MU195040A-x10/x20	Input amplitude: 0.05 to 1.0 Vp-p Threshold voltage: –3.5 to +3.3 V

(2) Connection

Refer to Figure 5.3.2.2.1-1 for the device connection.

(3) Procedure

1. Connect devices and configure the settings in the same manner as shown in Steps 1 to 5 in Section 5.3.2.1.1.
2. Set the output level of the MU195020A and the threshold voltage of the MU195040A as shown in Table 5.3.2.2.3-2. Set the output of the MU195020A to ON and touch **Start** on the MU195040A.Adjust the phase as required, and check that no error occurs.

Table 5.3.2.1.3-2 Input Level Test Setting (MU195040A)

	MU195020A			MU195040A	
No.	Termination	Amplitude [Vp-p]	Offset (Vth) [V]	Termination	Threshold voltage [V]
1	GND	1.0	–2.5	GND	–2.500
2		0.05*	–2.25		–2.250
3		1.0	+2.8		+2.800
4		0.05*	+3.05		+3.050
5	NECL	0.8	–1.3	Variable: – 2.0 V	–1.300
6	LVPECL	0.8	+2.0	Variable: + 1.3 V	+2.000
7	PCML	0.5	+3.05	Variable: + 3.3 V	+3.050

*: For the signals of amplitude 0.05 Vp-p, set the MU195020A to 0.5 Vp-p and use the Precision Fixed Attenuator (20 dB, application part 41KC-20).

Note:

When changing the termination condition, configure the settings of the MU195020A and the MU195040A in the following order. The MU195020A and the MU195040A may be damaged if the settings are configured in an incorrect order or the termination condition is not set correctly.

(1) Set the output of the MU195020A to OFF.

(2) Set the termination condition for the MU195040A to GND.

(3) Change the termination condition for the MU195020A.

(4) Set the termination condition for the MU195040A to that for the MU195020A set in Step [3].

3. Remove the cable from the Data Input connectors, and then connect the XData Input connectors, using a coaxial cable. In the MU195040A **Input** tab window, set **Input Condition** to **Single-Ended** and **XData**. Next, set the output level of the MU195020A and the threshold voltage of the MU195040A as the procedure 2, and check that no error occurs.

5.3.2.1.4 Pattern

(1) Specifications

- PRBS pattern
- Zero Substitution pattern

(2) Connection

Refer to Figure 5.3.2.2.1-1 for the device connection.

(3) Procedure

1. Connect devices and configure the settings in the same manner as shown in Steps 1 to 5 in Section 5.3.2.1.1.
2. Set the output of the MU195020A to ON and touch **Start** on the MU195040A. Adjust the phase as required, and check that no error occurs.
3. For both the MU195040A and the MU195020A, set the PRBS pattern length to 2^n-1, changing the value of n to 7, 9, 10, 11, 15, 20, 23, and 31, and check that no error occurs.
   For the MU195040A, the PRBS pattern length can be set in the **Pattern** tab window.
4. Set the PRBS pattern length to $2^{31}-1$.
   For the MU195040A, this operation can be performed by changing Logic POS/NEG on the **Pattern** tab window. Check that no error occurs.
5. For both the MU195040A and the MU195020A, set the test pattern to Zero Substitution, then, set Length to 2^n-1, changing the value of n to 7, 9, 10, 11, 15, 20, and 23, and check that no error occurs. Next, set Length to 2^n, changing the value of n to 7, 9, 10, 11, 15, 20, and 23, and confirm that no error occurs.

5.3.2.1.5 Error detection

(1) Specifications

Error rate:	0.0000 × 10^{-16} to 1.0000
Error count:	0 to 1 × 10^{16}
Error free interval (EFI):	0.0000 to 100.0000 %
Error interval (EI):	0 to 1 × 10^{16}
Clock frequency:	
MU195040A-001 is not installed	1.2 to 10.5 GHz, accuracy: ± (10 ppm + 1 kHz)
MU195040A-001 is installed	1.2 to 16.05 GHz, accuracy: ± (10 ppm + 1 kHz)

(2) Connection

Refer to Figure 5.3.2.2.1-1 for the device connection.

(3) Procedure

1. Connect devices and configure the settings in the same manner as shown in Steps 1 to 5 in Section 5.3.2.1.1.
2. Set the frequency of the MU181000A/B or MU191000A to 10 GHz, set the output of the MU195020A to ON, and then touch **Start** on the MU195040A. Adjust the phase as required, and check that no error occurs.
3. Turn On error insertion of the MU195020A, and make sure that the ER measurement results on the **Result** tab of the MU195040A match the values set on the **Error Addition** tab on the MU195020A.
4. Set "Single" for error insertion of the MU195020A (set Variation to **Single** in the MU195020A **Error Addition** tab window). In the Gating field on the MU195040A **Measurement** tab window, set **Cycle** to **Single**, and set the measurement time to 10 seconds.
5. Touch **Start** on the MU195040A. While the measurement is running for 10 seconds, touch **Single** once on the **Error Addition** tab of the MU195020A.

   When the measurement has finished, check that the measurement results are as follows.

Error rate (ER):	5.0000E–12
Error count (EC):	1.0000E–00
Error free interval (%EFI):	99.9900 %
Error interval (EI):	1

5.3.2.1.6 Noise evaluation test

(1) Specifications

Table 5.3.2.1.6-1 Specifications for MU195050A

Item	Specification
Common mode noise (CMI)	0 to 250 mVp-p *1
Differential mode noise (DMI)	0 to 200 mVp-p (Differential) *2
White noise*3	0.2 to 25 mVrms

*1: The setting range is available from 0 mVp-p, but accuracy is guaranteed from 10 mVp-p.

*2: The setting range is available from 0 mVp-p, but accuracy is guaranteed from 4 mVp-p.

*3: Available when MU195050A-001 is installed.

(2) Connection for CMI/DMI evaluation

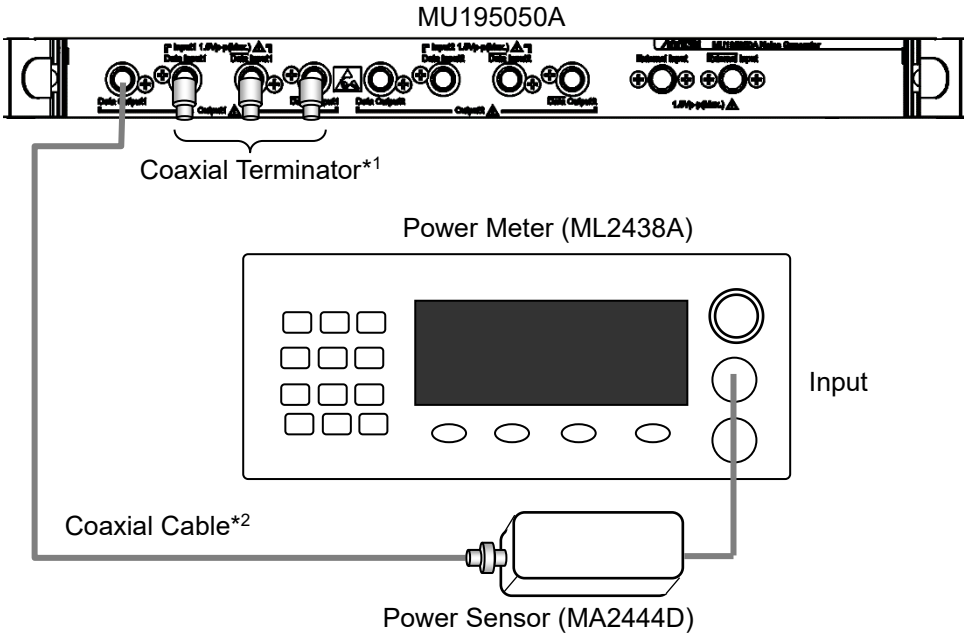


Figure 5.3.2.1.6-1 Connection for CMI/DMI Test

*1: J1632A or Equivalent

*2: J1741A or Equivalent (0.8 m, K connector)

(3) Connection for White noise evaluation

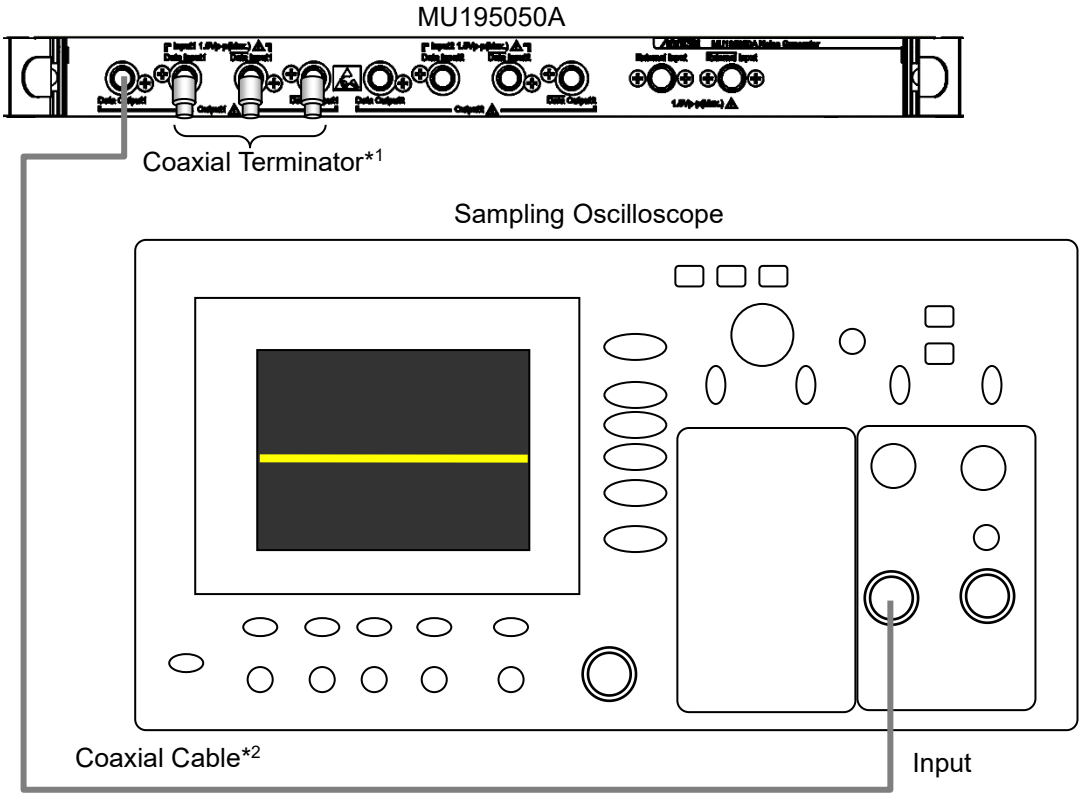


Figure 5.3.2.1.6-2 Connection for White Noise Test

*1: J1632A or Equivalent

*2: J1741A or Equivalent (0.8 m, K connector)

(4) Test procedure

CMI/DMI evaluation procedure

1. Install the MU195050A on the MP1900A and install Terminators to the connectors that are not used for the channel measurement. Turn On the MP1900A without connecting the cables to the connectors used for the measurement.
2. Specify output amplitude and frequency of CMI or DMI to be evaluated by the MU195050A module application.
3. When the setup is completed, turn Off the MP1900A.
4. Refer to Figure 5.3.2.1.6-1 “Connection for CMI/DMI Test” and connect the MU195050A and the Power Meter by coaxial cable.
5. Turn On the MP1900A and the Power Meter for warming up.
6. After warming up, turn On the MU195050A connector to test and output signal. Turn Off the connector outputs that are not tested.

7. Measure the power of output amplitude by Power Meter and check that all the items meet the standard.
8. Perform the measurement in Step 7 for every Data output and XData output.

White noise evaluation procedure

1. Install the MU195050A on the MP1900A and install Terminators to the output connectors that are not used for the measurement. Turn On the MP1900A without connecting the cables to the connectors used for the measurement.
2. Specify the output amplitude of White noise on the MU195050A module application.
3. When the setup is completed, turn Off the MP1900A.
4. Refer to Figure 5.3.2.1.6-2 “Connection for White Noise Test” and connect the MU195050A and the sampling oscilloscope by coaxial cable.
5. Turn On the MP1900A and the sampling oscilloscope for warming up.
6. After warming them up, turn On the White noise output of the MU195050A to output signal. Turn Off the connector outputs that are not tested.
7. Set the sampling oscilloscope to 50 GHz band and Free Run to observe the MU195050A output waveform. Make sure that all items meet the standards. Measure the output level of White noise by histogram (1σ = rms).
8. Perform the measurement in Step 7 for every Data output and XData output.

5.3.2.2 MU196020A/MU196040A/B

This section describes the following test items.

- Operating frequency range
- Waveform evaluation test
- Input level
- Pattern
- Error detection
- Self-loopback test

5.3.2.2.1 Operating frequency range

(1) Specifications

Table 5.3.2.2.1-1 Specifications

Option	Specifications
MU196020A-001	2.4 to 32.1 Gbit/s (Gbaud)
MU196020A-002, y12	2.4 to 58.2 Gbit/s (Gbaud)
MU196020A-003, y23	2.4 to 64.2 Gbit/s (Gbaud)
MU196040A-001 or MU196040B-001*	2.4 to 32.1 Gbit/s (Gbaud)
MU196040B-002, y12*	2.4 to 58.2 Gbaud 2.4 to 64.2 Gbit/s

*: For the MU196040B with Option 005, 115, or 125 installed, refer to Figure 5.3.2.3.1-1 for specifications.

(2) Device connection

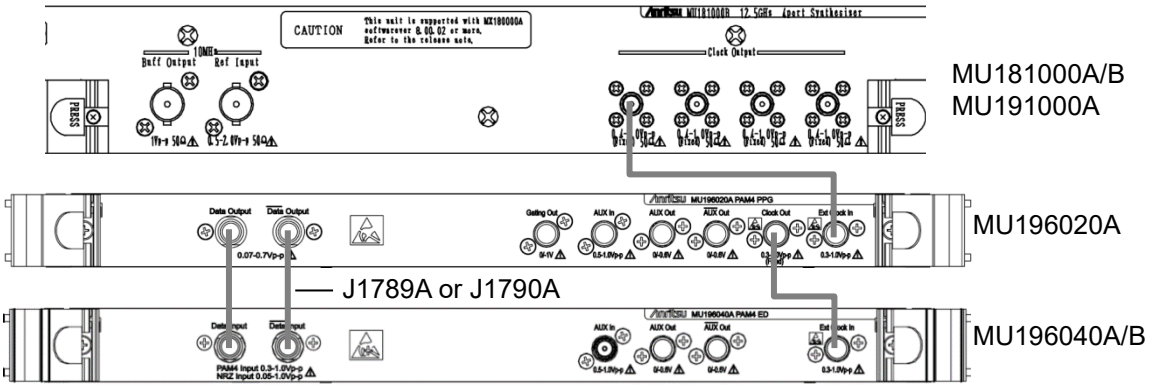


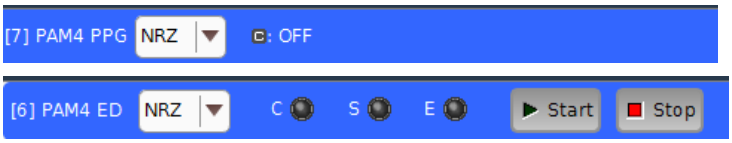
Figure 5.3.2.2.1-1 Connection Diagram for Operating Frequency Range Test

Note:

When using the MU181000A instead of the MU181000B or MU191000A, the 6 dB Coaxial Attenuator must be connected to the MU181000A Clock Output connector before connecting the measuring instrument cables.

(3) Procedure

1. Mount the MU196020A onto the MP1900A, and turn on the MP1900A with the cables unconnected.
2. Set the modulation scheme of the MU196020A and MU196040A/B to **NRZ**.



3. On the **Output** tab of the MU196020A, set **Amplitude** to 0.500 Vp-p, and **Offset** to 0.000 V and Vth.
4. On the **Pattern** tab of the MU196020A, set **Test Pattern** to **PRBS** and **Length** to **2^31–1**.
5. Turn off the MP1900A when setting the parameters completely.
6. Connect the measuring instrument cables as shown in Figure 5.3.2.2.1-1.
7. Turn on the MP1900A and the measuring instruments, and warm them up.
8. After warming up the instruments, turn on the MP1900A signal output and output MU196020A signals.
   There is a warm-up status indicator for the MU196020A. The indicator is turned on after the signals are output, and is turned off when the instruments are warmed up.



9. Adjust the phase and threshold voltage of the MU196040A/B to the optimum values.
10. Check that no error is detected by the MU196040A/B.
11. While varying the operating frequency in the following range different by model and option, check that no error has occurred in the range.

    MU196040A-001, MU196040B-001: 2.4 to 32.1 Gbit/s (Gbaud)

    MU196040B-002, y12: 2.4 to 64.2 Gbit/s, 2.4 to 58.2 Gbaud

    MU196040A and MU196040B-001 do not support the test of the operating frequency exceeding 32.1 Gbit/s (Gbaud).

    To check the MU196020A's performance at more than 32.1 Gbit/s when using the MU196040A and MU196040B-001, refer to 5.3.2.2.2, "Waveform evaluation test".

    For the MU196040B-002 or y12, tests above 58.2 Gbaud are not covered by the performance guarantee.

To verify the MU196020A performance above 58.2 Gbaud when using the MU196040B-002 or y12, refer to 5.3.2.2.2 “Waveform evaluation test”.

5.3.2.2.2 Waveform evaluation test

(1) Specifications

Table 5.3.2.2.2-1 Specifications for MU196020A

Item	Conditions	Specification
Amplitude	0.07 to 0.70 Vp-p*1, *2, *3, *4 0.07 to 0.60 Vp-p*5 0.07 to 0.55 Vp-p*6	±35 mV ±12 % of amplitude
Offset (Vth)	$-2.0-\frac{\text{Amp}}{2}$ to $+3.3-\frac{\text{Amp}}{2}$ V	±65 mV ±10 % of offset (Vth) ±(Eye Amplitude Accuracy / 2)*7, *8
Cross point*11	Amplitude: 0.50 Vp-p	Fixed at 50 %
Tr/Tf*11	Amplitude: 0.50 Vp-p	9.0 ps (20 to 80 %)*1, *7, *9 8.5 ps (20 to 80 %)*2, *3, *7, *9 9.5 ps (20 to 80 %)*4, *7, *9 8.8 ps (20 to 80 %)*5, *6, *7, *9
Jitter*10,*11,*12	Amplitude: 0.50 Vp-p	6.0 ps p-p*1, *2, *3, *4, *5, *6, *9 600 fs rms*1, *2, *3, *4, *5, *6, *9

*1: When using the J1789A cable with MU196020A-001, at 32.1 Gbit/s

*2: When using the J1789A cable with MU196020A-002, at 58.2 Gbit/s

*3: When using the J1789A cable with MU196020A-003, at 64.2 Gbit/s

*4: When using the J1790A cable with MU196020A-001, at 32.1 Gbit/s

*5: When using the J1790A cable with MU196020A-002, at 58.2 Gbit/s

*6: When using the J1790A cable with MU196020A-003, at 64.2 Gbit/s

*7: Except when **Emphasis** is turned **On** with the MU196020A-x11 installed.

*8: For PAM4, when setting each of PAM4 Amplitude (3/2, 2/1 and 1/0) equally to 33 %.

*9: Typical value

*10: The jitter specification value is defined assuming that the oscilloscope with residual jitter less than 200 fs (RMS) is used.

*11: NRZ

*12: Count of measured jitters: 30, at a constant temperature between 20 and 30 °C

(2) Device connection

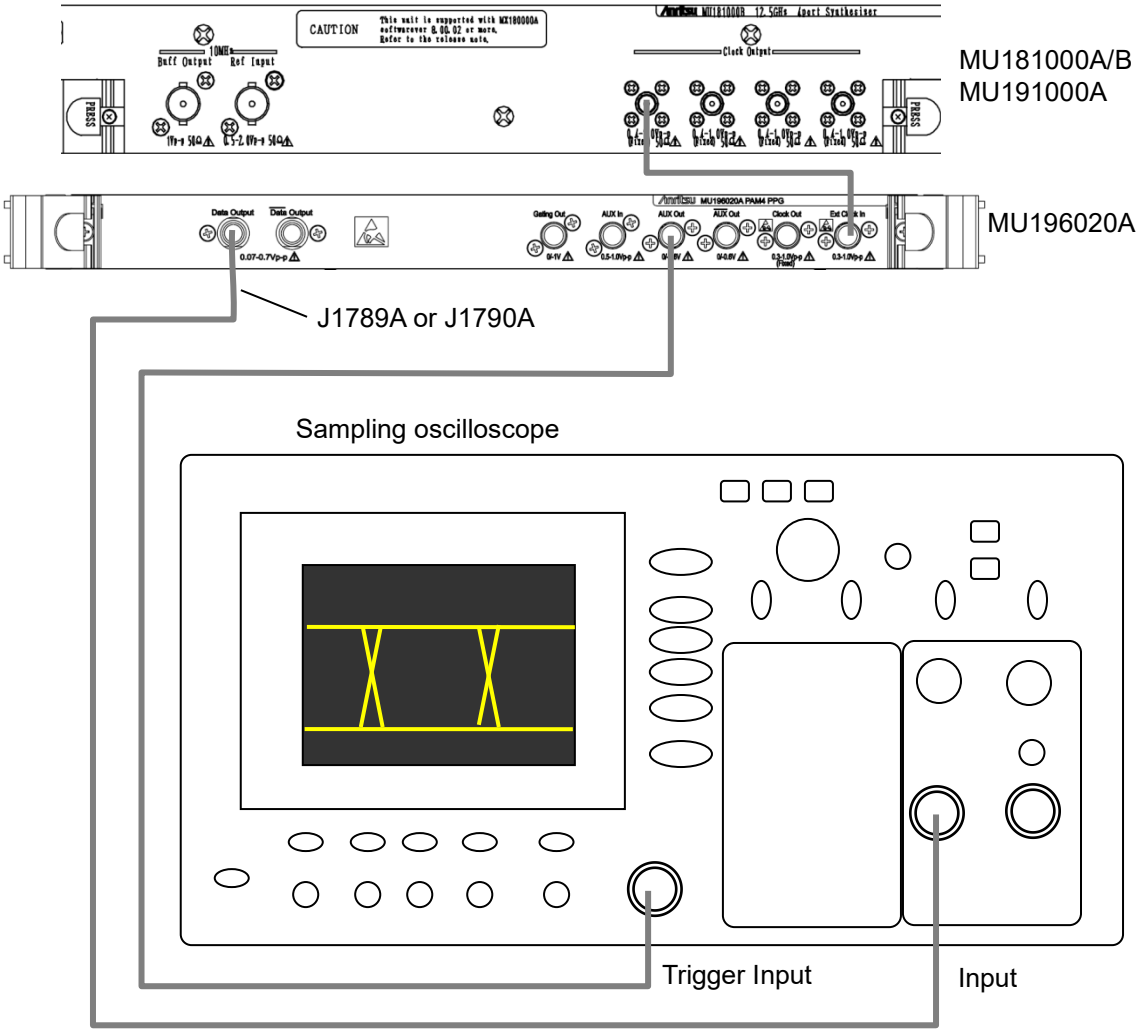


Figure 5.3.2.2.2-1 Connection Diagram for Waveform Test

Note:

When using the MU181000A instead of the MU181000B or MU191000A, connect the 6 dB Coaxial Attenuator connected to the MU181000A Clock Output connector before connecting the measuring instrument cables.

For waveform test, use a sampling oscilloscope that has a 70 GHz band and that has a residual jitter of less than 200 fs (RMS).

(3) Procedure

1. Mount the MU196020A onto the MP1900A, and turn on the MP1900A with the cables unconnected.
2. Set the modulation scheme of the MU196020A to **NRZ**.
3. On the **Output** tab of the MU196020A, set as follows:

Bit Rate	
MU196020A-001	32.100 000
MU196020A-002	58.200 000
MU196020A-003	64.200 000
Ext ATT Factor	0.000
Amplitude	0.070
Offset	AC OFF, 0.000, Vth
Half Period Jitter	0
Delay	0

In the **Cable for Data Output** box, select the model name of the cable used for connection to the sampling oscilloscope.

4. On the **Output** tab of the MU196020A, set the Data output amplitude, offset, and cross point to be tested.
5. On the **Pattern** tab of the MU196020A, set the test pattern.

   Since the specification parameters are evaluated by the eye pattern observation, set the test pattern to PRBS, 2^31–1.
6. Select a trigger signal to input to the sampling oscilloscope. Select 1/N Clock in the AUX Output dropdown list on the **Misc1** tab of the MU196020A, and set the division ratio according to the sampling oscilloscope used.
7. Turn off the MP1900A when setting the parameters completely.
8. Connect the measuring instrument cables as shown in Figure 5.3.2.2.2-1. Be sure to connect the terminators (standard accessories) to the Output connectors to which cables are not connected.
9. Turn on the MP1900A and the measuring instruments, and warm them up.
10. Enable the MP1900A signal output (ON) and output signals.
11. Measure the amplitude with the sampling oscilloscope, and record it.
12. On the **Output** tab of the MU196020A, set the value for **Amplitude**.

When using MU19620A-002 and J1790A cable:	0.600
When using MU19620A-003 and J1790A cable:	0.550
Other than those above:	0.700

13. Measure the amplitude with the sampling oscilloscope, and record it.
14. On the **Output** tab of the MU196020A, set the value for **Offset**.

    When using MU19620A-002 and J1790A cable: –2.300
    When using MU19620A-003 and J1790A cable: –2.275
    Other than those above: –2.350
15. Measure the middle level of the eye with the sampling oscilloscope, and record it.
16. On the **Output** tab of the MU196020A, set **Amplitude** to 0.070 and **Offset** to 3.265.
17. Measure the middle level of the eye with the sampling oscilloscope, and record it.
18. On the **Output** tab of the MU190020A, set **Amplitude** to 0.500 and **Offset** to 0.000.
19. Measure the cross point, Tr/Tf and jitter with the sampling oscilloscope, and record them.
20. Set the modulation scheme of the MU196020A to **PAM4**.
21. On the **Output** tab of the MU196020A, set **Total Amplitude** to 0.070 and select **Even**.
22. Measure the amplitude with the sampling oscilloscope, and record it.
23. On the **Output** tab of the MU196020A, set the value for **Total Amplitude**.

    When using MU19620A-002 and J1790A cable: 0.600
    When using MU19620A-003 and J1790A cable: 0.550
    Other than those above: 0.700
24. Measure the amplitude with the sampling oscilloscope, and record it.
25. On the **Output** tab of the MU196020A, set the value for **Offset**.

    When using MU19620A-002 and J1790A cable: –2.300
    When using MU19620A-003 and J1790A cable: –2.275
    Other than those above: –2.350
26. Measure the middle level of Level 2/1 with the sampling oscilloscope, and record it.
27. On the **Output** tab of the MU196020A, set **Total Amplitude** to 0.070 and **Offset** to 3.265.
28. Measure the middle level of Level 2/1 with the sampling oscilloscope, and record it.
29. Use a coaxial cable to connect the $\overline{\text{Data}}$ Output connector of the MU196020A and the Input connector of the sampling

oscilloscope. Be sure to connect the terminators (standard accessories) to the Output connectors to which cables are not connected. Repeat the procedure from steps 3 to 28.

5.3.2.2.3 Input level

(1) Specifications

Table 5.3.2.2.3-1 Specifications

Option	Specifications	
MU196040A-001	NRZ Input amplitude: PAM4 Input amplitude: Threshold voltage:	0.05 to 1.0 Vp-p 0.3 to 1.0 Vp-p –3.5 to +3.3 V
MU196040B-001*	NRZ Input amplitude: PAM4 Input amplitude: Threshold voltage:	0.05 to 1.0 Vp-p 0.3 to 1.0 Vp-p –3.5 to +3.3 V
MU196040B-002, MU196040B-001+y12 *	NRZ Input amplitude (≤32.1 Gbit/s): NRZ Input amplitude (>32.1 Gbit/s): PAM4 Input amplitude (≤32.1 Gbaud): PAM4 Input amplitude (>32.1 Gbaud): Threshold voltage:	0.05 to 1.0 Vp-p 0.1 to 1.0 Vp-p 0.3 to 1.0 Vp-p 0.4 to 1.0 Vp-p –3.5 to +3.3 V

*: For the MU196040B with Option 005, 115, or 125 installed, refer to Figure 5.3.2.3.3-1 for specifications.

(2) Connection

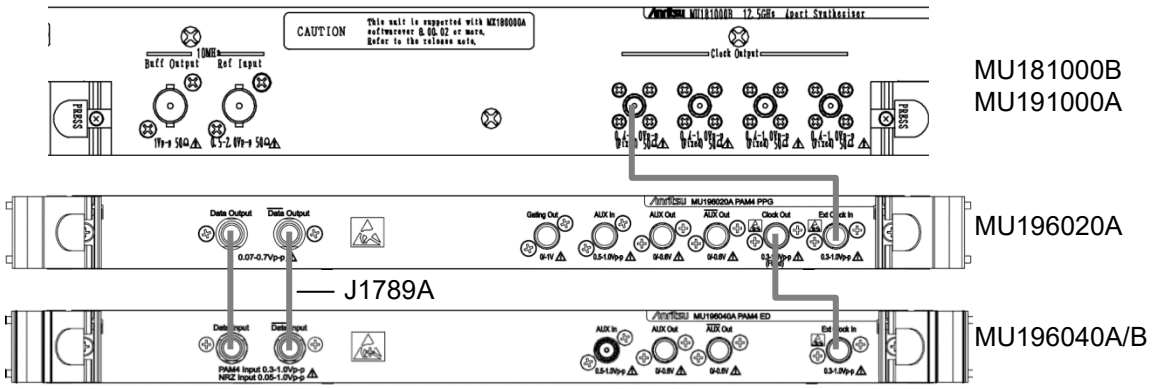


Figure 5.3.2.2.3-1 Connection Diagram for Input Level Test

(3) Procedure

1. Connect devices and configure the settings in the same manner as shown in steps 1 to 5 in Section 5.3.2.2.1.
2. Connect the measuring instrument cables as shown in Figure 5.3.2.2.3-1.
3. Turn on the MP1900A and the measuring instruments, and warm them up.

4. Configure the settings for the MU196020A and MU196040A/B as shown in items 1 to 4 of Table 5.3.2.2.3-2.

   To perform a test at more than 32.1 Gbit/s when using the MU196040B, configure the settings as shown in items 1, 3, 5 and 6 of Table 5.3.2.2.3-2.

5. Set the output of the MU196020A to ON and select **Start** on the MU196040B.

6. Touch **Auto Search**. In the **Mode** list, select **Fine**, and then select **Start**. Check that the threshold voltage and phase are adjusted to optimum values and that no error occurs.

7. Set the modulation scheme of the MU196020A and MU196040A/B to **PAM4**.

8. Configure the settings for the MU196020A and MU196040A/B as shown in items 1 to 4 of Table 5.3.2.2.3-3.

   To perform a test at more than 32.1 Gbaud when using the MU196040B, configure the settings as shown in items 1, 3, 5 and 6 of Table 5.3.2.2.3-3. Also, on the **Input** tab of the MU196040B, in the **Input Condition** box, select **Differential**.

9. Disconnect the cable from the Data Input connector, but leave t the $\overline{\text{Data}}$ Input connector connected. Be sure to connect the terminator (standard accessory) to the Output connector of MU196020A to which a cable is not connected.

10. On the **Input** tab of the MU196040A/B, set **Single-Ended** and **XData** for **Input Condition**. Repeat steps 4 to 8 to make sure that no errors have occurred.

Table 5.3.2.2.3-2 NRZ Input Level Test Settings (MU196040A/B)

No.	MU196020A			MU196040A/B	
	Termination	Amplitude [Vp-p]	Offset (Vth) [V]	Termination	Threshold Voltage [V]*3
1	GND	0.7	–2.35	GND	–2.350
2		0.05*1	–0.225*1		–0.225
3		0.7	+2.95		+2.950
4		0.05*2	+0.305*2		+0.305
5		0.1	–2.05		–2.050
6		0.1	+3.25		+3.250

*1: To output a signal with an amplitude of 0.05 Vp-p and an offset of −0.225 V, connect the Precision Fixed Attenuator 20 dB (optional accessory: 41VA-20) and the Precision Adaptor (optional accessory: 34VFK50) respectively to the Data Output and $\overline{\text{Data}}$ Output connectors of the MU196020A. And, set the MU196020A as follows:

Amplitude: 0.5 Vp-p
Offset: −2.25 V

*2: To output a signal with an amplitude of 0.05 Vp-p and an offset of +0.305 V, connect the Precision Fixed Attenuator 20 dB (optional accessory: 41VA-20) and the Precision Adaptor (optional accessory: 34VFK50) respectively to the Data Output and $\overline{\text{Data}}$ Output connectors of the MU196020A. And, set the MU196020A as follows:
Amplitude: 0.5 Vp-p
Offset: +3.05 V

*3: In the **Mode** list, select **Fine (NRZ)**, and then start Auto Search to adjust the threshold voltage and phase to optimum values.

Table 5.3.2.2.3-3 PAM4 Input Level Test Settings (MU196040A/B)

No.	MU196020A			MU196040A/B	
	Termination	Amplitude [Vp-p]	Offset (Vth) [V]	Termination	Threshold Voltage [V]*
1	GND	0.7	–2.35	GND	Upper: –2.350 + 0.233 (–2.117) Middle: –2.350 Lower: –2.350 – 0.233 (–2.583)
2		0.3	–2.15		Upper: –2.150 + 0.100 (–2.050) Middle: –2.150 Lower: –2.150 – 0.100 (–2.250)
3		0.7	+2.95		Upper: +2.950 + 0.233 (+3.183) Middle: +2.950 Lower: +2.950 – 0.233 (+2.717)
4		0.3	+3.15		Upper: +3.150 + 0.100 (+3.250) Middle: +3.150 Lower: +3.150 – 0.100 (+3.050)
5		0.4	–2.20		Upper: –2.20 + 0.133 (–2.067) Middle: –2.200 Lower: –2.200 – 0.133 (–2.333)
6		0.4	+3.10		Upper: +3.100 + 0.133 (+3.333) Middle: +3.100 Lower: +3.100 – 0.133 (+2.967)

*: In the **Mode** list, select **Fine (PAM4)**, and then start Auto Search to adjust the threshold voltage and phase to optimum values.

Note:

When changing the termination condition, configure the settings of the MU196020A and the MU196040A/B in the following order. The MU196020A and the MU196040A/B may be damaged if the settings are configured in an incorrect order or the termination condition is not set correctly.

(1) Set the output of the MU196020A to OFF.

(2) Set the termination condition for the MU196040A/B to GND.

(3) Change the termination condition for the MU196020A.

(4) Set the termination condition for the MU196040A/B to that for the MU196020A.

5.3.2.2.4 Pattern

(1) Specifications

- PRBS pattern (NRZ, PAM4)
- Zero Substitution pattern (NRZ)
- SSPRQ pattern (PAM4)

(2) Connection

Refer to Figure 5.3.2.2.3-1 for the device connection.

(3) Procedure

1. Configure the settings in the same manner as shown in steps 1 to 5 in Section 5.3.2.2.1.
2. Connect the measuring instrument cables as shown in Figure 5.3.2.2.3-1.
3. Turn on the MP1900A and the measuring instruments, and warm them up.
4. Set the modulation scheme of the MU196020A and MU196040A/B to **NRZ**.
5. Set the output of the MU196020A to ON and select **Start** on the MU196040B. Adjust the phase as required, and check that no error occurs.
6. On the **Pattern** tab of both of the MU196040A/B and the MU196020A, switch the PRBS pattern length to the following values in order, and check that no error occurs.

   2^7–1, 2^9–1, 2^10–1, 2^11–1, 2^13–1, 2^15–1, 2^20–1, 2^23–1, 2^31–1.
7. Set the PRBS pattern length of both MU196040A/B and MU196020A to 2^31–1. Then, verify that no error occurs with the following four combinations of modulation schemes and logic:

Table 5.3.2.2.4-1 Modulation Schemes and Logic Settings

	Modulation Scheme	Logic	Logic MSB	Logic LSB
1	NRZ	POS	–	–
2	NRZ	NEG	–	
3	PAM4	–	POS	POS
4	PAM4	–	NEG	NEG

8. Set the modulation scheme of the MU196020A and MU196040A/B to **NRZ**.
9. For both the MU196040A/B and the MU196020A, set the test pattern to Zero Substitution, then, switch the Length to the following values in order, and check that no error occurs.

2^7, 2^9, 2^10, 2^11, 2^15, 2^20, 2^23,2^7–1, 2^9–1, 2^10–1, 2^11–1, 2^15–1, 2^20–1, 2^23–1.

10. Set the modulation scheme of the MU196020A and MU196040A/B to **PAM4**.
11. Change the test patterns of both MU196040A/B and MU196020A to SSPRQ, and check that no error occurs.

5.3.2.2.5 Error detection

(1) Specifications

Error rate:	0.0000×10^{-16} to 1.0000
Error count:	0 to 1×10^{16}
Error free interval (EFI):	0.0000 to 100.0000 %
Error interval (EI):	0 to 1×10^{16}
Clock frequency:	
MU196040A-001	2.4 to 32.1 GHz,
MU196040B-001	2.4 to 32.1 GHz,
MU196040B-002	2.4 to 64.2 GHz,
Accuracy	±(10 ppm + 1 kHz)

(2) Connection

Refer to Figure 5.3.2.2.3-1 for the device connection.

(3) Procedure

1. Configure the settings in the same manner as shown in steps 1 to 5 in Section 5.3.2.2.1.
2. Connect the measuring instrument cables as shown in Figure 5.3.2.2.3-1.
3. Turn on the MP1900A and the measuring instruments, and warm them up.
4. Set the frequency of the MU181000B or MU191000A to 10 GHz.
5. Set the modulation scheme of the MU196020A and MU196040A/B to **NRZ**.
6. Check that MU196020A is set to NRZ 20 Gbit/s, turn **ON** the Output, and then select **Start** on the MU196040A/B. Adjust the phase as required, and check that no error occurs.
7. Turn On error insertion of the MU196020A, and make sure that the ER measurement results on the **Result** tab of the MU196040A/B match the values set on the **Error Addition** tab on the MU196020A.
8. Set “Single” for error insertion of the MU196020A (set Variation to **Single** on the MU196020A **Error Addition** tab).

9. In the Gating field of the **Measurement** tab of the MU196040A/B, set **Cycle** to **Single**, and set the measurement time to 10 seconds.
10. Touch **Start** on the MU196040A/B. While the measurement is running for 10 seconds, select **Single** once on the **Error Addition** tab of the MU196020A.

    When the measurement has finished, check that the measurement results are as follows.

Error rate (ER):	5.0000E–12
Error count (EC):	1.0000E–00
Error free interval (%EFI):	99.9900 %
Error interval (EI):	1

5.3.2.2.6 Self-loopback test

5.3.2.2.6.1 PAM4 PPG/ED

(1) Specifications

SSC=ON
NRZ: 125 s error free (16.0 Gbit/s, 32.0 Gbit/s)
PAM4: BER<1E-8 (32.0 Gbaud)
SSC=OFF
NRZ: 125 s error free (19.0 to 32.1 Gbit/s)
PAM4: BER<1E-8 (19.0 to 32.1 Gbaud)

(2) Connection

Note:

The connections below are diagrams explaining the connector connections between each MUxxxx module. This differs from the slot position actually inserted into the MP1900A main unit.

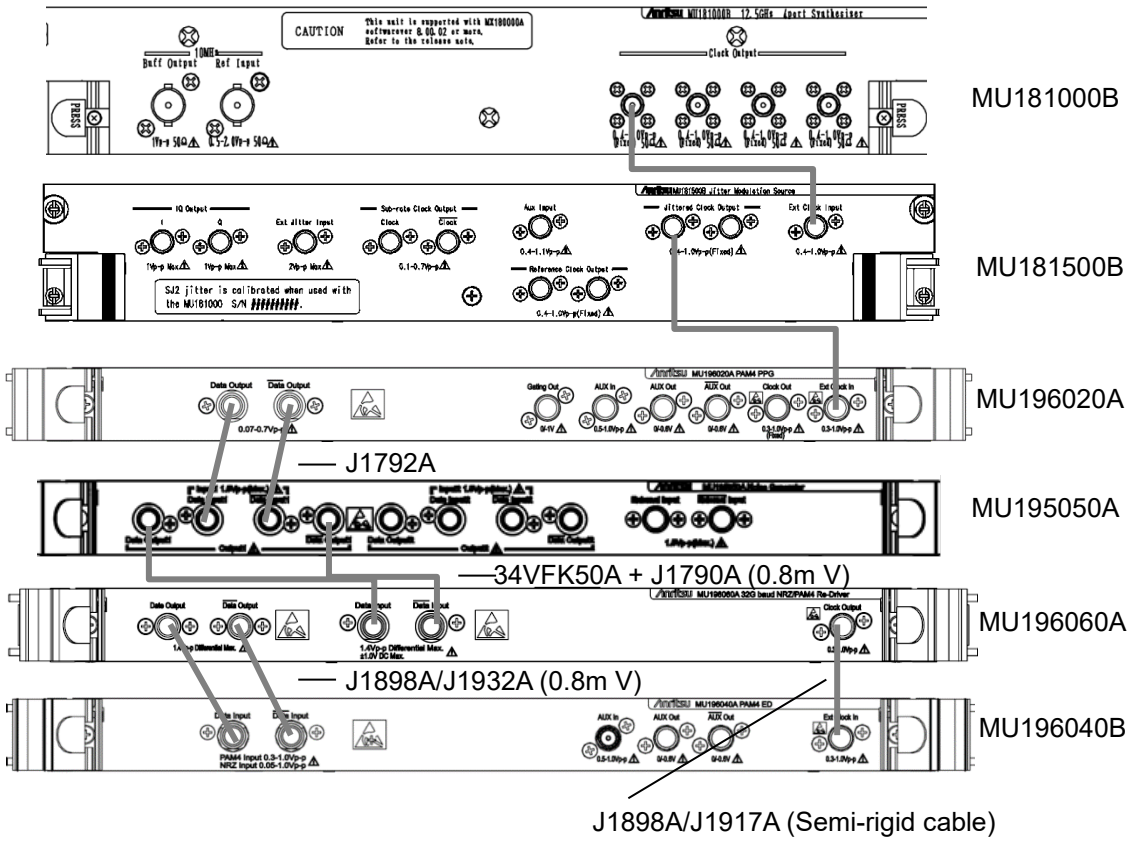


Figure 5.3.2.2.6.1-1 Self-Loopback Test Connection Diagram (When Using PAM4 PPG/ED)

(3) Procedure

Measurement when SSC=ON

1. Connect the measuring instrument cables as shown in Figure 5.3.2.2.6.1-1.
2. Turn on the MP1900A, launch the BERT for PCIe1-6 Application, and then warm up the measuring instruments.
3. Set the modulation scheme of the MU196020A and MU196040B to **NRZ**.
4. On the **Output** tab of the MU196020A, set as follows:
   Bitrate: **PCIe4** (16Gbit/s)
5. On the **Input** tab of the MU196040B, make sure that the following settings are made.
   Input Condition: Differential 50 Ohm
   Clock and Data Recovery: Clock from MU196060A
6. On the **Pattern** tab of each MU196020A and MU196040B, set as follows:
   Test Pattern: MCP in 128b/130b Encoding for PCIe4
7. Set the bitrate of MU196060A's Clock Recovery for SSC as follows:
   Tracking: Unit1:Slot7:MU196020A
8. Set the SSC of the MU181500B as follows, and set it to **On**.
   Type: Down
   Frequency: 33000 Hz
   Deviation: 5300ppm
9. Turn on the MU196020A output, and then select **Auto Search**. Set Advanced to **ON**, and then select **Start**.
   Advanced: ON
   Equalizer:LFE/DFE: OFF (Setup LFE/DFE of MU196040B)
   Equalizer:CTLE: ON (Setup CTLE of MU196060A)
10. On the **Measurement** tab of the MU196040B, set as follows:
    Gating Cycle: Single
    Unit: Time
    00:02:05 (2 min 5 s)
11. Select **Start** for the MU196040B. On the **Result** tab, make sure that the Bit ER measurement result is in an error-free state.
12. On the **Output** tab of the MU196020A, set as follows:
    Bitrate: **PCIe5** (32Gbit/s)
13. Retry steps 9 to 11, and then on the **Result** tab, make sure that the Bit ER measurement result is in an error-free state.
14. Set the modulation scheme of the MU196020A and MU196040B to **PAM4**.

15. On the **Output** tab of the MU196020A, set as follows:
    Baud Rate: **PCIe6** (32Gbaud)
16. On the **Pattern** tab of each MU196020A and MU196040B, set as follows:
    Test Pattern: MCP in 1b/1b Encoding for PCIe6
17. Turn on the MU196020A output, and then select **Auto Search**. Set as follows, and then select **Start**.
    Advanced: ON
    Equalizer:LFE/DFE: OFF (Setup LFE/DFE of MU196040B)
    Equalizer:CTLE: ON (Setup CTLE of MU196060A)
18. Touch **Start** for the MU196040B. On the **Result** tab, make sure that the ER measurement result is less than 1.0E-8.

Measurement when SSC=OFF

19. After performing steps 1 through 18, turn **Off** the SSC of the MU181500B.
20. Make the following settings:
    - Set the modulation scheme of the MU196020A and MU196040B to **NRZ** or **PAM4**.
    - On the **Output** tab, set Bitrate (Baud Rate) to any value in the range of 19 to 32.1 Gbit/s (19 to 32 Gbaud).
    - On the **Pattern** tab, set Test Pattern to **PRBS** and Length to **2^31–1**.
21. Turn on the MU196020A output, and then select **Auto Search**. Try step 9 or 16, and then select **Start**.
22. Touch **Start** for the MU196040B. Make sure the measurement result satisfies the ER value displayed on the **Result** tab.
    NRZ: 125 s error free
    PAM4: Less than 1.0E-8

5.3.2.2.6.2 SI PPG/ED

(1) Specifications

SSC=ON
NRZ: 125 s error free (16Gbit/s, 32.1Gbit/s)

(2) Connection

Note:

The connections below are diagrams explaining the connector connections between each MUxxxx module. This differs from the slot position actually inserted into the MP1900A main unit.

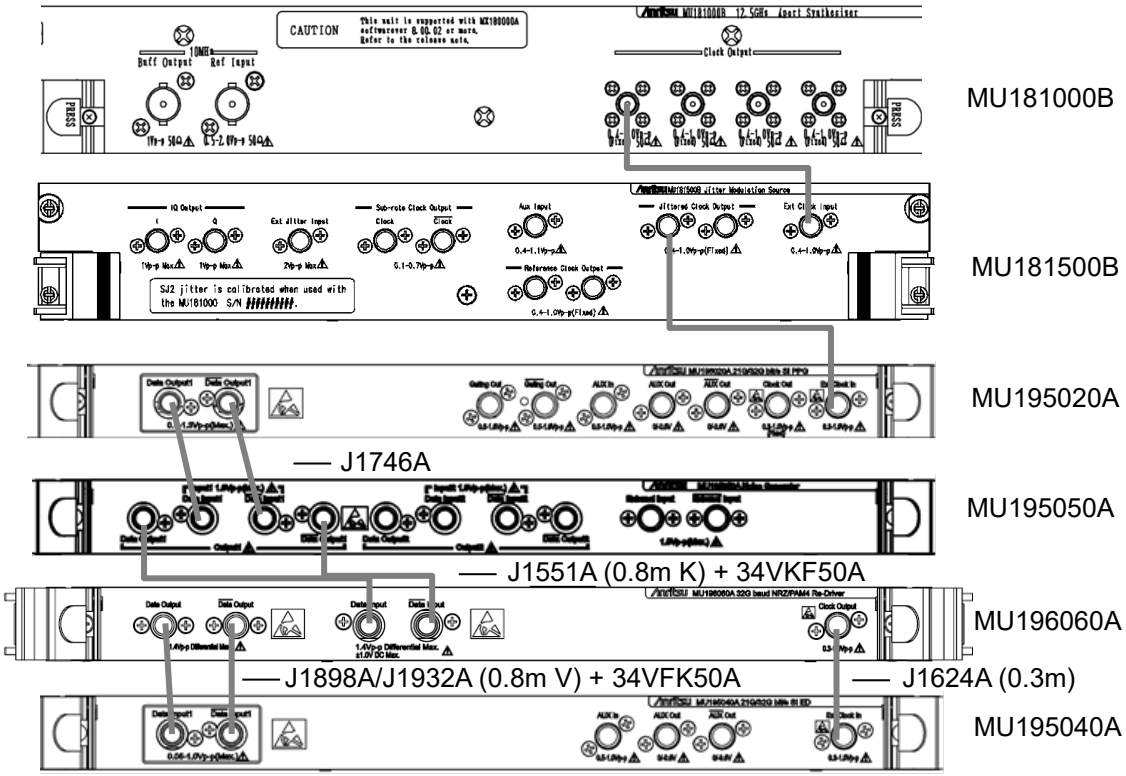


Figure 5.3.2.2.6.2-1 Self-Loopback Test Connection Diagram (When Using SI PPG/ ED)

(3) Procedure

1. Connect the measuring instrument cables as shown in Figure 5.3.2.2.6.2-1.
2. Turn on the MP1900A, launch the Standard BERT for SI Application, and then warm up the measuring instruments.
3. Set the bit rate of the MU195020A to **PCIe4** (16Gbit/s). On the **Emphasis** tab, set Channel Emulator to **On**, open the MU195050A_NOISE.S2P file at DUT S-parameter, and then set Response to **Inverse**.

4. On the **Input** tab of the MU195040B, make sure that the following settings are made.
   Input Condition: Differential 50 Ohm
   Selection: Clock and Data Recovery
   Bitrate: PCIe4
5. On the **Pattern** tab of MU195020A and MU195040A, set **Test Pattern** to **Data**. Open the Pattern Editor from the **Edit** button, select **File**, and set the following from **Open**.
   MU195020A Current Outputting Pattern /
   MU195040A Edit File Name: 128b130b_MCP_L0_Gen4.ptn
6. Set the SSC of the MU181500B as follows, and set it to **On**.
   Type: Down
   Frequency: 33000 Hz
   Deviation: 5300ppm
7. Turn on the MU195020A output, and then select **Auto Search**. Set as follows, and then select **Start**.
   Mode: Fine (NRZ)
   Adjust CTLE Gain: ON
   (Setup CTLE of MU195040A/ MU196060A)
   Assign Slot5 CTLE to: Slot6-1 ED (Slot5: Uses CTLE of MU196060A)
8. On the **Measurement** tab of the MU195040A, set as follows:
   Gating Cycle: Single
   Unit: Time
   00:02:05 (2 min 5 s)
9. Touch **Start** for the MU195040A. On the **Result** tab, make sure that the ER measurement result is in an error-free state.
10. On the **Output** tab of the MU195020A, set as follows:
    Bitrate: **PCIe5** (32Gbit/s)
11. On the **Input** tab of the MU195040A, make sure that the following settings are made.
    Input Condition: Differential 50 Ohm
    Selection: External Clock
12. On the **Pattern** tab of each MU195020A and MU195040A, set as follows:
    MU195020A Current Outputting Pattern /
    MU195040A Edit File Name: 128b130b_MCP_L0_Gen5.ptn
13. Retry steps 7 to 9, and then on the **Result** tab, make sure that the ER measurement result is in an error-free state.

5.3.2.3 MU196020C/MU196040B

This section describes the following test items.

- Operating frequency range
- Waveform evaluation test
- Input level
- Pattern
- Error detection
- Self-loopback test

5.3.2.3.1 Operating frequency range

(1) Specifications

Table 5.3.2.3.1-1 Specifications

Option	Specifications
MU196020C-001	2.4 to 32.1 Gbit/s(Gbaud)
MU196020C-002, y12	2.4 to 58.2 Gbit/s(Gbaud)
MU196020C-003, y23	2.4 to 64.2 Gbit/s(Gbaud)
MU196040B-005, 115, 125*	2.4 to 64.2 Gbit/s(Gbaud)

*: For the MU196040B with Option 001, 002, or y12 installed, refer to Figure 5.3.2.3.1-1 for specifications.

(2) Device connection

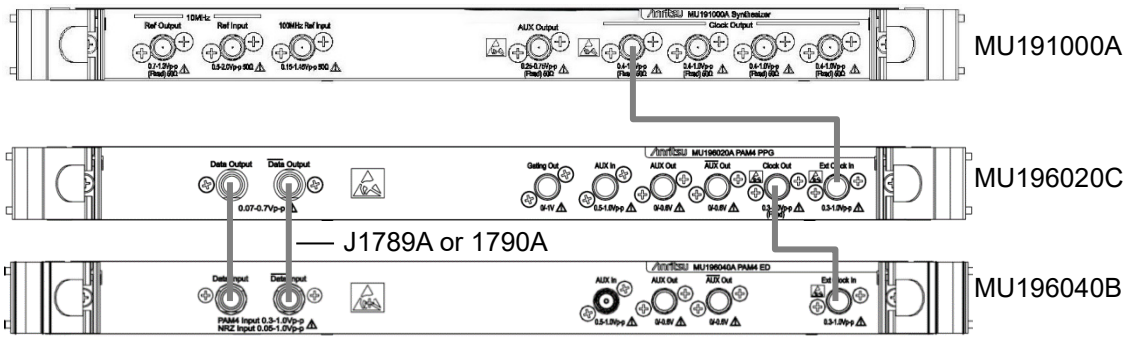
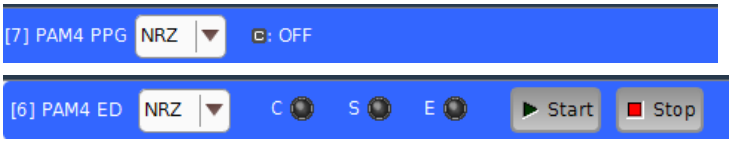


Figure 5.3.2.3.1-1 Connection Diagram for Operating Frequency Range Test

(3) Procedure

1. Mount the MU196020C onto the MP1900A, and turn on the MP1900A with the cables unconnected.
2. Set the modulation scheme of the MU196020C and MU196040A/B to **NRZ**.



3. On the **Output** tab of the MU196020C, set **Amplitude** to 0.500 Vp-p, and **Offset** to 0.000 V and Vth.
4. On the **Pattern** tab of the MU196020C, set **Test Pattern** to **PRBS** and **Length** to **2^31–1**.
5. Turn off the MP1900A when setting the parameters completely.
6. Connect the measuring instrument cables as shown in Figure 5.3.2.3.1-1.
7. Turn on the MP1900A and the measuring instruments, and warm them up.
8. After warming up the instruments, turn on the MP1900A signal output and output MU196020C signals.
   There is a warm-up status indicator for the MU196020C. The indicator is turned on after the signals are output, and is turned off when the instruments are warmed up.



9. Adjust the phase and threshold voltage of the MU196040B to the optimum values.
10. Check that no error is detected by the MU196040B.
11. While varying the operating frequency in the following range different by model and option, check that no error has occurred in the range.

    MU196040B-005: 2.4 to 64.2 Gbit/s (Gbaud)

    For the operating frequency range when using either the MU196040A or the MU196040B with Option 001, 002, or y12, refer to 5.3.2.2.1 “Operating frequency range”.

    To verify the MU196020C performance above its operating frequency range when using either the MU196040A or the MU196040B with Option 001, 002, or y12, refer to 5.3.2.3.2 “Waveform evaluation test”.

5.3.2.3.2 Waveform evaluation test

(1) Specifications

Table 5.3.2.3.2-1 Specifications for MU196020C

Item	Conditions	Specification
Amplitude	0.07 to 0.70 Vp-p*1, *2, *3, *4 0.07 to 0.60 Vp-p*5 0.07 to0.55 Vp-p*6	±35 mV ±12 % of amplitude
Offset (Vth)	$-2.0-\frac{\text{Amp}}{2}$ to $+3.3-\frac{\text{Amp}}{2}$ V	±65 mV ±10% of offset (Vth) ±(Eye Amplitude Accuracy / 2)*7, *8
Cross point*11	Amplitude: 0.50 Vp-p	Fixed at 50 %
Tr/Tf*11	Amplitude: 0.50 Vp-p	9.0 ps (20 to 80%)*1, *7, *9 8.5 ps (20 to 80%)*2, *3, *7, *9 9.5 ps (20 to 80%)*4, *7, *9 8.8 ps (20 to 80%)*5, *6, *7, *9
Jitter*10, *11, *12	Amplitude: 0.50 Vp-p	6.0 ps p-p*1, *2, *3, *4, *5, *6, *9 600 fs rms*1, *2, *3, *4, *5, *6, *9

*1: When using the J1789A cable with MU196020C-001, at 32.1 Gbit/s

*2: When using the J1789A cable with MU196020C-002, at 58.2 Gbit/s

*3: When using the J1789A cable with MU196020C-003, at 64.2 Gbit/s

*4: When using the J1790A cable with MU196020C-001, at 32.1 Gbit/s

*5: When using the J1790A cable with MU196020C-002, at 58.2 Gbit/s

*6: When using the J1790A cable with MU196020C-003, at 64.2 Gbit/s

*7: Except when **Emphasis** is turned **On** with the MU196020C-x11 installed.

*8: For PAM4, when setting each of PAM4 Amplitude (3/2, 2/1 and 1/0) equally to 33 %.

*9: Typical value

*10: The jitter specification value is defined assuming that the oscilloscope with residual jitter less than 200 fs (RMS) is used.

*11: NRZ

*12: Count of measured jitters: 30, at a constant temperature between 20 and 30 °C

(2) Device connection

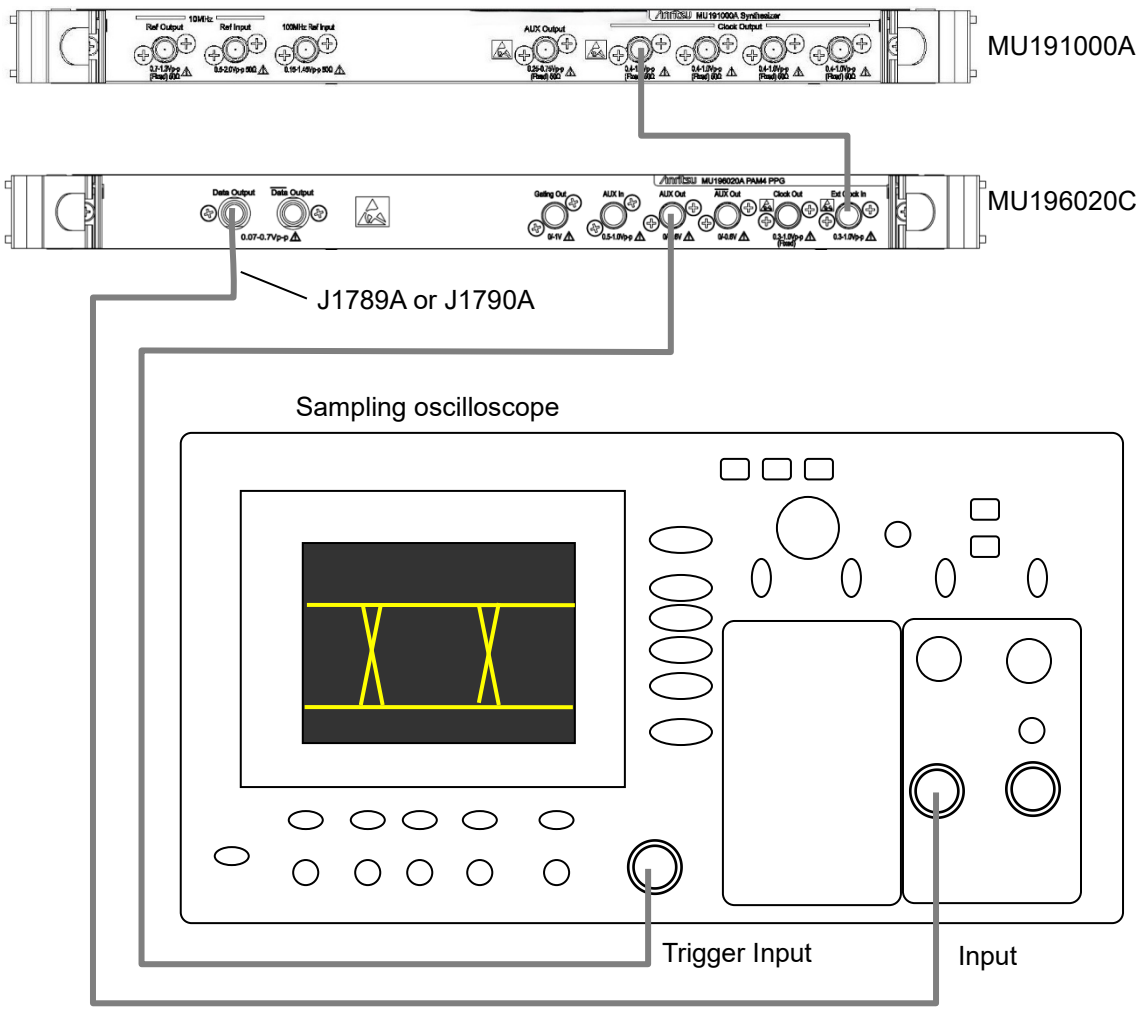


Figure 5.3.2.3.2-1 Connection Diagram for Waveform Test

For waveform test, use a sampling oscilloscope that has a 70 GHz band and that has a residual jitter of less than 200 fs (RMS).

(3) Procedure

1. Mount the MU196020C onto the MP1900A, and turn on the MP1900A with the cables unconnected.
2. Set the modulation scheme of the MU196020C to **NRZ**.
3. On the **Output** tab of the MU196020C, set as follows:

Bit Rate	
MU196020C-001	32.100 000
MU196020C-002	58.200 000
MU196020C-003	64.200 000
Ext ATT Factor	0.000
Amplitude	0.070
Offset	AC OFF, 0.000, Vth
Half Period Jitter	0
Delay	0

   In the **Cable for Data Output** box, select the model name of the cable used for connection to the sampling oscilloscope.
4. On the **Output** tab of the MU196020C, set the Data output amplitude, offset, and cross point to be tested.
5. On the **Pattern** tab of the MU196020C, set the test pattern.

   Since the specification parameters are evaluated by the eye pattern observation, set the test pattern to PRBS, 2^31–1.
6. Select a trigger signal to input to the sampling oscilloscope. Select 1/N Clock in the AUX Output dropdown list on the **Misc1** tab of the MU196020C, and set the division ratio according to the sampling oscilloscope used.
7. Turn off the MP1900A when setting the parameters completely.
8. Connect the measuring instrument cables as shown in Figure 5.3.2.3.2-1. Be sure to connect the terminators (standard accessories) to the Output connectors to which cables are not connected.
9. Turn on the MP1900A and the measuring instruments, and warm them up.
10. Enable the MP1900A signal output (ON) and output signals.
11. Measure the amplitude with the sampling oscilloscope, and record it.
12. On the **Output** tab of the MU196020C, set the value for **Amplitude**.

When using MU19620C-002 and J1790A cable:	0.600
When using MU19620C-003 and J1790A cable:	0.550
Other than those above:	0.700

13. Measure the amplitude with the sampling oscilloscope, and record it.
14. On the **Output** tab of the MU196020C, set the value for **Offset**.

    When using MU19620C-002 and J1790A cable: –2.300
    When using MU19620C-003 and J1790A cable: –2.275
    Other than those above: –2.350
15. Measure the middle level of the eye with the sampling oscilloscope, and record it.
16. On the **Output** tab of the MU196020C, set **Amplitude** to 0.070 and **Offset** to 3.265.
17. Measure the middle level of the eye with the sampling oscilloscope, and record it.
18. On the **Output** tab of the MU190020C, set **Amplitude** to 0.500 and **Offset** to 0.000.
19. Measure the cross point, Tr/Tf and jitter with the sampling oscilloscope, and record them.
20. Set the modulation scheme of the MU196020C to **PAM4**.
21. On the **Output** tab of the MU196020C, set **Total Amplitude** to 0.070 and select **Even**.
22. Measure the amplitude with the sampling oscilloscope, and record it.
23. On the **Output** tab of the MU196020C, set the value for **Total Amplitude**.

    When using MU19620C-002 and J1790A cable: 0.600
    When using MU19620C-003 and J1790A cable: 0.550
    Other than those above: 0.700
24. Measure the amplitude with the sampling oscilloscope, and record it.
25. On the **Output** tab of the MU196020C, set the value for **Offset**.

    When using MU19620C-002 and J1790A cable: –2.300
    When using MU19620C-003 and J1790A cable: –2.275
    Other than those above: –2.350
26. Measure the middle level of Level 2/1 with the sampling oscilloscope, and record it.
27. On the **Output** tab of the MU196020C, set **Total Amplitude** to 0.070 and **Offset** to 3.265.
28. Measure the middle level of Level 2/1 with the sampling oscilloscope, and record it.
29. Use a coaxial cable to connect the $\overline{\text{Data}}$ Output connector of the MU196020C and the Input connector of the sampling

oscilloscope. Be sure to connect the terminators (standard accessories) to the Output connectors to which cables are not connected. Repeat the procedure from steps 3 to 28.

5.3.2.3.3 Input level

(1) Specifications

Table 5.3.2.3.3-1 Specifications

Option	Specifications
MU196040B-005, 115, 125*	NRZ Input amplitude (≤32.1 Gbit/s): 0.05 to 1.0 Vp-p NRZ Input amplitude (>32.1 Gbit/s):0.1 to 1.0 Vp-p PAM4 Input amplitude (≤32.1 Gbaud):0.3 to 1.0 Vp-p PAM4 Input amplitude (>32.1 Gbaud): 0.4 to 1.0 Vp-p Threshold voltage: –3.5 to +3.3 V

*: For the MU196040B with Option 001, 002, or y12 installed, refer to Table 5.3.2.2.3-1 for specifications.

(2) Connection

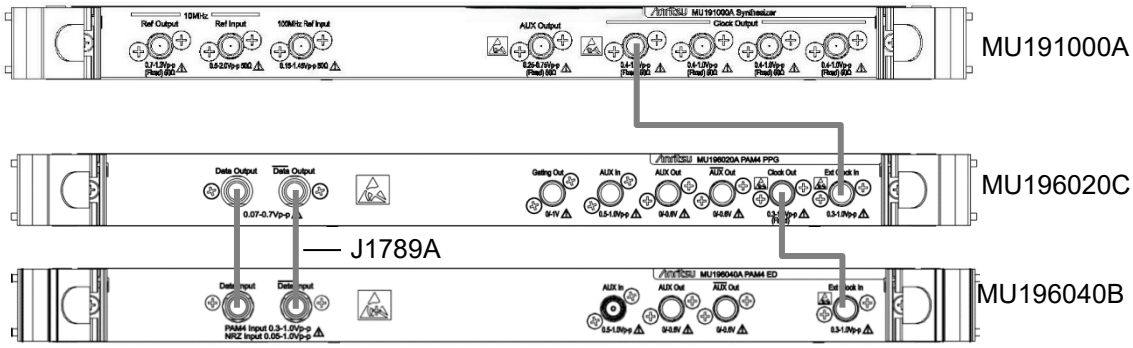


Figure 5.3.2.3.3-1 Connection Diagram for Input Level Test

(3) Procedure

1. Connect devices and configure the settings in the same manner as shown in steps 1 to 5 in Section 5.3.2.3.1.
2. Connect the measuring instrument cables as shown in Figure 5.3.2.3.3-1.
3. Turn on the MP1900A and the measuring instruments, and warm them up.
4. Configure the settings for the MU196020C and MU196040B as shown in items 1 to 4 of Table 5.3.2.3.3-2.

To perform a test at more than 32.1 Gbit/s when using the MU196040B, configure the settings as shown in items 1, 3, 5 and 6 of Table 5.3.2.3.3-2.

5. Set the output of the MU196020A to ON and select **Start** on the MU196040B.
6. Touch **Auto Search**. In the **Mode** list, select **Fine**, and then select **Start**. Check that the threshold voltage and phase are adjusted to optimum values and that no error occurs.
7. Set the modulation scheme of the MU196020C and MU196040B to **PAM4**.
8. Configure the settings for the MU196020A and MU196040A/B as shown in items 1 to 4 of Table 5.3.2.3.3-3.

   To perform a test at more than 32.1 Gbaud when using the MU196040B, configure the settings as shown in items 1, 3, 5 and 6 of Table 5.3.2.3.3-3. Also, on the **Input** tab of the MU196040B, in the **Input Condition** box, select **Differential**.
9. Disconnect the cable from the Data Input connector, but leave t the $\overline{\text{Data}}$ Input connector connected. Be sure to connect the terminator (standard accessory) to the Output connector of MU196020C to which a cable is not connected.
10. On the **Input** tab of the MU196040B, set **Single-Ended** and **XData** for **Input Condition**. Repeat steps 4 to 8 to make sure that no errors have occurred.

Table 5.3.2.3.3-2 NRZ Input Level Test Settings (MU196040B)

No.	MU196020C			MU196040B	
	Termination	Amplitude [Vp-p]	Offset (Vth) [V]	Termination	Threshold Voltage [V]*3
1	GND	0.7	–2.35	GND	–2.350
2		0.05*1	–0.225*1		–0.225
3		0.7	+2.95		+2.950
4		0.05*2	+0.305*2		+0.305
5		0.1	–2.05		–2.050
6		0.1	+3.25		+3.250

*1: To output a signal with an amplitude of 0.05 Vp-p and an offset of −0.225 V, connect the Precision Fixed Attenuator 20 dB (optional accessory: 41VA-20) and the Precision Adaptor (optional accessory: 34VFK50) respectively to the Data Output and $\overline{\text{Data}}$ Output connectors of the MU196020C. And, set the MU196020C as follows:

Amplitude: 0.5 Vp-p
Offset: −2.25 V

*2: To output a signal with an amplitude of 0.05 Vp-p and an offset of +0.305 V, connect the Precision Fixed Attenuator 20 dB (optional accessory: 41VA-20) and the Precision Adaptor (optional accessory: 34VFK50) respectively to the Data Output and $\overline{\text{Data}}$ Output connectors of the MU196020C. And, set the MU196020C as follows:

Amplitude: 0.5 Vp-p
Offset: +3.05 V

*3: In the **Mode** list, select **Fine (NRZ)**, and then start Auto Search to adjust the threshold voltage and phase to optimum values.

Table 5.3.2.3.3-3 PAM4 Input Level Test Settings (MU196040B)

No.	MU196020C			MU196040B	
	Termination	Amplitude [Vp-p]	Offset (Vth) [V]	Termination	Threshold Voltage [V]*
1	GND	0.7	–2.35	GND	Upper: –2.350 + 0.233 (–2.117) Middle: –2.350 Lower: –2.350 – 0.233 (–2.583)
2		0.3	–2.15		Upper: –2.150 + 0.100 (–2.050) Middle: –2.150 Lower: –2.150 – 0.100 (–2.250)
3		0.7	+2.95		Upper: +2.950 + 0.233 (+3.183) Middle: +2.950 Lower: +2.950 – 0.233 (+2.717)
4		0.3	+3.15		Upper: +3.150 + 0.100 (+3.250) Middle: +3.150 Lower: +3.150 – 0.100 (+3.050)
5		0.4	–2.20		Upper: –2.20 + 0.133 (–2.067) Middle: –2.200 Lower: –2.200 – 0.133 (–2.333)
6		0.4	+3.10		Upper: +3.100 + 0.133 (+3.333) Middle: +3.100 Lower: +3.100 – 0.133 (+2.967)

*: In the **Mode** list, select **Fine (PAM4)**, and then start Auto Search to adjust the threshold voltage and phase to optimum values.

Note:

When changing the termination condition, configure the settings of the MU196020C and the MU196040B in the following order. The MU196020C and the MU196040B may be damaged if the settings are configured in an incorrect order or the termination condition is not set correctly.

(1) Set the output of the MU196020C to OFF.

(2) Set the termination condition for the MU196040B to GND.

(3) Change the termination condition for the MU196020C.

(4) Set the termination condition for the MU196040B to that for the MU196020C.

5.3.2.3.4 Pattern

(1) Specifications

- PRBS pattern (NRZ, PAM4)
- Zero Substitution pattern (NRZ)
- SSPRQ pattern (PAM4)

(2) Connection

Refer toFigure 5.3.2.3.3-1 for the device connection.

(3) Procedure

1. Configure the settings in the same manner as shown in steps 1 to 5 in Section 5.3.2.3.1.
2. Connect the measuring instrument cables as shown in Figure 5.3.2.3.3-1.
3. Turn on the MP1900A and the measuring instruments, and warm them up.
4. Set the modulation scheme of the MU196020C and MU196040B to **NRZ**.
5. Set the output of the MU196020C to ON and select **Start** on the MU196040B. Adjust the phase as required, and check that no error occurs.
6. On the **Pattern** tab of both of the MU196040B and the MU196020C, switch the PRBS pattern length to the following values in order, and check that no error occurs.

   2^7–1, 2^9–1, 2^10–1, 2^11–1, 2^13–1, 2^15–1, 2^20–1, 2^23–1, 2^31–1.
7. Set the PRBS pattern length of both MU196040B and MU196020C to 2^31–1. Then, verify that no error occurs with the following four combinations of modulation schemes and logic:

Table 5.3.2.3.4-1 Modulation Schemes and Logic Settings

	Modulation Scheme	Logic	Logic MSB	Logic LSB
1	NRZ	POS	–	–
2	NRZ	NEG	–	
3	PAM4	–	POS	POS
4	PAM4	–	NEG	NEG

8. Set the modulation scheme of the MU196020C and MU196040B to **NRZ**.
9. For both the MU196040B and the MU196020, set the test pattern to Zero Substitution, then, switch the Length to the following values in order, and check that no error occurs.

2^7, 2^9, 2^10, 2^11, 2^15, 2^20, 2^23, 2^7–1, 2^9–1, 2^10–1, 2^11–1, 2^15–1, 2^20–1, 2^23–1

10. Set the modulation scheme of the MU196020C and MU196040B to **PAM4**.
11. Change the test patterns of both MU196040B and MU196020C to SSPRQ, and check that no error occurs.

5.3.2.3.5 Error detection

(1) Specifications

Error rate:	0.0000×10^{-16} to 1.0000
Error count:	0 to 1×10^{16}
Error free interval (EFI):	0.0000 to 100.0000 %
Error interval (EI):	0 to 1×10^{16}
Clock frequency:	
MU196040B-001	2.4 to 32.1 GHz,
MU196040B-002	2.4 to 64.2 GHz,
Accuracy	±(10 ppm + 1 kHz)

(2) Connection

Refer to Figure 5.3.2.3.3-1 for the device connection.

(3) Procedure

1. Configure the settings in the same manner as shown in steps 1 to 5 in Section 5.3.2.3.1.
2. Connect the measuring instrument cables as shown in Figure 5.3.2.3.3-1.
3. Turn on the MP1900A and the measuring instruments, and warm them up.
4. Set the frequency of the MU191000A to 10 GHz.
5. Set the modulation scheme of the MU196020C and MU196040B to **NRZ**.
6. Check that MU196020C is set to NRZ 20 Gbit/s, turn **ON** the Output, and then select **Start** on the MU196040B. Adjust the phase as required, and check that no error occurs.
7. Turn On error insertion of the MU196020C, and make sure that the ER measurement results on the **Result** tab of the MU196040B match the values set on the **Error Addition** tab on the MU196020C.
8. Set "Single" for error insertion of the MU196020C (set Variation to **Single** on the MU196020C **Error Addition** tab).
9. In the Gating field of the **Measurement** tab of the MU196040B, set **Cycle** to **Single**, and set the measurement time to 10 seconds.
10. Touch **Start** on the MU196040B. While the measurement is running for 10 seconds, select **Single** once on the **Error Addition** tab of the MU196020C.

    When the measurement has finished, check that the measurement results are as follows.

    Error rate (ER): 5.0000E–12

Error count (EC):	1.0000E–00
Error free interval (%EFI):	99.9900 %
Error interval (EI):	1

5.3.2.3.6 Self-loopback test

5.3.2.3.6.1 PAM4 PPG/ED

(1) Specifications

SSC=ON
NRZ: 125 s error free (16.0 Gbit/s, 32.0 Gbit/s)
PAM4: BER<1E-8 (32.0 Gbaud)
SSC=OFF
NRZ: 125 s error free (19.0 to 32.1 Gbit/s)
PAM4: BER<1E-8 (19.0 to 32.1 Gbaud)

(2) Connection

Note:

The connections below are diagrams explaining the connector connections between each MUxxxx module. This differs from the slot position actually inserted into the MP1900A main unit.

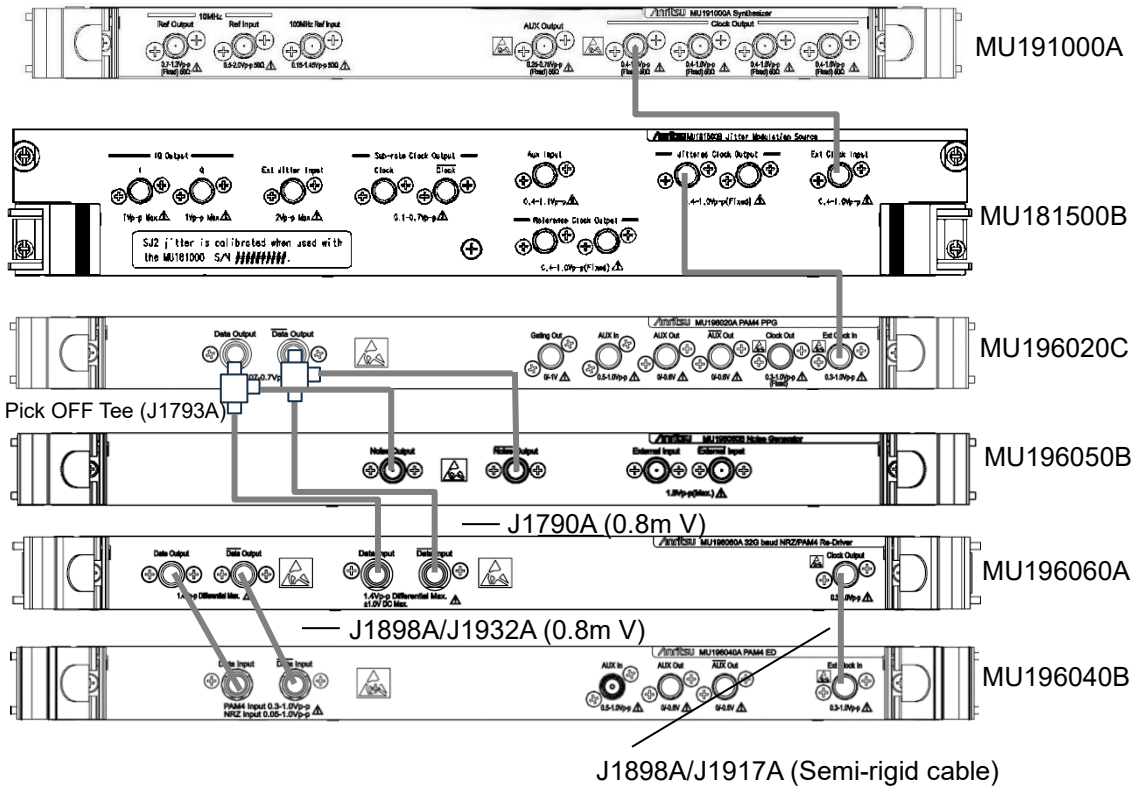


Figure 5.3.2.3.6.1-1 Self-Loopback Test Connection Diagram (When Using PAM4 PPG/ED)

(3) Procedure

Measurement when SSC=ON

1. Connect the measuring instrument cables as shown in Figure 5.3.2.3.6.1-1.
2. Turn on the MP1900A, launch the BERT for PCIe1-6 Application, and then warm up the measuring instruments.
3. Set the modulation scheme of the MU196020C and MU196040B to **NRZ**.
4. On the **Output** tab of the MU196020C, set as follows:
   Bitrate: **PCIe4** (16Gbit/s)
5. On the **Input** tab of the MU196040B, make sure that the following settings are made.
   Input Condition: Differential 50 Ohm
   Clock and Data Recovery: Clock from MU196060A
6. On the **Pattern** tab of each MU196020C and MU196040B, set as follows:
   Test Pattern: MCP in 128b/130b Encoding for PCIe4
7. Set the bitrate of MU196060A's Clock Recovery for SSC as follows:
   Tracking: Unit1:Slot7:MU196020C
8. Set the SSC of the MU181500B as follows, and set it to **On**.
   Type: Down
   Frequency: 33000 Hz
   Deviation: 5300ppm
9. Turn on the MU196020C output, and then select **Auto Search**. Set Advanced to **ON**, and then select **Start**.
   Advanced: ON
   Equalizer:LFE/DFE: OFF (Setup LFE/DFE of MU196040B)
   Equalizer:CTLE: ON (Setup CTLE of MU196060A)
10. On the **Measurement** tab of the MU196040B, set as follows:
    Gating Cycle: Single
    Unit: Time
    00:02:05 (2 min 5 s)
11. Select **Start** for the MU196040B. On the **Result** tab, make sure that the Bit ER measurement result is in an error-free state.
12. On the **Output** tab of the MU196020C, set as follows:
    Bitrate: **PCIe5** (32Gbit/s)
13. Retry steps 9 to 11, and then on the **Result** tab, make sure that the Bit ER measurement result is in an error-free state.
14. Set the modulation scheme of the MU196020C and MU196040B to **PAM4**.

15. On the **Output** tab of the MU196020C, set as follows:
    Baud Rate: **PCIe6** (32Gbaud)
16. On the **Pattern** tab of each MU196020C and MU196040B, set as follows:
    Test Pattern: MCP in 1b/1b Encoding for PCIe6
17. Turn on the MU196020C output, and then select **Auto Search**. Set as follows, and then select **Start**.
    Advanced: ON
    Equalizer:LFE/DFE: OFF (Setup LFE/DFE of MU196040B)
    Equalizer:CTLE: ON (Setup CTLE of MU196060A)
18. Touch **Start** for the MU196040B. On the **Result** tab, make sure that the ER measurement result is less than 1.0E-8.

Measurement when SSC=OFF

19. After performing steps 1 through 18, turn **Off** the SSC of the MU181500B.
20. Make the following settings:
    - Set the modulation scheme of the MU196020C and MU196040B to **NRZ** or **PAM4**.
    - On the **Output** tab, set Bitrate (Baud Rate) to any value in the range of 19 to 32.1 Gbit/s (19 to 32 Gbaud).
    - On the **Pattern** tab, set Test Pattern to **PRBS** and Length to **2^31–1**.
21. Turn on the MU196020C output, and then select **Auto Search**. Try step 9 or 16, and then select **Start**.
22. Touch **Start** for the MU196040B. Make sure the measurement result satisfies the ER value displayed on the **Result** tab.
    NRZ: 125 s error free
    PAM4: Less than 1.0E-8

5.3.2.3.6.2 SI PPG/ED

(1) Specifications

SSC = ON
NRZ: 125 s error free (16Gbit/s, 32.1Gbit/s)

(2) Connection

Note:

The connections below are diagrams explaining the connector connections between each MUxxxx module. This differs from the slot position actually inserted into the MP1900A main unit.

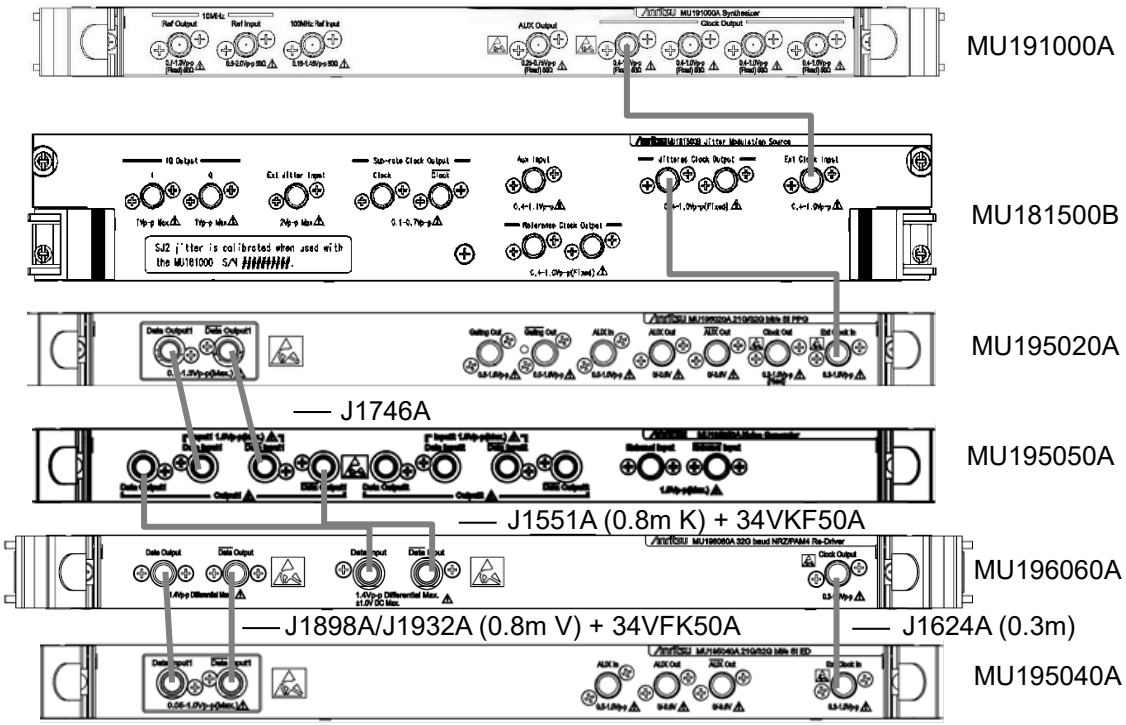


Figure 5.3.2.3.6.2-1 Self-Loopback Test Connection Diagram (When Using SI PPG/ ED)

(3) Procedure

1. Connect the measuring instrument cables as shown in Figure 5.3.2.3.6.2-1.
2. Turn on the MP1900A, launch the Standard BERT for SI Application, and then warm up the measuring instruments.
3. Set the bit rate of the MU195020A to **PCIe4** (16Gbit/s). On the **Emphasis** tab, set Channel Emulator to **On**, open the MU195050A_NOISE.S2P file at DUT S-parameter, and then set Response to **Inverse**.

4. On the **Input** tab of the MU195040B, make sure that the following settings are made.
   Input Condition: Differential 50 Ohm
   Selection: Clock and Data Recovery
   Bitrate: PCIe4
5. On the **Pattern** tab of MU195020A and MU195040A, set **Test Pattern** to **Data**. Open the Pattern Editor from the **Edit** button, select **File**, and set the following from **Open**.
   MU195020A Current Outputting Pattern /
   MU195040A Edit File Name: 128b130b_MCP_L0_Gen4.ptn
6. Set the SSC of the MU181500B as follows, and set it to **On**.
   Type: Down
   Frequency: 33000 Hz
   Deviation: 5300ppm
7. Turn on the MU195020A output, and then select **Auto Search**. Set as follows, and then select **Start**.
   Mode: Fine (NRZ)
   Adjust CTLE Gain: ON
   (Setup CTLE of MU195040A/ MU196060A)
   Assign Slot5 CTLE to: Slot6-1 ED (Slot5: Uses CTLE of MU196060A)
8. On the **Measurement** tab of the MU195040A, set as follows:
   Gating Cycle: Single
   Unit: Time
   00:02:05 (2 min 5 s)
9. Touch **Start** for the MU195040A. On the **Result** tab, make sure that the ER measurement result is in an error-free state.
10. On the **Output** tab of the MU195020A, set as follows:
    Bitrate: **PCIe5** (32Gbit/s)
11. On the **Input** tab of the MU195040A, make sure that the following settings are made.
    Input Condition: Differential 50 Ohm
    Selection: External Clock
12. On the **Pattern** tab of each MU195020A and MU195040A, set as follows:
    MU195020A Current Outputting Pattern /
    MU195040A Edit File Name: 128b130b_MCP_L0_Gen5.ptn
13. Retry steps 7 to 9, and then on the **Result** tab, make sure that the ER measurement result is in an error-free state.

Chapter 6 Maintenance

This chapter describes maintenance of the MP1900A modules.

6.1 Daily Maintenance 6-2
6.2 Cautions on Storage 6-2
6.3 Transportation 6-3
6.4 Calibration 6-3

6.1 Daily Maintenance

- Wipe off any external stains with a cloth damped with diluted mild detergent.
- Vacuum away any accumulated dust or dirt with a vacuum cleaner.
- Tighten any loose parts fixed with screws, using the specified tools.

6.2 Cautions on Storage

Wipe off any dust, soil, or stain on the MP1900A modules prior to storage. Install the supplied Opens or Terminators to the connectors on the panel.

Avoid storing the MP1900A modules in any of the following locations:

- In direct sunlight for extended periods
- Outdoors
- In excessively dusty locations
- Where condensation may occur
- In liquids, such as water, oil, or organic solvents, and medical fluids, or places where these liquids may adhere
- In salty air or in place chemically active gases (sulfur dioxide, hydrogen sulfide, chlorine, ammonia, nitrogen dioxide, or hydrogen chloride etc.) are present
- Where toppling over may occur
- In the presence of lubricating oil mists
- In places at an altitude of more than 2,000 m
- In the presence of frequent vibration or mechanical shock, such as in cars, ships, or airplanes
- Under the following temperature and humidity conditions:
  Temperature range of ≤ –20 °C or ≥ 60 °C
  Humidity range of ≥ 85 %

Recommended storage conditions

In addition to the abovementioned storage cautions, the following environment conditions are recommended for long-term storage.

- Temperature range of 5 to 30 °C
- Humidity range of 40 to 75 %
- Slight daily fluctuation in temperature and humidity

6.3 Transportation

Use the original packing materials, if possible, when packing the MP1900A modules for transport. If you do not have the original packing materials, pack the MP1900A modules according to the following procedure. When handling the MP1900A modules, always wear clean gloves, and handle it gently so as not to damage it.

<Procedure>

1. Use a dry cloth to wipe off any stain or dust on the exterior of the MP1900A module.
2. Check for loose or missing screws.
3. Provide protection for structural protrusions and parts that can easily be deformed, and wrap the MP1900A module with a sheet of polyethylene. Finally, cover with moisture-proof paper.
4. Place the wrapped MP1900A module into a cardboard box, and tape the flaps with adhesive tape. Furthermore, store it in a wooden box as required by the transportation distance or method.
5. During transportation, place it under an environment that meets the conditions described in 6.2 “Cautions on Storage”.

6.4 Calibration

Regular maintenance such as periodic inspections and calibration is essential for the Signal Quality Analyzer-R series for long-term stable performance. Regular inspection and calibration are recommended for using the Signal Quality Analyzer Series in its prime condition at all times. The recommended calibration cycle after delivery of the Signal Quality Analyzer Series is twelve months.

If you require support after delivery, contact an Anritsu Service and Sales office. Contact information can be found on the Anritsu website.

We may not provide calibration or repair if any of the following cases apply.

- Seven or more years have elapsed after production and parts for the instrument are difficult to obtain, or it is determined that reliability cannot be maintained after calibration/repair due to significant wear.
- Circuit changes, repair, or modifications are done without our approval.
- It is determined that the repair cost would be higher than the price of a new item

Chapter 7 Troubleshooting

This chapter describes how to determine if a failure has occurred when a problem occurs during the MP1900A module operation.

7.1 Problems That Occur When Replacing Modules.....7-2
7.2 Problems That Occur During Output Waveform Observation 7-3
7.3 Problems That Occur During Error Rate Measurement.....7-4
7.4 Synchronization Failures 7-5

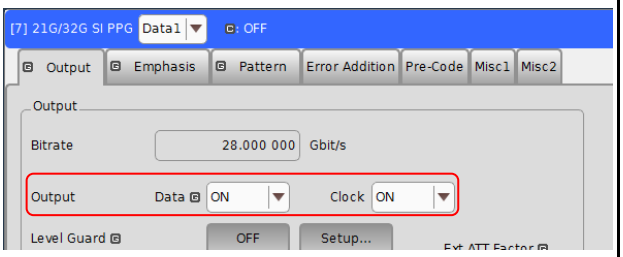
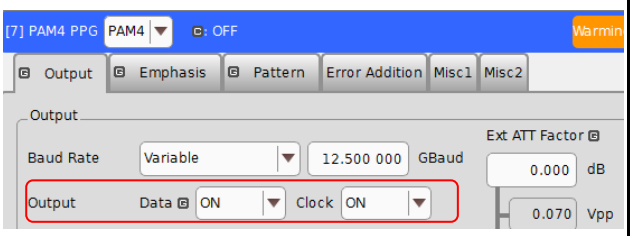
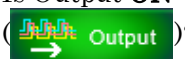
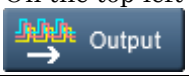
7.1 Problems That Occur When Replacing Modules

Table 7.1-1 Remedies for Problems That Occur When Replacing MP1900A Modules

Symptom	Check Item	Remedy
Module recognition failed.	Is the module(s) installed properly?	Reinstall the module according to 3.3 "Installing and Removing Modules" in the *MP1900A Signal Quality Analyzer-R Operation Manual*.
	Are the appropriate modules installed?	Confirm the MP1900A software version and the supported modules by visiting the MP1900A Series Signal Quality Analyzers-R product information page in the Anritsu web site (https://www.anritsu.com). If the appropriate modulus are not recognized, it may have failed. Contact an Anritsu Service and Sales office. Contact information can be found on the Anritsu website.

7.2 Problems That Occur During Output Waveform Observation

Table 7.2-1 Remedies for Problems That Occur During Waveform Observation

Symptom	Check Item	Remedy
Output waveform cannot be monitored normally.	Is the **Data** or **Clock** on the **Output** tab set to **ON**?	On the **Output** tab, set **Data** or **Clock** to be output to ON. MU195020A  MU196020A  When Output is **OFF**, turn it **ON** by touching the list box.
	Is Output **ON** ()?	On the top left corner of the screen, touch  to turn **ON**.
	Is the operating clock supplied normally?	When using the internal clock, check the bit rate setting. When the clock is supplied externally, check the connection interface. Refer to 3.1 “Panel Layout” for the interface.
	Is the trigger clock set correctly?	It is recommended to use the signal output from the AUX Output connector as the trigger clock. Check the AUX Output connector settings and interface with the sampling oscilloscope which measures the waveforms.
	Is the electrical interface cable loose?	Tighten the connector.
	Do the cables used have good high-frequency characteristics?	Use the cables and connectors that support 65 GHz or higher frequency band. If the bit rate is 32.1 Gbit/s (Gbaud) or less, use the cables and connectors that support 40 GHz or higher frequency band.

7.3 Problems That Occur During Error Rate Measurement

Table 7.3-1 Remedies for Problems That Occur During Error Rate Measurement

Symptom	Check Item	Remedy
An error occurs.	Is the connection interface with the DUT correct?	Check that the data rate, level, offset and termination conditions match those of the DUT.
	Are the logical patterns correctly set on the MU195020A/MU196020A and the error detector (ED)?	Check if the patterns generated by the MU195020A/MU196020A are set such that they can be received by the DUT, and if the set patterns generated by the DUT and detected by the ED are the same. If the DUT outputs the patterns from the MU195020A/MU196020A as they are, connect the MU195020A/MU196020A and ED directly to check if an error is detected. Prevent the bit rate (baud rate) from exceeding 32.1 Gbit/s (Gbaud) when using MU196040A or MU196040B-001.
	Is the error addition function set to off?	On the **Error Addition** tab, check that the Error Addition switch is set to **OFF**.
	Is the electrical interface cable loose?	Tighten the connector.
	Do the cables used have good high-frequency characteristics?	Use the cables and connectors that support 65 GHz or higher frequency band. If the bit rate is 32.1 Gbit/s (Gbaud) or less, use the cables and connectors that support 40 GHz or higher frequency band.
	Are sufficient phase margin and threshold margin are secured?	Adjust the phase and offset to between the MU196020A and the DUT and between the DUT and ED, respectively so that they can be optimal.

7.4 Synchronization Failures

Table 7.4-1 Remedies for Synchronization Failures

Item	Check Item	Remedy
Common		
Input conditions	Do the quality, status and length of the connection cables comply with the specifications?	Replace the cables with appropriate ones in the following cases: • Frequency characteristics are not sufficient. • Loss is large. • Cables and connectors are damaged. • Connectors are contaminated.
	Is the cable connection correct and secure?	Confirm the destination and check if the connector is tightened securely.
	Are the single and differential (50/100 Ω) inputs set correctly?	Set the correct value.
	Is the input level correct?	Check the level by using an oscilloscope, etc.
	Are the input bit rate and clock frequency set correctly?	Set the bit rate and clock frequency correctly. ***Note:*** Use the frequency counter to check the current clock frequency.
	Is the frequency set near the bit rate when using clock recovery?	Set the frequency near the bit rate to be used.
	Has the clock loss display disappeared?	Check the data and clock signals to be input or clock recovery settings.
Termination conditions	Was the termination potential adjusted?	Set the termination potential correctly. ***Note:*** Incorrect setting may result in unit failure.
Clock setting conditions	Do the clock settings for PAM4 PPG and PAM4 ED match?	PAM4 PPG: On the **Misc2** tab, check the settings for **Output Clock Rate** and **Operation Baud Rate** (when **Clock Source** is **External**). On the **Output** tab, check the setting for **Baud Rate**. PAM4 ED: On the **Input** tab, check the setting for **Operation Baud Rate** in the **Clock** area (when **Selection** is set to **External Clock**). On the **Result** tab, check the **Clock Count** or **Frequency** value. ***Note:*** Without properly configured clock settings, expected measurement results cannot be obtained.

Table 7.4-1 Remedies for Synchronization Failures (Cont'd)

Item	Check Item	Remedy
SI		
Threshold	During differential input, is the difference between the Data and XData threshold voltages above 3 V?	The difference value should be within 3 V.
	Is the operating limit for Auto Adjust or Auto Search out of range?	Adjust it manually.
Phase	Is the operating limit for Auto Adjust or Auto Search out of range?	Adjust it manually.
Pattern	Are the patterns matched?	Match the patterns between MU195020A and MU195040A.
Synchronization	Is Auto Sync set to **ON**?	Set it to **ON**. Re-synchronization is performed automatically.
	Have you tried with a different Sync Control setting?	Optimal synchronization method varies according to the pattern type. ***Note:*** Can be set for patterns except PRBS.
Other	Is Bit/Block Window set to **OFF**?	Set it to **OFF**.
	Is MU195040A External Mask set to **OFF**?	Set it to **OFF**.
	Is the **Repeat** mode set?	Set the **Repeat** mode.
PAM4		
PAM4 symbol synchronization conditions	Has symbol synchronization been established between PAM4 MSB and LSB?	In Diagnostics Mode, check that **MSB/LSB Diff** is 0. If it is 0, symbol synchronization has been established. If, on the **Result** tab of the PAM4 ED, either or both of **Upper Eye Threshold** and **Lower Eye Threshold** are set to a voltage within the range of **Middle Eye Height**, "-----" may be displayed in **MSB/LSB Diff**. ***Note:*** MSB**/LSB Diff** must be 0 when performing symbol measurement.
PAM4 Auto Search conditions	Has the Auto Search function failed?	In Diagnostics Mode, check that **MSB/LSB Diff** is within ±48. Make sure the input level is sufficient. ***Note:*** **MSB/LSB Diff** must be within ±48 when performing Auto Search.
PAM4 pattern conditions	Is the pattern of PAM4 MSB and LSB different?	In Diagnostics Mode, check that symbol synchronization can be established between MSB and LSB. As necessary, change the logic polarity and coding condition settings for MSB or LSB.

Appendix A Pseudo-Random Pattern

A.1 Pseudo-Random Pattern A-2
A.2 Zero-Substitution Pattern A-3

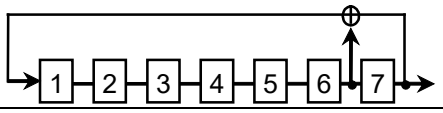
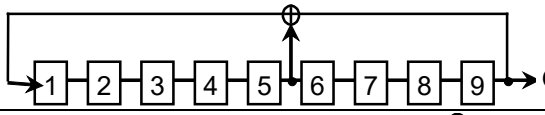
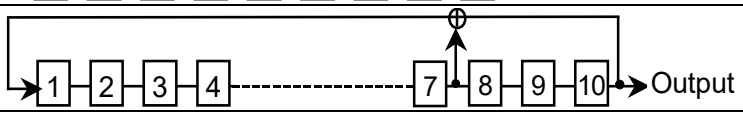
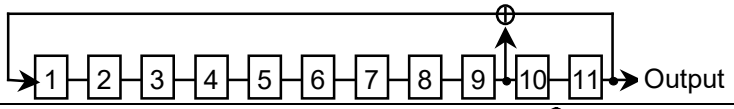
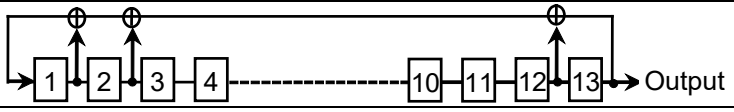
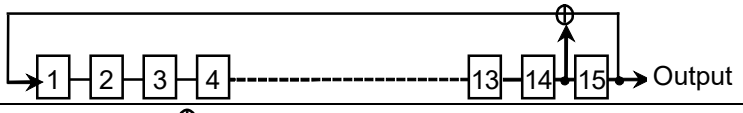
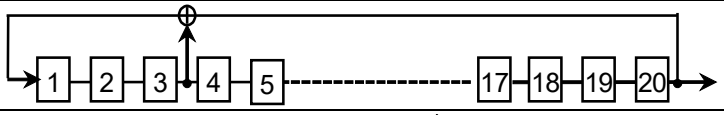
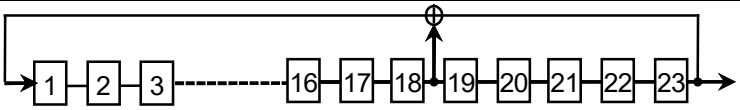
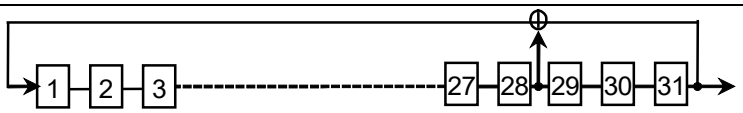
A.1 Pseudo-Random Pattern

Table A.1-1 shows the principle of pseudo-random pattern generation. A pseudo-random pattern is expressed in an N-th degree generating polynomial, with one cycle of 2^n-1. For a PRBS pattern with a cycle of 2^n-1, a pattern of successive "1s" for the number N is generated once in a cycle.

For the output level of the PRBS pattern, "1" indicates the low level and "0" indicates the high level when Logic is set to POS (positive).

The mark ratios of the PRBS pattern are generated as shown in the block diagrams of Table A.1-1.

Table A.1-1 Principle of Pseudo-Random Pattern Generation

Cycle	Generating Polynomial	Pattern Generation Block Diagram
2^7-1	$1 + X^6 + X^7$	
2^9-1	$1 + X^5 + X^9$	
$2^{10}-1$	$1 + X^7 + X^{10}$	
$2^{11}-1$	$1 + X^9 + X^{11}$	
$2^{13}-1$	$1 + X + X^2 + X^{12} + X^{13}$	
$2^{15}-1$	$1 + X^{14} + X^{15}$	
$2^{20}-1$	$1 + X^3 + X^{20}$	
$2^{23}-1$	$1 + X^{18} + X^{23}$	
$2^{31}-1$	$1 + X^{28} + X^{31}$	

N: Shift register (N=1, 2, 3….)

⊕: Exclusive OR

A.2 Zero-Substitution Pattern

A string of successive "0s" for the number of set bits is made by substituting "0" for the pattern that follows the longest bit string of successive 0s in a PRBS pattern. In this event, if the bit immediately after the bit substituted to "0" is also "0", it is inverted to "1".

Example: For a PRBS pattern with a cycle of 2^7, the largest number of successive 0s is 6 bits (7 – 1), and zero substitution starts from the following position:

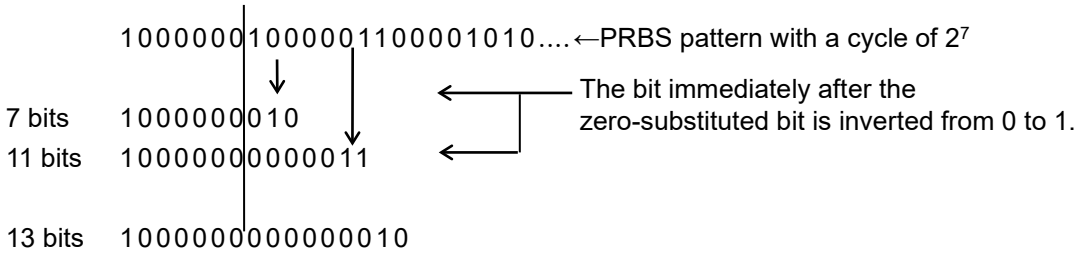


Figure A.2-1 Zero-Substitution Pattern

Appendix B List of Default Settings

Appendix B lists the factory default settings for MU191000A, MU195020A, MU195040A, MU195050A, MU196020A/C, MU196040A/B, MU196050B, and MU196060A.

To initialize all settings, select **Menu** → **Initialize**.

B.1 Synthesizer B-2
B.1.1 MU191000A B-2
B.2 PPG B-3
B.2.1 MU195020A B-3
B.2.2 MU196020A B-9
B.2.3 MU196020C B-31
B.3 ED B-54
B.3.1 MU195040A B-54
B.3.2 MU196040A B-58
B.3.3 MU196040B B-67
B.4 Noise Generator B-83
B.4.1 MU195050A B-83
B.4.2 MU196050B B-84
B.5 Re-Driver B-85
B.5.1 MU196060A B-85

B.1 Synthesizer

B.1.1 MU191000A

Table B.1.1-1 List of MU191000A Initialized Items

Item		Value
Operation Frequency	Operation	Variable
	Center Frequency	12500 MHz*
	Offset	0
Reference Clock	Source	Internal
Spectrum Spread	SSC	OFF
	Spread Method	Down
	Deviation	5000 ppm

*: When the MX190000A is started as PAM4 PPG/ED Based System.

B.2 PPG

B.2.1 MU195020A

Table B.2.1-1 List of MU195020A Initialized Items

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Output	Bitrate			Variable
		Bitrate		10.000 000 Gbit/s
	Data, XData Output			ON
	Clock Output			ON
	Data/XData			
		Level Guard		OFF
		Level Guard Setup	Amplitude	1.000 Vp-p
			Offset limit	–4.000 to 3.300 V
	Defined Interface			Variable
			Amplitude	1.000 Vp-p
			Offset switching	AC OFF
			Offset	0.000 V
			External ATT Factor	0 dB
	Half Period Jitter			0
	Glitch-free			OFF
	Delay			0 mUI
			Calibration	–
		Jitter Input		OFF

Table B.2.1-1 List of MU195020A Initialized Items (Cont'd)

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Emphasis	Manual Setting	Emphasis Function		OFF
		Standard/Preset		USER
				De-Emphasis
				Preset0
		Amplitude		1.000 Vp-p
		Each Cursor Value		0 dB
	ISI	ISI Function		OFF
		Standard/Channel		USER
				–
		Board Type		Not Use
		NF Insertion Loss		10.00 dB
		1/2 NF Insertion Loss		5.00 dB
	Channel Emulator	Channel Emulator Function		OFF
		Response		Inverse

Table B.2.1-1 List of MU195020A Initialized Items (Cont'd)

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Pattern	PRBS	Length		2^15–1
		Logic		POS
		Mark Ratio		1/2
	ZeroSubstitution	Length		2^15
		Zero-Substitution Length		1 bit
		Additional Bit		1
	Data	Logic		POS
		Current Outputting Pattern		No.1
		Length		2 bits At 2ch Combination: 4 bits
		Maximum List Num		1
	Mixed Data	Logic		POS
		Row Length		2048 bits At 2ch Combination: 4096 bits
		Data Length		1024 bits At 2ch Combination: 2048 bits
		Number of Block		1
		Number of Row		1
		PRBS	Pattern	PRBS15
			Mark Ratio	1/2
		Scramble		OFF
		Scramble Setup		All OFF
		PRBS Sequence		Consecutive
	PAM4*1	Logic		POS
		Sequence		PRBS31Q
	Sequence*2	Logic		POS
		PRBS Inversion		ON
		Specification		PCIe1
		Trigger Block No.		1

*1: Configurable when 2ch Combination or 64G x 2ch Combination is set

*2: Configurable when Independent is set
This function is available for the MU195020A-x50.

Table B.2.1-1 List of MU195020A Initialized Items (Cont'd)

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Pattern (Cont'd)	Pattern Editor	Zoom		× 1
		Row Length		2048 bits At 2ch Combination: 4096 bits
		Data Length	Data	2 bits At 2ch Combination: 4 bits
			Mixed	1024 bits At 2ch Combination: 2048 bits (When Mixed-Data is selected)
		Number of Block		1
		Number of Row		1
		Format		Hex
		Edit Mode		Overwrite
	Sequence Editor	Preset	2.5G	P4
			5.0G	P0
			8.0G	P7
			16.0G	P7
			32.0G	P7
		8b10b SKP OS	Symbol Length	COM+3
			Interval	1538
			Symbol Length x2	OFF
		128b130b SKP OS	Symbol Length	16
			Interval	20
			Symbol Length x2	OFF
		Scrambler Seed	8b10b	FFFF
			128b130b	Lane0: 1DBFBC
		Precoding for 32 FT/s		OFF
	8b10b Pattern Editor	Data Length		32 bits
		Notation		Symbol(8b10b)
		Edit Mode		Overwrite
	128b130b Pattern Editor	Data Length		128 bits
		Notation		Hex(Byte)
		Edit Mode		Overwrite
	128b132b Pattern Editor	Data Length		128 bits
		Notation		Hex(Byte)
		Edit Mode		Overwrite

Table B.2.1-1 List of MU195020A Initialized Items (Cont'd)

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Error Addition	Error Addition			OFF
		Source		Internal
		Variation		Repeat
		Route		Select, 1
		Error Rate		1E–3
		When Test Pattern is Mixed Row 1		Data: Unselected PRBS: Unselected
Pre-Code*3	Pre-Code			
		Pre-Code		OFF
		Type		DQPSK
		Initial Data		1
Misc1	Pattern Sequence			Repeat
		Repeat	Pulse Width	128 bits
			Delay	128
		Burst	Source	Internal
			Data Sequence	Restart
			Enable Period	128 000 bits 2ch Combination: Default × 2
			Burst Cycle	12 800 000 bits 2ch Combination: Default × 2
			Delay	0 bits
			Pulse Width	128 000 bits 2ch Combination: Default × 2
	Aux Input			Error Injection
			Vth	0 V
	Aux Output			1/N Clock
		1/N Clock	(Divide ratio)	1/64 clock
		Pattern Sync	For PRBS, Zero-Substitution, Data Position	1 bits
			For Mixed Data Block No. Row No.	1 1
		Burst Output 2	Delay	0
			Pulse Width	128 000 bits 2ch Combination: Default × 2
		Pattern change Trigger		OFF

*3: This function is available for the MU195020A-x20.

Table B.2.1-1 List of MU195020A Initialized Items (Cont'd)

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Misc2	Clock Setting			
		Clock Source*4		External
		Bit Rate		12.500 000 Gbit/s
		Offset		0 ppm
		Output Clock Rate		Half rate
		Reference Clock		Internal
		Operation Bit Rate		2.4 to 32.1

*4: When the MX190000A is started as Miscellaneous System.

B.2.2 **MU196020A**

B.2.2.1 PAM4

Table B.2.2.1-1 Output Tab

Main Item	Secondary Item	Tertiary Item	Default
Baud Rate			Variable
	Baud Rate		12.500 000 Gbaud*
Output	Data		ON
	Clock		ON
Level Guard			OFF
	Level Guard Setup	Total Amplitude	0.800 V
		Offset Max(Voh)	3.300 V
		Offset Min(Vol)	–2.800 V
Glitch-free			OFF
(PAM4 pattern settings)		Offset switching	AC OFF
		Total Amplitude	0.500 Vp-p
		Upper Eye Ratio	33.300 %
		Level2 Voltage	0.083 V
		Offset	0.000 V
		Level1 Voltage	–0.083 V
		Lower Eye Ratio	33.300 %
		External ATT Factor	0.000 dB
Half Period Jitter			0
Cable for Data Output			J1789A 0.4m Cable (Recommend)
Delay			0 mUI
		Calibration	–
	Jitter Input		OFF
	Relative		0 mUI

*: When the MX190000A is started as PAM4 PPG/ED Based System or SI and PAM4 Combined System.

Table B.2.2.1-2 Emphasis Tab

Main Item	Secondary Item	Tertiary Item	Default
Manual Setting	Emphasis		Off
	Standard/Preset		USER
			De-Emphasis
			Preset0
Graph	Total Amplitude		0.500 Vp-p
	Upper Eye		33.300 %
	Lower Eye		33.300 %
	Pre	Cursor2	0.000 dB
		Cursor1	0.000 dB
	Post	Cursor1	0.000 dB
	Coefficient	C-2	0.000 000
		C-1	0.000 000
		C0	1.000 000
		C1	0.000 000
Channel Emulator	Channel Emulator Function		OFF
	Response		Normal
	Graph Mode		Freq. Domain
	Gain Adjust		1 GHz
ISI	ISI Function		OFF
	Standard/Interface		User
	Loss Channel		Not Specified
	Graph Mode		Freq. Domain
	Multi Point Mode		1point
	Tuning NF Insertion Loss		4.0 dB
	Tuning 1/2 NF Insertion Loss		2.0 dB

Table B.2.2.1-3 Pattern Tab

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			All List
	PRBS	Length	2^15–1
		PRBS Inv MSB	ON
		PRBS Inv LSB	ON
		Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Bit Shift	0
		1st Bit	MSB
	Data	Length	4 bits
		Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Bit Shift	0
	Pattern Editor	Data Length	4 bits
		Notation	Hex(Byte)
		Edit Mode	Overwrite
		Cursor Addr	0x00000000
	PRBS23Q, PRBS31Q, PRBS31Q (Infiniband), PRBS31Q (Fibre Channel)	PRBS Inv MSB	ON
		PRBS Inv LSB	ON
		Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Bit Shift	0

Table B.2.2.1-3 Pattern Tab (Cont'd)

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			
	PRBS9Q, PRBS13Q, QPRBS13-CEI, QPRBS31-CEI, PRBS13Q (Infiniband)	PRBS Inv MSB	OFF
		PRBS Inv LSB	OFF
		Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Bit Shift	0
	QPRBS13	Seed	Lane 0
		Gray Coder	ON
		Pre Coder	ON
		Logic MSB	POS
		Logic LSB	POS
		Bit Shift	0
	SSPRQ, JP03A, JP03B, Square Wave, Transmitter Linearity	Logic MSB	POS
		Logic LSB	POS
		Bit Shift	0
	RS-FEC Scrambled Idle 50G 1Lane, RS-FEC Scrambled Idle 100G 1Lane, RS-FEC-Int Scrambled Idle 100G 1Lane	Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Bit Shift	0
	RS-FEC Scrambled Idle 100G 2Lanes, RS-FEC Scrambled Idle 200G 2Lanes, RS-FEC Scrambled Idle 200G 4Lanes, RS-FEC Scrambled Idle 400G 4Lanes, RS-FEC Scrambled Idle 400G 8Lanes	Lane	0
		Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Bit Shift	0

Table B.2.2.1-3 Pattern Tab (Cont'd)

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			
	CP in 1b/1b Encoding for PCIe6	Gray Coder	OFF
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Seed	Lane 0
		EIEOS	ON
	MCP in 1b/1b Encoding for PCIe6	Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Seed	Lane 0
		SRIS	OFF
		SKP	SKPx1
		EIEOS	ON
	Jitter Measurement Pattern in 1b/1b Encoding for PCIe6 High Swing Toggle Pattern in 1b/1b Encoding for PCIe6 Low Swing Toggle Pattern 1b/1b Encoding for PCIe6 Jitter Calibration Pattern for PCIe6 Preset Calibration Pattern for PCIe6	Logic MSB	POS
		Logic LSB	POS
	NOP Flit Layout in a x1 Link	SRIS	OFF
		SKP	SKPx1
		EIEOS	ON
		Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
	NOP Flit Layout in a x2 Link NOP Flit Layout in a x4 Link NOP Flit Layout in a x8 Link NOP Flit Layout in a x16 Link	Lane	0
		SRIS	OFF
		SKP	SKPx1
		EIEOS	ON
		Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS

Table B.2.2.1-3 Pattern Tab (Cont'd)

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			
	Sequence	Specification	PCIe6/CXL3
		Trigger Block No.	1
		Logic	POS
		PRBS Inversion	ON
	Sequence Editor		
	Preset	2.5G	P4
		5.0G	P0
		8.0G	P7
		16.0G	P7
		32.0G	P7
		64.0G	Q0
	SKP OS		
	8b10b	Symbol Length	COM+3
		Interval for Common Clock/SRNS	1538
		Interval for SRIS	152
		Symbol Length x2	OFF
	128b130b	Symbol Length	16
		Interval for Common Clock/SRNS	375
		Interval for SRIS	37
		Symbol Length x2	OFF
	1b1b	Symbol Length	40
		Interval for Common Clock/SRNS	750
		Interval for SRIS	75
		Symbol Length x2	OFF

Table B.2.2.1-3 Pattern Tab (Cont'd)

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			
	SRIS		OFF
	Link Width		x1
	Enable SRIS from Block		1
	Scrambler		
	8b10b	Seed	FFFF
	128b130b/1b1b	Lane	Lane0
		Seed	1DBFBC
	General	Gray Coder	ON
		Pre Coder	OFF
		Seed	Lane 0
		SRIS	OFF
		SKP	ON
		EIEOS	ON
	PCIe/CXL Flit		
	68B NULL Flit SKP OS Interval	Sync Header Bypass	340
		No Sync Header Bypass	375
	256B Flit SKP OS Interval 128b130b	Interval Common Clock/SRNS	23
		Interval for SRIS	2
	256B Flit SKP OS Interval 1b1b	Interval Common Clock/SRNS	46
		Interval for SRIS	4
	8b10b Pattern Editor	Data Length	32
		Notation	Symbol(8b10b)
		MSB/LSB First	MSB First
		Edit Mode	Overwrite
		Cursor Addr	0
	128b130b Pattern Editor	Data Length	128
		Notation	Hex(Byte)
		MSB/LSB First	MSB First
		Edit Mode	Overwrite
		Cursor Addr	0
	1b1b Pattern Editor	Data Length	128
		Notation	Symbol(PAM4)
		MSB/LSB First	MSB First
		Edit Mode	Overwrite
		Cursor Addr	0

Table B.2.2.1-4 Error Addition Tab

Main Item	Secondary Item	Tertiary Item	Default
Error Addition			OFF
	Error Addition Mode		Bit Error on MSB
	Bit Error on MSB	Symbol/Burst	Symbol
		Source	Internal
		Variation	Repeat
		Rate	1E–3
		Burst Length	1 Symbols
	Bit Error on LSB	Symbol/Burst	Symbol
		Source	Internal
		Variation	Repeat
		Rate	1E–3
		Burst Length	1 Symbols
	Bit Error on LSB&MSB	Symbol/Burst	Symbol
		Source	Internal
		Variation	Repeat
		Rate	1E–3
		Burst Length	1 Symbols
		Error Addition Method	Type 4
	RS-FEC Symbol Error	Standard	RS-FEC 50G 1Lane
		Source	Internal
		Variation	Repeat
		Total BER for All Lanes	1E-4
		SER for One Lane	1E-4
		PAM4 Symbol Error per Codeword	1
		Error Addition Method	Type 4

Table B.2.2.1-4 Error Addition Tab (Cont'd)

Main Item	Secondary Item	Tertiary Item	Default
Error Addition	PCIe6 FEC Symbol Error	Standard	x1 Link Common CLK/SRNS Mode
		SKP	No SKP
		Source	Internal
		Variation	Repeat
		Total BER for All Lanes	1E-5
		PAM4 Symbol Error for One Lane	1E-5
		Flit Error Interval	Add every 8 bits (Do not distinguish ECC groups)
		PAM4 Symbol Error per Flit	4
		Flit Error per Control SKP Interval	1
		Error Addition Method	Type 4

Table B.2.2.1-5 Misc1 Tab

Main Item	Secondary Item	Tertiary Item	Default
Pattern Sequence			Repeat
	Gating Output		ON
	Repeat	Pulse Width	256 symbols
		Delay	0 symbols
AUX Input			Error Injection
		Vth	0V
AUX Output			1/N Clock
	1/N Clock	(Divide ratio)	1/64 Clock
	Pattern Sync	Position	1 symbols

Table B.2.2.1-6 Misc2 Tab

Main Item	Secondary Item	Tertiary Item	Default
Clock Setting	Clock Source		Unit1:Slot4:MU181500B*1 Unit1:Slot3:MU181500B*2
	Baud Rate		Variable*1
		Baud Rate	12.500 000 GBaud*1
		Offset*1	0 ppm
	Output Clock Rate		Halfrate
	Reference Clock*1		Internal
	Operation Bit Rate*3		2.40 – 32.10 GBaud

*1: When the MX190000A is started as PAM4 PPG/ED Based System or SI and PAM4 Combined System.

*2: When the MU191000A is installed in Slot1.

*3: When the MX190000A is started as SI PPG/ED Based System or Miscellaneous System.

B.2.2.2 NRZ

Table B.2.2.2-1 Output Tab

Main Item	Secondary Item	Tertiary Item	Default
Bitrate			Variable*
	Bitrate		12.500 000 Gbit/s*
Output	Data		ON
	Clock		ON
Level Guard			OFF
	Level Guard Setup	Amplitude	0.800 V
		Offset Max(Voh)	3.300 V
		Offset Min(Vol)	–2.800 V
Glitch-free			OFF
(NRZ pattern settings)		Amplitude	0.500 Vp-p
		Offset switching	AC OFF
		Offset	0.000 V
		Offset Position	Vth
		External ATT Factor	0.000 dB
Half Period Jitter			0
Cable for Data Output			J1789A 0.4m Cable (Recommend)
Delay			0 mUI
		Calibration	–
	Jitter Input		OFF
	Relative		0 mUI

*: When the MX190000A is started as PAM4 PPG/ED Based System or SI and PAM4 Combined System.

Table B.2.2.2-2 Emphasis Tab

Main Item	Secondary Item	Tertiary Item	Default
Manual Setting	Emphasis Function		Off
	Standard/Preset		USER
			De-Emphasis
			Preset0
Graph	Amplitude		0.500 Vp-p
	Pre	Cursor2	0.000 dB
		Cursor1	0.000 dB
	Post	Cursor1	0.000 dB
	Coefficient	C-2	0.000 000
		C-1	0.000 000
		C0	1.000 000
		C1	0.000 000
Channel Emulator	Channel Emulator Function		OFF
	Response		Normal
	Graph Mode		Freq. Domain
	Gain Adjust		1 GHz
ISI	ISI Function		OFF
	Standard/Interface		User
	Loss Channel		Not Specified
	Graph Mode		Freq. Domain
	Multi Point Mode		1point
	Tuning NF Insertion Loss		4.0 dB
	Tuning 1/2 NF Insertion Loss		2.0 dB

Table B.2.2.2-3 Pattern Tab

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			All List
	PRBS	Length	2^15–1
		Mark Ratio	1/2
		Logic	POS
	Zero Substitution	Length	2^15
		Zero Substitution Length	1 bits
		Additional Bit	1
		Logic	POS
	Data	Length	2
		Logic	POS
	Pattern Editor	Data Length	2
		Notation	Hex(Byte)
		Edit Mode	Overwrite
		Cursor Addr	0x00000000
	SSPR	Logic	POS
	RS-FEC Scrambled Idle 25G 1Lane	Logic	POS
	RS-FEC Scrambled Idle 50G 2Lanes RS(544,514), RS-FEC Scrambled Idle 100G 4Lanes, RS-FEC Scrambled Idle 100G 4Lanes RS(544,514)	Lane	0
		Logic	POS
	CP in 8b/10b Encoding for PCIe1 CP in 8b/10b Encoding for PCIe2	Seed	Lane 0
		Delay Symbol	OFF
		SKP	No SKP
		Logic	POS
	MCP in 8b/10b Encoding for PCIe1 MCP in 8b/10b Encoding for PCIe2	Seed	Lane 0
		Delay Symbol	OFF
		SKP	No SKP
		Logic	POS

Table B.2.2.2-3 Pattern Tab (Cont'd)

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			
	CP in 128b/130b Encoding for PCIe3 CP in 128b/130b Encoding for PCIe4 CP in 128b/130b Encoding for PCIe5	Seed	Lane 0
		Preset	P0
		EIEOS	ON
		SKP	No SKP
		Logic	POS
	MCP in 128b/130b Encoding for PCIe3 MCP in 128b/130b Encoding for PCIe4	SRIS	OFF
		Seed	Lane 0
		EIEOS	ON
		SKP	SKPx1
		Logic	POS
	MCP in 128b/130b Encoding for PCIe5	SRIS	OFF
		Seed	Lane 0
		Pre Coder	ON
		EIEOS	ON
		SKP	SKPx1
		Logic	POS
	Jitter Calibration Pattern for PCIe1 Preset Calibration Pattern for PCIe1 Jitter Calibration Pattern for PCIe2 Preset Calibration Pattern for PCIe2 Jitter Calibration Pattern for PCIe3 Preset Calibration Pattern for PCIe3 Jitter Calibration Pattern for PCIe4 Preset Calibration Pattern for PCIe4 Jitter Calibration Pattern for PCIe5 Preset Calibration Pattern for PCIe5	Logic	POS

Table B.2.2.2-3 Pattern Tab (Cont'd)

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			
	Sequence	Specification	Refer to "Sequence" in Table B.2.2.1-3 Pattern Tab.
		Trigger Block No.	
		Logic	
		PRBS Inversion	
	Sequence Editor		
	Preset	2.5G	
		5.0G	
		8.0G	
		16.0G	
		32.0G	
		64.0G	
	SKP OS		
	8b10b	Symbol Length	
		Interval for Common Clock/SRNS	
		Interval for SRIS	
		Symbol Length x2	
	128b130b	Symbol Length	
		Interval for Common Clock/SRNS	
		Interval for SRIS	
		Symbol Length x2	
	1b1b	Symbol Length	
		Interval for Common Clock/SRNS	
		Interval for SRIS	
		Symbol Length x2	
	SRIS		
	Link Width		
	Enable SRIS from Block		
	Scrambler		
	8b10b	Seed	
	128b130b/1b1b	Lane	
		Seed	

Table B.2.2.2-3 Pattern Tab (Cont'd)

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			
	General	Seed	Lane0
		Delay Symbol	OFF
		SKP	OFF
	PCIe/CXL Flit		Refer to "Sequence" in Table B.2.2.1-3 Pattern Tab.
	68B NULL Flit SKP OS Interval	Sync Header Bypass	
		No Sync Header Bypass	
	256B Flit SKP OS Interval 128b130b	Interval Common Clock/SRNS	
		Interval for SRIS	
	256B Flit SKP OS Interval 1b1b	Interval Common Clock/SRNS	
		Interval for SRIS	
	8b10b Pattern Editor	Data Length	
		Notation	
		MSB/LSB First	
		Edit Mode	
		Cursor Addr	
	128b130b Pattern Editor	Data Length	
		Notation	
		MSB/LSB First	
		Edit Mode	
		Cursor Addr	
	1b1b Pattern Editor	Data Length	
		Notation	
		MSB/LSB First	
		Edit Mode	
		Cursor Addr	

Table B.2.2.2-4 Error Addition Tab

Main Item	Secondary Item	Tertiary Item	Default
Error Addition			OFF
	Error Addition Mode		Bit Error
	Bit Error	Bit/Burst	Bit
		Source	Internal
		Variation	Repeat
		Route	Select
		Rate	1E–3
		Burst Length	1 bits
	RS-FEC Symbol Error	Standard	RS-FEC 25G 1Lane
		Source	Internal
		Variation	Repeat
		Total BER for All Lanes	1E-4
		PAM4 Symbol Error per Codeword	1

Table B.2.2.2-5 Misc1 Tab

Main Item	Secondary Item	Tertiary Item	Default
Pattern Sequence			Repeat
	Gating Output		ON
	Repeat	Pulse Width	256 bits
		Delay	0 bits
	Burst	Source	Internal
		Data Sequence	Restart
		Enable Period	128 000 bits
		Burst Cycle	128 000 000 bits
		Delay	0 bits
		Pulse Width	128 000 bits
AUX Input			Error Injection
		Vth	0V
AUX Output			1/N Clock
	1/N Clock	(Divide ratio)	1/64 Clock
	Pattern Sync	Position	1 bits

Table B.2.2.2-6 Misc2 Tab

Main Item	Secondary Item	Tertiary Item	Default
Clock Setting	Clock Source		Unit1:Slot4:MU181500B*1 Unit1:Slot3:MU181500B*2
	Bit Rate		Variable*1
		Baud Rate	12.500 000 Gbit/s*1
		Offset*1	0 ppm
	Output Clock Rate		Halfrate
	Reference Clock*1		Internal
	Operation Bit Rate*3		2.40 – 32.10 Gbit/s

*1: When the MX190000A is started as PAM4 PPG/ED Based System or SI and PAM4 Combined System.

*2: When the MU191000A is installed in Slot1.

*3: When the MX190000A is started as SI PPG/ED Based System or Miscellaneous System.

B.2.2.3 PAM3

Table B.2.2.3-1 Output Tab

Main Item	Secondary Item	Tertiary Item	Default
Baud Rate			Variable*
	Baud Rate		12.500 000 Gbaud*
Output	Data		ON
	Clock		ON
Level Guard			OFF
	Level Guard Setup	Total Amplitude	0.532 V
		Offset Max(Voh)	3.300 V
		Offset Min(Vol)	–2.800 V
Glitch-free			OFF
(PAM3 pattern settings)		Offset switching	AC OFF
		Total Amplitude	0.300 Vp-p
		Offset	0.000 V
		Level1 Voltage	0.000 V
		Lower Eye Ratio	50.000 %
		External ATT Factor	0.000 dB
Half Period Jitter			0
Cable for Data Output			J1789A 0.4m Cable (Recommend)
Delay			0 mUI
		Calibration	–
	Jitter Input		OFF
	Relative		0 mUI

*: When the MX190000A is started as PAM4 PPG/ED Based System or SI and PAM4 Combined System.

Table B.2.2.3-2 Emphasis Tab

Main Item	Secondary Item	Tertiary Item	Default
Manual Setting	Emphasis		Off
	Standard/Preset		USER
			De-Emphasis
			Preset0
Graph	Total Amplitude		0.300 Vp-p
	Lower Eye		50.000 %
	Pre	Cursor2	0.000 dB
		Cursor1	0.000 dB
	Post	Cursor1	0.000 dB
	Coefficient	C-2	0.000 000
		C-1	0.000 000
		C0	1.000 000
		C1	0.000 000
Channel Emulator	Channel Emulator Function		OFF
	Response		Normal
	Graph Mode		Freq. Domain
	Gain Adjust		1 GHz
ISI	ISI Function		OFF
	Standard/Interface		User
	Loss Channel		Not Specified
	Graph Mode		Freq. Domain
	Multi Point Mode		1point
	Tuning NF Insertion Loss		4.0 dB
	Tuning 1/2 NF Insertion Loss		2.0 dB

Table B.2.2.3-3 Pattern Tab

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			All List
	PRBS	Length	2^15–1
		PRBS Inv	ON
		Polarity Inv	OFF
	Data	Length	4 bits
		Pre Coder	OFF
		Polarity Inv	OFF
	Pattern Editor	Data Length	4 bits
		Notation	Hex(Byte)
		Edit Mode	Overwrite
		Cursor Addr	0x00000000
	PRTS	Length	3^7–1
		Pre Coder	OFF
		Polarity Inv	OFF
	TS2clksw	Pre Coder	OFF
		Polarity Inv	OFF
	USB4 Gen4 Power Management State Signal	USB4 Data	PRBS7
		Pre Coder	OFF
		Polarity Inv	OFF
		PRBS Inv	ON
		tPeriod	50 ns
		Duty Cycle	50 %
		tPreData	100 ns
		Break	Block #1,2,4: Manual Block #3: Auto
		LFPS Swing	High
	USB4 Gen4 Rx Frequency Variation Training Sequence	Pre Coder	OFF
		Polarity Inv	OFF
		PRBS Inv	ON
		Test flow type	Type1
		Break	Flow No3: Manual
		Pattern	Flow #1: PRBS11 Flow #2, 3: PRTS7
		Transmission Time	Flow #3: 2 000 ms
		Test flow type	Type2
		Break	Flow #3: Auto Flow #4: Manual
		Pattern	Flow #1: PRBS11 Flow #2, 4: PRTS7
		Transmission Time	Flow #3: 10.000 us Flow #4: 2 000 ms

Table B.2.2.3-4 Error Addition Tab

Main Item	Secondary Item	Tertiary Item	Default
Error Addition			OFF
	Error Addition Mode		Bit Error on LSB&MSB
	Bit Error on LSB&MSB	Symbol/Burst	Symbol
		Source	Internal
		Variation	Repeat
		Rate	1E–3
		Burst Length	1 Symbols
		Error Addition Method	Type 6

Table B.2.2.3-5 Misc1 Tab

Main Item	Secondary Item	Tertiary Item	Default
Pattern Sequence			Repeat
	Gating Output		ON
	Repeat	Pulse Width	256 symbols
		Delay	0 symbols
AUX Input			Error Injection
		Vth	0V
AUX Output			1/N Clock
	1/N Clock	(Division Ratio)	1/64 Clock
	Pattern Sync	Position	1 symbols

Table B.2.2.3-6 Misc2 Tab

Main Item	Secondary Item	Tertiary Item	Default
Clock Setting	Clock Source		Unit1:Slot4:MU181500B*1 Unit1:Slot3:MU181500B*2
	Baud Rate		Variable*1
		Baud Rate	12.500 000 GBaud*1
		Offset*1	0 ppm
	Output Clock Rate		Halfrate
	Reference Clock*1		Internal
	Operation Bit Rate*3		2.40 – 32.10 GBaud
Insertion Loss Compensation			ON
	Setting Range		0.5 dB

*1: When the MX190000A is started as PAM4 PPG/ED Based System or SI and PAM4 Combined System.

*2: When the MU191000A is installed in Slot1.

*3: When the MX190000A is started as SI PPG/ED Based System or Miscellaneous System.

B.2.3 **MU196020C**

B.2.3.1 PAM4

Table B.2.3.1-1 Output Tab

Main Item	Secondary Item	Tertiary Item	Default
Baud Rate			Variable
	Baud Rate		12.500 000 Gbaud*
Output	Data		ON
	Clock		ON
Level Guard			OFF
	Level Guard Setup	Total Amplitude	0.800 V
		Offset Max(Voh)	3.300 V
		Offset Min(Vol)	–2.800 V
Glitch-free			OFF
(PAM4 pattern settings)		Offset switching	AC OFF
		Total Amplitude	0.500 Vp-p
		Upper Eye Ratio	33.300 %
		Level2 Voltage	0.083 V
		Offset	0.000 V
		Level1 Voltage	–0.083 V
		Lower Eye Ratio	33.300 %
		External ATT Factor	0.000 dB
Half Period Jitter			0
Cable for Data Output			J1789A 0.4m Cable (Recommend)
Delay			0 mUI
		Calibration	–
	Jitter Input		OFF
	Relative		0 mUI

*: When the MX190000A is started as PAM4 PPG/ED Based System or SI and PAM4 Combined System.

Table B.2.3.1-2 Emphasis Tab

Main Item	Secondary Item	Tertiary Item	Default
Manual Setting	Emphasis		Off
	Standard/Preset		USER
			De-Emphasis
			Preset0
Graph	Total Amplitude		0.500 Vp-p
	Upper Eye		33.300 %
	Lower Eye		33.300 %
	Pre	Cursor2	0.000 dB
		Cursor1	0.000 dB
	Post	Cursor1	0.000 dB
	Coefficient	C-2	0.000 000
		C-1	0.000 000
		C0	1.000 000
		C1	0.000 000
Channel Emulator	Channel Emulator Function		OFF
	Response		Normal
	Graph Mode		Freq. Domain
	Gain Adjust		1 GHz
ISI	ISI Function		OFF
	Standard/Interface		User
	Loss Channel		Not Specified
	Graph Mode		Freq. Domain
	Multi Point Mode		1point
	Tuning NF Insertion Loss		4.0 dB
	Tuning 1/2 NF Insertion Loss		2.0 dB

Table B.2.3.1-3 Pattern Tab

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			All List
	PRBS	Length	2^15–1
		PRBS Inv MSB	ON
		PRBS Inv LSB	ON
		Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Bit Shift	0
		1st Bit	MSB
	Data	Length	4 bits
		Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Bit Shift	0
	Pattern Editor	Data Length	4 bits
		Notation	Hex(Byte)
		Edit Mode	Overwrite
		Cursor Addr	0x00000000
	PRBS23Q, PRBS31Q, PRBS31Q (Infiniband), PRBS31Q (Fibre Channel)	PRBS Inv MSB	ON
		PRBS Inv LSB	ON
		Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Bit Shift	0

Table B.2.3.1-3 Pattern Tab (Cont'd)

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			
	PRBS9Q, PRBS13Q, QPRBS13-CEI, QPRBS31-CEI, PRBS13Q (Infiniband)	PRBS Inv MSB	OFF
		PRBS Inv LSB	OFF
		Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Bit Shift	0
	QPRBS13	Seed	Lane 0
		Gray Coder	ON
		Pre Coder	ON
		Logic MSB	POS
		Logic LSB	POS
		Bit Shift	0
	SSPRQ, JP03A, JP03B, Square Wave, Transmitter Linearity	Logic MSB	POS
		Logic LSB	POS
		Bit Shift	0
	RS-FEC Scrambled Idle 50G 1Lane, RS-FEC Scrambled Idle 100G 1Lane, RS-FEC-Int Scrambled Idle 100G 1Lane	Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Bit Shift	0
	RS-FEC Scrambled Idle 100G 2Lanes, RS-FEC Scrambled Idle 200G 2Lanes, RS-FEC Scrambled Idle 200G 4Lanes, RS-FEC Scrambled Idle 400G 4Lanes, RS-FEC Scrambled Idle 400G 8Lanes	Lane	0
		Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Bit Shift	0

Table B.2.3.1-3 Pattern Tab (Cont'd)

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			
	CP in 1b/1b Encoding for PCIe6	Gray Coder	OFF
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Seed	Lane 0
		EIEOS	ON
	MCP in 1b/1b Encoding for PCIe6	Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Seed	Lane 0
		SRIS	OFF
		SKP	SKPx1
		EIEOS	ON
	Jitter Measurement Pattern in 1b/1b Encoding for PCIe6 High Swing Toggle Pattern in 1b/1b Encoding for PCIe6 Low Swing Toggle Pattern 1b/1b Encoding for PCIe6 Jitter Calibration Pattern for PCIe6 Preset Calibration Pattern for PCIe6	Logic MSB	POS
		Logic LSB	POS

Table B.2.3.1-3 Pattern Tab (Cont'd)

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			
	CP in 1b/1b Encoding for PCIe7	Gray Coder	OFF
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Seed	Lane 0
		EIEOS	ON
	MCP in 1b/1b Encoding for PCIe7	Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Seed	Lane 0
		SRIS	OFF
		SKP	SKPx1
		EIEOS	ON
	Jitter Measurement Pattern in 1b/1b Encoding for PCIe7 High Swing Toggle Pattern in 1b/1b Encoding for PCIe7 Low Swing Toggle Pattern x* 1b/1b Encoding for PCIe7 Slow High Swing Toggle Pattern (SHSTP) for PCIe7 Jitter Calibration Pattern for PCIe7 Preset Calibration Pattern for PCIe7	Logic MSB	POS
		Logic LSB	POS
	NOP Flit Layout in a x1 Link	SRIS	OFF
		SKP	SKPx1
		EIEOS	ON
		Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS

*: x = 0 to 4

Table B.2.3.1-3 Pattern Tab (Cont'd)

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			
	NOP Flit Layout in a x2 Link NOP Flit Layout in a x4 Link NOP Flit Layout in a x8 Link NOP Flit Layout in a x16 Link	Lane	0
		SRIS	OFF
		SKP	SKPx1
		EIEOS	ON
		Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS

Table B.2.3.1-4 Error Addition Tab

Main Item	Secondary Item	Tertiary Item	Default
Error Addition			OFF
	Error Addition Mode		Bit Error on MSB
	Bit Error on MSB	Symbol/Burst	Symbol
		Source	Internal
		Variation	Repeat
		Rate	1E–3
		Burst Length	1 Symbols
	Bit Error on LSB	Symbol/Burst	Symbol
		Source	Internal
		Variation	Repeat
		Rate	1E–3
		Burst Length	1 Symbols
	Bit Error on LSB&MSB	Symbol/Burst	Symbol
		Source	Internal
		Variation	Repeat
		Rate	1E–3
		Burst Length	1 Symbols
		Error Addition Method	Type 4
	RS-FEC Symbol Error	Standard	RS-FEC 50G 1Lane
		Source	Internal
		Variation	Repeat
		Total BER for All Lanes	1E-4
		SER for One Lane	1E-4
		PAM4 Symbol Error per Codeword	1
		Error Addition Method	Type 4

Table B.2.3.1-4 Error Addition Tab (Cont'd)

Main Item	Secondary Item	Tertiary Item	Default
Error Addition	PCIe6 FEC Symbol Error	Standard	x1 Link Common CLK/SRNS Mode
		SKP	No SKP
		Source	Internal
		Variation	Repeat
		Total BER for All Lanes	1E-5
		PAM4 Symbol Error for One Lane	1E-5
		Flit Error Interval	Add every 8 bits (Do not distinguish ECC groups)
		PAM4 Symbol Error per Flit	4
		Flit Error per Control SKP Interval	1
		Error Addition Method	Type 4

Table B.2.3.1-5 Misc1 Tab

Main Item	Secondary Item	Tertiary Item	Default
Pattern Sequence			Repeat
	Gating Output		ON
	Repeat	Pulse Width	256 symbols
		Delay	0 symbols
AUX Input			Error Injection
		Vth	0V
AUX Output			1/N Clock
	1/N Clock	(Divide ratio)	1/64 Clock
	Pattern Sync	Position	1 symbols

Table B.2.3.1-6 Misc2 Tab

Main Item	Secondary Item	Tertiary Item	Default
Clock Setting	Clock Source		Unit1:Slot4:MU181500B*1 Unit1:Slot3:MU181500B*2
	Baud Rate		Variable*1
		Baud Rate	12.500 000 GBaud*1
		Offset*1	0 ppm
	Output Clock Rate		Halfrate
	Reference Clock*1		Internal
	Operation Bit Rate*3		2.40 – 32.10 GBaud

*1: When the MX190000A is started as PAM4 PPG/ED Based System or SI and PAM4 Combined System.

*2: When the MU191000A is installed in Slot1.

*3: When the MX190000A is started as SI PPG/ED Based System or Miscellaneous System.

B.2.3.2 NRZ

Table B.2.3.2-1 Output Tab

Main Item	Secondary Item	Tertiary Item	Default
Bitrate			Variable*
	Bitrate		12.500 000 Gbit/s*
Output	Data		ON
	Clock		ON
Level Guard			OFF
	Level Guard Setup	Amplitude	0.800 V
		Offset Max(Voh)	3.300 V
		Offset Min(Vol)	–2.800 V
Glitch-free			OFF
(NRZ pattern settings)		Amplitude	0.500 Vp-p
		Offset switching	AC OFF
		Offset	0.000 V
		Offset Position	Vth
		External ATT Factor	0.000 dB
Half Period Jitter			0
Cable for Data Output			J1789A 0.4m Cable (Recommend)
Delay			0 mUI
		Calibration	–
	Jitter Input		OFF
	Relative		0 mUI

*: When the MX190000A is started as PAM4 PPG/ED Based System or SI and PAM4 Combined System.

Table B.2.3.2-2 Emphasis Tab

Main Item	Secondary Item	Tertiary Item	Default
Manual Setting	Emphasis Function		Off
	Standard/Preset		USER
			De-Emphasis
			Preset0
Graph	Amplitude		0.500 Vp-p
	Pre	Cursor2	0.000 dB
		Cursor1	0.000 dB
	Post	Cursor1	0.000 dB
	Coefficient	C-2	0.000 000
		C-1	0.000 000
		C0	1.000 000
		C1	0.000 000
Channel Emulator	Channel Emulator Function		OFF
	Response		Normal
	Graph Mode		Freq. Domain
	Gain Adjust		1 GHz
ISI	ISI Function		OFF
	Standard/Interface		User
	Loss Channel		Not Specified
	Graph Mode		Freq. Domain
	Multi Point Mode		1point
	Tuning NF Insertion Loss		4.0 dB
	Tuning 1/2 NF Insertion Loss		2.0 dB

Table B.2.3.2-3 Pattern Tab

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			All List
	PRBS	Length	2^15–1
		Mark Ratio	1/2
		Logic	POS
	Zero Substitution	Length	2^15
		Zero Substitution Length	1 bits
		Additional Bit	1
		Logic	POS
	Data	Length	2
		Logic	POS
	Pattern Editor	Data Length	2
		Notation	Hex(Byte)
		Edit Mode	Overwrite
		Cursor Addr	0x00000000
	SSPR	Logic	POS
	RS-FEC Scrambled Idle 25G 1Lane	Logic	POS
	RS-FEC Scrambled Idle 50G 2Lanes RS(544,514), RS-FEC Scrambled Idle 100G 4Lanes, RS-FEC Scrambled Idle 100G 4Lanes RS(544,514)	Lane	0
		Logic	POS
	CP in 8b/10b Encoding for PCIe1 CP in 8b/10b Encoding for PCIe2	Seed	Lane 0
		Delay Symbol	OFF
		SKP	No SKP
		Logic	POS
	MCP in 8b/10b Encoding for PCIe1 MCP in 8b/10b Encoding for PCIe2	Seed	Lane 0
		Delay Symbol	OFF
		SKP	No SKP
		Logic	POS

Table B.2.3.2-3 Pattern Tab (Cont'd)

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			
	CP in 128b/130b Encoding for PCIe3 CP in 128b/130b Encoding for PCIe4 CP in 128b/130b Encoding for PCIe5	Seed	Lane 0
		Preset	P0
		EIEOS	ON
		SKP	No SKP
		Logic	POS
	MCP in 128b/130b Encoding for PCIe3 MCP in 128b/130b Encoding for PCIe4	SRIS	OFF
		Seed	Lane 0
		EIEOS	ON
		SKP	SKPx1
		Logic	POS
	MCP in 128b/130b Encoding for PCIe5	SRIS	OFF
		Seed	Lane 0
		Pre Coder	ON
		EIEOS	ON
		SKP	SKPx1
		Logic	POS
	Jitter Calibration Pattern for PCIe1 Preset Calibration Pattern for PCIe1 Jitter Calibration Pattern for PCIe2 Preset Calibration Pattern for PCIe2 Jitter Calibration Pattern for PCIe3 Preset Calibration Pattern for PCIe3 Jitter Calibration Pattern for PCIe4 Preset Calibration Pattern for PCIe4 Jitter Calibration Pattern for PCIe5 Preset Calibration Pattern for PCIe5	Logic	POS

Table B.2.3.2-3 Pattern Tab (Cont'd)

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			
	Sequence	Specification	Refer to "Sequence".
		Trigger Block No.	
		Logic	
		PRBS Inversion	
	Sequence Editor		
	Preset	2.5G	
		5.0G	
		8.0G	
		16.0G	
		32.0G	
		64.0G	
	SKP OS		
	8b10b	Symbol Length	
		Interval for Common Clock/SRNS	
		Interval for SRIS	
		Symbol Length x2	
	128b130b	Symbol Length	
		Interval for Common Clock/SRNS	
		Interval for SRIS	
		Symbol Length x2	
	1b1b	Symbol Length	
		Interval for Common Clock/SRNS	
		Interval for SRIS	
		Symbol Length x2	
	SRIS		
	Link Width		
	Enable SRIS from Block		
	Scrambler		
	8b10b	Seed	
	128b130b/1b1b	Lane	
		Seed	

Table B.2.3.2-3 Pattern Tab (Cont'd)

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			
	General	Seed	Lane0
		Delay Symbol	OFF
		SKP	OFF
	8b10b Pattern Editor	Data Length	Refer to "Sequence".
		Notation	
		MSB/LSB First	
		Edit Mode	
		Cursor Addr	
	128b130b Pattern Editor	Data Length	
		Notation	
		MSB/LSB First	
		Edit Mode	
		Cursor Addr	
	1b1b Pattern Editor	Data Length	
		Notation	
		MSB/LSB First	
		Edit Mode	
		Cursor Addr	

Table B.2.3.2-4 Error Addition Tab

Main Item	Secondary Item	Tertiary Item	Default
Error Addition			OFF
	Error Addition Mode		Bit Error
	Bit Error	Bit/Burst	Bit
		Source	Internal
		Variation	Repeat
		Route	Select
		Rate	1E–3
		Burst Length	1 bits
	RS-FEC Symbol Error	Standard	RS-FEC 25G 1Lane
		Source	Internal
		Variation	Repeat
		Total BER for All Lanes	1E-4
		BER for One Lane	1E-4
		FEC Symbol Error per Codeword	1

Table B.2.3.2-5 Misc1 Tab

Main Item	Secondary Item	Tertiary Item	Default
Pattern Sequence			Repeat
	Gating Output		ON
	Repeat	Pulse Width	256 bits
		Delay	0 bits
	Burst	Source	Internal
		Data Sequence	Restart
		Enable Period	128 000 bits
		Burst Cycle	12 800 000 bits
		Delay	0 bits
		Pulse Width	128 000 bits
AUX Input			Error Injection
		Vth	0V
AUX Output			1/N Clock
	1/N Clock	(Divide ratio)	1/64 Clock
	Pattern Sync	Position	1 bits

Table B.2.3.2-6 Misc2 Tab

Main Item	Secondary Item	Tertiary Item	Default
Clock Setting	Clock Source		Unit1:Slot4:MU181500B*1 Unit1:Slot3:MU181500B*2
	Bit Rate		Variable*1
		Baud Rate	12.500 000 Gbit/s*1
		Offset*1	0 ppm
	Output Clock Rate		Halfrate
	Reference Clock*1		Internal
	Operation Bit Rate*3		2.40 – 32.10 GBaud

*1: When the MX190000A is started as PAM4 PPG/ED Based System or SI and PAM4 Combined System.

*2: When the MU191000A is installed in Slot1.

*3: When the MX190000A is started as SI PPG/ED Based System or Miscellaneous System.

B.2.3.3 PAM3

Table B.2.3.3-1 Output Tab

Main Item	Secondary Item	Tertiary Item	Default
Baud Rate			Variable*
	Baud Rate		12.500 000 Gbaud*
Output	Data		ON
	Clock		ON
Level Guard			OFF
	Level Guard Setup	Total Amplitude	0.532 V
		Offset Max(Voh)	3.300 V
		Offset Min(Vol)	–2.800 V
Glitch-free			OFF
(PAM3 pattern settings)		Offset switching	AC OFF
		Total Amplitude	0.300 Vp-p
		Offset	0.000 V
		Level1 Voltage	0.000 V
		Lower Eye Ratio	50.000 %
		External ATT Factor	0.000 dB
Half Period Jitter			0
Cable for Data Output			J1789A 0.4m Cable (Recommend)
Delay			0 mUI
		Calibration	–
	Jitter Input		OFF
	Relative		0 mUI

*: When the MX190000A is started as PAM4 PPG/ED Based System or SI and PAM4 Combined System.

Table B.2.3.3-2 Emphasis Tab

Main Item	Secondary Item	Tertiary Item	Default
Manual Setting	Emphasis		Off
	Standard/Preset		USER
			De-Emphasis
			Preset0
Graph	Total Amplitude		0.300 Vp-p
	Lower Eye		50.000 %
	Pre	Cursor2	0.000 dB
		Cursor1	0.000 dB
	Post	Cursor1	0.000 dB
	Coefficient	C-2	0.000 000
		C-1	0.000 000
		C0	1.000 000
		C1	0.000 000
Channel Emulator	Channel Emulator Function		OFF
	Response		Normal
	Graph Mode		Freq. Domain
	Gain Adjust		1 GHz
ISI	ISI Function		OFF
	Standard/Interface		User
	Loss Channel		Not Specified
	Graph Mode		Freq. Domain
	Multi Point Mode		1point
	Tuning NF Insertion Loss		4.0 dB
	Tuning 1/2 NF Insertion Loss		2.0 dB

Table B.2.3.3-3 Pattern Tab

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			All List
	PRBS	Length	2^15–1
		PRBS Inv	ON
		Polarity Inv	OFF
	Data	Length	4 bits
		Pre Coder	OFF
		Polarity Inv	OFF
	Pattern Editor	Data Length	4 bits
		Notation	Hex(Byte)
		Edit Mode	Overwrite
		Cursor Addr	0x00000000
	PRTS	Length	3^7–1
		Pre Coder	OFF
		Polarity Inv	OFF
	TS2clksw	Pre Coder	OFF
		Polarity Inv	OFF
	USB4 Gen4 Power Management State Signal	USB4 Data	PRBS7
		Pre Coder	OFF
		Polarity Inv	OFF
		PRBS Inv	ON
		tPeriod	50 ns
		Duty Cycle	50 %
		tPreData	100 ns
		Break	Block #1,2,4: Manual Block #3: Auto
		LFPS Swing	High

Table B.2.3.3-3 Pattern Tab (Cont'd)

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			
	USB4 Gen4 Rx Frequency Variation Training Sequence	Pre Coder	OFF
		Polarity Inv	OFF
		PRBS Inv	ON
		Test flow type	Type1
		Break	Flow No3: Manual
		Pattern	Flow #1: PRBS11 Flow #2, 3: PRTS7
		Transmission Time	Flow #3: 2 000 ms
		Test flow type	Type2
		Break	Flow #3: Auto Flow #4: Manual
		Pattern	Flow #1: PRBS11 Flow #2, 4: PRTS7
		Transmission Time	Flow #3: 10.000 us Flow #4: 2 000 ms

Table B.2.3.3-4 Error Addition Tab

Main Item	Secondary Item	Tertiary Item	Default
Error Addition			OFF
	Error Addition Mode		Bit Error on LSB&MSB
	Bit Error on LSB&MSB	Symbol/Burst	Symbol
		Source	Internal
		Variation	Repeat
		Rate	1E–3
		Burst Length	1 Symbols
		Error Addition Method	Type 6

Table B.2.3.3-5 Misc1 Tab

Main Item	Secondary Item	Tertiary Item	Default
Pattern Sequence			Repeat
	Gating Output		ON
	Repeat	Pulse Width	256 symbols
		Delay	0 symbols
AUX Input			Error Injection
		Vth	0V
AUX Output			1/N Clock
	1/N Clock	(Divide ratio)	1/64 Clock
	Pattern Sync	Position	1 symbols
		Pattern Change Trigger	OFF

Table B.2.3.3-6 Misc2 Tab

Main Item	Secondary Item	Tertiary Item	Default
Clock Setting	Clock Source		Unit1:Slot4:MU181500B*1 Unit1:Slot3:MU181500B*2
	Baud Rate		Variable*1
		Baud Rate	12.500 000 GBaud*1
		Offset*1	0 ppm
	Output Clock Rate		Halfrate
	Reference Clock*1		Internal
	Operation Bit Rate*3		2.40 – 32.10 GBaud
Insertion Loss Compensation			ON
	Setting Range		0.5 dB

*1: When the MX190000A is started as PAM4 PPG/ED Based System or SI and PAM4 Combined System.

*2: When the MU191000A is installed in Slot1.

*3: When the MX190000A is started as SI PPG/ED Based System or Miscellaneous System.

B.3 ED

B.3.1 MU195040A

Table B.3.1-1 List of MU195040A Initialized Items

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Result	Switch of setting items	Setting display format		Gating
		Result display format		Error/Alarm
		Time display format		Date&Time
		Error/Alarm display	Zoom	OFF
			Overall Ch	OFF
	Start of Error/Alarm measurement			–
	Stop of Error/Alarm measurement			–
Measurement	Measurement Period (Gating)	Measurement period unit (Unit)		Time
		Measurement period time		00 00:00:01
		Clock count for measurement period		>E+10
		Error count for measurement period		>E+10
		Block count for measurement period		>E+2
		Measurement processing method (Cycle)		Repeat
		Target ER		1E-12
		Target EC		1
		Target Bitrate		12.500 000 Gbit/s
		Measurement result data display (Current)		ON
		Known data processing method (Calculation)		Progressive
		Known data display update cycle		100 ms
	Re-synchronization (Auto Sync)	Re-synchronization execution		ON
		Threshold for automatic synchronization function		INT
	SKP Ordered Set filter (SKP Ordered Set)	Filtering		OFF
		Specification		PCIe4
	Synchronization method (Sync Control)	Synchronization method		Invalid
		Unique pattern length for frame synchronization		64 bits
		PRGM pattern start position		1 bit
		Edit of synchronization mask pattern		All 0
	Measurement Condition (Error/Alarm Condition)	Bit error, alarm measurement processing method		Insertion/Omission
		Interval for EI and EFI measurements		100 ms

Table B.3.1-1 List of MU195040A Initialized Items (Cont'd)

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Pattern*	Mask	Block Window execution		OFF
		Block Window setting		All 0
		Bit Window execution		OFF
		Bit Window bit string setting		All 0
		External Mask ON/OFF		OFF
	HSSB Data	Logic		POS
		Length		32
		Specification		PCIe1
		Scrambler Seed		FFFF
		EIEOSQ Insertion		OFF
		EIEOSQ Interval		32

*: Items shared with the pulse pattern generator are omitted.
See Table B.2.1-1 “List of MU195020A Initialized Items” for details.

Table B.3.1-1 List of MU195040A Initialized Items (Cont'd)

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Input	Data	Input condition		Single-Ended
		Differential type		Independent
		Data/XData selection		Data
		Data input threshold		–0.500 V
		XData input threshold		–0.500 V
		Data input threshold differential type		Data-XData
		Data input threshold differential		0.000 V
		Data input termination setup dialog box display		–
		Data input termination condition		GND
		Data input termination voltage		0.00 V
		CTLE		OFF
	Clock	Selection		External Clock
		Standard for Recovered Clock Bitrate		Variable (MU195040A-x22)
		Recovered Clock Bitrate		28.000 000 Gbit/s (MU195040A-x22)
		Loop Bandwidth		17 MHz (MU195040A-x22)
		The value of division for calculating the Loop Bandwidth		1667 (MU195040A-x22)
		Clock phase unit		mUI
		Clock phase variable (mUI)		0 mUI
		Clock phase variable (ps)		0.00 ps
		Clock phase calibration		–
			Clock phase reference	OFF
			Clock phase variable (reference mUI)	0 mUI
			Clock phase variable (reference ps)	0.00 ps
			Clock phase variable (Jitter Input)	OFF
	Measurement Restart	Data Threshold		OFF
		Clock Delay		OFF

Table B.3.1-1 List of MU195040A Initialized Items (Cont'd)

Setting Function	Main Item	Secondary Item	Tertiary Item	Default Setting
Capture	Condition	Number of Block		128
		Trigger		Match Pattern
			Position	Top
		Match Pattern Length		4 bits
		Format		Hex
		Match Pattern		0
		Mask Pattern		0
	Capture Acquisition	Start Block No.		1
		Number of Block		1
	Capture	Block		1
		Viewer Mode	Notation	Hex(Byte)
			Format	Pattern
		Error Search	Continuous Error	≧ 1 bit
Misc1	Pattern Sequence			Repeat
		Burst	Source	External-Enable
			Delay	0 bits
			Auto/Manual	Manual
			Enable Period	128 000 bits*1
			Burst Cycle	12 800 000 bits*1
	Aux Input			External Mask
			Vth	0 V
	Aux Output			1/N Clock
		1/N Clock	(Divide ratio)	1/64 clock
		Pattern Sync	For PRBS, Zero-Substitution, Data Position	1 bits
			For Mixed Data Block No. Row No.	1 1
	Confidence Level	PPG Target Bitrate Tracking		OFF
				Unitx:Sloty:MU195020A*2
				Unitx:Sloty:MU196020A*3
		Target Bitrate		12.500 000 GBit/s

*1: 2ch Combination: Default × 2

*2: When the MX190000A is started as Standard BERT for SI

*3: When the MX190000A is started as Standard BERT for SI and PAM4 or PCIe1-5 and PCIe6 Base

B.3.2 **MU196040A**

B.3.2.1 PAM4

Table B.3.2.1-1 Result Tab

Main Item	Secondary Item	Tertiary Item	Default
Switch of setting items	Setting display format		Gating
	Input	Upper Eye Threshold	0.095 V
		Middle Eye Threshold	0.000 V
		Lower Eye Threshold	–0.095 V
		UL Threshold	ON
		Delay	0 mUI
	Gating	Cycle	Repeat
		Unit	Time
		Time	0 day 00:00:01
		Current	ON
		Calculation	Progressive
		Interval	100 ms
	Condition	EI/EFI Interval	100 ms
		Bit Mask (Block Window)	OFF
	Auto Sync	Auto Sync	ON
		Threshold	INT
	Sync Control	Frame Length	64 symbols
		Frame Position	1 symbols
Time display format			Date&Time
Error/Alarm display	Details		OFF
	Zoom		OFF

Table B.3.2.1-2 Measurement Tab

Main Item	Secondary Item	Tertiary Item	Default
Gating	Cycle		Repeat
	Unit		Time
		Time	0 day 00:00:01
		Clock Count	>E+10
		Error Count	>E+10
	Current		ON
		Calculation	Progressive
		Interval	100 ms
Auto Sync	Auto Sync		ON
	Threshold		INT
Sync Control	Frame Length		64 symbols
	Frame Position		1 symbols
	Mask		All 00
Error/Alarm Condition	EI/EFI Interval		100 ms

Table B.3.2.1-3 Pattern Tab

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			All List
	PRBS	Length	2^15–1
		PRBS Inv MSB	ON
		PRBS Inv LSB	ON
		Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
	Data	Length	4
		Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
	Pattern Editor	Data Length	4
		Notation	Hex(Byte)
		Edit Mode	Overwrite
		Cursor Addr	0x00000000

Table B.3.2.1-3 Pattern Tab (Cont'd)

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			
	PRBS23Q, PRBS31Q, PRBS31Q (Infiniband), PRBS31Q (Fibre Channel)	PRBS Inv MSB	ON
		PRBS Inv LSB	ON
		Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
	PRBS13Q, QPRBS13-CEI, QPRBS31-CEI, PRBS13Q (Infiniband)	PRBS Inv MSB	OFF
		PRBS Inv LSB	OFF
		Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
	QPRBS13	Seed	Lane 0
		Gray Coder	ON
		Pre Coder	ON
		Logic MSB	POS
		Logic LSB	POS
	SSPRQ, JP03A, JP03B, Square Wave, Transmitter Linearity	Logic MSB	POS
		Logic LSB	POS
Mask	Bit Mask (Block Window)		OFF
	External Mask		OFF

Table B.3.2.1-4 Input Tab

Main Item	Secondary Item	Tertiary Item	Default
Data	Input Condition		Single-Ended
		Single-Ended	Data
		Differential 50Ohm	Independent
		Differential 100Ohm	Independent
	Termination		GND
	Data	Upper Eye Threshold	0.095 V
		Middle Eye Threshold	0.000 V
		Lower Eye Threshold	–0.095 V
	XData	Upper Eye Threshold	0.095 V
		Middle Eye Threshold	0.000 V
		Lower Eye Threshold	–0.095 V
	UL Threshold		ON
		Differential Selection	Data-XData
		Threshold	0.000 V
Clock	Selection		External Clock
	Operation Baud Rate		2.40 – 16.05 GBaud
	Input Clock Freq.		2.40 – 16.05 GHz (1/1 Clock)
	Delay		0 mUI
		Relative	0 mUI
		Jitter Input	OFF
Measurement Restart	Data Threshold		OFF
	Clock Delay		OFF

Table B.3.2.1-5 Capture Tab

Main Item	Secondary Item	Tertiary Item	Default
Acquisition			Bit Pattern
Condition			
	Number of Block		128
	Condition	Trigger	
	Trigger		Match Pattern
		Position	Top
	Match Pattern Length		4 bits
	Format		HEX
	Math Pattern		0
	Mask Pattern		0

Table B.3.2.1-6 Misc1 Tab

Main Item	Secondary Item	Tertiary Item	Default
Pattern Sequence			Repeat
	Source		External -Enable
AUX Input			External Mask
		Vth	0V
AUX Output			1/N Clock
	1/N Clock	(Divide ratio)	1/64 Clock
	Pattern Sync	Position	1 symbols

B.3.2.2 NRZ

Table B.3.2.2-1 Result Tab

Main Item	Secondary Item	Tertiary Item	Default
Switch of setting items	Setting display format		Gating
	Input	Data Threshold	0.000 V
		XData Threshold	–
		Differential Selection	Data-XData
		Threshold	–
		Delay	0 mUI
	Gating	Cycle	Repeat
		Unit	Time
		Time	0 day 00:00:01
		Current	ON
		Calculation	Progressive
		Interval	100 ms
	Condition	Error Detection	Insertion/Omission
		EI/EFI Interval	100 ms
		Bit Mask (Block Window)	OFF
		Lane Mask (Bit Window)	OFF
	Auto Sync	Auto Sync	ON
		Threshold	INT
	Sync Control	Frame Length	64 bits
		Frame Position	1 bit
Result display format			Error/Alarm
Time display format			Date&Time
Error/Alarm display	Zoom		OFF
	All Channel		OFF

Table B.3.2.2-2 Measurement Tab

Main Item	Secondary Item	Tertiary Item	Default
Gating	Cycle		Repeat
	Unit		Time
		Time	0 day 00:00:01
		Clock Count	>E+10
		Error Count	>E+10
	Current		ON
		Calculation	Progressive
		Interval	100 ms
Auto Sync	Auto Sync		ON
	Threshold		INT
Sync Control	Frame Length		64 bits
	Frame Position		1 bit
	Mask		All 00
Error/Alarm Condition	Error Detection		Insertion/Omission
	EI/EFI Interval		100 ms

Table B.3.2.2-3 Pattern Tab

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			All List
	PRBS	Length	2^15–1
		Mark Ratio	1/2
		Logic	POS
	Zero Substitution	Length	2^15
		Zero Substitution Length	1 bits
		Additional Bit	1
		Logic	POS
	Data	Length	2
		Logic	POS
	Pattern Editor	Data Length	2
		Notation	Hex(Byte)
		Edit Mode	Overwrite
		Cursor Addr	0x00000000
	SSPR	Logic	POS
Mask	Bit Mask (Block Window)		OFF
	Lane Mask (Bit Window)		OFF
	External Mask		OFF

Table B.3.2.2-4 Input Tab

Main Item	Secondary Item	Tertiary Item	Default
Data	Input Condition		Single-Ended
		Single-Ended	Data
		Differential 50Ohm	Independent
		Differential 100Ohm	Independent
	Data Threshold		0.000 V
	Termination		GND
		Variable	0.000 V
	XData Threshold		0.000 V
	Differential Selection		Data-XData
	Threshold		0.000 V
Clock	Selection		External Clock
	Operation Bitrate		2.40 – 16.05 GBit/s
	Input Clock Freq.		2.40 – 16.05 GHz (1/1 Clock)
	Delay		0 mUI
		Relative	0 mUI
		Jitter Input	OFF
Measurement Restart	Data Threshold		OFF
	Clock Delay		OFF

Table B.3.2.2-5 Misc1 Tab

Main Item	Secondary Item	Tertiary Item	Default
Pattern Sequence			Repeat
	Burst	Source	External -Enable
		Delay	0 bits
		Enable Period	128 000 bits
		Burst Cycle	128 000 000 bits
		Auto/Manual	Manual
AUX Input			External Mask
		Vth	0V
AUX Output			1/N Clock
	1/N Clock	(Divide ratio)	1/64 Clock
	Pattern Sync	Position	1 bits

B.3.3 **MU196040B**

B.3.3.1 PAM4

Table B.3.3.1-1 Result Tab

Main Item	Secondary Item	Tertiary Item	Default
Switch of setting items	Setting display format		Gating
	Input	Upper Eye Threshold	0.095 V
		Middle Eye Threshold	0.000 V
		Lower Eye Threshold	–0.095 V
		U/L Threshold Sync	ON
		Low Frequency Equalizer	OFF*
			0.000 dB*
		DFE	OFF
			0
		Delay	0 mUI
	Gating	Cycle	Repeat
		Unit	Time
		Time	0 day 00:00:01
		Target ER	1E-12
		Target EC	1
		Target Unit	Bit
		Target Baud Rate	12.500 000 GBaud
		Current	ON
		Calculation	Progressive
		Interval	100 ms
	Condition	EI/EFI Interval	100 ms
		Bit Mask (Block Window)	OFF
	Auto Sync	Auto Sync	ON
		Threshold	INT
	Sync Control	Frame Length	64 symbols
		Frame Position	1 symbol
	RS-FEC Symbol	Capture Mode	FEC Symbol Capture
		Preset	Variable
		Measurement Condition	Intermittent Error Detect
		Codeword Length	544
		FEC Symbol Length	10
		FEC Symbol Error Threshold	16

*: When the MX190000A is started as Standard BERT for PAM4 or Expert BERT.

Table B.3.3.1-1 Result Tab (Cont'd)

Main Item	Secondary Item	Tertiary Item	Default
Switch of setting items	PCIe6 FEC Symbol	Capture Mode	PCIe6 FEC Symbol Capture
		Preset	x1 Link Common CLK/SRNS Mode
		SKP	No SKP
		FEC Symbol Error Threshold in One ECC Group	2
		Consecutive FEC Symbol Error Threshold	4
		Consecutive Errored Flit Threshold	1
Time display format			Date&Time
Error/Alarm display	Details		OFF
	Zoom		OFF

Table B.3.3.1-2 Measurement Tab

Main Item	Secondary Item	Tertiary Item	Default
Gating	Cycle		Repeat
	Unit		Time
		Time	0 day 00:00:01
		Clock Count	>E+10
		Error Count	>E+10
	Target ER		1E-12
	Target EC		1
	Target Unit		Bit
	Target Baud Rate		12.500 000 GBaud
	Current		ON
		Calculation	Progressive
		Interval	100 ms
Auto Sync	Auto Sync		ON
	Threshold		INT
Sync Control	Frame Length		64 symbols
	Frame Position		1 symbol
	Mask		00 00 00 00 00 00 00 00
Error/Alarm Condition	EI/EFI Interval		100 ms
Measurement Restart	Data Threshold		OFF
	Clock Delay		OFF

Table B.3.3.1-3 Pattern Tab

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			All List
	PRBS	Length	2^15–1
		PRBS Inv MSB	ON
		PRBS Inv LSB	ON
		Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Input Signal Decoder	OFF
		1st Bit	MSB*
	Data	Length	4
		Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Input Signal Decoder	OFF
	Pattern Editor	Data Length	4
		Notation	Hex(Byte)
		Edit Mode	Overwrite
		Cursor Addr	0x00000000
	PRBS23Q, PRBS31Q, PRBS31Q (Infiniband), PRBS31Q (Fibre Channel)	PRBS Inv MSB	ON
		PRBS Inv LSB	ON
		Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Input Signal Decoder	OFF
	PRBS9Q, PRBS13Q, QPRBS13-CEI, PRBS13Q, (Infiniband), QPRBS31-CEI	PRBS Inv MSB	OFF
		PRBS Inv LSB	OFF
		Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Input Signal Decoder	OFF

*: When the MX190000A is started as BERT for PCIe1-7 or BERT for PCIe1-5 and PCIe6Base, the default value is LSB.

Table B.3.3.1-3 Pattern Tab (Cont'd)

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern (Cont'd)			
	QPRBS13	Seed	Lane 0
		Gray Coder	ON
		Pre Coder	ON
		Logic MSB	POS
		Logic LSB	POS
		Input Signal Decoder	OFF
	SSPRQ, JP03A, JP03B, Square Wave, Transmitter Linearity	Logic MSB	POS
		Logic LSB	POS
		Input Signal Decoder	OFF
	RS-FEC Scrambled Idle 50G 1Lane, RS-FEC Scrambled Idle 100G 1Lane, RS-FEC-Int Scrambled Idle 100G 1Lane	Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Input Signal Decoder	ON
		Inverse Gray Coder	ON
		Pre-Code Remover	OFF
	RS-FEC Scrambled Idle 100G 2Lanes, RS-FEC Scrambled Idle 200G 2Lanes, RS-FEC Scrambled Idle 200G 4Lanes, RS-FEC Scrambled Idle 400G 4Lanes, RS-FEC Scrambled Idle 400G 8Lanes	Lane	0
		Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Input Signal Decoder	ON
		Inverse Gray Coder	ON
		Pre-Code Remover	OFF

Table B.3.3.1-3 Pattern Tab (Cont'd)

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern (Cont'd)			
	CP in 1b/1b Encoding for PCIe6 CP in 1b/1b Encoding for PCIe7	Gray Coder	OFF
		Pre Coder	OFF
		EIEOS	ON
		Logic MSB	POS
		Logic LSB	POS
		Seed	Lane 0
		SKP OS Filter	OFF
		Input Signal Decoder	OFF
	MCP in 1b/1b Encoding for PCIe6	Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Seed	Lane 0
		SRIS	OFF
		SKP	No SKP
		EIEOS	ON
		SKP OS Filter	ON
		Input Signal Decoder	OFF
		Inverse Gray Coder	ON
		Pre-Code Remover	OFF
	NOP Flit Layout in a x1 Link	SRIS	OFF
		SKP	No SKP
		EIEOS	ON
		Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		SKP OS Filter	ON
		Input Signal Decoder	ON
		Inverse Gray Coder	ON
		Pre-Code Remover	OFF

Table B.3.3.1-3 Pattern Tab (Cont'd)

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern (Cont'd)			
	NOP Flit Layout in a x2 Link NOP Flit Layout in a x4 Link NOP Flit Layout in a x8 Link NOP Flit Layout in a x16 Link	Lane	0
		SRIS	OFF
		SKP	No SKP
		EIEOS	ON
		Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		SKP OS Filter	ON
		Input Signal Decoder	ON
		Inverse Gray Coder	ON
		Pre-Code Remover	OFF
	MCP in 1b/1b Encoding for PCIe7	Gray Coder	ON
		Pre Coder	OFF
		Logic MSB	POS
		Logic LSB	POS
		Seed	Lane 0
		SRIS	OFF
		SKP	No SKP
		EIEOS	ON
		SKP OS Filter	ON
		Input Signal Decoder	OFF
	HSSB Data	Specification	PCIe6/CXL3
		EIEOSQ Insertion	ON
		EIEOSQ Interval	32
		EIEOS Count	4
		Scrambler Mode	PAM4
		Gray Coder	ON
		Pre Coder	ON
		Logic	POS
	1b1b Pattern Editor	Data Length	128
		Notation	Symbol (PAM4)
		MSB/LSB First	MSB First
		Edit Mode	Overwrite
		Cursor Addr	0
Mask	Bit Mask (Block Window)		OFF
	External Mask		OFF

Table B.3.3.1-4 Input Tab

Main Item	Secondary Item	Tertiary Item	Default
Data	Input Condition		Single-Ended
		Single-Ended	Data
		Differential 50Ohm	Independent
		Differential 100Ohm	Independent
	Termination		GND
	Data	Upper Eye Threshold	0.095 V
		Middle Eye Threshold	0.000 V
		Lower Eye Threshold	–0.095 V
	XData	Upper Eye Threshold	0.095 V
		Middle Eye Threshold	0.000 V
		Lower Eye Threshold	–0.095 V
	UL Threshold		ON
		Differential Selection	Data-XData
		Threshold	0.000 V
Equalizer	Low Frequency Equalizer		OFF
			0.000 dB
	Decision Feedback Equalizer		OFF
			0
Clock	Selection		External Clock
	Operation Baud Rate		2.40 – 32.10 Gaud*1 Auto*2
	Input Clock Freq.		1.20 – 16.05 GHz (1/2 Clock)*1 1.20 – 32.1 GHz (1/2 Clock)*2
	Delay		0 mUI
		Relative	0 mUI
		Jitter Input	OFF

*1: When MU196040B-001 is installed.

*2: When MU196040B-002, MU196040B-005, MU196040B-y12, MU196040B-115, or MU196040B-125 is installed.

Table B.3.3.1-5 Capture Tab

Main Item	Secondary Item	Tertiary Item	Default
Capture Mode	Capture Mode		FEC Symbol Capture*1
			PCIe6 FEC Symbol Capture*2
			Sync Mode Capture*3
		State	-----
Capture Result Display	Auto Launch		Capture Data
Condition	Number of Blocks		128
	Capture Area		Around The Trigger
	Trigger		Intermittent Error Detect*1
			Intermittent FEC Symbol Error Detect*2
RS-FEC Symbol*1			Variable
	FEC Symbol Length		10
	FEC Symbols per Lane		544
	FEC Symbol Error Threshold		16
PCIe6 FEC Symbol*2			x1 Link Common CLK/SRNS Mode
			No SKP
	FEC Symbol Error Threshold in One ECC Group		2

*1: When the MX190000A is started as Standard BERT for PAM4, Standard BERT for SI and PAM4, or Expert BERT.

*2: When the MX190000A is started as BERT for PCIe1-7 or BERT for PCIe1-5 and PCIe6 Base.

*3: When the MX190000A is started as BERT for PCIe1-6 Forced Link.

Table B.3.3.1-6 Misc1 Tab

Main Item	Secondary Item	Tertiary Item	Default
Pattern Sequence			Repeat
	Source		External-Enable
AUX Input			External Mask
		Vth	0V
AUX Output			1/N Clock
	1/N Clock	(Divide ratio)	1/64 Clock
	Pattern Sync	Position	1 symbols
PPG Target Baud Rate Tracking			OFF Unitx:Sloty:MU196020A*
Target Baud Rate			12.500 000 GBaud

*: When the MX190000A is started as BERT for PCIe1-7, BERT for PCIe1-5 and PCIe6 Base, Standard BERT for PAM4, or Standard BERT for SI and PAM4.

Table B.3.3.1-7 Logging Tab

Main Item	Secondary Item	Tertiary Item	Default
BER/SER Logging	Logging		OFF
	Cycle		00:00:05
	ER (Symbol)		OFF
	ER (Bit)		OFF
	ER (MSB)		OFF
	ER (LSB)		OFF
	EC (Symbol)		OFF
	EC (Bit)		OFF
	EC (MSB)		OFF
	EC (LSB)		OFF
	Clock Loss		OFF
	Sync Loss		OFF

B.3.3.2 NRZ

Table B.3.3.2-1 Result Tab

Main Item	Secondary Item	Tertiary Item	Default
Switch of setting items	Setting display format		Gating
	Input	Data Threshold	0.000 V
		XData Threshold	–
		Differential Selection	Data-XData
		Threshold	–
		Delay	0 mUI
		LFE	OFF
			0.000 dB
		DFE	OFF
			0
	Gating	Cycle	Repeat
		Unit	Time
		Time	0 day 00:00:01
		Target ER	1E-12
		Target EC	1
		Target Unit	Bit
		Target Bitrate	12.500 000 Gbit/s
		Current	ON
		Calculation	Progressive
		Interval	100 ms
	Condition	Error Detection	Insertion/Omission
		EI/EFI Interval	100 ms
		Bit Mask (Block Window)	OFF
		Lane Mask (Bit Window)	OFF
	Auto Sync	Auto Sync	ON
		Threshold	INT
	Sync Control	Frame Length	64 bits
		Frame Position	1 bit
	RS-FEC Symbol	Capture Mode	FEC Symbol Capture
		Preset	Variable
		Measurement Condition	Intermittent Error Detect
		Codeword Length	528
		FEC Symbol Length	10
		FEC Symbol Error Threshold	8

Table B.3.3.2-1 Result Tab (Cont'd)

Main Item	Secondary Item	Tertiary Item	Default
Result display format			Error/Alarm Independent
Time display format			Date&Time
Error/Alarm display	Zoom		OFF
	Show in Window		OFF

Table B.3.3.2-2 Measurement Tab

Main Item	Secondary Item	Tertiary Item	Default
Gating	Cycle		Repeat
	Unit		Time
		Time	0 day 00:00:01
		Clock Count	>E+10
		Error Count	>E+10
	Target ER		1E-12
	Target EC		1
	Target Unit		Bit
	Target Bitrate		12.500 000 Gbit/s
	Current		ON
		Calculation	Progressive
		Interval	100 ms
Auto Sync	Auto Sync		ON
	Threshold		INT
Sync Control	Frame Length		64 bits
	Frame Position		1 bit
	Mask		All 00
Error/Alarm Condition	Error Detection		Insertion/Omission
	EI/EFI Interval		100 ms
Measurement Restart	Data Threshold		OFF
	Clock Delay		OFF

Table B.3.3.2-3 Pattern Tab

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			All List
	PRBS	Length	2^15–1
		Mark Ratio	1/2
		Logic	POS
	Zero Substitution	Length	2^15
		Zero Substitution Length	1 bits
		Additional Bit	1
		Logic	POS
	Data	Length	2
		Logic	POS
	Pattern Editor	Data Length	2
		Notation	Hex(Byte)
		Edit Mode	Overwrite
		Cursor Addr	0x00000000
	SSPR	Logic	POS
	RS-FEC Scrambled Idle 25G 1Lane	Logic	POS
	RS-FEC Scrambled Idle 50G 2Lanes RS(544,514), RS-FEC Scrambled Idle 100G 4Lanes, RS-FEC Scrambled Idle 100G 4Lanes RS(544,514)	Lane	0
		Logic	POS
	CP in 8b/10b Encoding for PCIe1 CP in 8b/10b Encoding for PCIe2	Seed	Lane 0
		Delay Symbol	OFF
		SKP	No SKP
		SKP OS Filter	OFF
		Logic	POS
	MCP in 8b/10b Encoding for PCIe1 MCP in 8b/10b Encoding for PCIe2	Seed	Lane 0
		Delay Symbol	OFF
		SKP	No SKP
		SKP OS Filter	OFF
		Logic	POS

Table B.3.3.2-3 Pattern Tab (Cont'd)

Main Item	Secondary Item	Tertiary Item	Default
Test Pattern			
	CP in 128b/130b Encoding for PCIe3 CP in 128b/130b Encoding for PCIe4 CP in 128b/130b Encoding for PCIe5	Seed	Lane 0
		Preset	P0
		SKP	No SKP
		EIEOS	ON
		SKP OS Filter	OFF
		Logic	POS
	MCP in 128b/130b Encoding for PCIe3 MCP in 128b/130b Encoding for PCIe4	Seed	Lane 0
		SRIS	OFF
		SKP	No SKP
		EIEOS	ON
		SKP OS Filter	ON
		Logic	POS
	MCP in 128b/130b Encoding for PCIe5	Seed	Lane 0
		SRIS	OFF
		SKP	No SKP
		EIEOS	ON
		Pre Coder	ON
		SKP OS Filter	ON
		Logic	POS
	HSSB Data	Specification	PCIe1
		EIEOSQ Insertion	OFF
		EIEOSQ Interval	32
		Logic	POS
	8b10b Pattern Editor	Data Length	32
		Notation	Symbol(8b10b)
		MSB/LSB First	MSB First
		Edit Mode	Overwrite
		Cursor Addr	0
	128b130b Pattern Editor	Data Length	128
		Notation	Hex(Byte)
		MSB/LSB First	MSB First
		Edit Mode	Overwrite
		Cursor Addr	0
Mask	Bit Mask (Block Window)		OFF
	Lane Mask (Bit Window)		OFF
	External Mask		OFF

Table B.3.3.2-4 Input Tab

Main Item	Secondary Item	Tertiary Item	Default
Data	Input Condition		Single-Ended
		Single-Ended	Data
		Differential 50Ohm	Independent
		Differential 100Ohm	Independent
	Data Threshold		0.000 V
	Termination		GND
		Variable	0.000 V
	XData Threshold		0.000 V
	Differential Selection		Data-XData
	Threshold		0.000 V
Equalizer	Low Frequency Equalizer		OFF
			0.000 dB
	Decision Feedback Equalizer		OFF
			0
Clock	Selection		External Clock
	Operation Bitrate		2.40 – 32.10 Gbit/s*1 Auto*2
	Input Clock Freq.		1.20–16.05 GHz (1/2 Clock)*1 1.20–32.1 GHz (1/2 Clock)*2
	Delay		0 mUI
		Relative	0 mUI
		Jitter Input	OFF

*1: When MU196040B-001 is installed.

*2: When MU196040B-002, MU196040B-005, MU196040B-y12, MU196040B-115, or MU196040B-125 is installed.

Table B.3.3.2-5 Capture Tab

Main Item	Secondary Item	Tertiary Item	Default
Capture Mode	Capture Mode		FEC Symbol Capture*1
			Sync Mode Capture*2
		State	-----
Capture Result Display	Auto Launch		Capture Data
Condition	Number of Blocks		128
	Capture Area		Around The Trigger*1
			After The Trigger*2
	Trigger		Intermittent Error Detect*1
			Error Detect*2
RS-FEC Symbol*1			Variable
	FEC Symbol Length		10
	FEC Symbols per Lane		528
	FEC Symbol Error Threshold		8

*1: When the MX190000A is started as Standard BERT for PAM4, Standard BERT for SI and PAM4, or Expert BERT.

*2: When the MX190000A is started as BERT for PCIe1-7, BERT for PCIe1-5 and PCIe6 Base, or BERT for PCIe1-6 Forced Link.

Table B.3.3.2-6 Misc1 Tab

Main Item	Secondary Item	Tertiary Item	Default
Pattern Sequence			Repeat
	Burst	Source	External -Enable
		Delay	0 bits
		Enable Period	128 000 bits
		Burst Cycle	12 800 000 bits
		Auto/Manual	Manual
AUX Input			External Mask
		Vth	0V
AUX Output			1/N Clock
	1/N Clock	(Divide ratio)	1/64 Clock
	Pattern Sync	Position	1 bits
PPG Target Bitrate Tracking			OFF Unitx:Sloty:MU196020A*
Target Bitrate			12.500 000 Gbit/s

*: When the MX190000A is started as Standard BERT for PAM4 or Standard BERT for SI and PAM4.

Table B.3.3.2-7 Logging Tab

Main Item	Secondary Item	Tertiary Item	Default
BER/SER Logging	Logging		OFF
	Cycle		00:00:05
	ER (Total)		OFF
	ER (INS)		OFF
	ER (OMI)		OFF
	EC (Total)		OFF
	EC (INS)		OFF
	EC (OMI)		OFF
	Clock Loss		OFF
	Sync Loss		OFF

B.4 Noise Generator

B.4.1 MU195050A

Table B.4.1-1 List of MU195050A Initialized Items

Setting Function	Item	Default Setting
Common Mode Noise	Presets	Manual
	Output	OFF
	Amplitude	10 mVp-p
	Frequency	120 MHz
	Band	Low
Differential Mode Noise	Presets	Manual
	Output	OFF
	Amplitude	4 mVp-p
	Frequency	2.1 GHz
White Noise	Output	OFF
	Amplitude	0.2 mVrms
External Input	Output	OFF

B.4.2 **MU196050B**

Table B.4.2-1 List of MU196050B Initialized Items

Setting Function	Item	Default Setting
Common Mode Noise	Presets	Manual
	Output	OFF
	Amplitude	10 mVp-p
	Frequency	120 MHz
	Band	Low
Differential Mode Noise	Presets	Manual
	Output	OFF
	Amplitude	4 mVp-p
	Frequency	2.1 GHz
External Input	Output	OFF

B.5 Re-Driver

B.5.1 MU196060A

Table B.5.1-1 32G baud NRZ/PAM4 Re-Driver

Main Item	Secondary Item	Tertiary Item	Default
PAM4/NRZ switching			NRZ
Data/XData Output Clock Output			ON
Equalizer	CTLE		ON
			0.000 dB
Clock Recovery	Baud Rate		Variable
			16.000 000 Gbit/s
	Tracking		OFF

Appendix C Performance Test Record Sheet

C.1 Performance Test Result Sheet

Document number: _____

Test Location: _____

Date: _____

Test person in charge: _____

Product name: _____

Serial number: _____

Software version: _____

_____

Option: _____

Power voltage: _____ V

Power frequency: _____ Hz

Ambient temperature _____ °C

Relative humidity _____ %

Instruments used: Model name _____ Serial number _____

Model name _____ Serial number _____

Model name _____ Serial number _____

Model name _____ Serial number _____

Remarks _____

_____

_____

C.2 Synthsizer

C.2.1 MU191000A

Table C.2.1-1 Clock Output Waveform Test Results

Frequency [MHz]	Specifications	Results
16050	Amplitude 0.4 to 1.0 Vp-p Duty ratio 40% to 60%	
12000		
8000		
5000		
2500		
1250		
100		

Table C.2.1-2 AUX Output Waveform Test Results

Frequency [MHz]	Specifications	Results
16050	Amplitude 0.25 to 0.75 Vp-p Duty ratio 40% to 60%	
12000		
8000		
5000		
2500		
1250		
100		

Table C.2.1-3 Clock Output Phase Noise Test Results

Frequency [MHz]	Specifications	Results		
		10 kHz Offset	100 kHz Offset	1MHz Offset
16050	≤–110 dBc/Hz at 10 kHz offset ≤–111 dBc/Hz at 100 kHz offset ≤–110 dBc/Hz at 1 MHz offset Note: None of the above specification values include non-harmonic spurious components.			
12000				
8000				
5000				
2500				
1250				
100				

C.3 PPG/ED/Re-Driver

C.3.1 MU196020A/MU196040A/B

C.3.1.1 MU196020A-001

Table C.3.1.1-1 Operating Frequency Range

Specification	Results	
	Data	$\overline{\text{Data}}$
No errors occur within the range from 2.4 to 32.1 Gbit/s.*		
No errors occur within the range from 2.4 to 32.1 Gbaud.*		

*: Pattern PRBS, 2^31–1

Table C.3.1.1-2 MU196020A-001 Waveform Evaluation Test- Amplitude (NRZ)

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (Vp-p)	Upper Limit (Vp-p)	Data	$\overline{\text{Data}}$
32.1 Gbit/s	0.70	0.581	0.819		
	0.07	0.027	0.113		

Table C.3.1.1-3 MU196020A-001 Waveform Evaluation Test- 0/3 Level Amplitude (PAM4)

Settings		Specification		Results	
Baud rate	Amplitude (Vp-p)	Lower Limit (Vp-p)	Upper Limit (Vp-p)	Data	$\overline{\text{Data}}$
32.1 Gbaud	0.70	0.581	0.819		
	0.07	0.027	0.113		

Table C.3.1.1-4 MU196020A-001 Waveform Evaluation Test- Offset (NRZ)

Settings		Specification		Results	
Bit rate	Offset (Vth)	Lower Limit (V)	Upper Limit (V)	Data	$\overline{\text{Data}}$
32.1 Gbit/s	3.265	2.817	3.713		
	–2.35	–2.590	–2.111		

Table C.3.1.1-5 MU196020A-001 Waveform Evaluation Test- Offset (PAM4)

Settings		Specification		Results	
Baud rate	Offset (Vth)	Lower Limit (V)	Upper Limit (V)	Data	$\overline{\text{Data}}$
32.1 Gbaud	3.265	2.817	3.713		
	–2.35	–2.590	–2.111		

Table C.3.1.1-6 MU196020A-001 Waveform Evaluation Test-Cross point (NRZ)

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (%)	Upper Limit (%)	Data	$\overline{\text{Data}}$
32.1 Gbit/s	0.50	40	60		

Table C.3.1.1-7 MU196020A-001 Waveform Evaluation Test- Tr/Tf (NRZ)

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (ps)	Upper Limit (ps)	Data	$\overline{\text{Data}}$
32.1 Gbit/s	0.50	–	9.0*1		
		–	9.5*2		

*1: When J1789A cables are used.

*2: When J1790A cables are used.

Table C.3.1.1-8 MU196020A-001 Waveform Evaluation Test- Jitter (NRZ)

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (ps)	Upper Limit (ps p-p)	Data	$\overline{\text{Data}}$
32.1 Gbit/s	0.50	–	6.0		

C.3.1.2 MU196020A-002

Table C.3.1.2-1 Operating Frequency Range

Specification	Results	
	Data	$\overline{\text{Data}}$
No errors occur within the range from 2.4 to 32.1 Gbit/s.*		
No errors occur within the range from 2.4 to 32.1 Gbaud.*		

*: Pattern PRBS, 2^31–1

Table C.3.1.2-2 MU196020A-002 Waveform Evaluation Test- Amplitude (NRZ)

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (Vp-p)	Upper Limit (Vp-p)	Data	$\overline{\text{Data}}$
58.2 Gbit/s	0.70*1	0.581	0.819		
	0.60*2	0.493	0.707		
	0.07	0.027	0.113		

*1: When J1789A cables are used.

*2: When J1790A cables are used.

Table C.3.1.2-3 MU196020A-002 Waveform Evaluation Test-0/3 Level Amplitude (PAM4)

Settings		Specification		Results	
Baud rate	Amplitude (Vp-p)	Lower Limit (Vp-p)	Upper Limit (Vp-p)	Data	$\overline{\text{Data}}$
58.2 Gbaud	0.70*1	0.581	0.819		
	0.60*2	0.493	0.707		
	0.07	0.027	0.113		

*1: When J1789A cables are used.

*2: When J1790A cables are used.

Table C.3.1.2-4 MU196020A-002 Waveform Evaluation Test- Offset (NRZ)

Settings		Specification		Results	
Bit rate	Offset (Vth)	Lower Limit (V)	Upper Limit (V)	Data	$\overline{\text{Data}}$
58.2 Gbit/s	3.265	2.817	3.713		
	–2.30*1	–2.489	–2.112		
	–2.35*2	–2.590	–2.111		

*1: When J1790A cables are used, Amplitude 0.60 Vp-p

*2: When J1789A cables are used, Amplitude 0.70 Vp-p

Table C.3.1.2-5 MU196020A-002 Waveform Evaluation Test- Offset (PAM4)

Settings		Specification		Results	
Baud rate	Offset (Vth)	Lower Limit (V)	Upper Limit (V)	Data	$\overline{\text{Data}}$
58.2 Gbaud	3.265	2.817	3.713		
	–2.30*1	–2.489	–2.112		
	–2.35*2	–2.590	–2.111		

*1: When J1790A cables are used, Amplitude 0.60 Vp-p

*2: When J1789A cables are used, Amplitude 0.70 Vp-p

Table C.3.1.2-6 MU196020A-002 Waveform Evaluation Test- Cross point (NRZ)

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (%)	Upper Limit (%)	Data	$\overline{\text{Data}}$
58.2 Gbit/s	0.50	40	60		

Table C.3.1.2-7 MU196020A-002 Waveform Evaluation Test- Tr/Tf (NRZ)

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (ps)	Upper Limit (ps)	Data	$\overline{\text{Data}}$
58.2 Gbit/s	0.50	–	8.5*1		
		–	8.8*2		

*1: When J1789A cables are used.

*2: When J1790A cables are used.

Table C.3.1.2-8 MU196020A-002 Waveform Evaluation Test- Jitter (NRZ)

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (ps)	Upper Limit (ps p-p)	Data	$\overline{\text{Data}}$
58.2 Gbit/s	0.50	–	6.0		

C.3.1.3 MU196020A-003

Table C.3.1.3-1 Operating Frequency Range

Specification	Results	
	Data	$\overline{\text{Data}}$
No errors occur within the range from 2.4 to 32.1 Gbit/s.*		
No errors occur within the range from 2.4 to 32.1 Gbaud.*		

*: Pattern PRBS, 2^31–1

Table C.3.1.3-2 MU196020A-003 Waveform Evaluation Test- Amplitude (NRZ)

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (Vp-p)	Upper Limit (Vp-p)	Data	$\overline{\text{Data}}$
64.2 Gbit/s	0.70*1	0.581	0.819		
	0.55*2	0.405	0.595		
	0.07	0.027	0.113		

*1: When J1789A cables are used.

*2: When J1790A cables are used.

Table C.3.1.3-3 MU196020A-003 Waveform Evaluation Test-0/3 Level Amplitude (PAM4)

Settings		Specification		Results	
Baud rate	Amplitude (Vp-p)	Lower Limit (Vp-p)	Upper Limit (Vp-p)	Data	$\overline{\text{Data}}$
64.2 Gbaud	0.70*1	0.581	0.819		
	0.55*2	0.405	0.595		
	0.07	0.027	0.113		

*1: When J1789A cables are used.

*2: When J1790A cables are used.

Table C.3.1.3-4 MU196020A-003 Waveform Evaluation Test- Offset (NRZ)

Settings		Specification		Results	
Bit rate	Offset (Vth)	Lower Limit (V)	Upper Limit (V)	Data	$\overline{\text{Data}}$
64.2 Gbit/s	3.265	2.817	3.713		
	–2.275*1	–2.438	–2.112		
	–2.35*2	–2.590	–2.111		

*1: When J1790A cables are used, Amplitude 0.55 Vp-p

*2: When J1789A cables are used, Amplitude 0.70 Vp-p

Table C.3.1.3-5 MU196020A-003 Waveform Evaluation Test- Offset (PAM4)

Settings		Specification		Results	
Baud rate	Offset (Vth)	Lower Limit (V)	Upper Limit (V)	Data	$\overline{\text{Data}}$
64.2 Gbaud	3.265	2.817	3.713		
	–2.275*1	–2.438	–2.112		
	–2.35*2	–2.590	–2.111		

*1: When J1790A cables are used, Amplitude 0.55 Vp-p

*2: When J1789A cables are used, Amplitude 0.70 Vp-p

Table C.3.1.3-6 MU196020A-003 Waveform Evaluation Test - Cross point (NRZ)

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (%)	Upper Limit (%)	Data	$\overline{\text{Data}}$
64.2 Gbit/s	0.50	40	60		

Table C.3.1.3-7 MU196020A-003 Waveform Evaluation Test - Tr/Tf (NRZ)

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (ps)	Upper Limit (ps)	Data	$\overline{\text{Data}}$
64.2 Gbit/s	0.50	–	8.5*1		
		–	8.8*2		

*1: When J1789A cables are used.

*2: When J1790A cables are used.

Table C.3.1.3-8 MU196020A-003 Waveform Evaluation Test- Jitter (NRZ)

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (ps)	Upper Limit (ps p-p)	Data	$\overline{\text{Data}}$
64.2 Gbit/s	0.50	–	6.0		

C.3.1.4 MU196040A

Table C.3.1.4-1 Input Level Range (NRZ)

Settings					Specification	Results	
MU196020A			MU196040A				
Termination	Amplitude (Vp-p)	Offset (Vth) (V)	Termination	Threshold Voltage (V)		Data	$\overline{\text{Data}}$
GND	0.7	–2.35	GND	–2.350	No errors occur.		
	0.05	–0.225		–0.225			
	0.7	+2.95		+2.950			
	0.05	+0.305		+0.305			

Table C.3.1.4-2 Input Level Range (PAM4)

Settings					Specification	Results	
MU196020A			MU196040A				
Termination	Amplitude (Vp-p)	Offset (Vth) (V)	Termination	Threshold Voltage (V)		Data	$\overline{\text{Data}}$
GND	0.7	–2.35	GND	Upper: –2.117 Middle: –2.350 Lower: –2.583	No errors occur.		
	0.3	–2.15		Upper: –2.050 Middle: –2.150 Lower: –2.250			
	0.7	+2.95		Upper: 3.183 Middle: 2.950 Lower: 2.717			
	0.3	+3.15		Upper: 3.250 Middle: 3.150 Lower: 3.050			

Table C.3.1.4-3 Test Pattern (PRBS-NRZ)

Settings				Specification	Results	
MU196020A		MU196040A				
Length	Logic	Length	Logic		Data	$\overline{\text{Data}}$
2^7–1	POS	2^7–1	POS	No errors occur.		
2^9–1	POS	2^9–1	POS			
2^11–1	POS	2^11–1	POS			
2^13–1	POS	2^13–1	POS			
2^15–1	POS	2^15–1	POS			
2^20–1	POS	2^20–1	POS			
2^23–1	POS	2^23–1	POS			
2^31–1	POS	2^31–1	POS			
2^31–1	NEG	2^31–1	NEG			

Table C.3.1.4-4 Test Pattern (PRBS-PAM4)

Settings						Specification	Results	
MU196020A			MU196040A					
Length	Logic MSB	Logic LSB	Length	Logic MSB	Logic LSB		Data	$\overline{\text{Data}}$
2^7–1	POS	POS	2^7–1	POS	POS	No errors occur.		
2^9–1	POS	POS	2^9–1	POS	POS			
2^11–1	POS	POS	2^11–1	POS	POS			
2^15–1	POS	POS	2^15–1	POS	POS			
2^20–1	POS	POS	2^20–1	POS	POS			
2^23–1	POS	POS	2^23–1	POS	POS			
2^31–1	POS	POS	2^31–1	POS	POS			
2^31–1	NEG	NEG	2^31–1	NEG	NEG			

Table C.3.1.4-5 Test Pattern (Zero Substitution-NRZ)

Settings				Specification	Results	
MU196020A		MU196040A				
Length	Logic	Length	Logic		Data	$\overline{\text{Data}}$
2^7	POS	2^7	POS	No errors occur.		
2^9	POS	2^9	POS			
2^10	POS	2^10	POS			
2^11	POS	2^11	POS			
2^15	POS	2^15	POS			
2^20	POS	2^20	POS			
2^23	POS	2^23	POS			
2^7–1	POS	2^7–1	POS			
2^9–1	POS	2^9–1	POS			
2^10–1	POS	2^10–1	POS			
2^11–1	POS	2^11–1	POS			
2^15–1	POS	2^15–1	POS			
2^20–1	POS	2^20–1	POS			
2^23–1	POS	2^23–1	POS			

Table C.3.1.4-6 Test Pattern (SSPRQ-PAM4)

Settings				Specification	Results	
MU196020A		MU196040A				
Pattern	Logic	Pattern	Logic		Data	$\overline{\text{Data}}$
SSPRQ	POS	SSPRQ	POS	No errors occur.		

Table C.3.1.4-7 Error Detection

Item	Specification	Results	
		Data	$\overline{\text{Data}}$
Error rate (ER)	5.0000E–12		
Error count (EC)	1.0000E–00		
Error free interval (%EFI)	99.9900%		
Error interval (EI)	1		

C.3.1.5 MU196040B

Table C.3.1.5-1 Input Level Range (NRZ ≤32.1 Gbit/s)

Settings					Specification	Results	
MU196020A			MU196040B				
Termination	Amplitude (Vp-p)	Offset (Vth) (V)	Termination	Threshold Voltage (V)		Data	$\overline{\text{Data}}$
GND	0.7	–2.35	GND	–2.350	No errors occur.		
	0.05	–0.225		–0.225			
	0.7	+2.95		+2.950			
	0.05	+0.305		+0.305			

Table C.3.1.5-2 Input Level Range (NRZ >32.1 Gbit/s)

Settings					Specification	Results	
MU196020A			MU196040B				
Termination	Amplitude (Vp-p)	Offset (Vth) (V)	Termination	Threshold Voltage (V)		Data	$\overline{\text{Data}}$
GND	0.7	–2.35	GND	–2.350	No errors occur.		
	0.1	–2.05		–2.050			
	0.7	+2.95		+2.950			
	0.1	+3.25		+3.250			

Table C.3.1.5-3 Input Level Range (PAM4 ≤32.1 Gbaud)

Settings					Specification	Results	
MU196020A			MU196040B				
Termination	Amplitude (Vp-p)	Offset (Vth) (V)	Termination	Threshold Voltage (V)		Data	$\overline{\text{Data}}$
GND	0.7	–2.35	GND	Upper: –2.117 Middle: –2.350 Lower: –2.583	No errors occur.		
	0.3	–2.15		Upper: –2.050 Middle: –2.150 Lower: –2.250			
	0.7	+2.95		Upper: 3.183 Middle: 2.950 Lower: 2.717			
	0.3	+3.15		Upper: 3.250 Middle: 3.150 Lower: 3.050			

Table C.3.1.5-4 Input Level Range (PAM4 >32.1 Gbaud)

Settings					Specification	Results	
MU196020A			MU196040B				
Termination	Amplitude (Vp-p)	Offset (Vth) (V)	Termination	Threshold Voltage (V)		Data	$\overline{\text{Data}}$
GND	0.7	–2.35	GND	Upper: –2.117 Middle: –2.350 Lower: –2.583	No errors occur.		
	0.4	–2.20		Upper: –2.067 Middle: –2.200 Lower: –2.333			
	0.7	+2.95		Upper: 3.183 Middle: 2.950 Lower: 2.717			
	0.4	+3.10		Upper: 3.233 Middle: 3.100 Lower: 2.967			

Table C.3.1.5-5 Test Pattern (PRBS-NRZ)

Settings				Specification	Results	
MU196020A		MU196040B				
Length	Logic	Length	Logic		Data	$\overline{\text{Data}}$
2^7–1	POS	2^7–1	POS	No errors occur.		
2^9–1	POS	2^9–1	POS			
2^11–1	POS	2^11–1	POS			
2^13–1	POS	2^13–1	POS			
2^15–1	POS	2^15–1	POS			
2^20–1	POS	2^20–1	POS			
2^23–1	POS	2^23–1	POS			
2^31–1	POS	2^31–1	POS			
2^31–1	NEG	2^31–1	NEG			

Table C.3.1.5-6 Test Pattern (PRBS-PAM4)

Settings						Specification	Results	
MU196020A			MU196040B					
Length	Logic MSB	Logic LSB	Length	Logic MSB	Logic LSB		Data	$\overline{\text{Data}}$
2^7–1	POS	POS	2^7–1	POS	POS	No errors occur.		
2^9–1	POS	POS	2^9–1	POS	POS			
2^11–1	POS	POS	2^11–1	POS	POS			
2^15–1	POS	POS	2^15–1	POS	POS			
2^20–1	POS	POS	2^20–1	POS	POS			
2^23–1	POS	POS	2^23–1	POS	POS			
2^31–1	POS	POS	2^31–1	POS	POS			
2^31–1	NEG	NEG	2^31–1	NEG	NEG			

Table C.3.1.5-7 Test Pattern (Zero Substitution -NRZ)

Settings				Specification	Results	
MU196020A		MU196040B				
Length	Logic	Length	Logic		Data	$\overline{\text{Data}}$
2^7	POS	2^7	POS	No errors occur.		
2^9	POS	2^9	POS			
2^10	POS	2^10	POS			
2^11	POS	2^11	POS			
2^15	POS	2^15	POS			
2^20	POS	2^20	POS			
2^23	POS	2^23	POS			
2^7–1	POS	2^7–1	POS			
2^9–1	POS	2^9–1	POS			
2^10–1	POS	2^10–1	POS			
2^11–1	POS	2^11–1	POS			
2^15–1	POS	2^15–1	POS			
2^20–1	POS	2^20–1	POS			
2^23–1	POS	2^23–1	POS			

Table C.3.1.5-8 Test Pattern (SSPRQ-PAM4)

Settings				Specification	Results	
MU196020A		MU196040B				
Pattern	Logic	Pattern	Logic		Data	$\overline{\text{Data}}$
SSPRQ	POS	SSPRQ	POS	No errors occur.		

Table C.3.1.5-9 Error Detection

Item	Specification	Results	
		Data	$\overline{\text{Data}}$
Error rate (ER)	5.0000E–12		
Error count (EC)	1.0000E–00		
Error free interval (%EFI)	99.9900%		
Error interval (EI)	1		

C.3.2 MU196020C/MU196040B

C.3.2.1 MU196020C-001

Table C.3.2.1-1 Operating Frequency Range

Specification	Results	
	Data	$\overline{\text{Data}}$
No errors occur within the range from 2.4 to 32.1 Gbit/s.*		
No errors occur within the range from 2.4 to 32.1 Gbaud.*		

*: Pattern PRBS, 2^31–1

Table C.3.2.1-2 MU196020C-001 Waveform Evaluation Test- Amplitude (NRZ)

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (Vp-p)	Upper Limit (Vp-p)	Data	$\overline{\text{Data}}$
32.1 Gbit/s	0.70	0.581	0.819		
	0.07	0.027	0.113		

Table C.3.2.1-3 MU196020C-001 Waveform Evaluation Test- 0/3 Level Amplitude (PAM4)

Settings		Specification		Results	
Baud rate	Amplitude (Vp-p)	Lower Limit (Vp-p)	Upper Limit (Vp-p)	Data	$\overline{\text{Data}}$
32.1 Gbaud	0.70	0.581	0.819		
	0.07	0.027	0.113		

Table C.3.2.1-4 Waveform Evaluation Test- Offset (NRZ)

Settings		Specification		Results	
Bit rate	Offset (Vth)	Lower Limit (V)	Upper Limit (V)	Data	$\overline{\text{Data}}$
32.1 Gbit/s	3.265	2.817	3.713		
	–2.35	–2.590	–2.111		

Table C.3.2.1-5 MU196020C-001 Waveform Evaluation Test- Offset (PAM4)

Settings		Specification		Results	
Baud rate	Offset (Vth)	Lower Limit (V)	Upper Limit (V)	Data	$\overline{\text{Data}}$
32.1 Gbaud	3.265	2.817	3.713		
	–2.35	–2.590	–2.111		

Table C.3.2.1-6 MU196020C-001 Waveform Evaluation Test-Cross point (NRZ)

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (%)	Upper Limit (%)	Data	$\overline{\text{Data}}$
32.1 Gbit/s	0.50	40	60		

Table C.3.2.1-7 MU196020C-001 Waveform Evaluation Test- Tr/Tf (NRZ)

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (ps)	Upper Limit (ps)	Data	$\overline{\text{Data}}$
32.1 Gbit/s	0.50	–	9.0*1		
		–	9.5*2		

*1: When J1789A cables are used.

*2: When J1790A cables are used.

Table C.3.2.1-8 MU196020C-001 Waveform Evaluation Test- Jitter (NRZ)

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (ps)	Upper Limit (ps p-p)	Data	$\overline{\text{Data}}$
32.1 Gbit/s	0.50	–	6.0		

C.3.2.2 MU196020C-002

Table C.3.2.2-1 Operating Frequency Range

Specification	Results	
	Data	$\overline{\text{Data}}$
No errors occur within the range from 2.4 to 32.1 Gbit/s.*		
No errors occur within the range from 2.4 to 32.1 Gbaud.*		

*: Pattern PRBS, 2^31–1

Table C.3.2.2-2 MU196020C-002 Waveform Evaluation Test- Amplitude (NRZ)

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (Vp-p)	Upper Limit (Vp-p)	Data	$\overline{\text{Data}}$
58.2 Gbit/s	0.70*1	0.581	0.819		
	0.60*2	0.493	0.707		
	0.07	0.027	0.113		

*1: When J1789A cables are used.

*2: When J1790A cables are used.

Table C.3.2.2-3 MU196020C-002 Waveform Evaluation Test-0/3 Level Amplitude (PAM4)

Settings		Specification		Results	
Baud rate	Amplitude (Vp-p)	Lower Limit (Vp-p)	Upper Limit (Vp-p)	Data	$\overline{\text{Data}}$
58.2 Gbaud	0.70*1	0.581	0.819		
	0.60*2	0.493	0.707		
	0.07	0.027	0.113		

*1: When J1789A cables are used.

*2: When J1790A cables are used.

Table C.3.2.2-4 MU196020C-002 Waveform Evaluation Test- Offset (NRZ)

Settings		Specification		Results	
Bit rate	Offset (Vth)	Lower Limit (V)	Upper Limit (V)	Data	$\overline{\text{Data}}$
58.2 Gbit/s	3.265	2.817	3.713		
	–2.30*1	–2.489	–2.112		
	–2.35*2	–2.590	–2.111		

*1: When J1790A cables are used, Amplitude 0.60 Vp-p

*2: When J1789A cables are used, Amplitude 0.70 Vp-p

Table C.3.2.2-5 MU196020C-002 Waveform Evaluation Test- Offset (PAM4)

Settings		Specification		Results	
Baud rate	Offset (Vth)	Lower Limit (V)	Upper Limit (V)	Data	$\overline{\text{Data}}$
58.2 Gbaud	3.265	2.817	3.713		
	–2.30*1	–2.489	–2.112		
	–2.35*2	–2.590	–2.111		

*1: When J1790A cables are used, Amplitude 0.60 Vp-p

*2: When J1789A cables are used, Amplitude 0.70 Vp-p

Table C.3.2.2-6 MU196020C-002 Waveform Evaluation Test- Cross point (NRZ)

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (%)	Upper Limit (%)	Data	$\overline{\text{Data}}$
58.2 Gbit/s	0.50	40	60		

Table C.3.2.2-7 MU196020C-002 Waveform Evaluation Test- Tr/Tf (NRZ)

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (ps)	Upper Limit (ps)	Data	$\overline{\text{Data}}$
58.2 Gbit/s	0.50	–	8.5*1		
		–	8.8*2		

*1: When J1789A cables are used.

*2: When J1790A cables are used.

Table C.3.2.2-8 MU196020C-002 Waveform Evaluation Test- Jitter (NRZ)

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (ps)	Upper Limit (ps p-p)	Data	$\overline{\text{Data}}$
58.2 Gbit/s	0.50	–	6.0		

C.3.2.3 MU196020C-003

Table C.3.2.3-1 Operating Frequency Range

Specification	Results	
	Data	$\overline{\text{Data}}$
No errors occur within the range from 2.4 to 32.1 Gbit/s.*		
No errors occur within the range from 2.4 to 32.1 Gbaud.*		

*: Pattern PRBS, 2^31–1

Table C.3.2.3-2 MU196020C-003 Waveform Evaluation Test- Amplitude (NRZ)

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (Vp-p)	Upper Limit (Vp-p)	Data	$\overline{\text{Data}}$
64.2 Gbit/s	0.70*1	0.581	0.819		
	0.55*2	0.405	0.595		
	0.07	0.027	0.113		

*1: When J1789A cables are used.

*2: When J1790A cables are used.

Table C.3.2.3-3 MU196020C-003 Waveform Evaluation Test-0/3 Level Amplitude (PAM4)

Settings		Specification		Results	
Baud rate	Amplitude (Vp-p)	Lower Limit (Vp-p)	Upper Limit (Vp-p)	Data	$\overline{\text{Data}}$
64.2 Gbaud	0.70*1	0.581	0.819		
	0.55*2	0.405	0.595		
	0.07	0.027	0.113		

*1: When J1789A cables are used.

*2: When J1790A cables are used.

Table C.3.2.3-4 MU196020C-003 Waveform Evaluation Test- Offset (NRZ)

Settings		Specification		Results	
Bit rate	Offset (Vth)	Lower Limit (V)	Upper Limit (V)	Data	$\overline{\text{Data}}$
64.2 Gbit/s	3.265	2.817	3.713		
	–2.275*1	–2.438	–2.112		
	–2.35*2	–2.590	–2.111		

*1: When J1790A cables are used, Amplitude 0.55 Vp-p

*2: When J1789A cables are used, Amplitude 0.70 Vp-p

Table C.3.2.3-5 MU196020C-003 Waveform Evaluation Test- Offset (PAM4)

Settings		Specification		Results	
Baud rate	Offset (Vth)	Lower Limit (V)	Upper Limit (V)	Data	$\overline{\text{Data}}$
64.2 Gbaud	3.265	2.817	3.713		
	–2.275*1	–2.438	–2.112		
	–2.35*2	–2.590	–2.111		

*1: When J1790A cables are used, Amplitude 0.55 Vp-p

*2: When J1789A cables are used, Amplitude 0.70 Vp-p

Table C.3.2.3-6 MU196020C-003 Waveform Evaluation Test - Cross point (NRZ)

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (%)	Upper Limit (%)	Data	$\overline{\text{Data}}$
64.2 Gbit/s	0.50	40	60		

Table C.3.2.3-7 MU196020C-003 Waveform Evaluation Test - Tr/Tf (NRZ)

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (ps)	Upper Limit (ps)	Data	$\overline{\text{Data}}$
64.2 Gbit/s	0.50	–	8.5*1		
		–	8.8*2		

*1: When J1789A cables are used.

*2: When J1790A cables are used.

Table C.3.2.3-8 MU196020C-003 Waveform Evaluation Test- Jitter (NRZ)

Settings		Specification		Results	
Bit rate	Amplitude (Vp-p)	Lower Limit (ps)	Upper Limit (ps p-p)	Data	$\overline{\text{Data}}$
64.2 Gbit/s	0.50	–	6.0		

C.3.2.4 MU196040B

Use the performance test record sheets in C.3.1.5 “MU196040B”.

C.3.3 MU196060A

Table C.3.3-1 Self-loopback (NRZ)

Settings*		Specification	Results
Bitrate	Differential Amplitude (Vp-p)		
16.0 Gbit/s	0.18	BER < 1E-12	
	0.8		
32.0 Gbit/s	0.18		
	0.8		

*: Modified Compliance Pattern

*: SSC 33 KHz 5300 ppm Down spread

Table C.3.3-2 Self-loopback (NRZ)

Settings*		Specification	Results
Bitrate	Differential Amplitude (Vp-p)		
19.0 Gbit/s	0.18	BER < 1E-12	
	0.8		
26.5625 Gbit/s	0.18		
	0.8		
32.1 Gbit/s	0.18		
	0.8		

*: Pattern PRBS, 2^31-1

*: SSC OFF

Table C.3.3-3 Self-loopback (PAM4)

Settings*		Specification	Results
Bitrate	**Differential Amplitude (Vp-p)**		
16.0 Gbaud	0.4	BER < 1E-8	
	0.8		
32.0 Gbaud	0.4		
	0.8		

*: Modified Compliance Pattern

*: SSC 33 KHz 5300 ppm Down spread

Table C.3.3-4 Self-loopback (PAM4)

Settings*		Specification	Results
Bitrate	**Differential Amplitude (Vp-p)**		
19.0 Gbaud	0.4	BER < 1E-8	
	0.8		
26.5625 Gbaud	0.4		
	0.8		
32.1 Gbaud	0.4		
	0.8		

*: Pattern PRBS, 2^31-1

*: SSC OFF