MS2690A/MS2691A/MS2692A and MS2830A/MS2840A Signal Analyzer Vector Signal Generator Operation Manual Standard Waveform Pattern

13th Edition

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ANRITSU CORPORATION

Document No.: M-W2929AE-13.0

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MS2690A/MS2691A/MS2692A and MS2830A/MS2840A
Signal Analyzer Vector Signal Generator
Operation Manual Standard Waveform Pattern

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Revision History:

February 29th, 2020
December 17th, 2021

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  - Install important updates of Windows.
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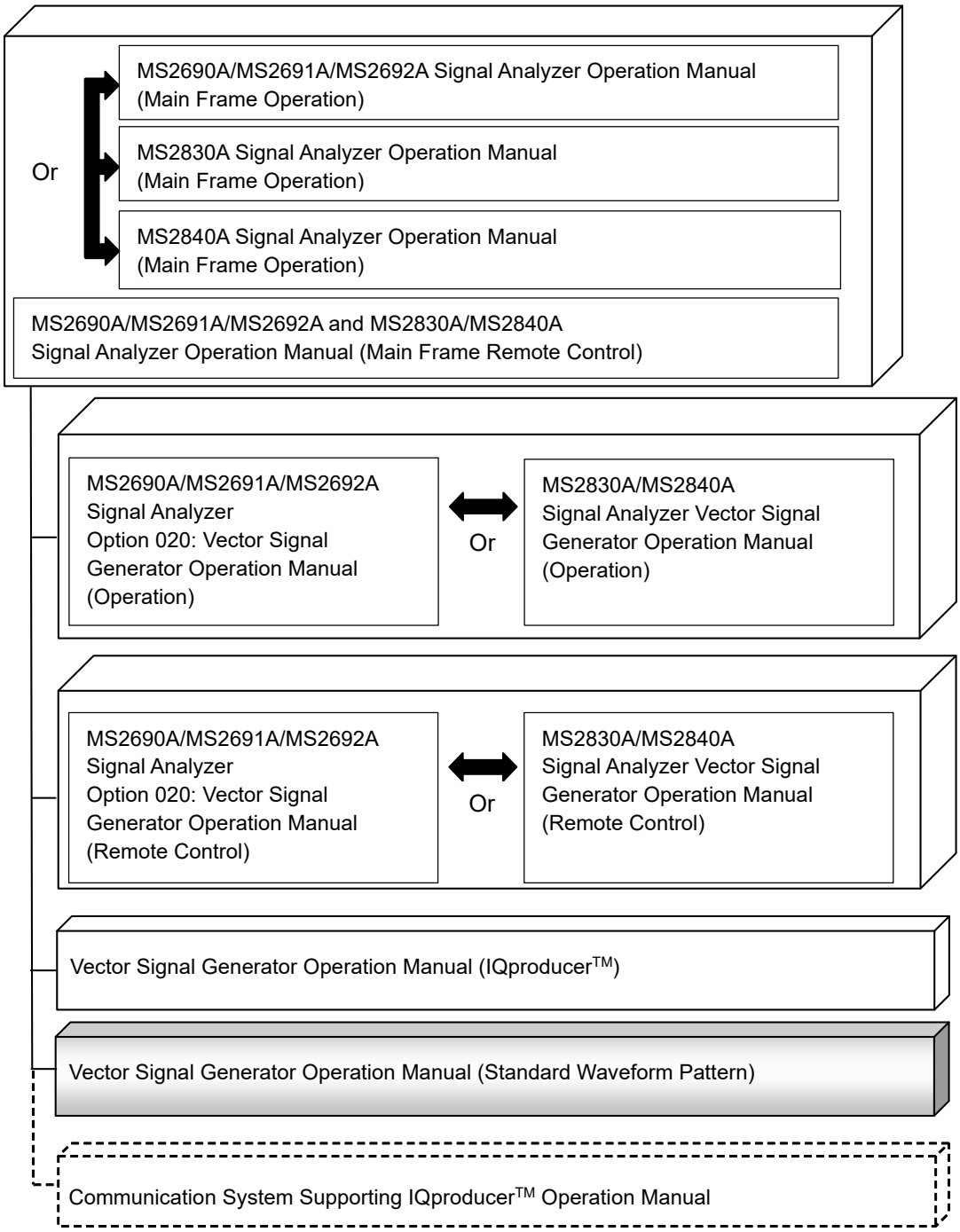
About This Manual

■ Associated Documents

The operation manuals for the MS2690A/MS2691A/MS2692A, MS2830A or MS2840A Signal Analyzer are comprised as shown in the figure below.



- **Signal Analyzer Operation Manual (Mainframe Operation)**
- **Signal Analyzer Operation Manual (Mainframe Remote Control)**

These manuals describe basic operating methods, maintenance procedures, common functions, and common remote control of the signal analyzer mainframe.

- **Vector Signal Generator Operation Manual (Operation)**

This manual describes functions, operating methods, and so on of the vector signal generator (option).

- **Vector Signal Generator Operation Manual (Remote Control)**

This manual describes remote control of the vector signal generator (option).

- **Vector Signal Generator Operation Manual (IQproducer™)**

This manual describes functions, operating methods, and so on of the IQproducer, which is application software used with the vector signal generator (option).

- **Vector Signal Generator Operation Manual (Standard Waveform Pattern) <This document>**

This manual describes details on the standard waveform pattern data used with the vector signal generator (option).

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IV.

Chapter 1 Overview

This chapter provides an overview of the standard waveform pattern for the MS2690A/MS2691A/MS2692A or MS2830A/MS2840A Signal Analyzer Vector Signal Generator option.

1.1 Overview of Product 1-2

1.1 Overview of Product

The standard waveform pattern for MS2690A/MS2691A/MS2692A or MS2830A/MS2840A Signal Analyzer Vector Signal Generator (hereinafter, referred to as “standard waveform pattern”) consists of waveform patterns* that are used in a wide range of applications from research and development to manufacturing of the systems, devices, and equipment in the field of digital mobile communications.

The standard waveform pattern can be used in MS2690A/MS2691A/MS2692A or MS2830A/MS2840A Signal Analyzer Vector Signal Generator option that integrates an arbitrary waveform generator.

*: The waveform pattern described here indicates arbitrary waveform data used for supporting various radio communication systems that can be used by the arbitrary waveform generator integrated in the Vector Signal Generator.
The waveform pattern consists of two files: an arbitrary waveform file and a waveform information file. The arbitrary waveform file is a binary-format file with the extension “.wvd”. The waveform information file is a text-format file with the extension “.wvi”, used to control waveform data and set the hardware for waveform data output.

Chapter 2 How to Use Standard Waveform Pattern

This chapter describes how to use the standard waveform pattern.

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2.2 Configuration of Standard Waveform Pattern Package 2-3
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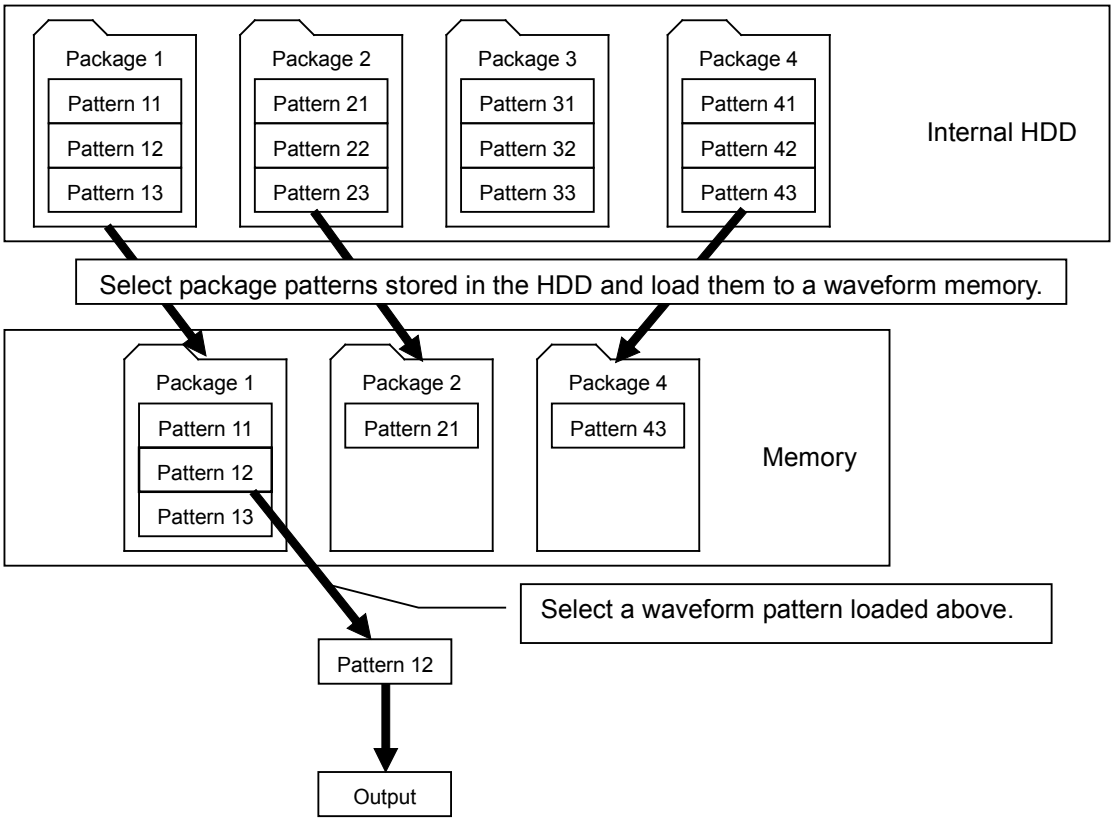
2.1 How to Use Standard Waveform Pattern

The standard waveform pattern is shipped stored in the internal HDD/SSD of the Vector Signal Generator.

The waveform pattern stored in the internal HDD/SSD is reproduced by the arbitrary waveform generator integrated in the Vector Signal Generator, and used to perform vector modulation.

The waveform patterns are classified by communication type and stored in a folder. This folder is called a "package", and the standard waveform patterns classified by communication type are stored in each package with the corresponding communication system name. When reproducing a waveform pattern, it is necessary first to load the package pattern stored in the internal HDD/SSD to a waveform memory in the Vector Signal Generator.

Next, select a waveform pattern to be output from those loaded into the waveform memory.



Refer to Section 2.4 "Setting Modulation Function" in the Vector Signal Generator Operation Manual (Operation) for details of waveform pattern selection.

2.2 Configuration of Standard Waveform Pattern Package

The standard waveform patterns are stored in the internal HDD/SSD of the Vector Signal Generator, and classified into packages with the corresponding communication system name.

Table 2.2-1 List of packages

Package name	Contents
W-CDMA (UE Rx test)	Waveform patterns for 3GPP W-CDMA, UE Rx test
W-CDMA (UE Tx test)	Waveform patterns for 3GPP W-CDMA, UE Tx test
W-CDMA (BS Rx test)	Waveform patterns for 3GPP W-CDMA, BS Rx test
W-CDMA (BS Tx test)	Waveform patterns for 3GPP W-CDMA, BS Tx test
GSM	Various waveform patterns for GSM
CDMA2000 1X	Various waveform patterns for CDMA2000 1X
CDMA2000_1xEV-DO	Various waveform patterns for CDMA2000 1xEV-DO
WLAN	Various waveform patterns for WLAN
Digital_Broadcast	Various waveform patterns for the ISDB-S, ISDB-T, ISDB-Tsb, DVB-S, ITU-T J83 AnnexC
Bluetooth®	Various waveform patterns for Bluetooth®
WCDMA-UL (RF_Device)	Waveform patterns for W-CDMA Uplink, RF Device test
WCDMA-DL (RF_Device)	Waveform patterns for W-CDMA Downlink, RF Device test
GSM (RF_Device)	Waveform pattern for GSM, RF Device test

Refer to the Appendix A “Standard Attached Waveform” in the MX269041A Digital I/F Control Software for DigRF2.5G/3G Operation Manual (BBIF Operation) for the standard waveform pattern with “(RF_Device)” at the end of the package name.

Note that these waveform patterns are not stored within the internal HDD/SSD of MS2830A or MS2840A.

2.3 Output Level Range of Standard Waveform Pattern

Table 2.3-1 shows the guaranteed range of level error (±0.2 dB) for the RF output signal of the Vector Signal Generator, between in vector modulation and CW mode.

Table 2.3-1 Guaranteed level range of RF output level accuracy

System name	Guaranteed level range
W-CDMA GSM CDMA2000 1X CDMA2000 1xEV-DO WLAN Digital_Broadcast *Bluetooth*®	125 MHz ≤ f ≤ 3 GHz: ≤ –15 dBm

Table 2.3-2 shows the level setting range in which the distortion characteristics of the RF output signal of the Vector Signal Generator (which effect the ACLR and other characteristics) are stable. The distortion characteristics become worse if the level exceeds the reference level shown in Table 2.3-2.

Table 2.3-2 Reference level for distortion characteristics of RF output signal

System name	Reference level
W-CDMA GSM CDMA2000 1X CDMA2000 1xEV-DO WLAN Digital_Broadcast *Bluetooth*®	Frequency range: 800 MHz to 2.7 GHz Level: –5 dBm

Chapter 3 Details of Standard Waveform Pattern

This chapter describes each standard waveform pattern in detail.

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3.1 W-CDMA Waveform Pattern

Table 3.1-1 lists the provided W-CDMA waveform patterns.

Table 3.1-1 List of W-CDMA waveform patterns (1/3)

Waveform Pattern Name	UL/DL	Channel Configuration	3GPP Reference Standard	Main Application
UL_RMC_12_2kbps*3	UL	DPCCH, DPDCH	TS25.141 A.2	BS RX test
UL_RMC_64kbps*3	UL	DPCCH, DPDCH	TS25.141 A.3	BS RX test
UL_RMC_144kbps*3	UL	DPCCH, DPDCH	TS25.141 A.4	BS RX test
UL_RMC_384kbps*3	UL	DPCCH, DPDCH	TS25.141 A.5	BS RX test
UL_AMR_TFCS1*3	UL	DPCCH, DPDCH	TS25.944 4.1.2	BS RX test
UL_AMR_TFCS2*3	UL	DPCCH, DPDCH	TS25.944 4.1.2	BS RX test
UL_AMR_TFCS3*3	UL	DPCCH, DPDCH	TS25.944 4.1.2	BS RX test
UL_ISDN*1, *3	UL	DPCCH, DPDCH	TS25.944 4.1.2	BS RX test
UL_64kbps_Packet*3	UL	DPCCH, DPDCH	TS25.944 4.1.2	BS RX test
UL_Interferer	UL	DPCCH, DPDCH	TS25.141 I	BS RX test
DL_RMC_12_2kbps_RX*3	DL	P-CPICH, SCH, PICH, DPCH	TS25.101 A.3.1 TS25.101 C.3.1	UE RX test
DL_RMC_12_2kbps*3	DL	P-CPICH, SCH, PICH, DPCH, OCNS	TS25.101 A.3.1 TS25.101 C.3.2	UE RX test
DL_RMC_12_2kbps_MIL*3	DL	P-CPICH, SCH, PICH, DPCH, OCNS	TS25.101 A.3.1 TS25.101 C.3.1	UE RX test
DL_RMC_64kbps*3	DL	P-CPICH, SCH, PICH, DPCH, OCNS	TS25.101 A.3.2 TS25.101 C.3.2	UE RX test
DL_RMC_144kbps*3	DL	P-CPICH, SCH, PICH, DPCH, OCNS	TS25.101 A.3.3 TS25.101 C.3.2	UE RX test
DL_RMC_384kbps*3	DL	P-CPICH, SCH, PICH, DPCH, OCNS	TS25.101 A.3.4 TS25.101 C.3.2	UE RX test
DL_AMR_TFCS1*3	DL	P-CPICH, SCH, PICH, DPCH, OCNS	TS25.944 4.1.1.3 TS25.101 C.3.2	UE RX test
DL_AMR_TFCS2*3	DL	P-CPICH, SCH, PICH, DPCH, OCNS	TS25.944 4.1.1.3 TS25.101 C.3.2	UE RX test
DL_AMR_TFCS3*3	DL	P-CPICH, SCH, PICH, DPCH, OCNS	TS25.944 4.1.1.3 TS25.101 C.3.2	UE RX test
DL_ISDN*3	DL	P-CPICH, SCH, PICH, DPCH, OCNS	TS25.944 4.1.1.3 TS25.101 C.3.2	UE RX test
DL_384kbps_Packet*3	DL	P-CPICH, SCH, PICH, DPCH, OCNS	TS25.944 4.1.1.3 TS25.101 C.3.2	UE RX test
DL_Interferer	DL	P-CPICH, P-CCPCH, SCH, PICH, OCNS	TS25.101 C.4	UE RX test

Table 3.1-1 List of W-CDMA waveform patterns (2/3)

Waveform Pattern Name	UL/DL	Channel Configuration	3GPP Reference Standard	Main Application
TestModel_1_4DPCH	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 4 DPCH	TS25.141 V11.4.0	BS TX device test
TestModel_1_8DPCH	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 8 DPCH	TS25.141 V11.4.0	BS TX device test
TestModel_1_16DPCH	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 16 DPCH	TS25.141 V11.4.0	BS TX device test
TestModel_1_32DPCH	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 32 DPCH	TS25.141 V11.4.0	BS TX device test
TestModel_1_64DPCH	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 64 DPCH	TS25.141 V11.4.0	BS TX device test
TestModel_2	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 3 DPCH	TS25.141 V11.4.0	BS TX device test
TestModel_3_4DPCH	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 4 DPCH	TS25.141 V11.4.0	BS TX device test
TestModel_3_8DPCH	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 8 DPCH	TS25.141 V11.4.0	BS TX device test
TestModel_3_16DPCH	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 16 DPCH	TS25.141 V11.4.0	BS TX device test
TestModel_3_32DPCH	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 32 DPCH	TS25.141 V11.4.0	BS TX device test
TestModel_4	DL	P-CCPCH, SCH	TS25.141 V11.4.0	BS TX device test
TestModel_4_CPICH	DL	P-CPICH, P-CCPCH, SCH	TS25.141 V11.4.0	BS TX device test
TestModel_ 1_64DPCHx2*1	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 64 DPCH	TS25.141 V11.4.0	BS TX device test
TestModel_ 1_64x2_10M*1, *2	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 64 DPCH	TS25.141 V11.4.0	BS TX device test
TestModel_ 1_64x2_15M*1, *2	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 64 DPCH	TS25.141 V11.4.0	BS TX device test

Table 3.1-1 List of W-CDMA waveform patterns (3/3)

Waveform Pattern Name	UL/DL	Channel Configuration	3GPP Reference Standard	Main Application
TestModel_ 1_64DPCHx3*1	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 64 DPCH	TS25.141 V11.4.0	BS TX device test
TestModel_ 1_64DPCHx4*1	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 64 DPCH	TS25.141 V11.4.0	BS TX device test
TestModel_5_4DPCH	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 4 DPCH, HS-SCCH, 4 HS-PDSCH	TS25.141 V11.4.0	BS TX device test
TestModel_5_2HSPDSCH	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 6 DPCH, HS-SCCH, 2 HS-PDSCH	TS25.141 V11.4.0	BS TX device test
TestModel_5_4HSPDSCH	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 14 DPCH, HS-SCCH, 4 HS-PDSCH	TS25.141 V11.4.0	BS TX device test
TestModel_5_8HSPDSCH	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 30 DPCH, HS-SCCH, 8 HS-PDSCH	TS25.141 V11.4.0	BS TX device test
TestModel_6_4HSPDSCH	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 4 DPCH, HS-SCCH, 4 HS-PDSCH	TS25.141 V11.4.0	BS TX device test
TestModel_6_8HSPDSCH	DL	P-CPICH, P-CCPCH, SCH, PICH, S-CCPCH, 30 DPCH, HS-SCCH, 8 HS-PDSCH	TS25.141 V11.4.0	BS TX device test
DL_CPICH	DL	P-CPICH	–	UE RX test
UL_RMC_12_2kbps_TX*3	UL	DPCCH, DPDCH	TS25.101 A.2.1	UE TX device test

*1: x2, x3, and x4 indicate the number of multicarriers 2, 3, and 4, respectively.

*2: 10M and 15M indicate the frequency spacing values of the multi-carrier.

*3: For MS2830A or MS2840A: ARB Memory Upgrade 256 Msamples (option 027) must be installed to use this waveform pattern.

3.1.1 UL_RMCxxxkbps

These waveform patterns execute channel coding, division and spreading to physical channels, and power setting conforming to the UL Reference Measurement Channel standard described in 3GPP TS 25.141 Annex A.

Table 3.1.1-1 lists the parameters commonly used by each waveform pattern. When outputting each waveform pattern, marker signals listed in the following table are output from the AUX connector at the rear panel.

Table 3.1.1-1 List of common parameters

Parameter	Setting Value
Scrambling Code	0_H
DTCH Information Data	PN9
DCCH information Data	All 0
Over sampling rate	3
Marker 1	Frame Clock
Marker 2	Slot Clock
Marker 3	–

Channel coding parameters for UL_RMC_12_2kbps

Table 3.1.1-2 Physical channel parameters for UL reference measurement channel 12.2 kbps

Parameter	Unit	Level
Information bit rate	kbps	12.2
DPDCH	kbps	60
DPCCH	kbps	15
DPCCH Slot Format #i	–	0
DPCCH/DPDCH power ratio	dB	–2.69
TFCI	–	On
Repetition	%	23

Table 3.1.1-3 Transport channel parameters for UL reference measurement channel 12.2 kbps

Parameter	DTCH	DCCH
Transport Channel Number	1	2
Transport Block Size	244	100
Transport Block Set Size	244	100
Transmission Time Interval	20 ms	40 ms
Type of Error Protection	Convolution Coding	Convolution Coding
Coding Rate	1/3	1/3
Rate Matching attribute	256	256
Size of CRC	16	12

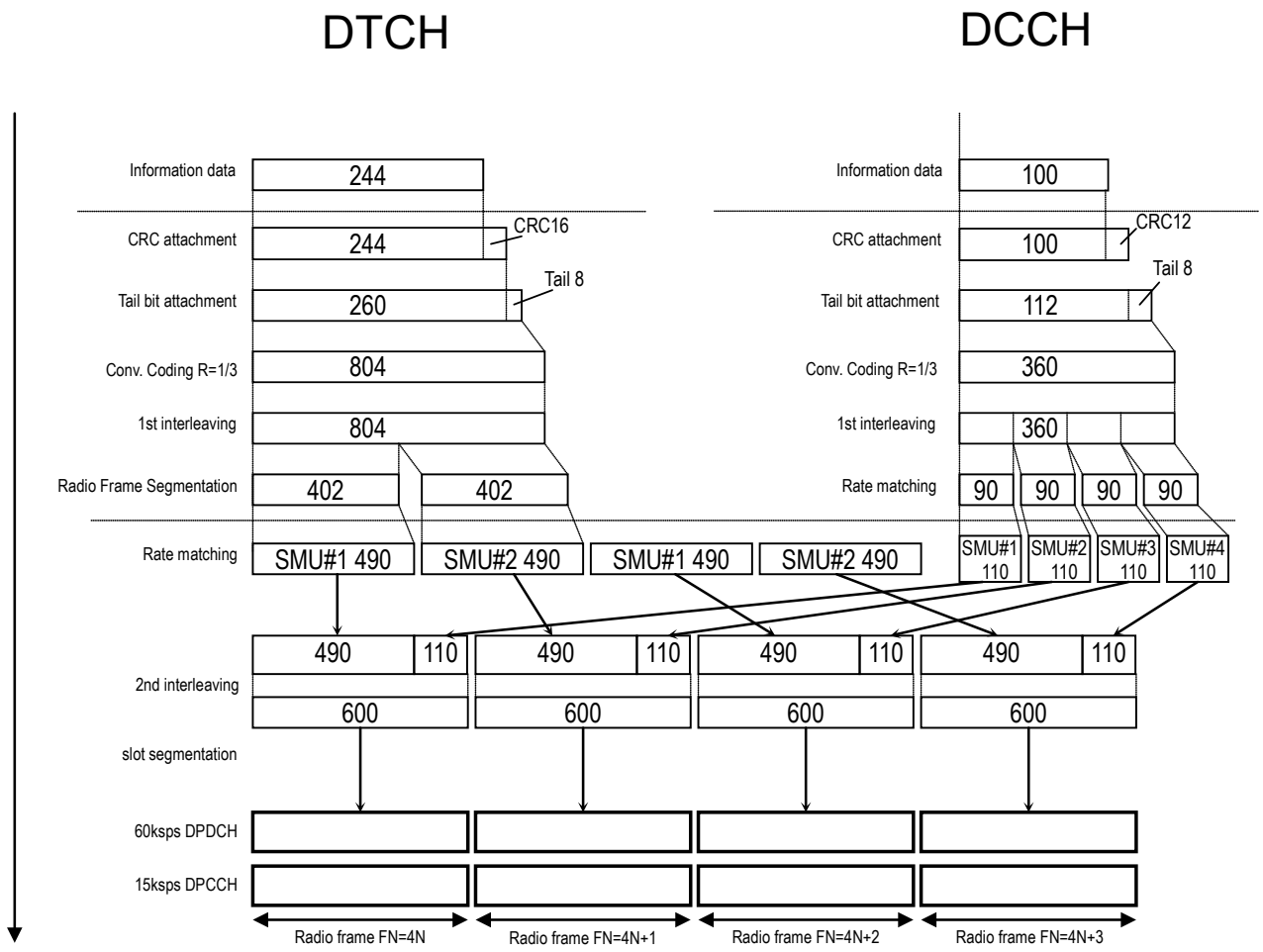


Figure 3.1.1-1 Channel coding for UL_RMC_12_2kbps

Channel coding parameters for UL_RMC_12_2kbps_TX

Table 3.1.1-4 Physical channel parameters for UL reference measurement channel 12.2 kbps for Tx test

Parameter	Unit	Level
Information bit rate	kbps	12.2
DPDCH	kbps	60
DPCCH	kbps	15
DPCCH Slot Format #i	–	0
DPCCH/DPDCH power ratio	dB	–5.46
TFCI	–	On
Repetition	%	23

Table 3.1.1-5 Transport channel parameters for UL reference measurement channel 12.2 kbps for Tx test

Parameters	DTCH	DCCH
Transport Channel Number	1	2
Transport Block Size	244	100
Transport Block Set Size	244	100
Transmission Time Interval	20 ms	40 ms
Type of Error Protection	Convolution Coding	Convolution Coding
Coding Rate	1/3	1/3
Rate Matching attribute	256	256
Size of CRC	16	12

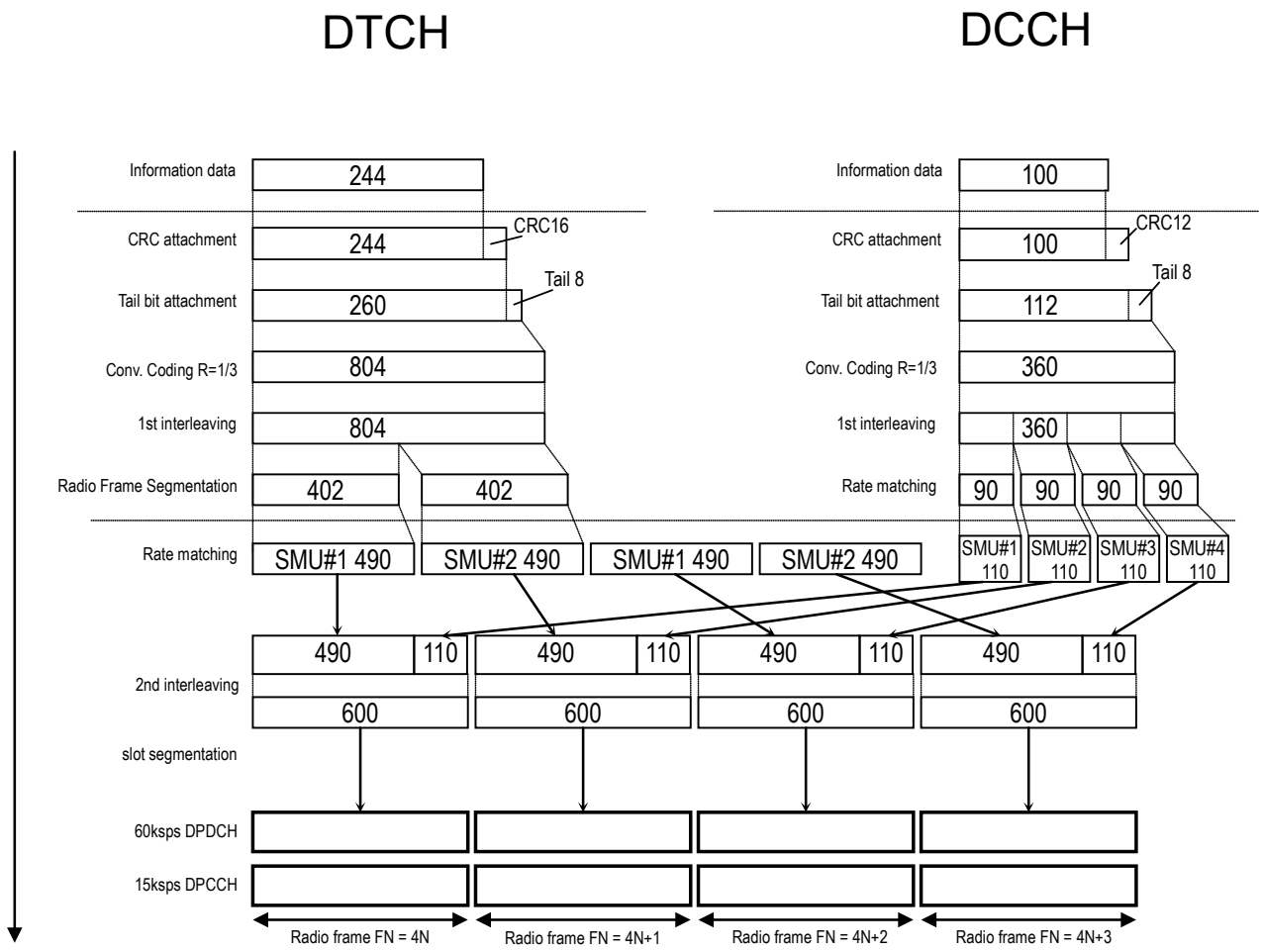


Figure 3.1.1-2 Channel coding for UL_RMC_12_2kbps_TX

Channel coding parameters for UL_RMC_64kbps

Table 3.1.1-6 Physical channel parameters for UL reference measurement channel 64 kbps

Parameter	Unit	Level
Information bit rate	kbps	64
DPDCH	kbps	240
DPCCH	kbps	15
DPCCH Slot Format #i	–	0
DPCCH/DPDCH power ratio	dB	–5.46
TFCI	–	On
Repetition	%	18

Table 3.1.1-7 Transport channel parameters for UL reference measurement channel 64 kbps

Parameter	DTCH	DCCH
Transport Channel Number	1	2
Transport Block Size	2560	100
Transport Block Set Size	2560	100
Transmission Time Interval	40 ms	40 ms
Type of Error Protection	Turbo Coding	Convolution Coding
Coding Rate	1/3	1/3
Rate Matching attribute	256	256
Size of CRC	16	12

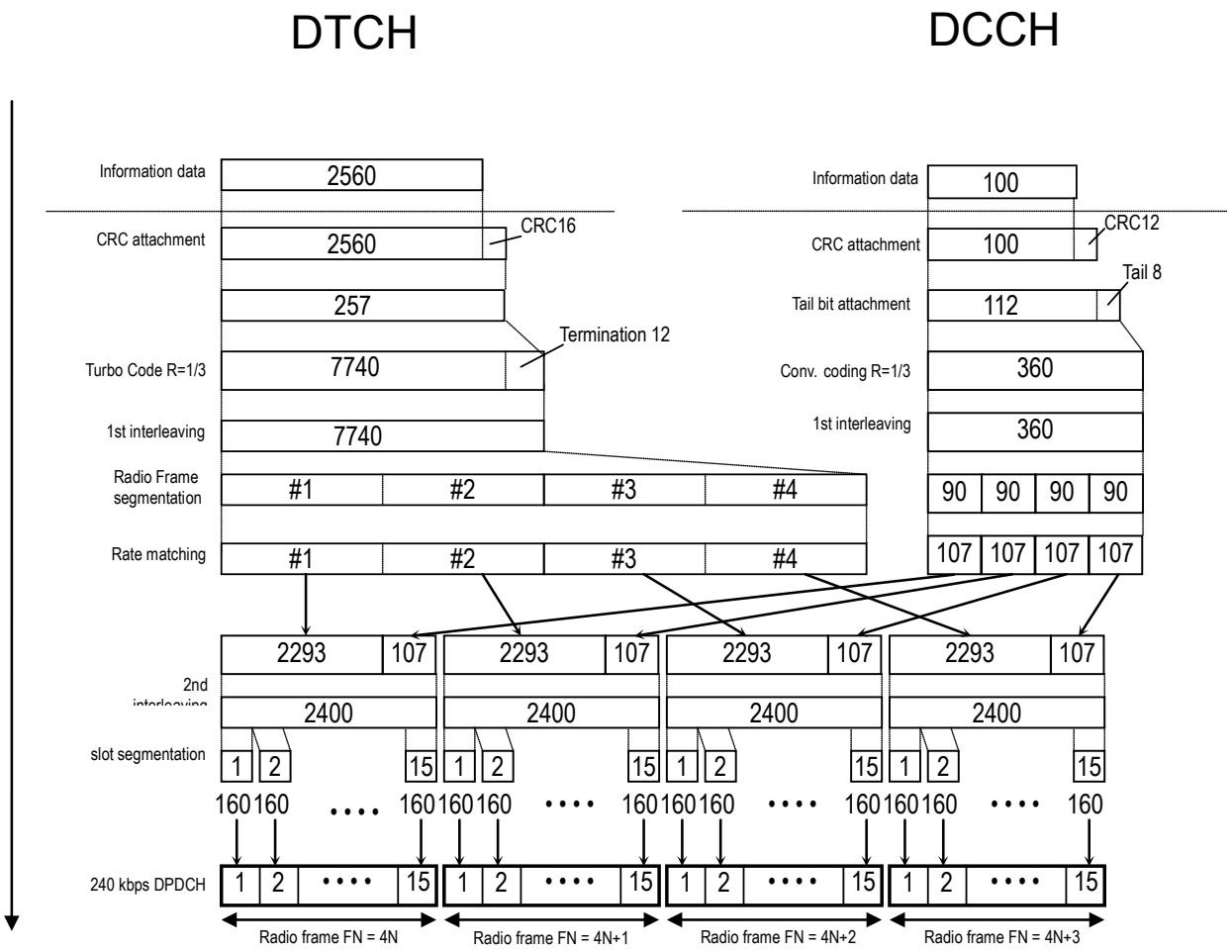


Figure 3.1.1-3 Channel coding for UL_RMC_64kbps

Channel coding parameters for UL_RMC_144kbps

Table 3.1.1-8 Physical channel parameters for UL reference measurement channel 144 kbps

Parameter	Unit	Level
Information bit rate	kbps	144
DPDCH	kbps	480
DPCCH	kbps	15
DPCCH Slot Format #i	–	0
DPCCH/DPDCH power ratio	dB	–9.54
TFCI	–	On
Repetition	%	8

Table 3.1.1-9 Transport channel parameters for UL reference measurement channel 144 kbps

Parameter	DTCH	DCCH
Transport Channel Number	1	2
Transport Block Size	2880	100
Transport Block Set Size	5760	100
Transmission Time Interval	40 ms	40 ms
Type of Error Protection	Turbo Coding	Convolution Coding
Coding Rate	1/3	1/3
Rate Matching attribute	256	256
Size of CRC	16	12

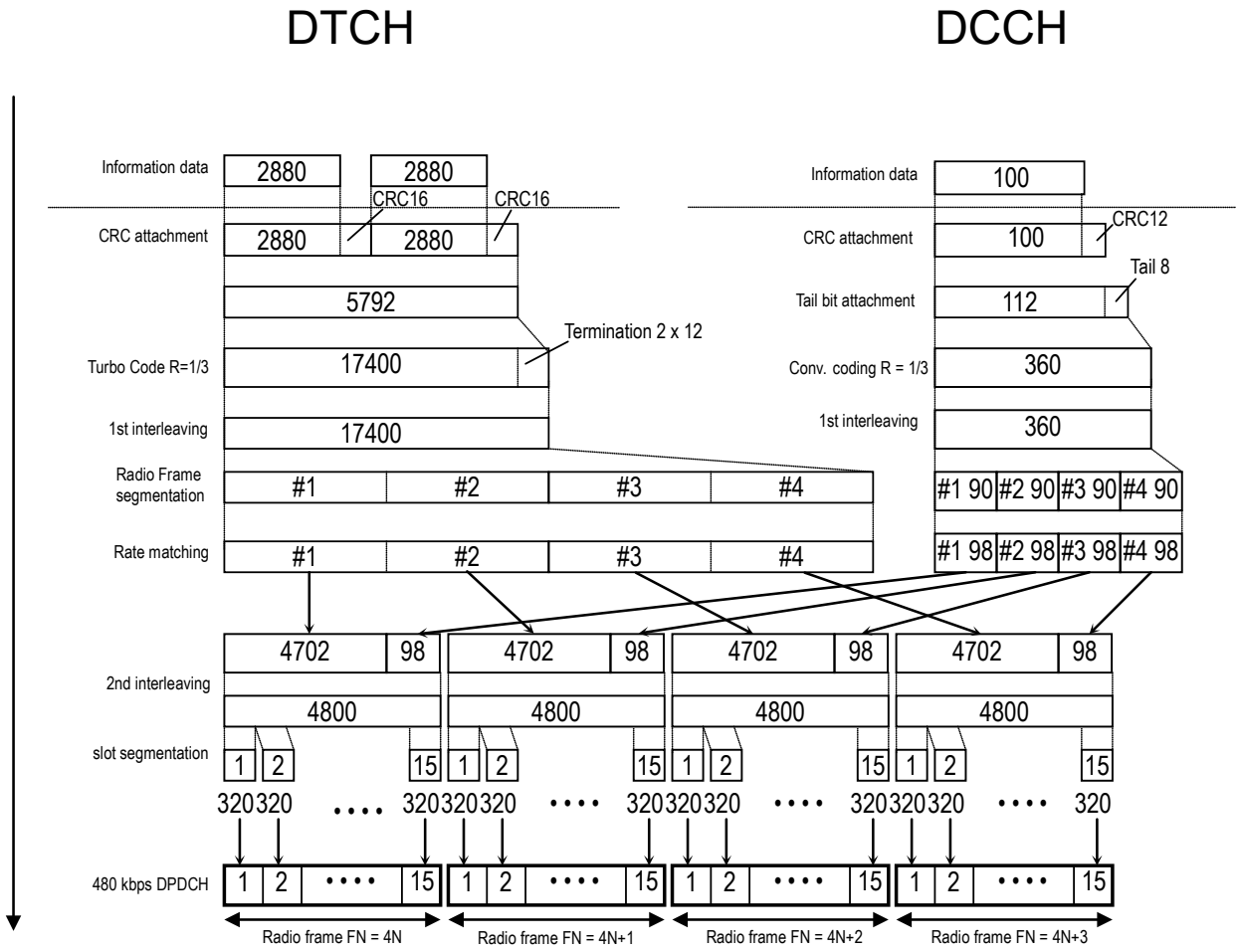


Figure 3.1.1-4 Channel coding for UL_RMC_144kbps

Channel coding parameters for UL_RMC_384kbps

Table 3.1.1-10 Physical channel parameters for UL reference measurement channel 384 kbps

Parameter	Unit	Level
Information bit rate	kbps	384
DPDCH	kbps	960
DPCCH	kbps	15
DPCCH Slot Format #i	–	0
DPCCH/DPDCH power ratio	dB	–9.54
TFCI	–	On
Puncturing	%	18

Table 3.1.1-11 Transport channel parameters for UL reference measurement channel 384 kbps

Parameter	DTCH	DCCH
Transport Channel Number	1	2
Transport Block Size	3840	100
Transport Block Set Size	15360	100
Transmission Time Interval	40 ms	40 ms
Type of Error Protection	Turbo Coding	Convolution Coding
Coding Rate	1/3	1/3
Rate Matching attribute	256	256
Size of CRC	16	12

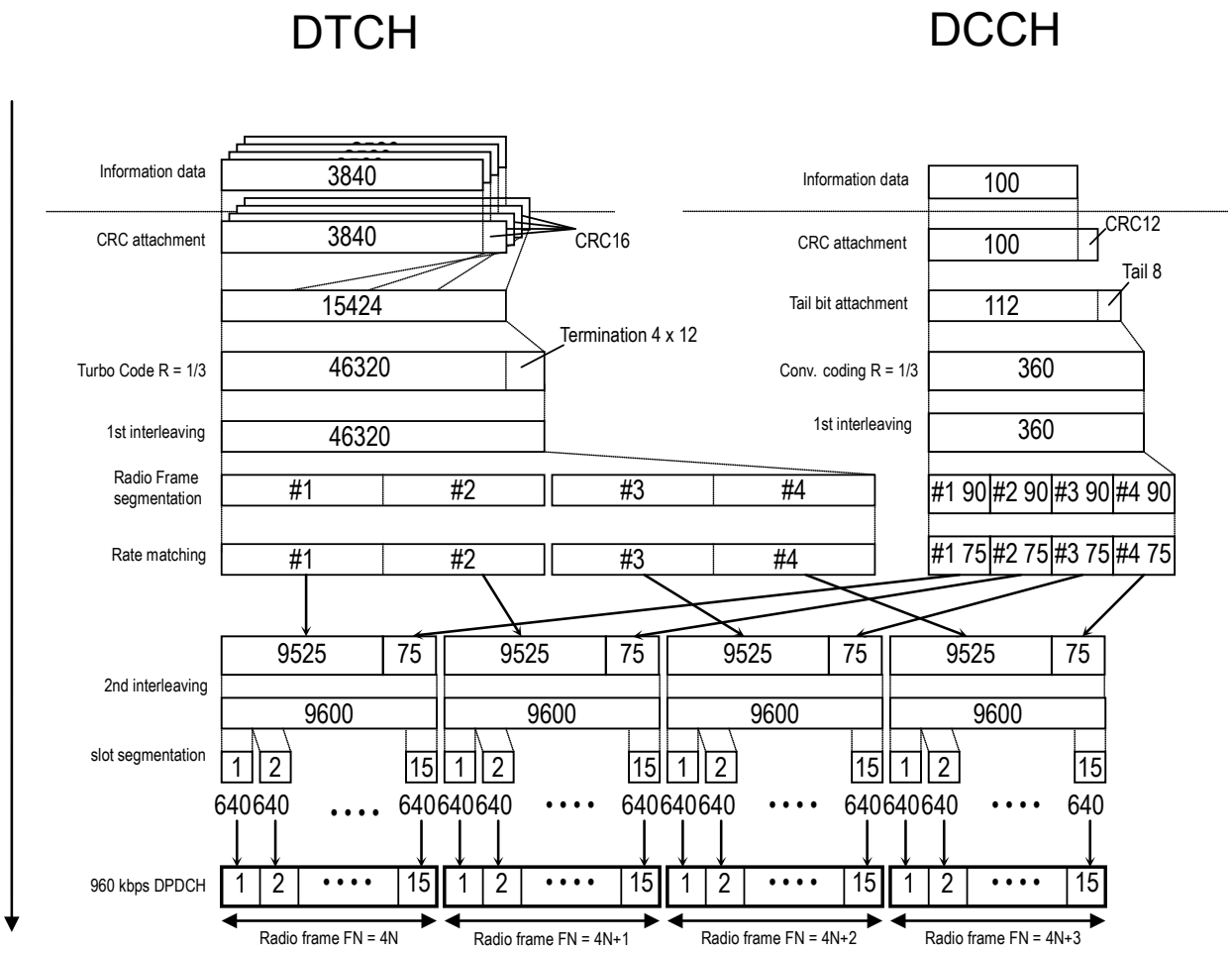


Figure 3.1.1-5 Channel coding for UL_RMC_384kbps

3.1.2 UL_AMR_TFCSx/UL_ISDN/UL_64kbps_Packet

These waveform patterns execute channel coding, division and spreading to physical channels, and power setting conforming to the Channel coding and multiplexing example (Uplink) standard described in 3GPP TS 25.944 Section 4.1.2.

Table 3.1.2-1 lists the parameters commonly used by each waveform pattern. When a waveform pattern is output, a marker signal shown in Table 3.1.2-1 is output from the AUX connector on the rear panel.

Table 3.1.2-1 List of common parameters

Parameter	Setting Value
Scrambling Code	0_H
DTCH Information Data	PN9
DCCH Information Data	All 0
Over sampling rate	3
Marker 1	Frame Clock
Marker 2	Slot Clock
Marker 3	–

Channel coding parameters for UL_AMR_TFCSx

Table 3.1.2-2 Physical channel parameters for UL_AMR_TFCSx

Parameter	Unit	Level
DPDCH	kbps	60
DPCCH	kbps	15
DPCCH Slot Format #i	–	0
DPCCH/DPDCH power ratio	dB	–2.69

Table 3.1.2-3 Parameters for 3.4 kbps data (DCCH)

Transport Block Size	148 bits
Transport Block Set Size	148 bits
Rate Matching attribute	160
CRC	16 bits
Coding	CC, coding rate = 1/3
TTI	40 ms

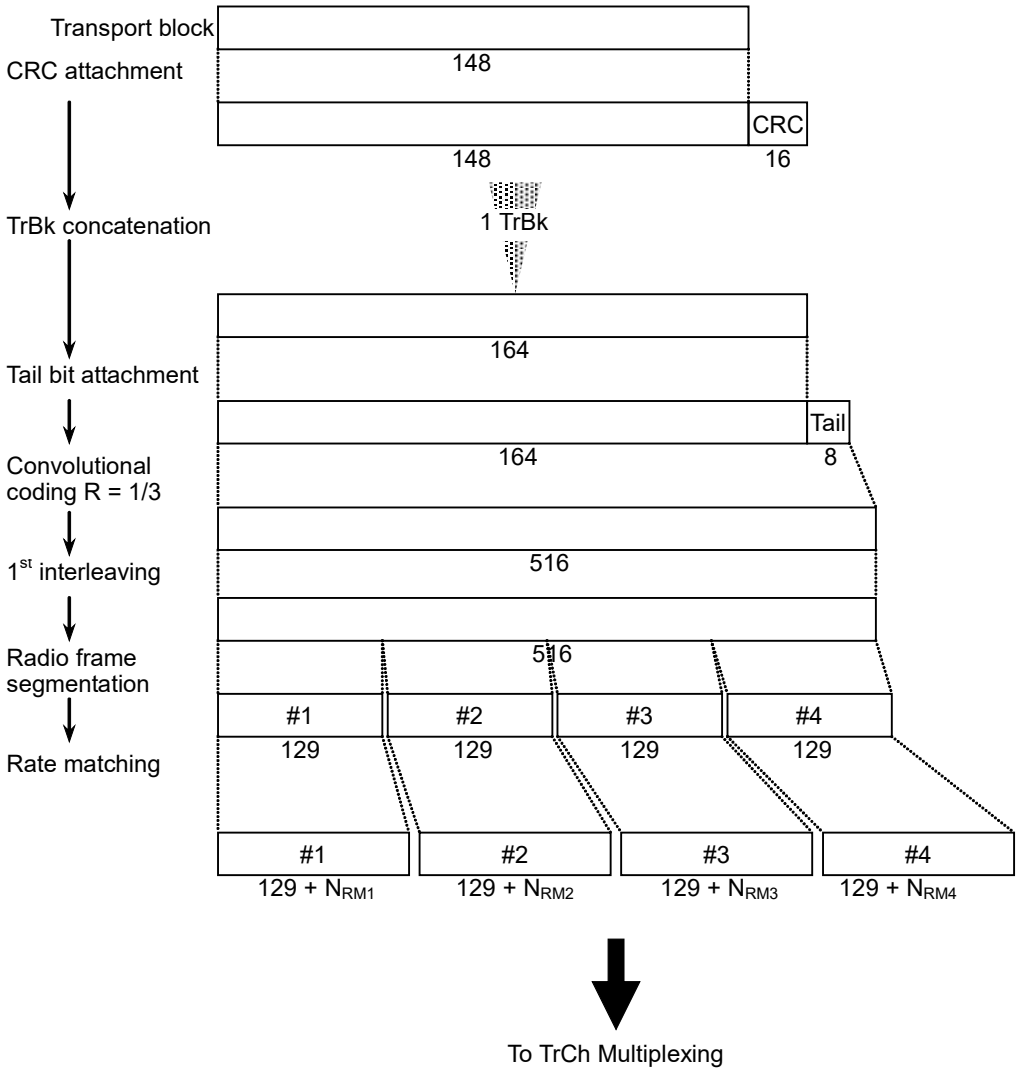
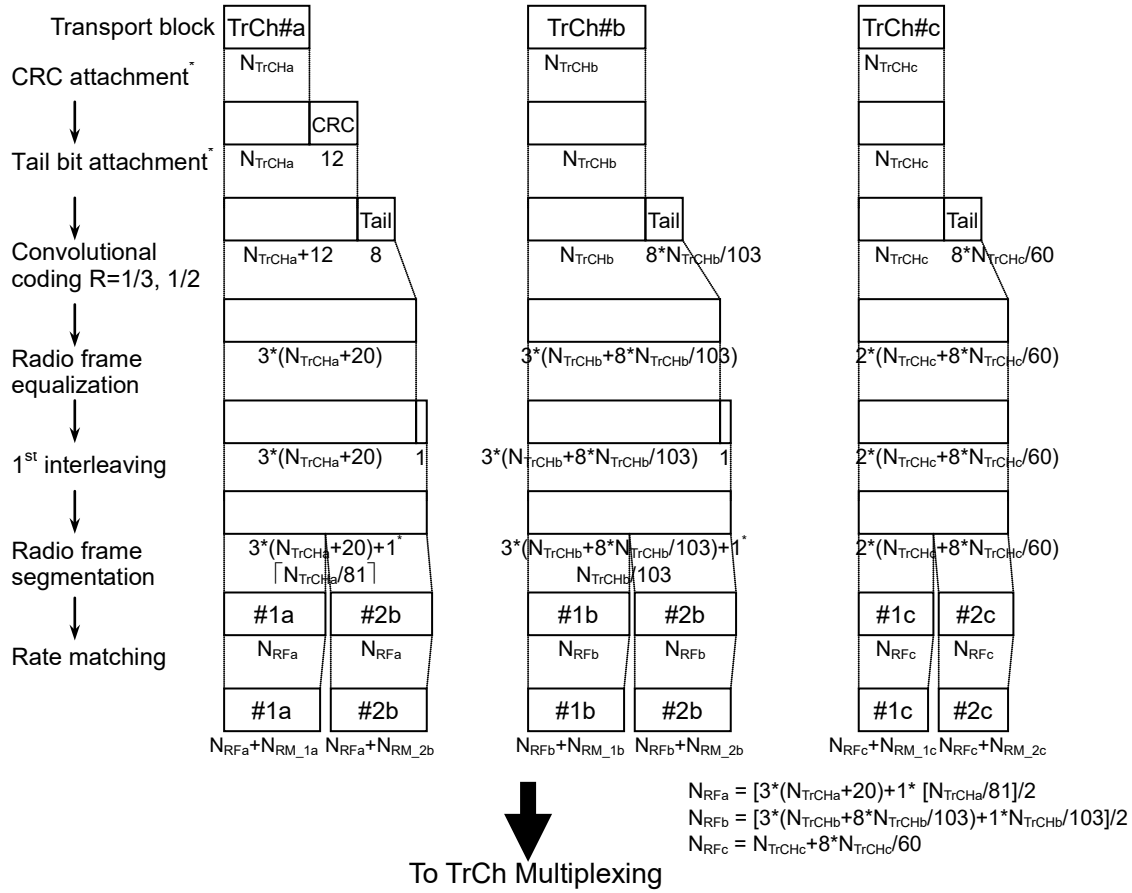


Figure 3.1.2-1 Channel coding and multiplexing for UL_AMR_TFCSx - 1

Table 3.1.2-4 Parameters for 12.2 kbps data (DTCH)

Number of TrCHs		3
Transport Block Size	**TrCH#a**	39 or 81 bits
	TrCH#b	103 bits
	TrCH#c	60 bits
TFCS	**#1**	N_{TrCHa} = 1*81, N_{TrCHb} = 1*103, N_{TrCHc} = 1*60 bits
	#2	N_{TrCHa} = 1*39, N_{TrCHb} = 0*103, N_{TrCHc} = 0*60 bits
	#3	N_{TrCHa} = 0*81, N_{TrCHb} = 0*103, N_{TrCHc} = 0*60 bits
Rate Matching attribute		RM_a = 200, RM_b = 190, RM_c = 235
CRC		12 bits (attached to TrCH#a only)
Coding		CC, coding rate = 1/3 for TrCH#a, b coding rate = 1/2 for TrCH#c
TTI		20 ms



*: CRC and tail bits for TrCH#a are attached even if N_{TrCha} = 0 bits since CRC parity bit attachment for 0-bit transport block is applied.

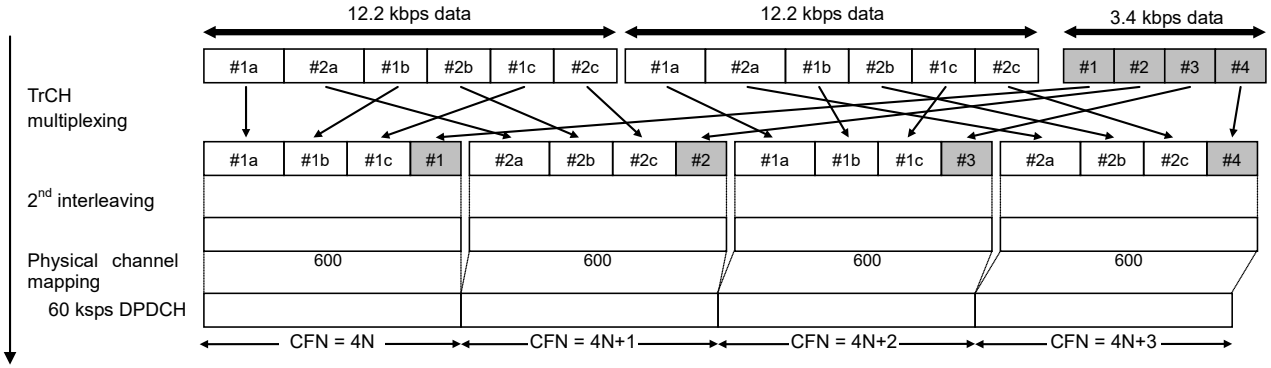


Figure 3.1.2-2 Channel coding and multiplexing for UL_AMR_TFCSx - 2

Channel coding parameters for UL_ISDN

Table 3.1.2-5 Physical channel parameters for UL_ISDN

Parameter	Unit	Level
Information bit rate	kbps	64
DPDCH	kbps	240
DPCCH	kbps	15
DPCCH Slot Format #i	–	0
DPCCH/DPDCH power ratio	dB	–5.46

Table 3.1.2-6 Parameters for 64 kbps data

Number of TrChs	1
Transport Block Size	640 bits
Transport Block Set Size	4*640 bits
Rate Matching attribute	170
CRC	16 bits
Coding	Turbo coding, coding rate = 1/3
TTI	40 ms

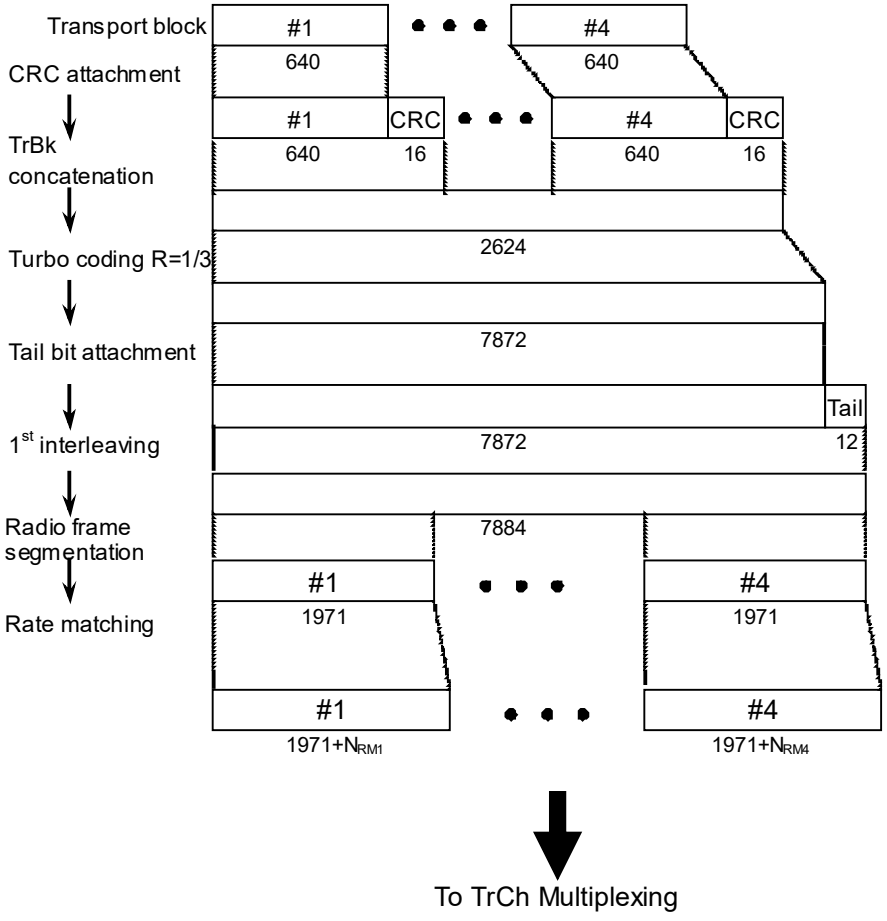


Figure 3.1.2-3 Channel coding and multiplexing for UL_ISDN - 1

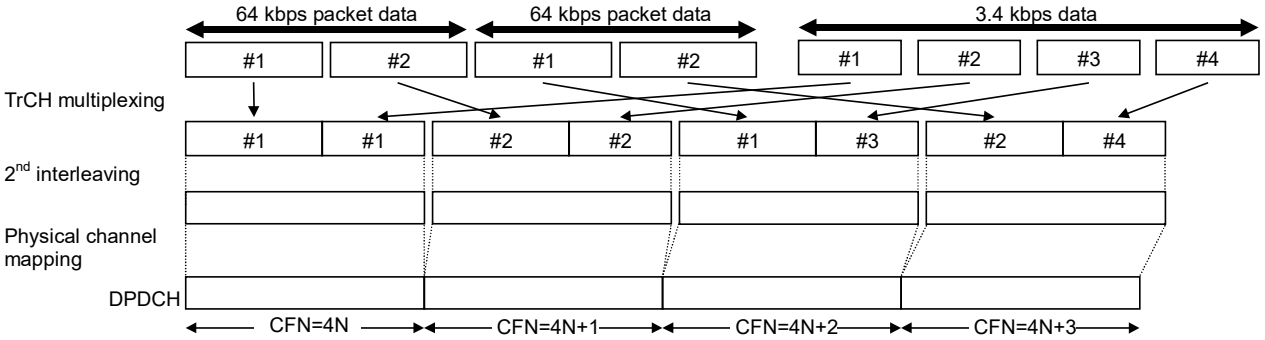


Figure 3.1.2-4 Channel coding and multiplexing for UL_ISDN - 2

Channel coding parameters for UL_64kbps_Packet

Table 3.1.2-7 Physical channel parameters for UL_64kbps_Packet

Parameter	Unit	Level
Information bit rate	kbps	64
DPDCH	kbps	240
DPCCH	kbps	15
DPCCH Slot Format #i	–	0
DPCCH/DPDCH power ratio	dB	–5.46

Table 3.1.2-8 Parameters for 64 kbps data

Number of TrChs		1
Transport Block Size		336 bits
Transport Block Set Size	**64 kbps**	336*B bits (B = 4)
Rate Matching attribute		150
CRC		16 bits
Coding		Turbo coding, coding rate = 1/3
TTI		20 ms

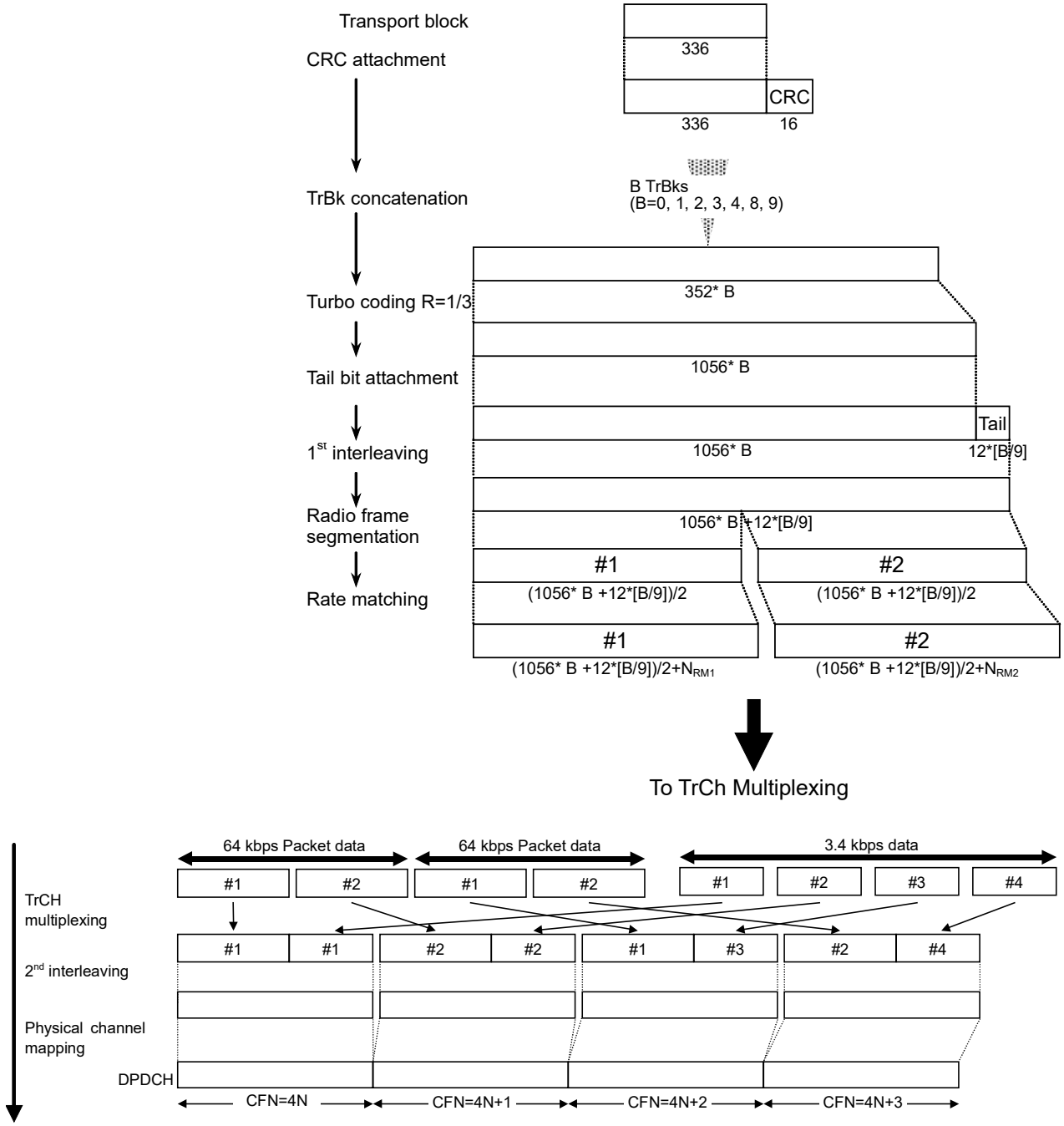


Figure 3.1.2-5 Channel coding and multiplexing for UL_64kbps_Packet

3.1.3 UL_Interferer

These waveform patterns execute division and spreading to physical channels, and power setting conforming to the Characteristics of the W-CDMA interference signal standard described in 3GPP TS 25.141 Annex I.

Table 3.1.3-1 Parameters for UL_Interferer

Parameter	Setting Value
Scrambling Code	1_H
DTCH Information Data	PN9
DCCH Information Data	All 0
Over sampling rate	3
Marker 1	Frame Clock
Marker 2	Slot Clock
Marker 3	–

Table 3.1.3-2 Physical channel parameters for UL_Interferer

Parameter	Unit	Level
Channel Bit Rate	kbps	64
DPDCH	kbps	240
DPCCH	kbps	15
DPCCH Slot Format #i	–	0
DPCCH/DPDCH power ratio	dB	–5.46

3.1.4 DL_RMCxxxkbps

These waveform patterns execute channel coding conforming to the DL Reference Measurement Channel standard described in 3GPP TS 25.101 Annex A, and execute division and spreading to physical channels in order to generate DPCH. They also execute power setting for control channels conforming to the standard described in 3GPP TS 25.101 Annex C.

Table 3.1.4-1 lists the parameters commonly used by each waveform pattern. When a waveform pattern is output, a marker signal shown in Table 3.1.4-1 is output from the AUX connector on the rear panel.

Table 3.1.4-1 List of common parameters

Parameter	Setting Value
Scrambling Code	80_H
DTCH Information Data	PN9
DCCH Information Data	All 0
SFN count	4096
Over sampling rate	4
Ch Code (P-CPICH)	0
Ch Code (P-CCPCH)	1
Ch Code (PICH)	16
Ch Code (DPCH for DL_RMC_12.2kbps)	96
Ch Code (DPCH for DL_RMC_12.2kbps_RX)	96
Ch Code (DPCH for DL_RMC_12.2kbps_MIL)	96
Ch Code (DPCH for DL_RMC_64kbps)	24
Ch Code (DPCH for DL_RMC_144kbps)	12
Ch Code (DPCH for DL_RMC_384kbps)	6
Ch Code (DPCH for DL_AMR_TFCSx)	96
Ch Code (DPCH for DL_ISDN)	24
Ch Code (DPCH for DL_384kbps_Packet)	6
OCNS	See Table 3.1.4-2.
Marker 1	TTI Pulse
Marker 2	–
Marker 3	–

Table 3.1.4-2 Parameters for OCNS

Channelization Code at SF = 128	Relative Level Setting (dB)	DPCH Data
2	–1	The DPCH data for each channelization code shall be in a bit sequence such that the data is uncorrelated with each other.
11	–3	
17	–3	
23	–5	
31	–2	
38	–4	
47	–8	
55	–7	
62	–4	
69	–6	
78	–5	
85	–9	
94	–10	
125	–8	
113	–6	
119	0	

Table 3.1.4-3 Physical channel powers for DL_RMC12_2kbps_RX

Physical Channel	Power Ratio
P-CPICH	P-CPICH_Ec/DPCH_Ec = 7 dB
P-CCPCH	P-CCPCH_Ec/DPCH_Ec = 5 dB
SCH	SCH_Ec/DPCH_Ec = 5 dB
PICH	PICH_Ec/DPCH_Ec = 2 dB
DPCH	DPCH_Ec/Ior = –10.3 dB

Table 3.1.4-4 Physical channel powers for DL_RMC12_2kbps_MIL

Physical Channel	Power ratio
P-CPICH	P-CPICH_Ec/Ior = –10 dB
P-CCPCH	P-CCPCH_Ec/Ior = –12 dB
SCH	SCH_Ec/Ior = –12 dB
PICH	PICH_Ec/Ior = –15 dB
DPCH	DPCH_Ec/Ior = –19 dB
OCNS	Power where the total power for all channels including OCNS is 0 dB

Table 3.1.4-5 Physical channel powers for DL_RMCxxxkbps (other than DL_RMC12_2kbps_RX and DL_RMC12_2kbps_MIL)

Physical Channel		Power ratio
P-CPICH		P-CPICH_Ec/Ior = –10 dB
P-CCPCH		P-CCPCH_Ec/Ior = –12 dB
SCH		SCH_Ec/Ior = –12 dB
PICH		PICH_Ec/Ior = –15 dB
DPCH	12.2 kbps	DPCH_Ec/Ior = –16.6 dB
	64 kbps	DPCH_Ec/Ior = –12.8 dB
	144 kbps	DPCH_Ec/Ior = –9.8 dB
	384 kbps	DPCH_Ec/Ior = –5.5 dB
OCNS		Power where the total power for all channels including OCNS is 0 dB

Channel coding parameters for DL_RMC_12_2kbps, DL_RMC_12_2kbps_RX, and DL_RMC_12_2kbps_MIL

Table 3.1.4-6 Physical channel parameters for DL reference measurement channel 12.2 kbps

Parameter	Unit	Level
Information bit rate	kbps	12.2
DPCH	ksps	30
Slot Format #i	–	11
TFCI	–	On
Power offsets PO1, PO2 and PO3	dB	0
Puncturing	%	14.7

Table 3.1.4-7 Transport channel parameters for DL reference measurement channel 12.2 kbps

Parameter	DTCH	DCCH
Transport Channel Number	1	2
Transport Block Size	244	100
Transport Block Set Size	244	100
Transmission Time Interval	20 ms	40 ms
Type of Error Protection	Convolution Coding	Convolution Coding
Coding Rate	1/3	1/3
Rate Matching attribute	256	256
Size of CRC	16	12

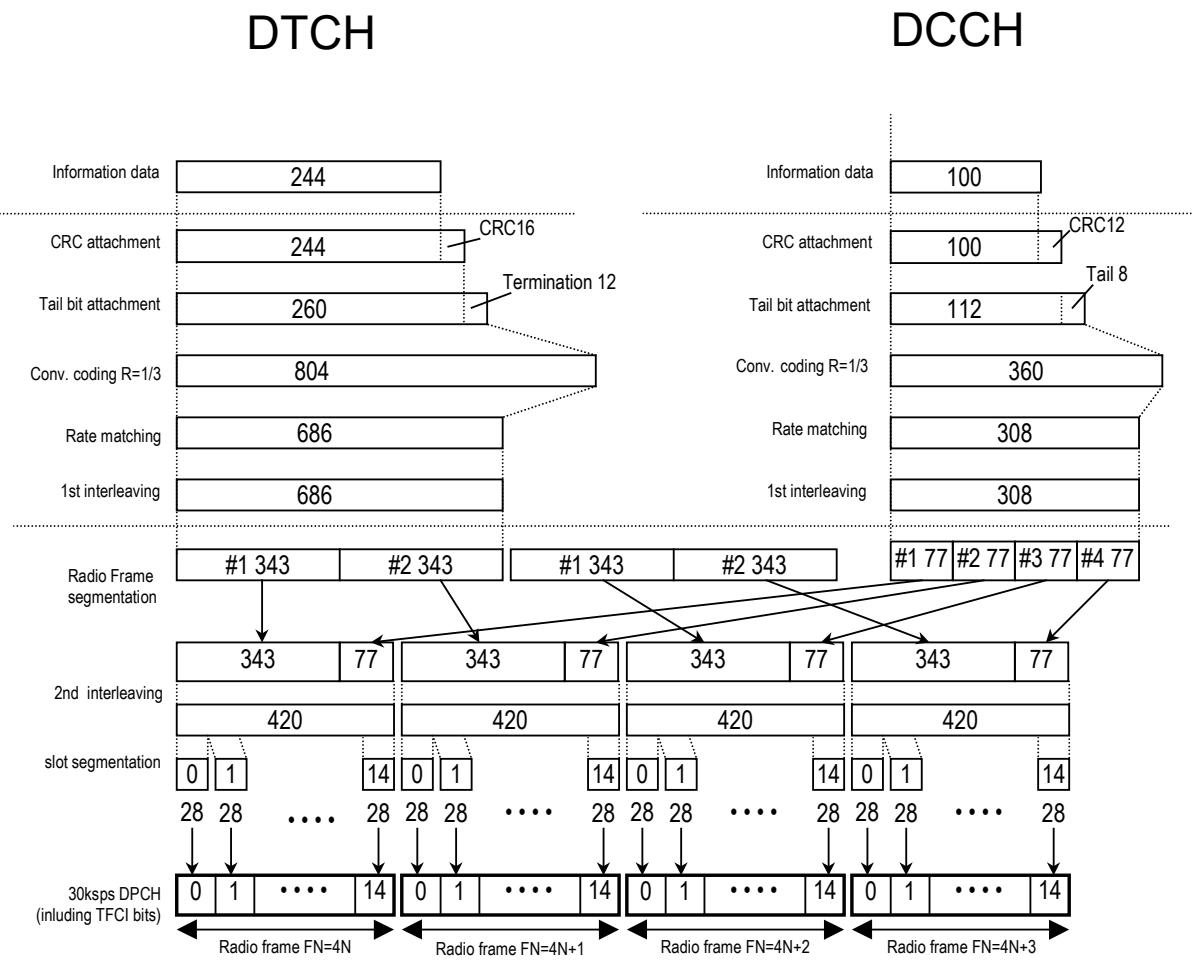


Figure 3.1.4-1 Channel coding for DL reference measurement channel 12.2 kbps

Channel coding parameters for DL_RMC_64kbps

Table 3.1.4-8 Physical channel parameters for DL reference measurement channel 64 kbps

Parameter	Unit	Level
Information bit rate	kbps	64
DPCH	ksps	120
Slot Format #i	–	13
TFCI	–	On
Power offsets PO1, PO2 and PO3	dB	0
Repetition	%	2.9

Table 3.1.4-9 Transport channel parameters for DL reference measurement channel 64 kbps

Parameter	DTCH	DCCH
Transport Channel Number	1	2
Transport Block Size	1280	100
Transport Block Set Size	1280	100
Transmission Time Interval	20 ms	40 ms
Type of Error Protection	Turbo Coding	Convolution Coding
Coding Rate	1/3	1/3
Rate Matching attribute	256	256
Size of CRC	16	12
Position of TrCH in radio frame	fixed	fixed

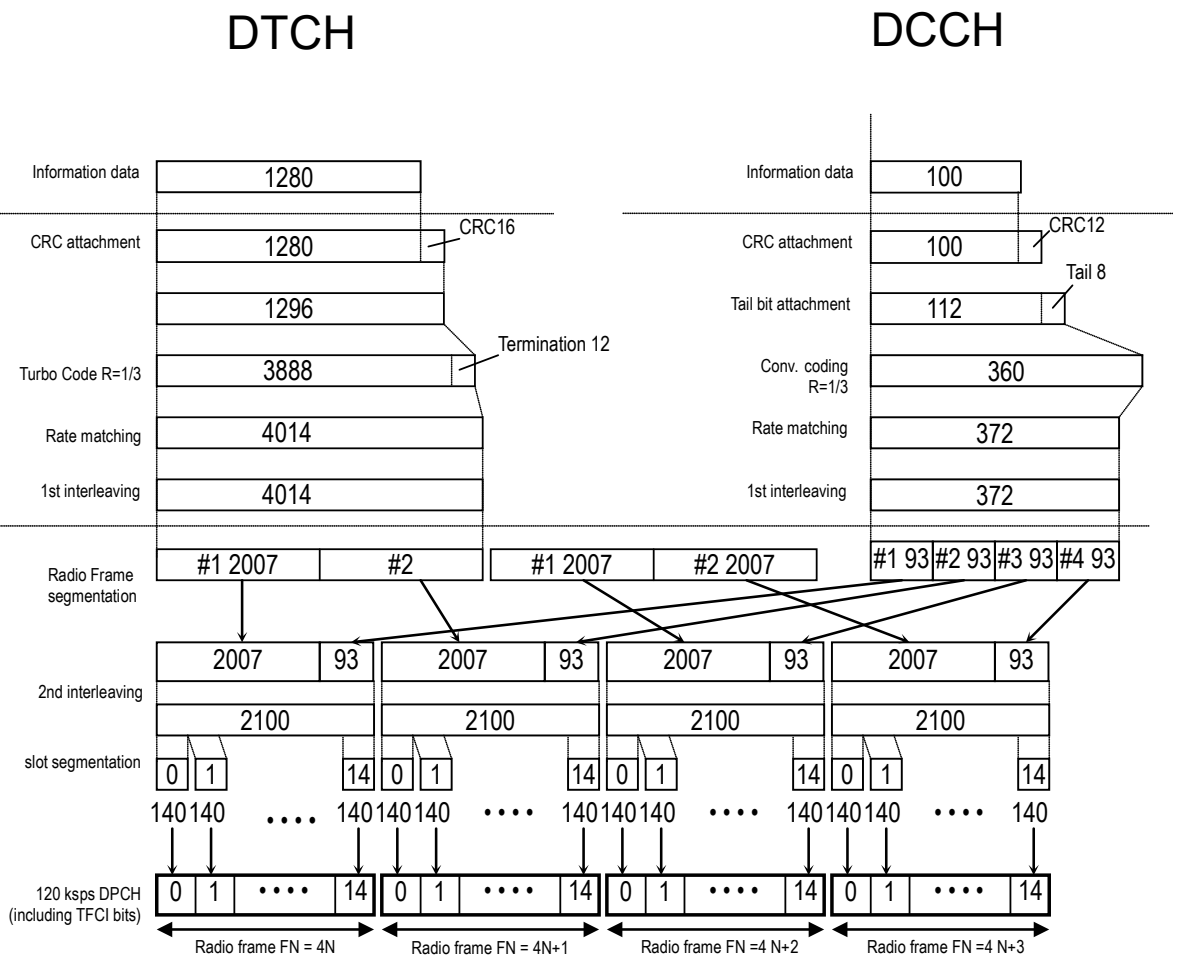


Figure 3.1.4-2 Channel coding for DL reference measurement channel 64 kbps

Channel coding parameters for DL_RMC_144kbps

Table 3.1.4-10 Physical channel parameters for DL reference measurement channel 144 kbps

Parameter	Unit	Level
Information bit rate	kbps	144
DPCH	ksps	240
Slot Format #i	–	14
TFCI	–	On
Power offsets PO1, PO2 and PO3	dB	0
Puncturing	%	2.7

Table 3.1.4-11 Transport channel parameters for DL reference measurement channel 144 kbps

Parameter	DTCH	DCCH
Transport Channel Number	1	2
Transport Block Size	2880	100
Transport Block Set Size	2880	100
Transmission Time Interval	20 ms	40 ms
Type of Error Protection	Turbo Coding	Convolution Coding
Coding Rate	1/3	1/3
Rate Matching attribute	256	256
Size of CRC	16	12
Position of TrCH in radio frame	fixed	fixed

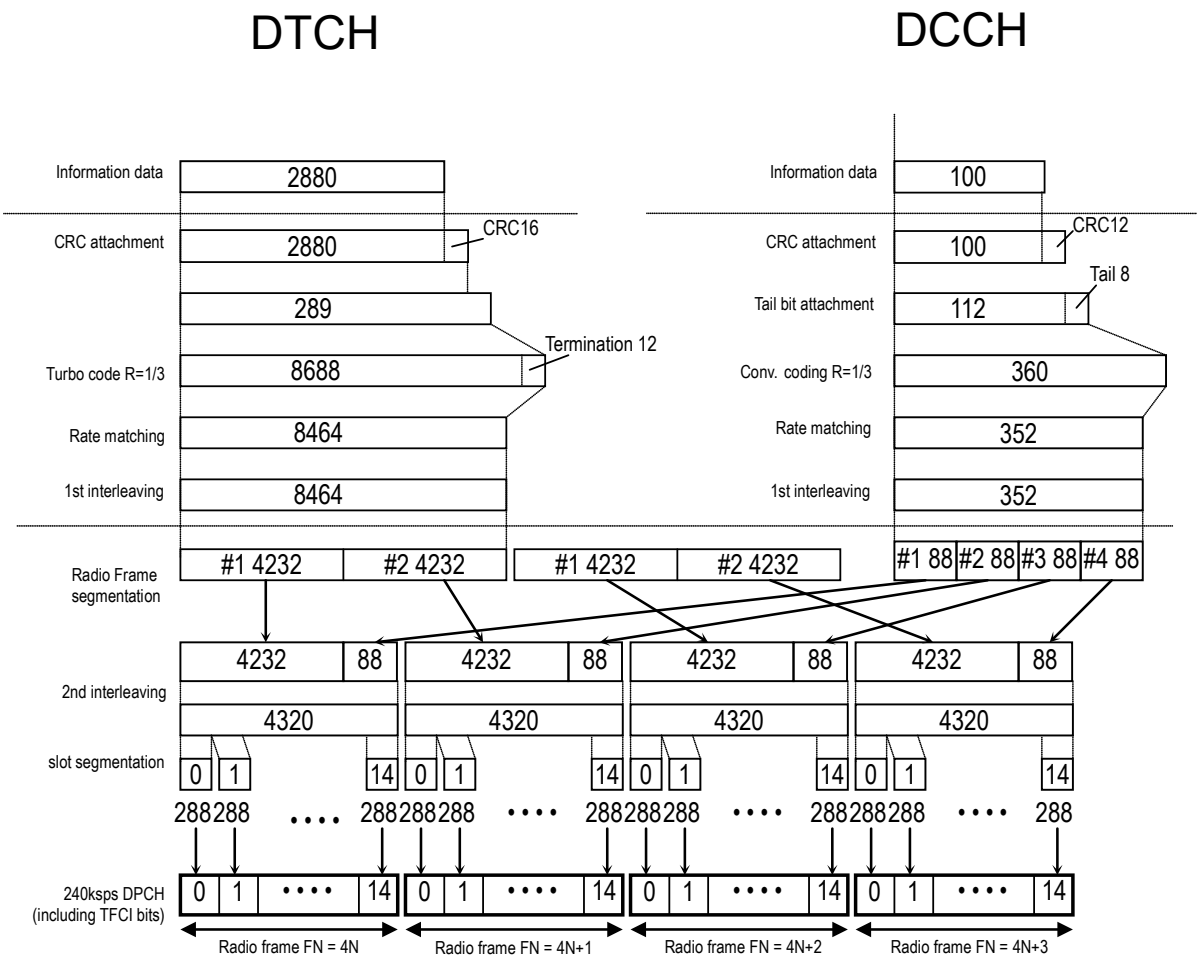


Figure 3.1.4-3 Channel coding for DL reference measurement channel 144 kbps

Channel coding parameters for DL_RMC_384kbps

Table 3.1.4-12 Physical channel parameters for DL reference measurement channel 384 kbps

Parameter	Unit	Level
Information bit rate	kbps	384
DPCH	ksps	480
Slot Format #i	–	15
TFCI	–	On
Power offsets PO1, PO2 and PO3	dB	0
Puncturing	%	22

Table 3.1.4-13 Transport channel parameters for DL reference measurement channel 384 kbps

Parameter	DTCH	DCCH
Transport Channel Number	1	2
Transport Block Size	3840	100
Transport Block Set Size	3840	100
Transmission Time Interval	10 ms	40 ms
Type of Error Protection	Turbo Coding	Convolution Coding
Coding Rate	1/3	1/3
Rate Matching attribute	256	256
Size of CRC	16	12
Position of TrCH in radio frame	fixed	fixed

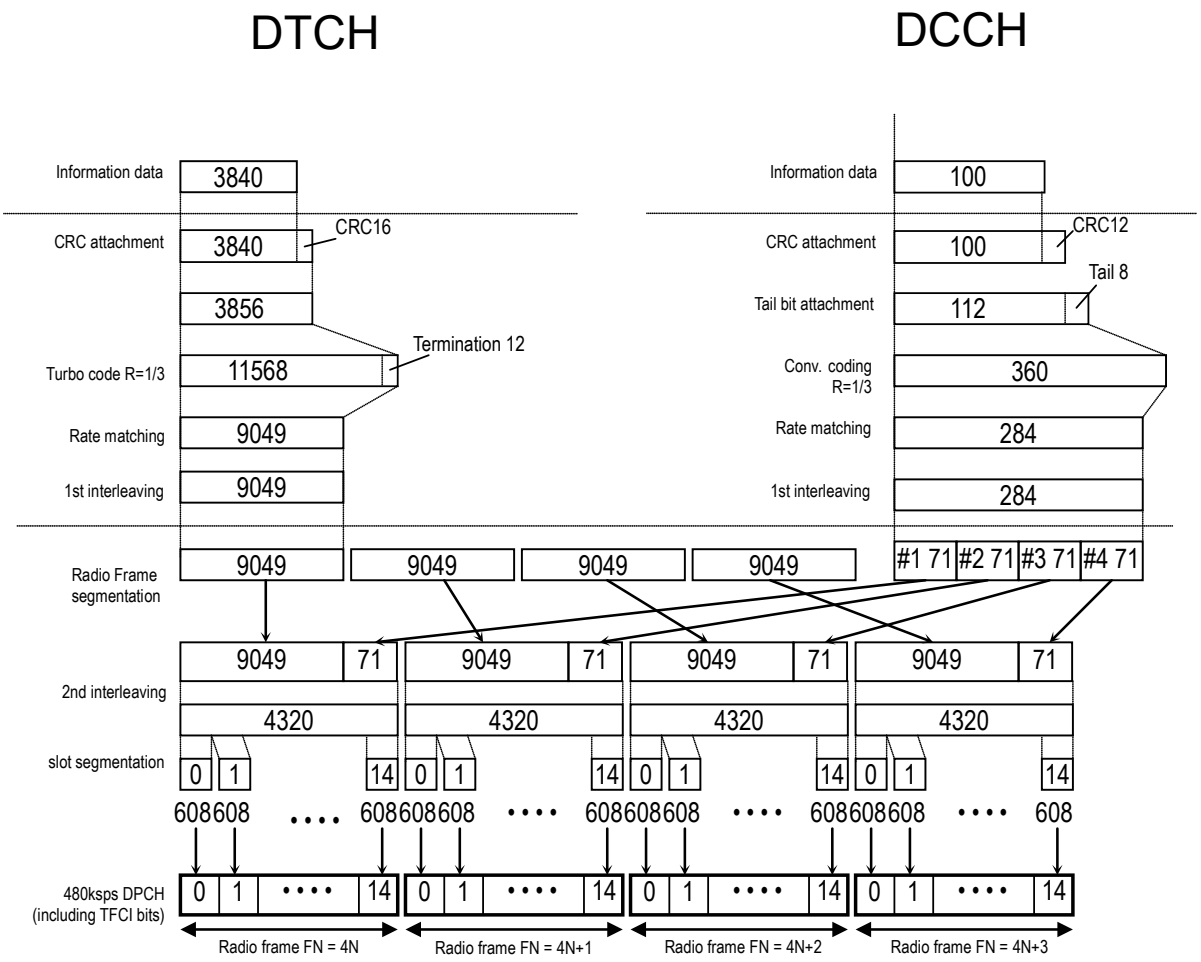


Figure 3.1.4-4 Channel coding for DL reference measurement channel 384 kbps

3.1.5 DL_AMR_TFCSx/DL_ISDN/DL_384kbps_Packet

These waveform patterns execute channel coding, division and spreading to physical channels, and power setting conforming to the Channel coding and multiplexing example (FDD, Downlink) standard described in 3GPP TS 25.944 Section 4.1.1.

Table 3.1.5-1 lists the parameters commonly used by each waveform pattern. When a waveform pattern is output, a marker signal shown in Table 3.1.5-1 is output from the AUX connector on the rear panel.

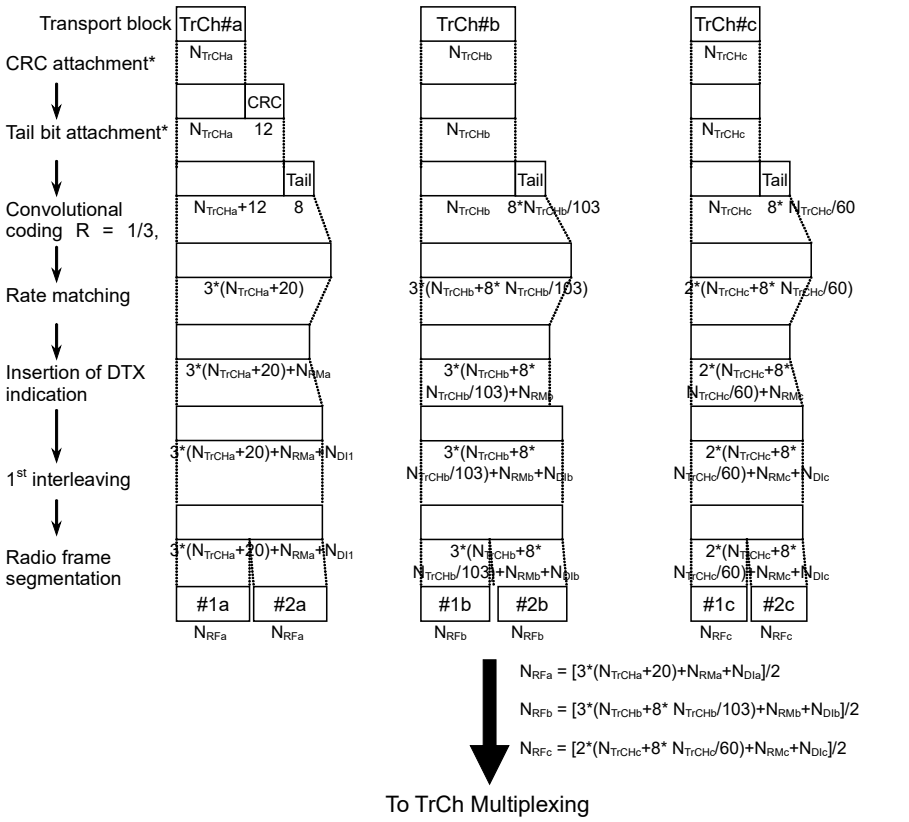
Table 3.1.5-1 List of common parameters

Parameter	Setting Value
Scrambling Code	80_H
DTCH Information Data	PN9
DCCH Information Data	All 0
Over sampling rate	4
Marker 1	TTI Clock
Marker 2	–
Marker 3	–

Channel coding parameters for DL_AMR_TFCSx

Table 3.1.5-2 Parameters for 12.2 kbps data

The number of TrChs		3
Transport Block Size	**TrCH#a**	0, 39 or 81 bits
	TrCH#b	103 bits
	TrCH#c	60 bits
TFCS	**#1**	N_{TrCHa} = 1*81, N_{TrCHb} = 1*103, N_{TrCHc} = 1*60 bits
	#2	N_{TrCHa} = 1*39, N_{TrCHb} = 0*103, N_{TrCHc} = 0*60 bits
	#3	N_{TrCHa} = 1*0, N_{TrCHb} = 0*103, N_{TrCHc} = 0*60 bits
Rate Matching attribute		RM_a = 200, RM_b = 190, RM_c = 235
CRC		12 bits (attached to TrCh#a only)
CRC parity bit attachment for 0 bit transport block		Applied to TrCh#a only.
Coding		CC, coding rate = 1/3 for TrCh#a, b coding rate = 1/2 for TrCh#c
TTI		20 ms

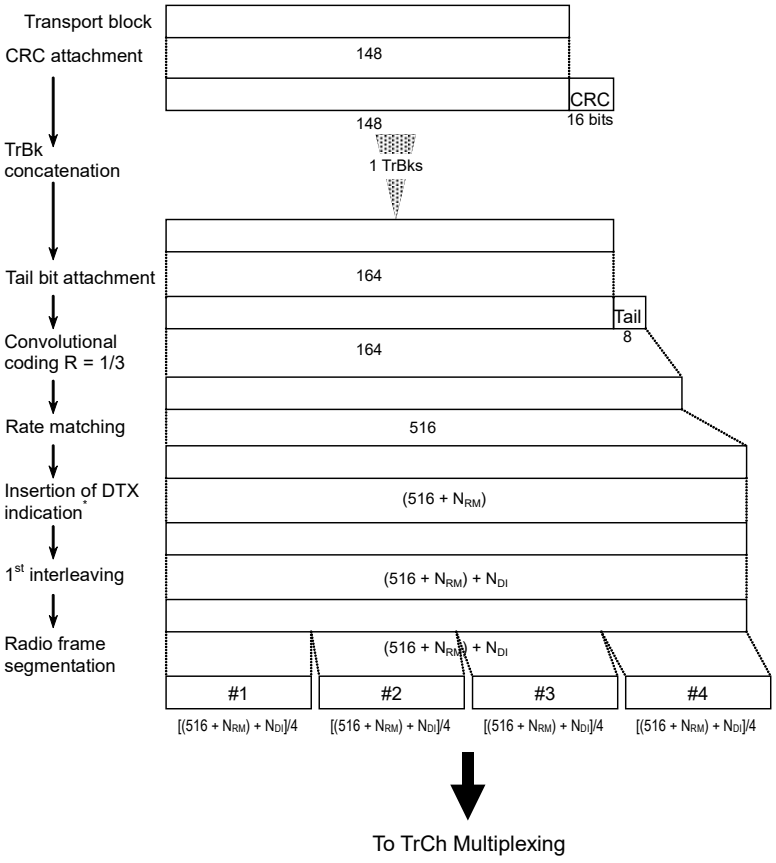


* CRC and tail bits for TrCH#a are attached even if N_{TrCha} = 0 bits since CRC parity bit attachment for 0 bit transport block is applied.

Figure 3.1.5-1 Channel coding and multiplexing for DL_AMR_TFCSx - 1

Table 3.1.5-3 Parameters for 3.4 kbps data

Parameter	Setting Value
Transport Block Size	148 bits
Transport Block Set Size	148 bits
Rate Matching attribute	160
CRC	16 bits
Coding	CC, coding rate = 1/3
TTI	40 ms



*: Insertion of DTX indication is used only if the position of the TrCHs in the radio frame is fixed.

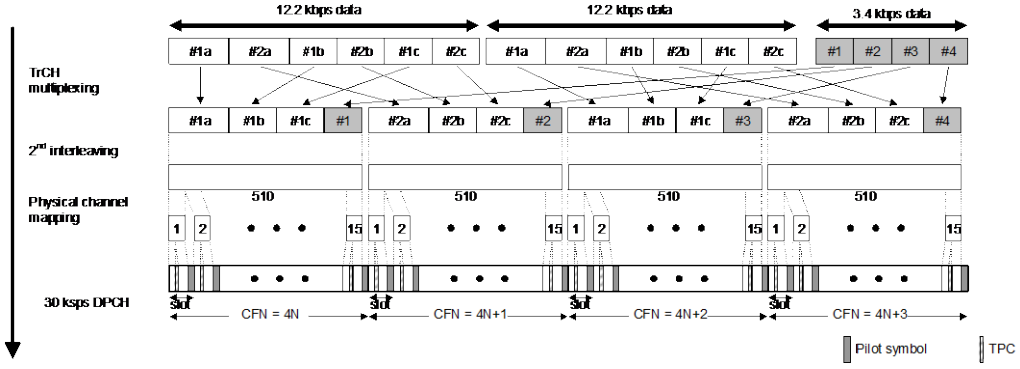


Figure 3.1.5-2 Channel coding and multiplexing for DL_AMR_TFCSx - 2

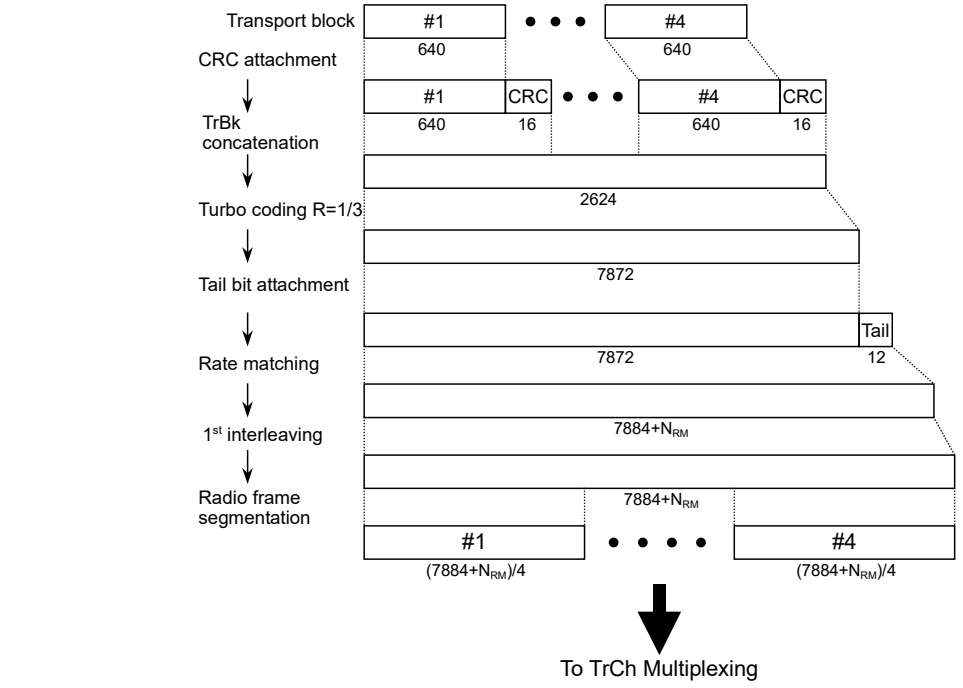
Table 3.1.5-4 Physical channel parameters for 12.2 kbps and 3.4 kbps data

Symbol Rate (ksps)	N_{pilot} (bits)	N_{TFCI} (bits)	N_{TPC} (bits)	N_{data1} (bits)	N_{data2} (bits)
30	4	0	2	6	28

Channel coding parameters for DL_ISDN

Table 3.1.5-5 Parameters for 64 kbps data

Parameter	Setting Value
Number of TrChs	1
Transport Block Size	640 bits
Transport Block Set Size	4*640 bits
Rate Matching attribute	170
CRC	16 bits
Coding	Turbo coding, coding rate = 1/3
TTI	40 ms



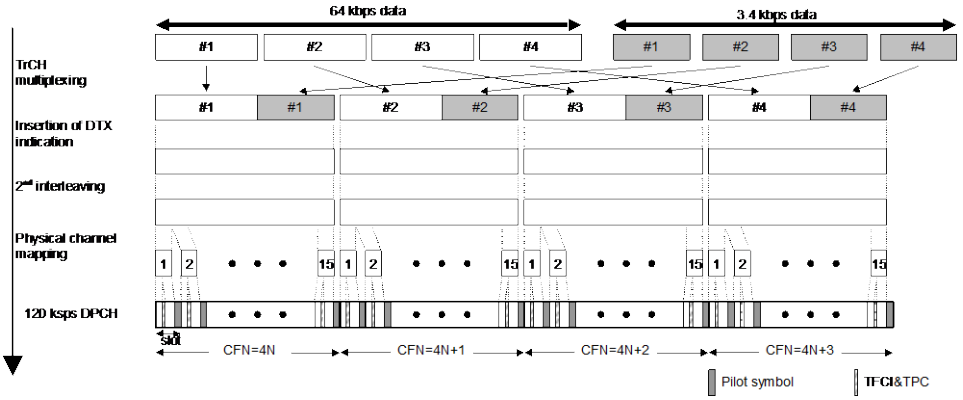


Figure 3.1.5-3 Channel coding and multiplexing for DL_ISDN

Table 3.1.5-6 Physical channel parameters for 64 kbps and 3.4 kbps data

Symbol Rate (ksps)	No. of Physical Channel	N_{pilot} (bits)	N_{TFCI} (bits)	N_{TPC} (bits)	N_{data1} (bits)	N_{data2} (bits)
120	1	8	8	4	28	112

Channel coding parameters for DL_384kbps_Packet

Table 3.1.5-7 Packet data parameters for 384 kbps data

Parameter	Setting Value
Number of TrChs	1
Transport Block Size	336 bits
Transport Block Set Size	336*B bits (B = 12)
Rate Matching attribute	145
CRC	16 bits
Coding	Turbo coding, coding rate = 1/3
TTI	10 ms

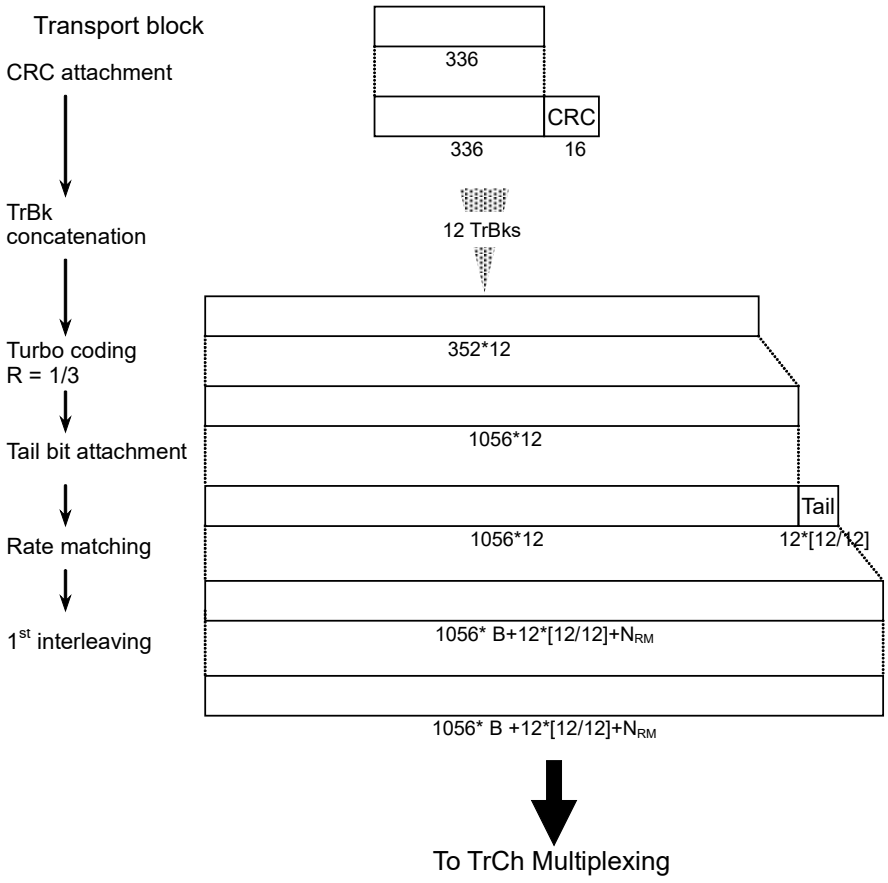


Figure 3.1.5-4 Channel coding and multiplexing for DL_384 kbps_Packet - 1

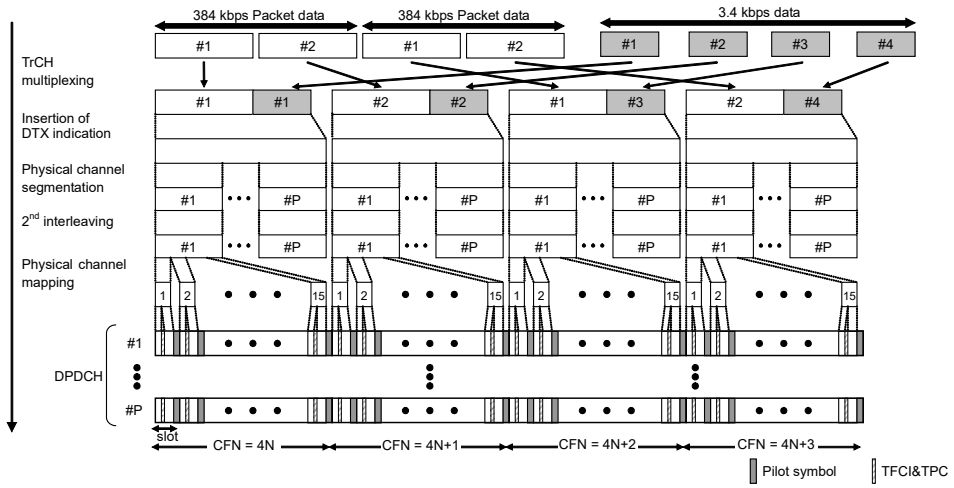


Figure 3.1.5-5 Channel coding and multiplexing for DL_384 kbps_Packet - 2

Table 3.1.5-8 Physical channel parameters for 384 kbps and 3.4 kbps data

Data Rate (kbps)	Symbol Rate (ksps)	No. of Physical Channel: P	N_{pilot} (bits)	N_{TFCI} (bits)	N_{TPC} (bits)	N_{data1} (bits)	N_{data2} (bits)
384	480	1	16	8	8	120	488

3.1.6 DL_Interferer

DL_Interferer is a modulated signal code-multiplexed according to the parameters described in 3GPP TS25.104 Annex C.4 W-CDMA Modulated Interferer.

Table 3.1.6-1 Parameters for DL_Interferer

Parameter	Setting Value
Scrambling Code	0_H
Over sampling rate	3

Table 3.1.6-2 Physical channel parameters for DL_Interferer

Channel Type	Spreading Factor	Channelization Code	Timing Offset ($x256T_{chip}$)	Power	Note
P-CCPCH	256	1	0	P-CCPCH_Ec/Ior = –10 dB	–
SCH	256	–	0	SCH_Ec/Ior = –10 dB	The SCH power is equally divided and distributed into 2 channels of P-SCH and S-SCH.
P-CPICH	256	0	0	P-CPICH_Ec/Ior = –10 dB	–
PICH	256	16	16	PICH_Ec/Ior = –15 dB	–
OCNS	See Table 3.1.6-3.				The total power of the OCNS channel and all the channels above is 0 dB.

Table 3.1.6-3 Parameters for OCNS

Channelization Code at SF = 128	Relative Level Setting (dB)	DPCH Data
2	–1	The DPCH data for each channelization code shall be in a bit sequence such that the data is uncorrelated with each other.
11	–3	
17	–3	
23	–5	
31	–2	
38	–4	
47	–8	
55	–7	
62	–4	
69	–6	
78	–5	
85	–9	
94	–10	
125	–8	
113	–6	
119	0	

3.1.7 TestModel_x_xxDPCH

TestModel_x_xxDPCH is a downlink multiplexed signal that is code-multiplexed according to the parameters described in 3GPP TS25.141 Section 11.4.0 Test Models.

Table 3.1.7-1 List of common parameters

Parameter	Setting Value
Scrambling Code*	0_H
Over sampling rate	4

*: For the offset frequency (5*N[MHz]) of the multicarrier when the lowest frequency carrier is 0, the Scrambling Code of each carrier is N. Time offset for each carrier frame is N/5, 2*N/5, 3*N/5, … when setting the carrier of N = 0 as the reference.

Test Model 1

Table 3.1.7-2 Channel configuration of Test Model 1

Type	Number of Channels	Fraction of Power (%)	Level Setting (dB)	Channelization Code	Timing Offset (x256T_{chip})
P-CCPCH+SCH	1	10	–10	1	0
Primary CPICH	1	10	–10	0	0
PICH	1	1.6	–18	16	120
S-CCPCH containing PCH (SF = 256)	1	1.6	–18	3	0
DPCH (SF = 128)	4/8/16/32/64	76.8 in total	See Table 3.1.7-3.		

The multicarriers (Test_Model_1_64DPCHx2/3/4) of Test Model 1 are assigned to the offset frequency as follows:

Test_Model_1_64DPCHx2 (2 carriers): –2.5 MHz, +2.5 MHz
Test_Model_1_64x2_10M (2 carriers): –5 MHz, +5 MHz
Test_Model_1_64x2_15M (2 carriers): –7.5 MHz, +7.5 MHz
Test_Model_1_64DPCHx3 (3 carriers): 0 MHz, +10 MHz, +15 MHz (+5 MHz carrier is blank.)
Test_Model_1_64DPCHx4 (4 carriers): –7.5 MHz, –2.5 MHz, +2.5 MHz, +7.5 MHz

Table 3.1.7-3 Parameters for DPCH

Code	Timing Offset (x256Tchip)	Level settings (dB) (4 codes)	Level settings (dB) (8 codes)	Level Settings (dB) (16 codes)	Level Settings (dB) (32 codes)	Level Settings (dB) (64 codes)
2	86	–5	–7	–10	–13	–16
11	134	-	–16	–12	–13	–16
17	52	-	-	–12	–14	–16
23	45	-	-	–14	–15	–17
31	143	-	-	–11	–17	–18
38	112	–7	–11	–13	–14	–20
47	59	-	-	–17	–16	–16
55	23	-	–11	–16	–18	–17
62	1	-	-	–13	–16	–16
69	88	-	-	–15	–19	–19
78	30	–9	–10	–14	–17	–22
85	18	-	–12	–18	–15	–20
94	30	-	-	–19	–17	–16
102	61	-	-	–17	–22	–17
113	128	-	–8	–15	–20	–19
119	143	–9	–12	–9	–24	–21
7	83	-	-	–	–20	–19
13	25	-	-	–	–18	–21
20	103	-	-	–	–14	–18
27	97	-	-	–	–14	–20
35	56	-	-	–	–16	–24
41	104	-	-	–	–19	–24
51	51	-	-	–	–18	–22
58	26	-	-	–	–17	–21
64	137	-	-	–	–22	–18
74	65	-	-	–	–19	–20
82	37	-	-	–	–19	–17
88	125	-	-	–	–16	–18
97	149	-	-	–	–18	–19
108	123	-	-	–	–15	–23
117	83	-	-	–	–17	–22
125	5	-	-	–	–12	–21
4	91	-	-	–	–	–17
9	7	-	-	–	–	–18
12	32	-	-	–	–	–20

Table 3.1.7-3 Parameters for DPCH (Cont'd)

Code	Timing Offset (x256Tchip)	Level settings (dB) (4 codes)	Level settings (dB) (8 codes)	Level Settings (dB) (16 codes)	Level Settings (dB) (32 codes)	Level Settings (dB) (64 codes)
14	21	-	-	–	–	–17
19	29	-	-	–	–	–19
22	59	-	-	–	–	–21
26	22	-	-	–	–	–19
28	138	-	-	–	–	–23
34	31	-	-	–	–	–22
36	17	-	-	–	–	–19
40	9	-	-	–	–	–24
44	69	-	-	–	–	–23
49	49	-	-	–	–	–22
53	20	-	-	–	–	–19
56	57	-	-	–	–	–22
61	121	-	-	–	–	–21
63	127	-	-	–	–	–18
66	114	-	-	–	–	–19
71	100	-	-	–	–	–22
76	76	-	-	–	–	–21
80	141	-	-	–	–	–19
84	82	-	-	–	–	–21
87	64	-	-	–	–	–19
91	149	-	-	–	–	–21
95	87	-	-	–	–	–20
99	98	-	-	–	–	–25
105	46	-	-	–	–	–25
110	37	-	-	–	–	–25
116	87	-	-	–	–	–24
118	149	-	-	–	–	–22
122	85	-	-	–	–	–20
126	69	-	-	–	–	–15

Test Model 2

Table 3.1.7-4 Channel configuration of Test Model 2

Type	Number of Channels	Fraction of Power (%)	Level Setting (dB)	Channelization Code	Timing Offset ($x256T_{chip}$)
P-CCPCH+SCH	1	10	–10	1	0
Primary CPICH	1	10	–10	0	0
PICH	1	5	–13	16	120
S-CCPCH containing PCH (SF = 256)	1	5	–13	3	0
DPCH (SF = 128)	3	2 × 10, 1 × 50	2 × –10, 1 × –3	24, 72, 120	1, 7, 2

Test Model 3

Table 3.1.7-5 Channel configuration of Test Model 3

Type	Number of Channels	Fraction of Power (%) 4/8/16/32	Level Setting (dB) 4/8/16/32	Channelization Code	Timing Offset ($x256T_{chip}$)
P-CCPCH+SCH	1	15.8/15.8 /12.6/7.9	–8/–8/ –9/–11	1	0
Primary CPICH	1	15.8/15.8 /12.6/7.9	–8/–8/ –9/–11	0	0
PICH	1	2.5/2.5/5/1.6	–16/–16/ –13/–18	16	120
S-CCPCH containing PCH (SF = 256)	1	2.5/2.5/5/1.6	–16/–16/ –13/–18	3	0
DPCH (SF = 256)	4/8/16/32	63.4/63.4 /63.7/80.4 in total	See Table 3.1.7-6.		

Table 3.1.7-6 Parameters for Test Model 3

Code	T_{offset}	Level settings (dB) (4 codes)	Level settings (dB) (8 codes)	Level Settings (dB) (16 codes)	Level Settings (dB) (32 codes)
64	86	–8	–11	–14	–16
69	134	-	-	–14	–16
74	52	-	–11	–14	–16
78	45	-	-	–14	–16
83	143	-	-	–14	–16
89	112	–8	–11	–14	–16
93	59	-	-	–14	–16
96	23	-	–11	–14	–16
100	1	-	-	–14	–16
105	88	-	-	–14	–16
109	30	–8	–11	–14	–16
111	18	-	–11	–14	–16
115	30	-	-	–14	–16
118	61	-	-	–14	–16
122	128	-	–11	–14	–16
125	143	–8	–11	–14	–16
67	83	-	-	–	–16
71	25	-	-	–	–16
76	103	-	-	–	–16
81	97	-	-	–	–16
86	56	-	-	–	–16
90	104	-	-	–	–16
95	51	-	-	–	–16
98	26	-	-	–	–16
103	137	-	-	–	–16
108	65	-	-	–	–16
110	37	-	-	–	–16
112	125	-	-	–	–16
117	149	-	-	–	–16
119	123	-	-	–	–16
123	83	-	-	–	–16
126	5	-	-	–	–16

Test Model 4

Table 3.1.7-7 Channel configuration of Test Model 4

Type	Number of Channels	Fraction of Power (%)	Level Setting (dB)	Channelization Code	Timing Offset
P-CCPCH+SCH when Primary CPICH is disabled	1	100	0	1	0
P-CCPCH+SCH when Primary CPICH is enabled	1	50	–3	1	0
Primary CPICH1	1	50	–3	0	0

3.1.8 TestModel_5_xDPCH

These waveforms are downlink multiplexed signals that include HS-SCCH and HS-PDSCH equivalent to Test Model 5, which is described in 3GPP TS25.141 Section 6.1.

The settings are the same as that shown in Section 3.1.9.
Refer to 3.1.9 "TestModel_5_xHSPDSCH" for details.

3.1.9 TestModel_5_xHSPDSCH

These waveforms are downlink multiplexed signals that include HS-SCCH and HS-PDSCH equivalent to Test Model 5, which is described in 3GPP TS25.141 Section 6.1.

Table 3.1.9-1 List of common parameters

Parameter	Setting Value
Scrambling Code	0_H
Over sampling rate	4

Table 3.1.9-2 Channel configuration of Test Model 5

Type	Number of Channels	Level Setting (dB)	Channelization Code	Timing Offset ($x256T_{chip}$)
P-CCPCH+SCH	1	–11	1	0
Primary CPICH	1	–11	0	0
PICH	1	–19	16	120
S-CCPCH containing PCH (SF = 256)	1	–19	3	0
DPCH (SF = 128)	30/14/6/4*	See Table 3.1.9-3.		
HS-SCCH	2	See Table 3.1.9-4.		
HS-PDSCH (16QAM)	8/4/2*	See Table 3.1.9-5.		

*: DPCH is 6 channels when HS-PDSCH is 2 channels,
4 channels or 14 channels when HS-PDSCH is 4 channels, and
30 channels when HS-PDSCH is 8 channels.

Table 3.1.9-3 Setting for DPCH

Code (SF = 128)	Timing Offset (x256Tchip)	Level Settings (dB) (30 codes)	Level Settings (dB) (14 codes)	Level Settings (dB) (6 codes)	Level settings (dB) (4 codes)
15	86	–20	–17	–17	–15
23	134	–20	–19	–15	–15
68	52	–21	–19	–15	–18
76	45	–22	–20	–18	–12
82	143	–24	–18	–16	-
90	112	–21	–20	–17	-
5	59	–23	–25	–	-
11	23	–25	–23	–	-
17	1	–23	–20	–	-
27	88	–26	–22	–	-
64	30	–24	–21	–	-
72	18	–22	–22	–	-
86	30	–24	–19	–	-
94	61	–28	–20	–	-
3	128	–27	–	–	-
7	143	–26	–	–	-
13	83	–27	–	–	-
19	25	–25	–	–	-
21	103	–21	–	–	-
25	97	–21	–	–	-
31	56	–23	–	–	-
66	104	–26	–	–	-
70	51	–25	–	–	-
74	26	–24	–	–	-
78	137	–27	–	–	-
80	65	–26	–	–	-
84	37	–23	–	–	-
88	125	–25	–	–	-
89	149	–22	–	–	-
92	123	–24	–	–	-

Table 3.1.9-4 Settings for HS-SCCH

Code (SF = 128)	Timing Offset (x256Tchip)	Level Settings (dB)
9	0	–15
29	0	–21

Table 3.1.9-5 Setting for HS-PDSCH

Code (SF = 16)	Timing Offset (x256Tchip)	Level Settings (dB) (8 codes)	Level Settings (dB) (4 codes)	Level Settings (dB) (2 codes)
4	0	–11	–8	–5
5	0	–11	–8	–
6	0	–11	–	–
7	0	–11	–	–
12	0	–11	–8	–5
13	0	–11	–8	–
14	0	–11	–	–
15	0	–11	–	–

3.1.10 TestModel_6_xHSPDSCH

These waveforms are downlink multiplexed signals that include HS-SCCH and HS-PDSCH equivalent to Test Model 6, which is described in 3GPP TS25.141 Section 6.1.

Table 3.1.10-1 List of common parameters

Parameter	Setting Value
Scrambling Code	0_H
Over sampling rate	4

Table 3.1.10-2 Channel configuration of Test Model 6

Type	Number of Channels	Level Setting (dB)	Channelization Code	Timing Offset ($x256T_{chip}$)
P-CCPCH+SCH	1	–11	1	0
Primary CPICH	1	–11	0	0
PICH	1	–19	16	120
S-CCPCH containing PCH (SF = 256)	1	–19	3	0
DPCH (SF = 128)	30/4*	See Table 3.1.10-3.		
HS-SCCH	2	See Table 3.1.10-4.		
HS-PDSCH (64QAM)	8/4*	See Table 3.1.10-5.		

*: DPCH is 4 channels when HS-PDSCH is 4 channels, and 30 channels when HS-PDSCH is 8 channels.

Table 3.1.10-3 Setting for DPCH

Code (SF = 128)	Timing Offset (x256Tchip)	Level Settings (dB) (30 codes)	Level settings (dB) (4 codes)
15	86	–17	–13
23	134	–17	–15
68	52	–18	–9
76	45	–19	–12
82	143	–21	–
90	112	–18	–
5	59	–20	–
11	23	–22	–
17	1	–20	–
27	88	–23	–
64	30	–21	–
72	18	–19	–
86	30	–21	–
94	61	–25	–
3	128	–24	–
7	143	–23	–
13	83	–24	–
19	25	–22	–
21	103	–18	–
25	97	–18	–
31	56	–20	–
66	104	–23	–
70	51	–22	–
74	26	–21	–
78	137	–24	–
80	65	–23	–
84	37	–22	–
88	125	–22	–
89	149	–22	–
92	123	–21	–

Table 3.1.10-4 Settings for HS-SCCH

Code (SF = 128)	Timing Offset (x256Tchip)	Level Settings (dB)
9	0	–15
29	0	–21

Table 3.1.10-5 Setting for HS-PDSCH

Code (SF = 16)	Timing Offset (x256Tchip)	Level Settings (dB) (8 codes)	Level settings (dB) (4 codes)
4	0	–12	–9
5	0	–12	–9
6	0	–12	–
7	0	–12	–
12	0	–12	–9
13	0	–12	–9
14	0	–12	–
15	0	–12	–

3.2 GSM Waveform Pattern

Table 3.2-1 lists the waveform patterns for uplink/downlink, provided as the GSM waveform pattern.

Table 3.2-1 List of GSM waveform patterns

Waveform Pattern Name	Uplink/Downlink	Data	Output Slot
GMSK_PN9	Uplink/Downlink	PN9*1	–
8PSK_PN9	Uplink/Downlink		–
GMSK_TN0	Uplink/Downlink	PN9*2	TN0
8PSK_TN0	Uplink/Downlink		TN0
NB_GMSK	Uplink/Downlink	PN9*3	TN0
NB_ALL_GMSK	Uplink/Downlink		All slots
NB_8PSK	Uplink/Downlink		TN0
NB_ALL_8PSK	Uplink/Downlink		All slots
TCH_FS	Uplink/Downlink	PN9*4	TN0
CS-1_1SLOT	Uplink/Downlink		TN0
CS-4_1SLOT	Uplink/Downlink		TN0
DL_MCS-1_1SLOT	Downlink		TN0
UL_MCS-1_1SLOT	Uplink		TN0
DL_MCS-5_1SLOT	Downlink		TN0
UL_MCS-5_1SLOT	Uplink		TN0
DL_MCS-9_1SLOT	Downlink		TN0
UL_MCS-9_1SLOT	Uplink		TN0
DL_MCS-9_4SLOT*5	Downlink		TN0, 1, 2, 3
UL_MCS-9_4SLOT*5	Uplink		TN0, 1, 2, 3

*1: PN9 data is inserted into all of the non-slot format fields.

*2: PN9 data is inserted into all of the fields in a slot except the guard.

*3: PN9 data is inserted into the encrypted bit fields of normal burst.

*4: A bit sequence generated by channel-coding the PN9 data is inserted to the encrypted bit fields of normal burst.

*5: For MS2830A or MS2840A: ARB Memory Upgrade 256 Msamples (option 027) must be installed to use this waveform pattern.

When a GSM waveform pattern is output, a marker signal shown in Table 3.2-2 is output from the AUX connector on the rear panel.

Table 3.2-2 Marker output data

Marker Signal	Output Data
Marker 1	Frame Clock
Marker 2	RF Gate
Marker 3	Multi-Frame Clock

3.2.1 Details of each pattern

GMSK_PN9, PSK_PN9

PN9 data which doesn't have slot format is inserted.

GMSK_TN0, 8PSK_TN0

PN9 data is inserted to all fields in a slot except the guard field. The PN9 data in each slot has continuity.

NB_GMSK, NB_ALL_GMSK, NB_8PSK, NB_ALL_8PSK

PN9 data is inserted to the encrypted bit fields of normal burst. The PN9 data in each slot has continuity.

TCH_FS

Supports Speech channel at full rate (TCH/FS) prescribed in 3GPP TS05.03 Section 3.1.

Table 3.2.1-1 Channel coding parameters

Type of Channel	Bits/Block Data + Parity + Tail1	Convolutional Code Rate	Coded Bits per Block	Interleaving Depth
TCH/FS			456	8
class I	182 + 3 + 4	1/2	378	
class II	78 + 0 + 0	–	78	

CS-1(4)_1SLOT

Supports Packet data block type 1 (CS-4), 4 (CS-1) of GPRS PDTCH prescribed in 3GPP TS05.03 Section 5.1.

Table 3.2.1-2 Channel coding parameters

Scheme	Code Rate	USF	Pre-coded USF	Radio Block except USF and BCS	BCS	Tail	Coded Bits	Punctured Bits
CS-1	1/2	3	3	181	40	4	456	0
CS-4	1	3	12	428	16	–	456	–

DL(UL)_MCS-1(5, 9)_1SLOT(_4SLOT)

Supports Packet data block type 5 (MCS-1), 9 (MCS-5), and 13 (MCS-9) of EGPRS PDTCH prescribed in 3GPP TS05.03 Section 5.1.

Table 3.2.1-3 Channel coding parameters

Scheme	Code Rate	Header Code Rate*	Modulation	RLC Blocks per Radio Block (20 ms)	Raw Data within One Radio Block	Family	BCS	Tail Payload	HCS	Data Rate kb/s
MCS-9	1.0	0.36	8PSK	2	2x592	A	2x12	2x6	8	59.2
MCS-5	0.37	1/3		1	448	B	12	6		22.4
MCS-1	0.53	0.53	GMSK	1	176	C				8.8

*: The Header data is all "0."

3.2.2 Frame configuration

Each frame is composed of eight slots. TCH/FS consist of 26 multiframes, and other channels consist of 52 multiframes.

3.2.3 Slot configuration

GMSK_TN0 and 8PSK_TN0 consist of the data field and guard field only as shown in the figures below:

PN 148	G 8.25

Unit: bit

PN: Data — PN9 pseudo random pattern (continuous between transmitted slots)

G: Guard bit — FF_H

Figure 3.2.3-1 Training burst (GMSK)

PN 444	G 24.75

Unit: bit

PN: Data — PN9 pseudo random pattern (continuous between transmitted slots)

G: Guard bit — FF_H

Figure 3.2.3-2 Training burst (8PSK)

The slot configuration for those other than GMSK_PN9, 8PSK_PN9, GMSK_TN0, and 8PSK_TN0 is normal burst as shown in the figure below:

T	E	S	TSC	S	E	T	G
3	57	1	26	1	57	3	8.25

Unit: bit

T: Tail bit 0_H (4 bits)
E: Encrypted bit Channel-coded* PN9 pseudo random pattern (continuous between transmitted slots)
S: Stealing bit Steal flag
TSC: Training sequence bit 097 0897_H
T: Tail bit 0_H (4 bits)
G: Guard bit FF_H

*: When the waveform pattern is NB_GMSK and NB_ALL_GMSK, PN9 data that has not been channel-coded is inserted directly.

Figure 3.2.3-3 Normal burst (GMSK)

T1	E	TSC	E	T2	G
9	174	78	174	9	24.75

Unit: bit

T1: Tail bit $1FF_H$ (9 bits)
E: Encrypted bit Channel-coded* PN9 pseudo random pattern (continuous between transmitted slots)
TSC: Training sequence bit 3F3F 9E29 FFF3 FF3F $9E49_H$
T2: Tail bit $1FF_H$ (9 bits)
G: Guard bit FF_H

*: When the waveform pattern is NB_8PSK and NB_ALL_8PSK, PN9 data that has not been channel-coded is inserted directly.

Figure 3.2.3-4 Normal burst (8PSK)

3.3 CDMA2000 1X Waveform Pattern

Table 3.3-1 lists the provided CDMA2000 1X waveform patterns.

Table 3.3-1 List of CDMA2000 1X waveform patterns

Waveform Pattern Name	Supported System	Frame Coding	Symbol Data
RVS_RC1_FCH	cdma2000 1xRTT RC1 Reverse	Available	FCH 9.6 kbps
RVS_RC2_FCH	cdma2000 1xRTT RC2 Reverse	Available	FCH 14.4 kbps
RVS_RC3_FCH	cdma2000 1xRTT RC3 Reverse	Available	PICH FCH 9.6 kbps
RVS_RC3_FCH_SCH	cdma2000 1xRTT RC3 Reverse	Available	PICH FCH 9.6 kbps SCH 9.6 kbps
RVS_RC3_DCCH	cdma2000 1xRTT RC3 Reverse	Available	PICH DCCH 9.6 kbps
RVS_RC4_FCH	cdma2000 1xRTT RC4 Reverse	Available	PICH FCH 14.4 kbps
FWD_RC1-2_9channel	cdma2000 1xRTT RC1, RC2 Forward	Only spreading available	PICH, SyncCH, PagingCH, FCH 19.2 ksps x 6
FWD_RC3-5_9channel	cdma2000 1xRTT RC3, RC4, RC5 Forward	Only spreading available	PICH, SyncCH, PagingCH, FCH 38.4 ksps x 6

When a CDMA2000 1X waveform pattern is output, a marker signal shown in Table 3.3-2 is output from the AUX connector on the rear panel.

Table 3.3-2 Marker output data

Marker Signal	Output Data
Marker 1	Frame Clock
Marker 2	RF Gate
Marker 3	Symbol Clock

3.3.1 1xRTT Reverse RC1 (RVS_RC1_FCH)

When the RVS_RC1_FCH waveform pattern is selected, a frame-coded R-FCH signal of 1xRTT Reverse RC1 is output. The frame coding and IQ modulation are performed conforming to 3GPP2 C.S0002-C-1. Table 3.3.1-1 lists the parameters of the output signal.

Table 3.3.1-1 R-FCH (Reverse Fundamental Channel)

	Data Rate	Data
R-FCH	9.6 kbps	PN9fix*

When this waveform pattern is selected, the output signal is frame-coded through the processing shown in the function block diagram in Figure 3.3.1-2. Frame coding is performed for four consecutive frames (outputting one frame takes about 20 ms), generating a 4-frame length signal pattern. The signal pattern obtained through frame coding is then repeatedly output. Since the length of three cycles of I Channel PN Sequence and Q Channel PN Sequence for short-code spreading is exactly 80 ms, which is equivalent to the length of four frames, the short code retains continuity while the signal is output. Therefore, the signal that is output when this waveform pattern is selected can be used for modulation accuracy measurement, as well as frame error rate measurement using CRC. Note that long-code spreading is not executed.

Figure 3.3.1-1 shows the bit sequence assignment before convolutional coding.

Figure 3.3.1-1 Frame configuration of RVS_RC1_FCH waveform pattern

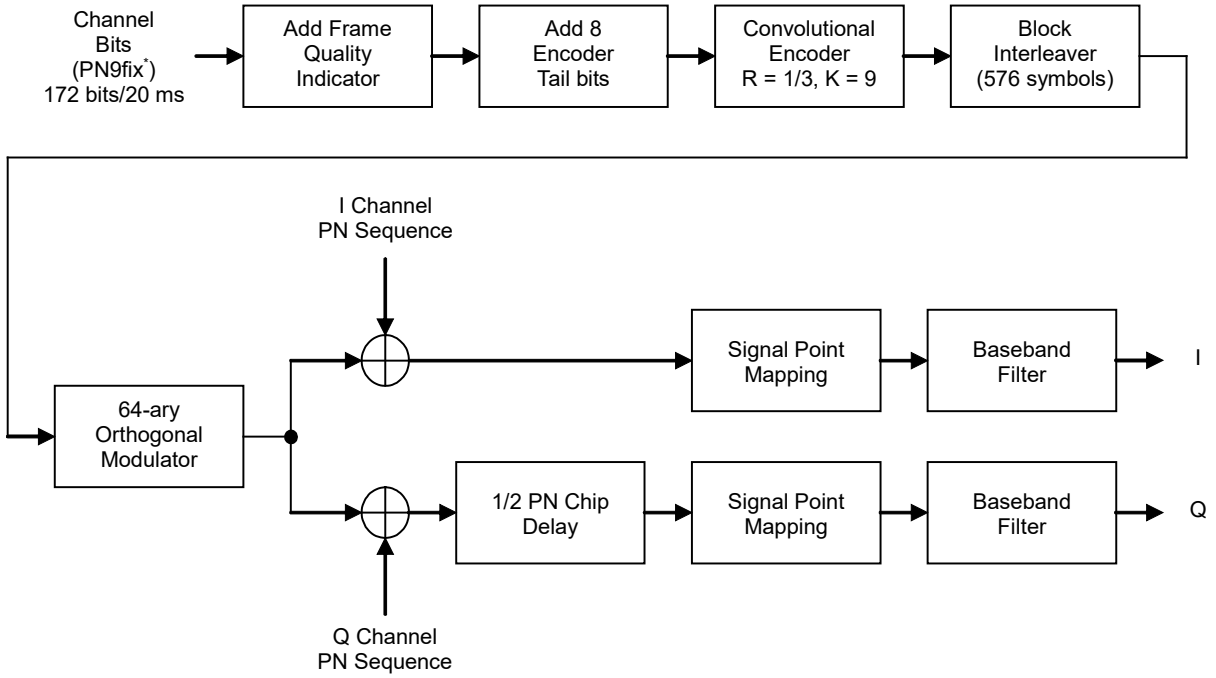


Figure 3.3.1-2 Signal generation block diagram for RVS_RC1_FCH waveform pattern

*: Since the PN9 generator is initialized every four frames, the same 4-frame length data is repeatedly output. For this reason, continuity of PN9fix is retained within a set of four consecutive frames, but lost with the adjacent sets of four consecutive frames. See Figure 3.3.1-3 for details.

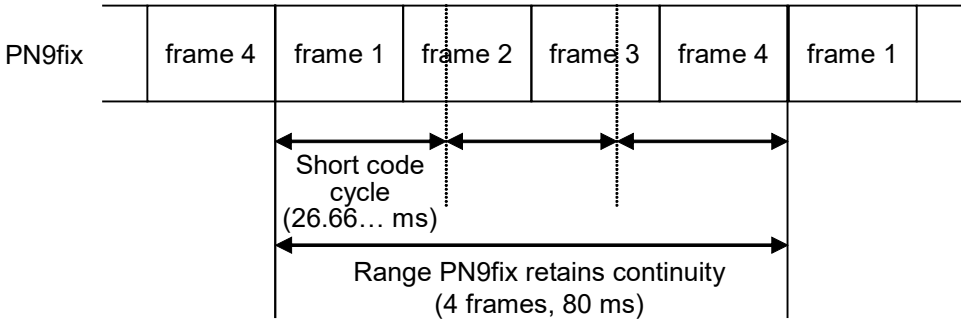


Figure 3.3.1-3 PN9fix data and short code

3.3.2 1xRTT Reverse RC2 (RVS_RC2_FCH)

When the RVS_RC2_FCH waveform pattern is selected, a frame-coded R-FCH signal of 1xRTT Reverse RC2 is output. The frame coding and IQ modulation are performed conforming to 3GPP2 C.S0002-C-1. Table 3.3.2-1 lists the parameters of the output signal.

Table 3.3.2-1 R-FCH (Reverse Fundamental Channel)

	Data Rate	Data
R-FCH	14.4 kbps	PN9fix*

When this waveform pattern is selected, the output signal is frame-coded through the processing shown in the function block diagram in Figure 3.3.2-2. Frame coding is performed for four consecutive frames (outputting one frame takes about 20 ms), generating a 4-frame length signal pattern. The signal pattern obtained through frame coding is then repeatedly output. Since the length of three cycles of I Channel PN Sequence and Q Channel PN Sequence for short-code spreading is exactly 80 ms, which is equivalent to the length of four frames, the short code retains continuity while the signal is output. Therefore, the signal that is output when this waveform pattern is selected can be used for modulation accuracy measurement, as well as frame error rate measurement using CRC. Note that long-code spreading is not executed.

Figure 3.3.2-1 shows the bit sequence assignment before convolutional coding.

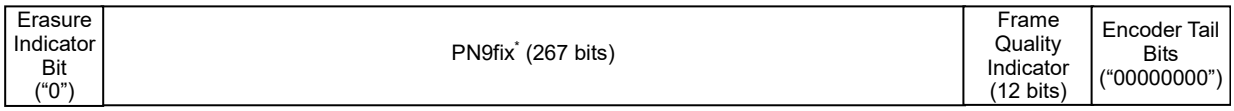


Figure 3.3.2-1 Frame configuration of RVS_RC2_FCH waveform pattern

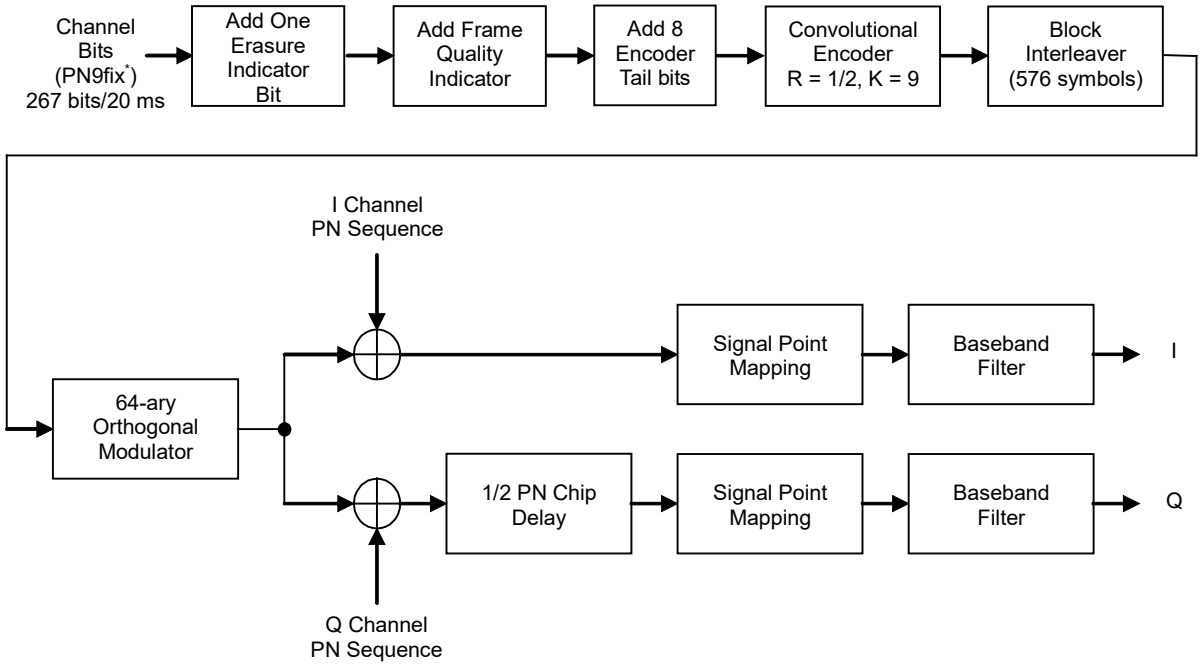


Figure 3.3.2-2 Signal generation block diagram for RVS_RC2_FCH waveform pattern

*: Since the PN9 generator is initialized every four frames, the same 4-frame length data is repeatedly output. For this reason, continuity of PN9fix is retained within a set of four consecutive frames, but lost with the adjacent sets of four consecutive frames. See Figure 3.3.1-3 “PN9fix data and short code” in Section 3.3.1 for details.

3.3.3 1xRTT Reverse RC3(1) (RVS_RC3_FCH)

When the RVS_RC3_FCH waveform pattern is selected, a frame-coded multiplexed signal of 1xRTT Reverse RC3 is output. The frame coding and IQ modulation are performed conforming to 3GPP2 C.S0002-C-1. The channels to be multiplexed are R-PICH and R-FCH. Table 3.3.3-1 lists the parameters of the multiplexed channels.

Table 3.3.3-1 R-PICH (Reverse Pilot Channel) and R-FCH (Reverse Fundamental Channel)

	Walsh Code	Code Power	Data Rate	Data
R-PICH	0	–5.278 dB	N/A	All 0
R-FCH	4	–1.528 dB	9.6 kbps	PN9fix*

When this waveform pattern is selected, the output signal is frame-coded through the processing shown in the function block diagrams in Figs. 3.3.3-2 and 3.3.3-3. Frame coding is performed for four consecutive frames (outputting one frame takes about 20 ms), generating a 4-frame length signal pattern. The signal pattern obtained through frame coding is then repeatedly output. Since the length of three cycles of I Channel PN Sequence and Q Channel PN Sequence for short-code spreading is equivalent to the length of four frames, the short code retains continuity while the signal is output. Therefore, the signal that is output when this waveform pattern is selected can be used for modulation accuracy measurement, as well as frame error rate measurement using CRC. Note that long-code spreading is not executed.

Figure 3.3.3-1 shows the bit sequence assignment before convolutional coding.

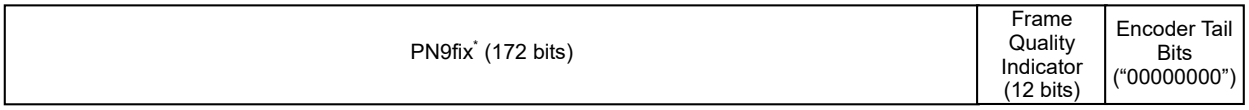


Figure 3.3.3-1 Frame configuration of traffic channel of RVS_RC3_FCH waveform pattern

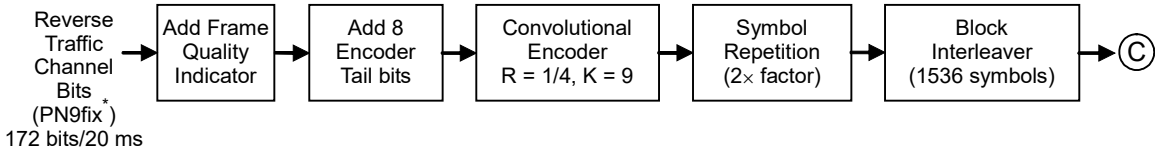
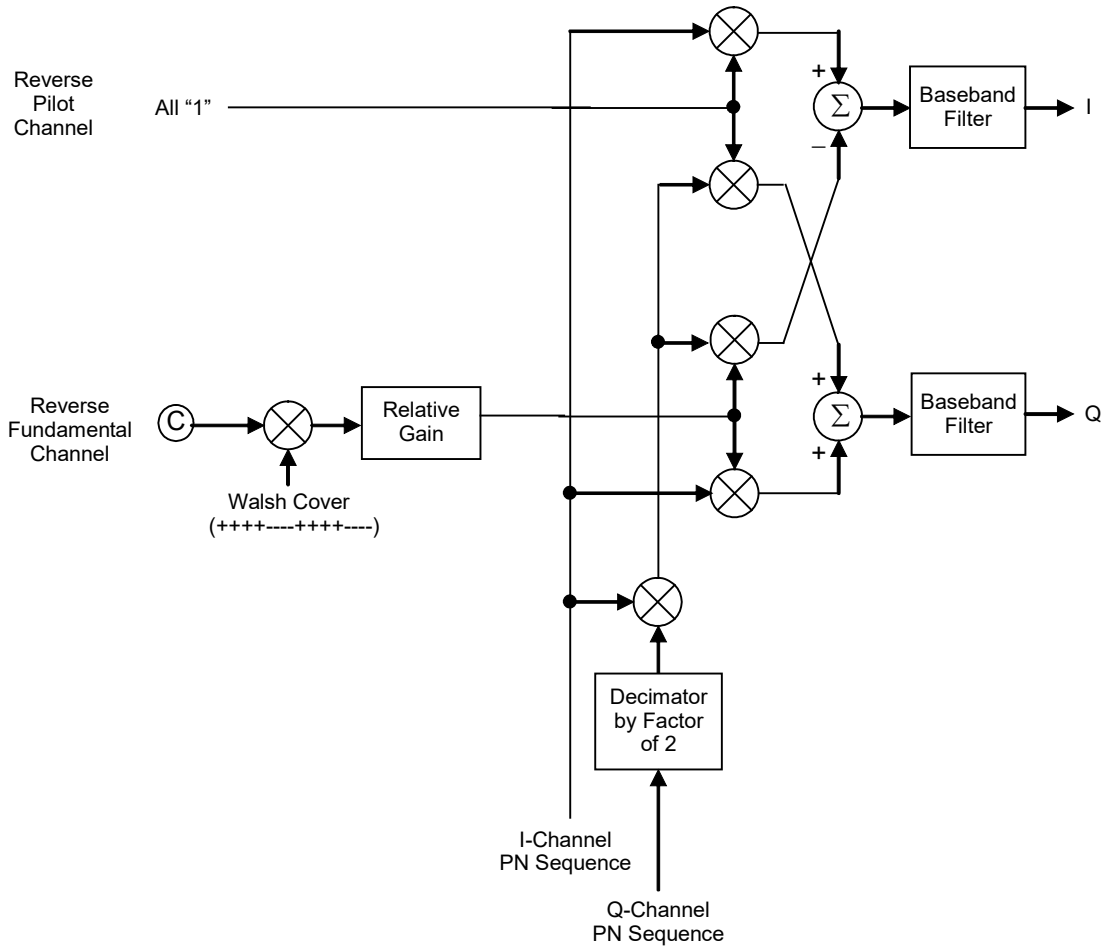


Figure 3.3.3-2 Signal generation block diagram for RVS_RC3_FCH waveform pattern (1 of 2)



Note:

Binary signals "0" and "1" are respectively substituted for 1 and –1.

Figure 3.3.3-3 Signal generation block diagram for RVS_RC3_FCH waveform pattern (2 of 2)

*: Since the PN9 generator is initialized every four frames, the same 4-frame length data is repeatedly output. For this reason, continuity of PN9fix is retained within a set of four consecutive frames, but lost with the adjacent sets of four consecutive frames. See Figure 3.3.1-3 "PN9fix data and short code" in Section 3.3.1 for details.

3.3.4 1xRTT Reverse RC3(2) (RVS_RC3_FCH_SCH)

When the RVS_RC3_FCH_SCH waveform pattern is selected, a frame-coded multiplexed signal of 1xRTT Reverse RC3 is output. The frame coding and IQ modulation are performed conforming to 3GPP2 C.S0002-C-1. The channels to be multiplexed are R-PICH, R-FCH, and R-SCH. Table 3.3.4-1 lists the parameters of the multiplexed channels.

Table 3.3.4-1 R-PICH (Reverse Pilot Channel), R-FCH (Reverse Fundamental Channel), and R-SCH (Reverse Supplemental Channel)

	Walsh Code	Code Power	Data Rate	Data
R-PICH	0	–7.5912 dB	N/A	All 0
R-FCH	4	–3.8412 dB	9.6 kbps	PN9fix*
R-SCH	2	–3.8412 dB	9.6 kbps	PN9fix*

When this waveform pattern is selected, the output signal is frame-coded through the processing shown in the function block diagrams in Figs. 3.3.4-2 and 3.3.4-3. Frame coding is performed for four consecutive frames (outputting one frame takes about 20 ms), generating a 4-frame length signal pattern. The signal pattern obtained through frame coding is then repeatedly output. Since the length of three cycles of I Channel PN Sequence and Q Channel PN Sequence for short-code spreading is equivalent to the length of four frames, the short code retains continuity while the signal is output. Therefore, the signal that is output when this waveform pattern is selected can be used for modulation accuracy measurement, as well as frame error rate measurement using CRC. Note that long-code spreading is not executed.

Figure 3.3.4-1 shows the bit sequence assignment before convolutional coding.

Figure 3.3.4-1 Frame configuration of traffic channel of RVS_RC3_FCH_SCH waveform pattern

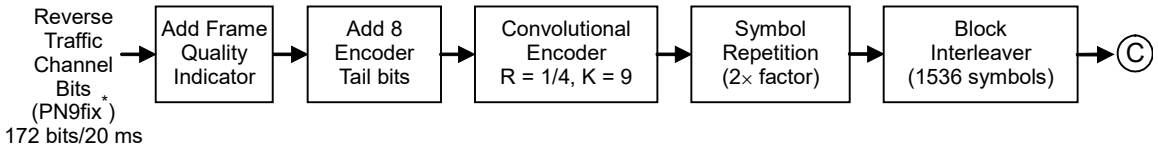
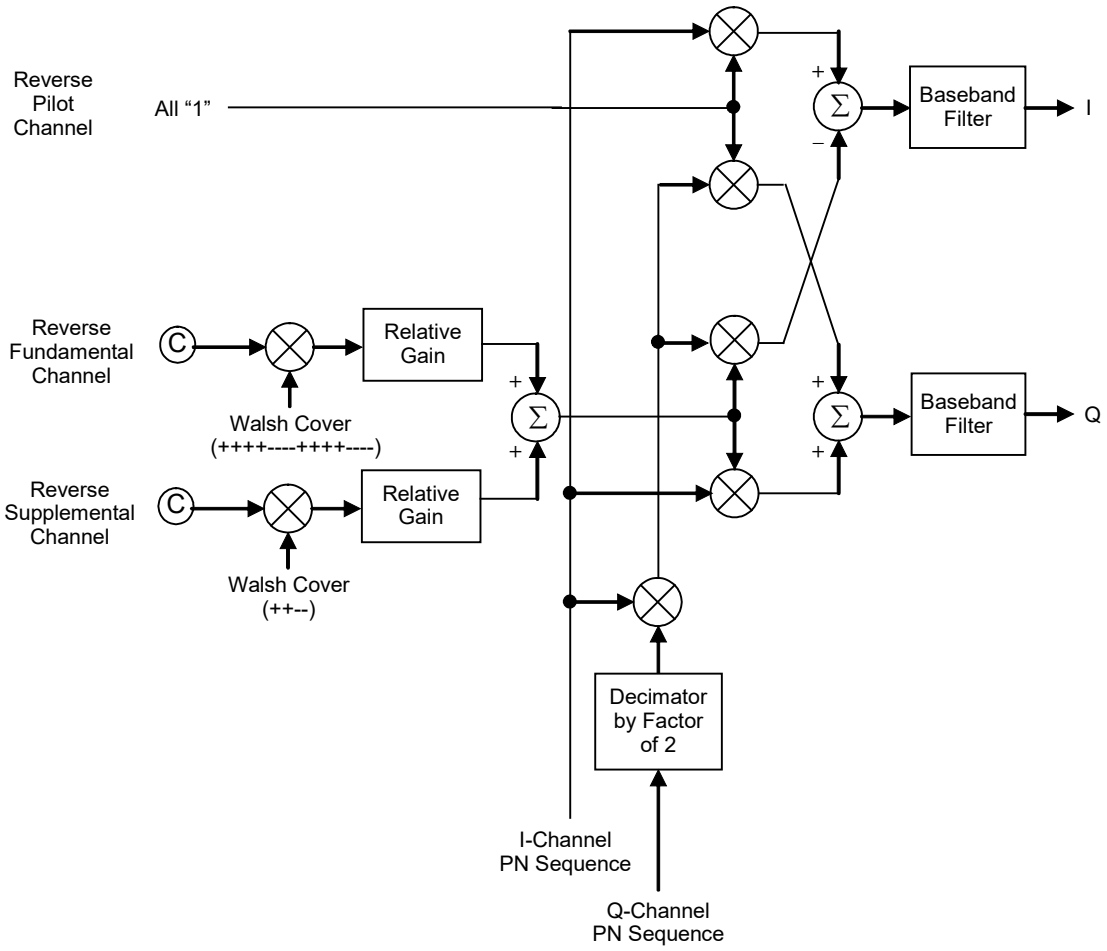


Figure 3.3.4-2 Signal generation block diagram for RVS_RC3_FCH_SCH waveform pattern (1 of 2)



Note:

Binary signals "0" and "1" are respectively substituted for 1 and –1.

Figure 3.3.4-3 Signal generation block diagram for RVS_RC3_FCH_SCH waveform pattern (2 of 2)

*: Since the PN9 generator is initialized every four frames, the same 4-frame length data is repeatedly output. For this reason, continuity of PN9fix is retained within a set of four consecutive frames, but lost with the adjacent sets of four consecutive frames. See Figure 3.3.1-3 "PN9fix data and short code" in Section 3.3.1 for details.

3.3.5 1xRTT Reverse RC3(3) (RVS_RC3_DCCH)

When the RVS_RC3_DCCH waveform pattern is selected, a frame-coded multiplexed signal of 1xRTT Reverse RC3 is output. The frame coding and IQ modulation are performed conforming to 3GPP2 C.S0002-C-1. The channels to be multiplexed are R-PICH and R-DCCH. Table 3.3.5-1 lists the parameters of the multiplexed channels.

Table 3.3.5-1 R-PICH (Reverse Pilot Channel) and R-DCCH (Reverse Dedicated Control Channel)

	Walsh Code	Code Power	Data Rate	Data
R-PICH	0	–5.278 dB	N/A	All 0
R-DCCH	8	–1.528 dB	9.6 kbps	PN9fix*

When this waveform pattern is selected, the output signal is frame-coded through the processing shown in the function block diagrams in Figs. 3.3.5-2 and 3.3.5-3. Frame coding is performed for four consecutive frames (outputting one frame takes about 20 ms), generating a 4-frame length signal pattern. The signal pattern obtained through frame coding is then repeatedly output. Since the length of three cycles of I Channel PN Sequence and Q Channel PN Sequence for short-code spreading is equivalent to the length of four frames, the short code retains continuity while the signal is output. Therefore, the signal that is output when this waveform pattern is selected can be used for modulation accuracy measurement, as well as frame error rate measurement using CRC. Note that long-code spreading is not executed.

Figure 3.3.5-1 shows the bit sequence assignment before convolutional coding.

Figure 3.3.5-1 Frame configuration of traffic channel of RVS_RC3_DCCH waveform pattern

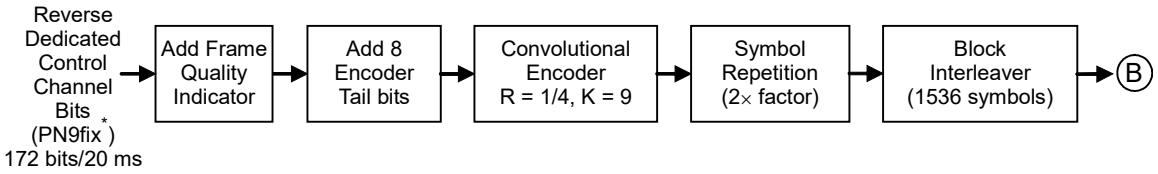
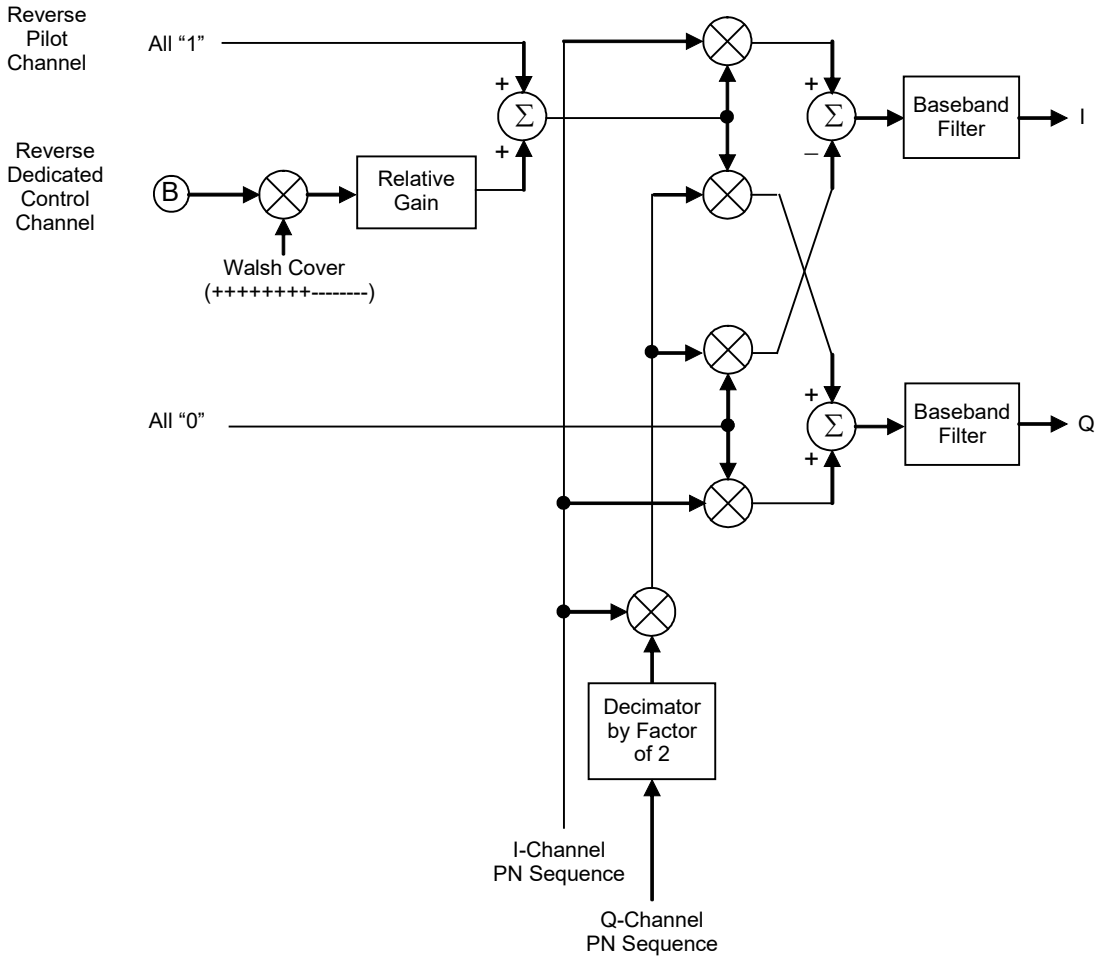


Figure 3.3.5-2 Signal generation block diagram for RVS_RC3_DCCH waveform pattern (1 of 2)



Note:

Binary signals "0" and "1" are respectively substituted for 1 and –1.

Figure 3.3.5-3 Signal generation block diagram for RVS_RC3_DCCH waveform pattern (2 of 2)

*: Since the PN9 generator is initialized every four frames, the same 4-frame length data is repeatedly output. For this reason, continuity of PN9fix is retained within a set of four consecutive frames, but lost with the adjacent sets of four consecutive frames. See Figure 3.3.1-3 "PN9fix data and short code" in Section 3.3.1 for details.

3.3.6 1xRTT Reverse RC4 (RVS_RC4_FCH)

When the RVS_RC4_FCH waveform pattern is selected, a frame-coded multiplexed signal of 1xRTT Reverse RC4 is output. The frame coding and IQ modulation are performed conforming to 3GPP2 C.S0002-C-1. The channels to be multiplexed are R-PICH and R-FCH. Table 3.3.6-1 lists the parameters of the multiplexed channels.

Table 3.3.6-1 R-PICH (Reverse Pilot Channel) and R-FCH (Reverse Fundamental Channel)

	Walsh Code	Code Power	Data Rate	Data
R-PICH	0	–5.278 dB	N/A	All 0
R-FCH	4	–1.528 dB	14.4 kbps	PN9fix*

When this waveform pattern is selected, the output signal is frame-coded through the processing shown in the function block diagrams in Figs. 3.3.6-2 and 3.3.6-3. Frame coding is performed for four consecutive frames (outputting one frame takes about 20 ms), generating a 4-frame length signal pattern. The signal pattern obtained through frame coding is then repeatedly output. Since the length of three cycles of I Channel PN Sequence and Q Channel PN Sequence for short-code spreading is equivalent to the length of four frames, the short code retains continuity while the signal is output. Therefore, the signal that is output when this waveform pattern is selected can be used for modulation accuracy measurement, as well as frame error rate measurement using CRC. Note that long-code spreading is not executed.

Figure 3.3.6-1 shows the bit sequence assignment before convolutional coding.

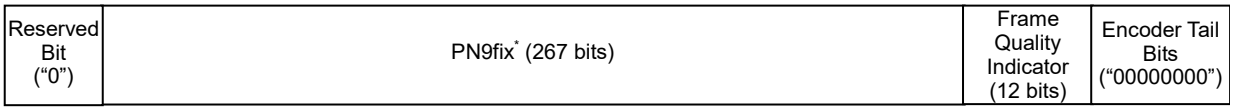


Figure 3.3.6-1 Frame configuration of traffic channel of RVS_RC4_FCH waveform pattern

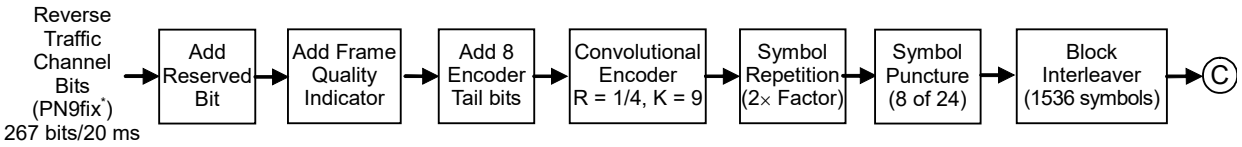
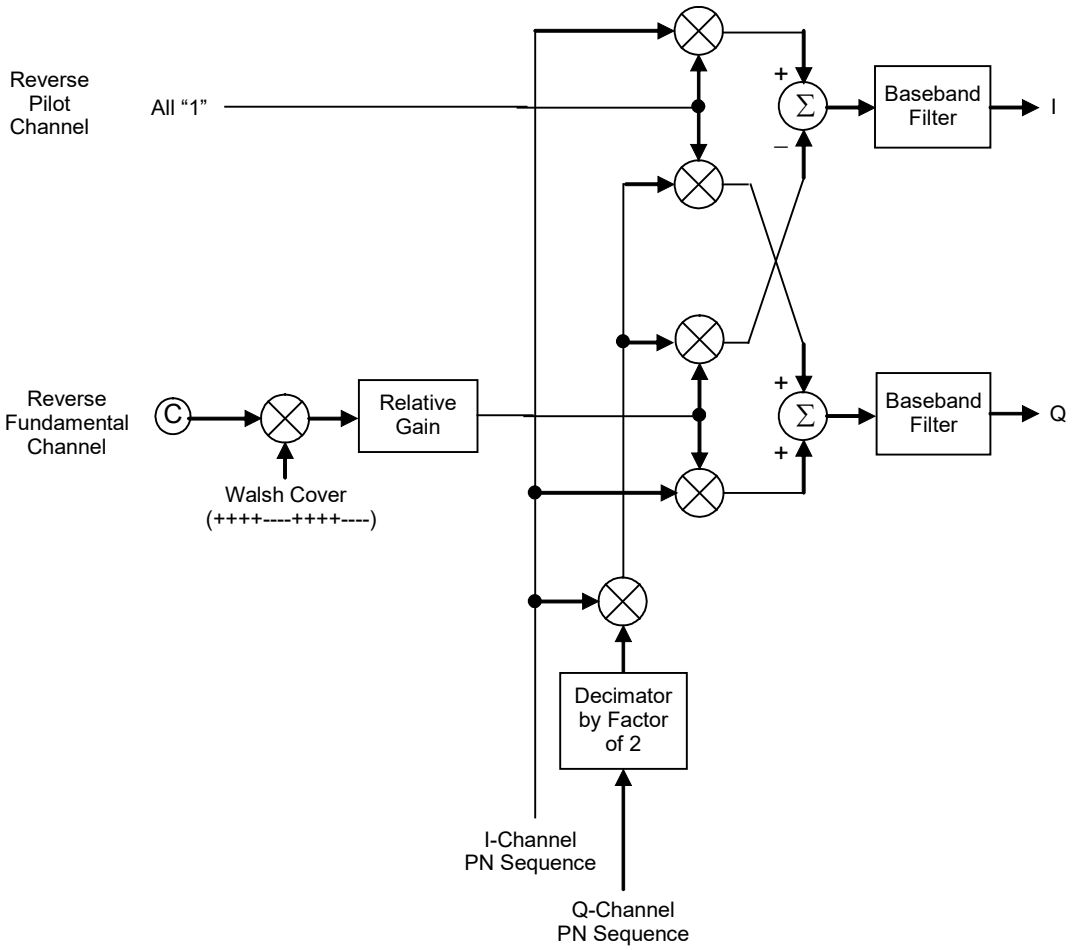


Figure 3.3.6-2 Signal generation block diagram for RVS_RC4_FCH waveform pattern (1 of 2)



Note:

Binary signals "0" and "1" are respectively substituted for 1 and –1.

Figure 3.3.6-3 Signal generation block diagram for RVS_RC4_FCH waveform pattern (2 of 2)

*: Since the PN9 generator is initialized every four frames, the same 4-frame length data is repeatedly output. For this reason, continuity of PN9fix is retained within a set of four consecutive frames, but lost with the adjacent sets of four consecutive frames. See Figure 3.3.1-3 "PN9fix data and short code" in Section 3.3.1 for details.

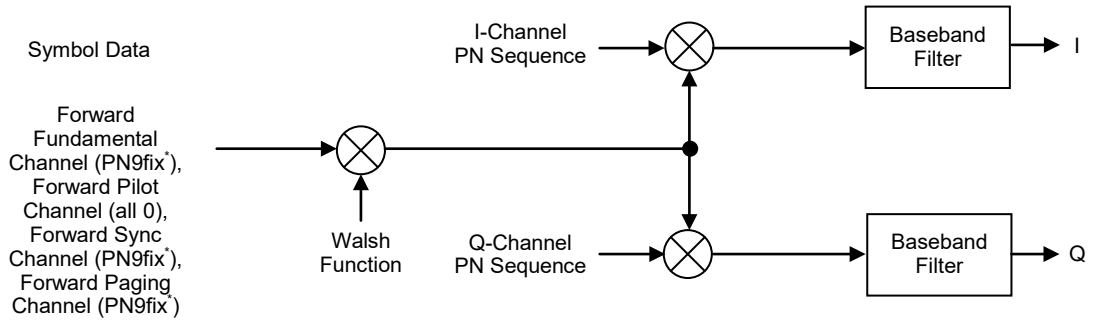
3.3.7 1xRTT Forward RC1, 2 (FWD_RC1-2 9channel)

When the FWD_RC1-2 9channel waveform pattern is selected, a multiplexed signal corresponding to 1xRTT Forward RC1 and RC2 that conform to 3GPP2 C.S0002-C-1 is output. The channels to be multiplexed are F-PICH, F-SyncCH, PagingCH, and F-FCH × 6 (data strings obtained by spreading six symbol data strings using spreading codes of Walsh codes 8 to 13). Table 3.3.7-1 lists the parameters of the multiplexed channels.

Table 3.3.7-1 F-PICH (Forward Pilot Channel), F-SyncCH (Forward Sync Channel), PagingCH (Paging Channel), and F-FCH (Forward Fundamental Channel)

	Walsh Code	Code Power	Data Rate	Data
F-PICH	0	–7.0 dB	N/A	All 0
F-SyncCH	32	–13.3 dB	4.8 ksps	PN9fix*
PagingCH	1	–7.3 dB	19.2 ksps	PN9fix*
F-FCH × 6	8 to 13	–10.3 dB	19.2 kbps	PN9fix*

When this waveform pattern is selected, the output signal is processed as shown in the function block diagram in Figure 3.3.7-1, without convolutional coding and interleaving. This function block diagram shows the processing of each channel. The symbol data of each channel is processed through this processing, and the processed symbol data of the multiplexed channels are then integrated. This processing is performed for four consecutive frames (outputting one frame takes about 20 ms), generating a 4-frame length signal pattern. The signal pattern obtained through this processing is then repeatedly output. Since the length of three cycles of I Channel PN Sequence and Q Channel PN Sequence for short-code spreading is equivalent to the length of four frames, the short code retains continuity while the signal is output. Therefore, the signal that is output when this waveform pattern is selected can be used for modulation accuracy measurement. Note that long-code scrambling and PCB Mux are not executed.



Note:

Binary signals "0" and "1" are respectively substituted for 1 and –1.

Figure 3.3.7-1 Signal generation block diagram for FWD_RC1-2 9channel waveform pattern

*: Since the PN9 generator is initialized every four frames, the same 4-frame length data is repeatedly output. For this reason, continuity of PN9fix is retained within a set of four consecutive frames, but lost with the adjacent sets of four consecutive frames. See Figure 3.3.1-3 "PN9fix data and short code" in Section 3.3.1 for details.

3.3.8 1xRTT Forward RC3, 4, 5 (FWD_RC3-5 9channel)

When the FWD_RC3-5 9channel waveform pattern is selected, a multiplexed signal corresponding to 1xRTT Forward RC3, RC4, and RC5 that conform to 3GPP2 C.S0002-C-1 is output. The channels to be multiplexed are F-PICH, F-SyncCH, PagingCH, and F-FCH × 6 (data strings obtained by spreading six symbol data strings using spreading codes of Walsh codes 8 to 13). Table 3.3.8-1 lists the parameters of the multiplexed channels.

Table 3.3.8-1 F-PICH (Forward Pilot Channel), F-SyncCH (Forward Sync Channel), PagingCH (Paging Channel), and F-FCH (Forward Fundamental Channel)

	Walsh Code	Code Power	Data Rate	Data
F-PICH	0	–7.0 dB	N/A	All 0
F-SyncCH	32	–13.3 dB	4.8 ksps	PN9fix*
PagingCH	1	–7.3 dB	19.2 ksps	PN9fix*
F-FCH × 6	8 to 13	–10.3 dB	19.2 kbps	PN9fix*

When this waveform pattern is selected, the output signal is processed as shown in the function block diagrams in Figs. 3.3.8-1 and 3.3.8-2, without convolutional coding and interleaving. These function block diagrams show processing of each channel. The symbol data of each channel is processed through this processing, and the processed symbol data of the multiplexed channels are then integrated. This processing is performed for four consecutive frames (outputting one frame takes about 20 ms), generating a 4-frame length signal pattern. The signal pattern obtained through this processing is then repeatedly output. Since the length of three cycles of I Channel PN Sequence and Q Channel PN Sequence for short-code spreading is equivalent to the length of four frames, the short code retains continuity while the signal is output. Therefore, the signal that is output when this waveform pattern is selected can be used for modulation accuracy measurement. Note that long-code scrambling and PCB Mux are not executed.

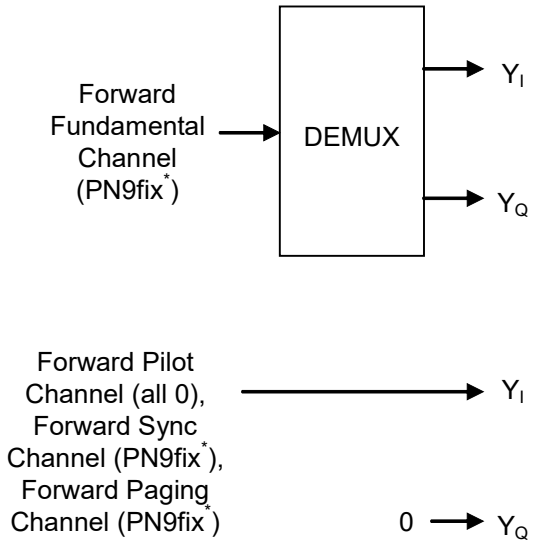
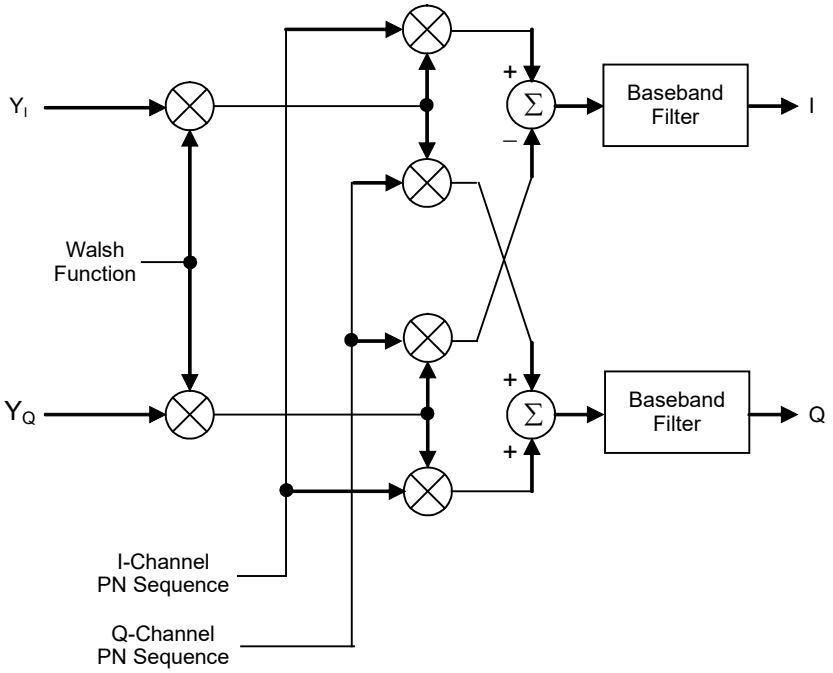


Figure 3.3.8-1 Signal generation block diagram for FWD_RC3-5 9channel (1 of 2)



Note:

Binary signals "0" and "1" are respectively substituted for 1 and –1.

Figure 3.3.8-2 Signal generation block diagram for FWD_RC3-5 9channel (2 of 2)

*: Since the PN9 generator is initialized every four frames, the same 4-frame length data is repeatedly output. For this reason, continuity of PN9fix is retained within a set of four consecutive frames, but lost with the adjacent sets of four consecutive frames. See Figure 3.3.1-3 “PN9fix data and short code” in Section 3.3.1 for details.

3.4 CDMA2000 1xEV-DO Waveform Pattern

The following CDMA2000 1xEV-DO waveform patterns are provided.

FWD_38_4_16slot/…/FWD_2457_6_1slot
When these waveform patterns are selected, a CDMA2000 1xEV-DO forward modulation signal is output after channel coding, time-division multiplexing (TDM), and IQ mapping are performed for that signal, in conformance with 3GPP2 C.S0024.

FWD_Idle
When this waveform pattern is selected, a CDMA2000 1xEV-DO forward idle slot modulation signal is output after time-division multiplexing (TDM) and IQ mapping are performed for that signal, in conformance with 3GPP2 C.S0024.

RVS_9_6 kbps_RX/…/RVS_153_6 kbps_RX
When these waveform patterns are selected, a CDMA2000 1xEV-DO reverse modulation signal is output after channel coding and IQ mapping are performed for that signal, in conformance with 3GPP2 C.S0024.

Table 3.4-1 lists the provided CDMA2000 1xEV-DO waveform patterns.

Table 3.4-1 List of CDMA2000 1xEV-DO waveform patterns

Waveform Pattern Name	Supported System	Frame Coding	Symbol Data
FWD_38_4kbps_16slot	CDMA2000 1xEV-DO Forward	IS-95SPEC + EQ	PN15fix*
FWD_76_8kbps_8slot	CDMA2000 1xEV-DO Forward	IS-95SPEC + EQ	PN15fix*
FWD_153_6kbps_4slot	CDMA2000 1xEV-DO Forward	IS-95SPEC + EQ	PN15fix*
FWD_307_2kbps_2slot	CDMA2000 1xEV-DO Forward	IS-95SPEC + EQ	PN15fix*
FWD_614_4kbps_1slot	CDMA2000 1xEV-DO Forward	IS-95SPEC + EQ	PN15fix*
FWD_307_2kbps_4slot	CDMA2000 1xEV-DO Forward	IS-95SPEC + EQ	PN15fix*
FWD_614_4kbps_2slot	CDMA2000 1xEV-DO Forward	IS-95SPEC + EQ	PN15fix*
FWD_1228_8kbps_1slot	CDMA2000 1xEV-DO Forward	IS-95SPEC + EQ	PN15fix*
FWD_921_6kbps_2slot	CDMA2000 1xEV-DO Forward	IS-95SPEC + EQ	PN15fix*
FWD_1843_2kbps_1slot	CDMA2000 1xEV-DO Forward	IS-95SPEC + EQ	PN15fix*

*: Indicates PN sequences cut out for each packet. Therefore, the PN sequence is not continuous between the last data of one packet and the first data of the following packet.

Table 3.4-1 List of CDMA2000 1xEV-DO waveform patterns (Cont'd)

Waveform Pattern Name	Supported System	Frame Coding	Symbol Data
FWD_1228_8kbps_2slot	CDMA2000 1xEV-DO Forward	IS-95SPEC + EQ	PN15fix*
FWD_2457_6kbps_1slot	CDMA2000 1xEV-DO Forward	IS-95SPEC + EQ	PN15fix*
FWD_Idle	CDMA2000 1xEV-DO Forward	IS-95SPEC + EQ	–
RVS_9_6kbps_RX	CDMA2000 1xEV-DO Reverse	IS-95SPEC	PN9fix*
RVS_19_2kbps_RX	CDMA2000 1xEV-DO Reverse	IS-95SPEC	PN9fix*
RVS_38_4kbps_RX	CDMA2000 1xEV-DO Reverse	IS-95SPEC	PN9fix*
RVS_76_8kbps_RX	CDMA2000 1xEV-DO Reverse	IS-95SPEC	PN9fix*
RVS_153_6kbps_RX	CDMA2000 1xEV-DO Reverse	IS-95SPEC	PN9fix*
RVS_9_6kbps_TX	CDMA2000 1xEV-DO Reverse	IS-95SPEC	PN9fix*
RVS_19_2kbps_TX	CDMA2000 1xEV-DO Reverse	IS-95SPEC	PN9fix*
RVS_38_4kbps_TX	CDMA2000 1xEV-DO Reverse	IS-95SPEC	PN9fix*
RVS_76_8kbps_TX	CDMA2000 1xEV-DO Reverse	IS-95SPEC	PN9fix*
RVS_153_6kbps_TX	CDMA2000 1xEV-DO Reverse	IS-95SPEC	PN9fix*

*: Indicates PN sequences cut out for each packet. Therefore, the PN sequence is not continuous between the last data of one packet and the first data of the following packet.

When a CDMA2000 1xEV-DO waveform pattern is output, a marker signal shown in Table 3.4-2 is output from the AUX connector on the rear panel.

Table 3.4-2 Marker output data

Marker Signal	Output Data
Marker 1	Frame Clock
Marker 2	RF Gate
Marker 3	Symbol Clock

3.4.1 1xEV-DO forward (excluding FWD_Idle)

When one of the FWD_38_4kbps_16slot to FWD_2457_6kbps_1slot waveform patterns is selected, a CDMA2000 1xEV-DO forward modulation signal is output after channel coding and IQ mapping are performed for that signal, in conformance with 3GPP2 C.S0024. This output signal has a pilot channel, forward MAC channel, and forward traffic channel multiplexed. The forward traffic channel uses PN15fix* for data before a frame check sequence (FCS).
Figure 3.4.1-1 shows a bit sequence format where FCS and TAIL bit sequences are affixed to a PN15fix bit sequence.
Hereinafter, a bit sequence with FCS and TAIL bit sequences affixed to a PN15fix bit sequence is referred to as a "packet".

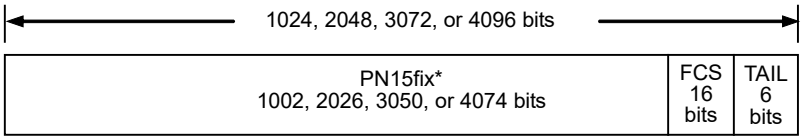


Figure 3.4.1-1 Format of 1xEV-DO forward packet

*: Indicates PN sequences cut out for each packet. Therefore, the PN sequence is not continuous between the last data of one packet and the first data of the following packet.

The packet is time-division multiplexed (TDM) with other channels after it is channel-coded including turbo coding, scrambling, channel interleaving, and modulation (QPSK, 8-PSK, and 16QAM). The MAC index used for scrambling is the same value as the MAC index used by the preamble of the same slot.

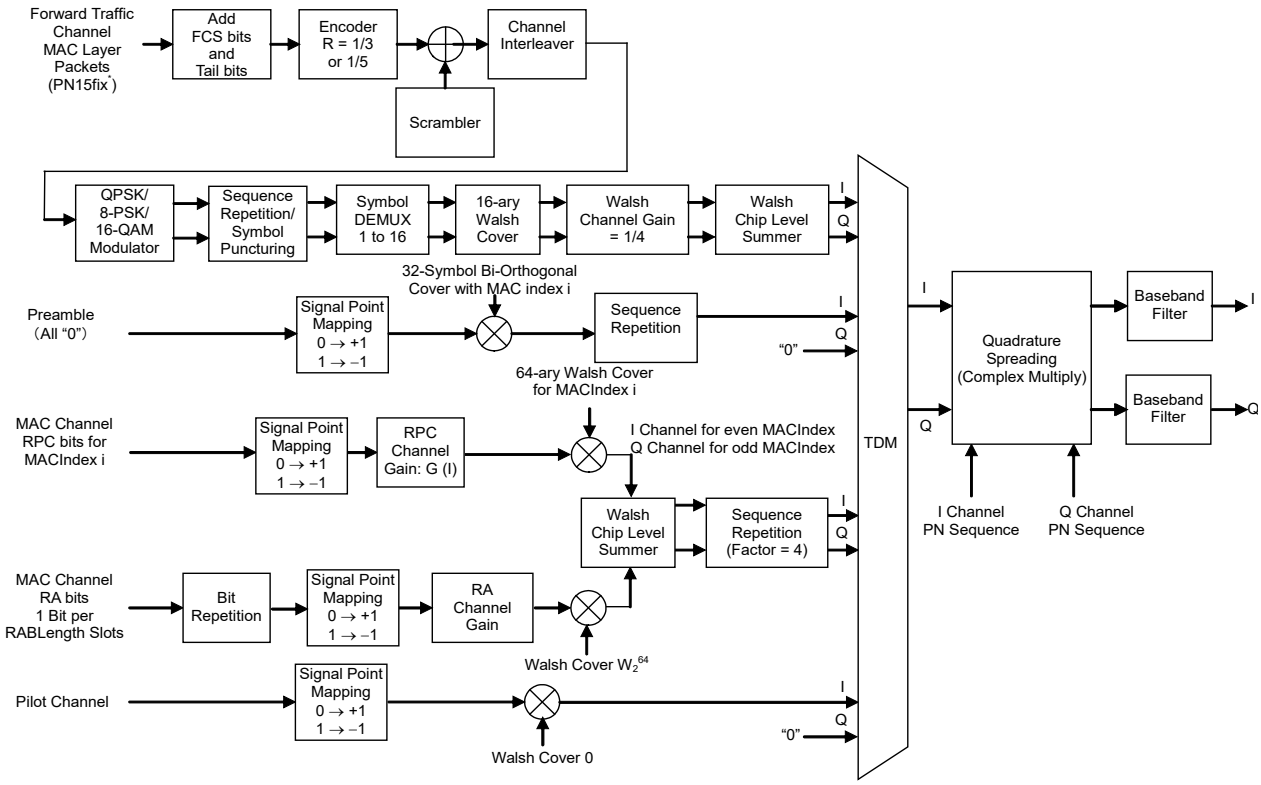


Figure 3.4.1-2 Block diagram of 1xEV-DO forward

*: Indicates PN sequences cut out for each packet. Therefore, the PN sequence is not continuous between the last data of one packet and the first data of the following packet.

Channel-coded packets are assigned to the data field of the slot through time-division multiplexing, along with preambles having the same MAC index. Figure 3.4.1-3 shows the slot format while Figure 3.4.1-4 shows the time-division multiplexing of the preamble, channel-coded packet, MAC channel, and pilot channel.

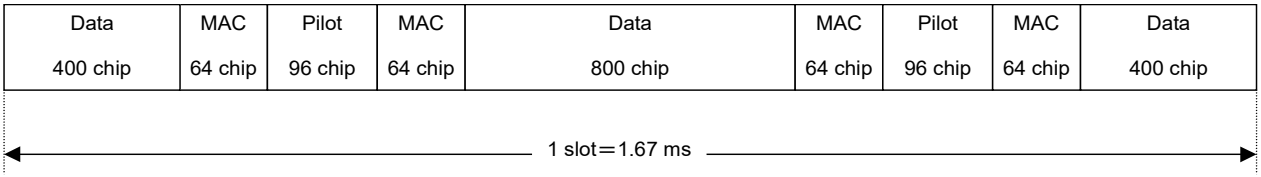


Figure 3.4.1-3 Format of 1xEV-DO forward slot (excluding Idle slots)

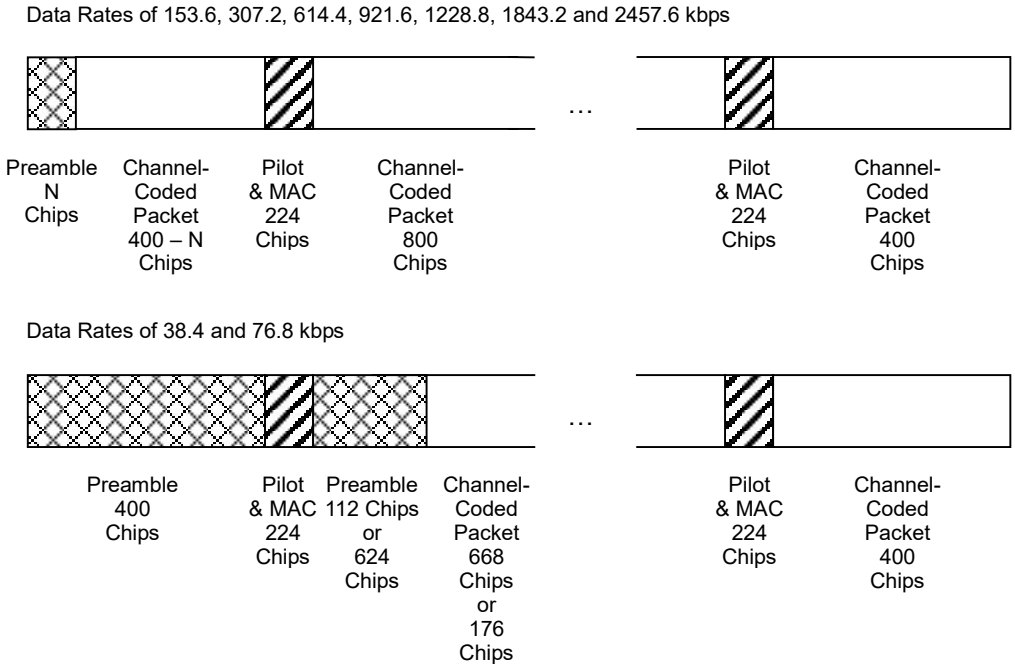


Figure 3.4.1-4 Timing diagrams

As data to be transferred on the forward traffic channel, the PN15 code generator generates a packet from each of four PN15fix data having different initial values. Each of these packets is then channel-coded. In this event, the MAC index used by the scrambler is different for each packet. However, for a preamble that is assigned to the same slot of a given packet, the MAC index for the packet is used. See Figure 3.4.1-5 for the MAC index values. A channel-coded packet is assigned to a slot every three slots, and different channel-coded packets are assigned to the three slots in between. Figure 3.4.1-5 shows traffic channels assigned every three slots and Table 3.4.1-1 lists the parameters of the forward traffic channel.

Table 3.4.1-1 Traffic channel parameters

1xEV-DO Waveform Pattern	Data Rate (kbps)	Slot	Packet (Bit)	Preamble (Chip)	Modulation Type
FWD_38_4kbps_16slot	38.4	16	1024	1024	QPSK
FWD_76_8kbps_8slot	76.8	8	1024	512	QPSK
FWD_153_6kbps_4slot	153.6	4	1024	256	QPSK
FWD_307_2kbps_2slot	307.2	2	1024	128	QPSK
FWD_614_4kbps_1slot	614.4	1	1024	64	QPSK
FWD_307_2kbps_4slot	307.2	4	2048	128	QPSK
FWD_614_4kbps_2slot	614.4	2	2048	64	QPSK
FWD_1228_8kbps_1slot	1228.8	1	2048	64	QPSK
FWD_921_6kbps_2slot	921.6	2	3072	64	8-PSK
FWD_1843_2kbps_1slot	1843.2	1	3072	64	8-PSK
FWD_1228_8kbps_2slot	1228.8	2	4096	64	16QAM
FWD_2457_6kbps_1slot	2457.6	1	4096	64	16QAM

Table 3.4.1-2 lists the parameters of the MAC channel.

Table 3.4.1-2 MAC channel parameters

MAC Index	RABit	RPCBit
4 (RA Channel), 5 to 17 (RPC Channel)	Random	Random

For MAC channels RPC and RA, the RPCBit transferred on an RPC channel and the RABit on an RA channel are random. There are thirteen RPC channels and one RA channel. These MAC channels are multiplexed after they are spread by the Walsh cover, which is determined by the MAC index. MAC channels are assigned to the MAC field of the slot as shown in Figure 3.4.1-3. Figure 3.4.1-5 shows the relationship between a slot and data transmitted on a MAC channel and traffic channel.

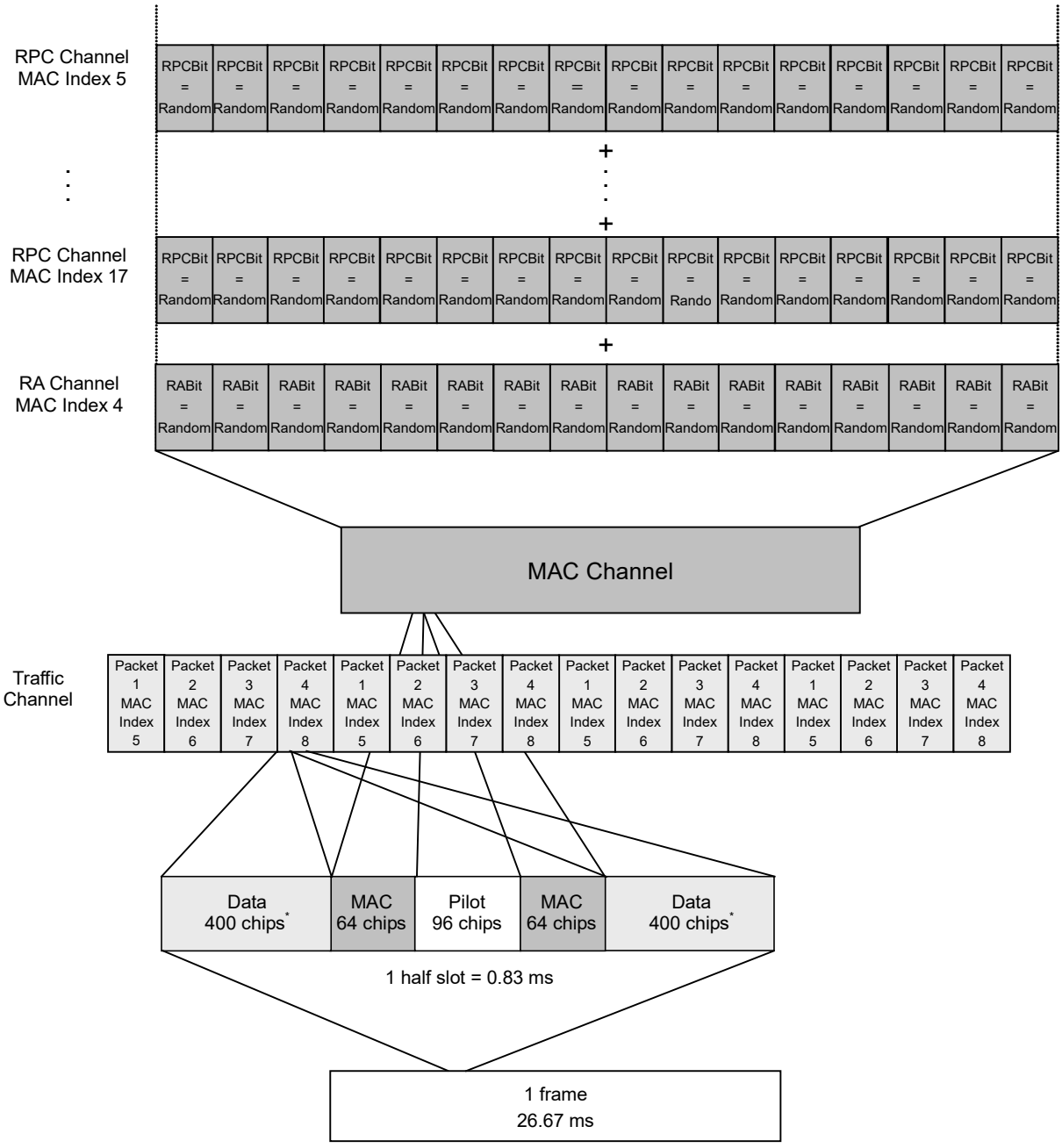


Figure 3.4.1-5 Channel Multiplexing

*: Data may contain a preamble.

3.4.2 1xEV-DO reverse

When one of the 1xEV-DO waveform patterns from RVS_9_6kbps_RX to RVS_153_6kbps_TX is selected, a CDMA2000 1xEV-DO reverse modulation signal is output after channel coding and IQ mapping are performed for that signal, in conformance with 3GPP2 C.S0024. This output signal has a pilot, RRI, DRC, ACK, and data channels multiplexed. The data channel uses PN9fix* for data before a frame check sequence (FCS).

Figure 3.4.2-1 shows a bit sequence format where FCS and TAIL bit sequences are affixed to a PN9fix bit sequence.

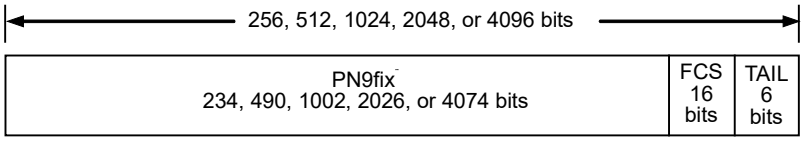


Figure 3.4.2-1 Format of 1xEV-DO reverse packet

*: The data length of PN9fix is not an integral multiple of the PN sequence length (511 bits), and the PN sequence is not continuous at the end of the data.

A bit sequence with FCS and TAIL bit sequences affixed to a PN15fix bit sequence is multiplexed with pilot, RRI, DRC, and ACK channels after it is channel-coded. Figure 3.4.2-2 shows a block diagram of 1xEV-DO reverse, Table 3.4.2-1 lists the modulation parameters, and Table 3.4.2-2 lists the gain of each channel.

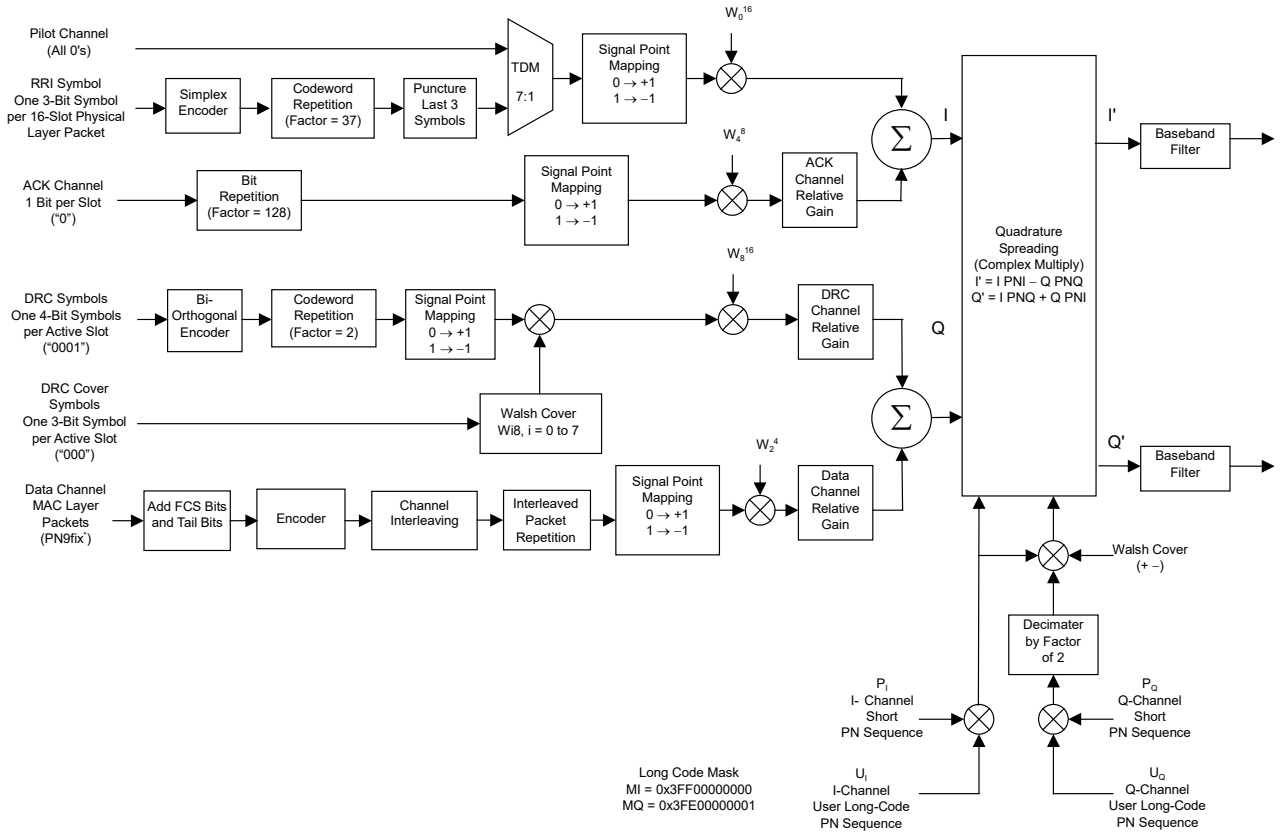


Figure 3.4.2-2 Block diagram of 1xEV-DO reverse

*: Data length is not an integral multiple of the PN sequence length (511 bits for PN9) and PN sequence is not continuous at the end of the data.

Table 3.4.2-1 1xEV-DO reverse modulation parameters

1xEV-DO Waveform Pattern	Data Rate (kbps)	RRI Symbol	DRC Value	DRC Cover	ACK Channel Bit	Long Code Mask
RVS_9_6kbps_RX	9.6	001	0x01	W_0^8	0	MI = 0x3FF00000000 MQ = 0x3FE00000001
RVS_19_2kbps_RX	19.2	010	0x01	W_0^8	0	
RVS_38_4kbps_RX	38.4	011	0x01	W_0^8	0	
RVS_76_8kbps_RX	76.8	100	0x01	W_0^8	0	
RVS_153_6kbps_RX	153.6	101	0x01	W_0^8	0	
RVS_9_6kbps_TX	9.6	001	0x01	W_0^8	0	
RVS_19_2kbps_TX	19.2	010	0x01	W_0^8	0	
RVS_38_4kbps_TX	38.4	011	0x01	W_0^8	0	
RVS_76_8kbps_TX	76.8	100	0x01	W_0^8	0	
RVS_153_6kbps_TX	153.6	101	0x01	W_0^8	0	

Table 3.4.2-2 Channel gain of 1xEV-DO Reverse

1xEV-DO Waveform Pattern	Data Rate (kbps)	Data/Pilot	RRI/Pilot	DRC/Pilot	ACK/Pilot
RVS_9_6kbps_RX	9.6	3.75 dB	0 dB	3.0 dB	0.0 dB
RVS_19_2kbps_RX	19.2	6.75 dB	0 dB	3.0 dB	0.0 dB
RVS_38_4kbps_RX	38.4	9.75 dB	0 dB	3.0 dB	0.0 dB
RVS_76_8kbps_RX	76.8	13.25 dB	0 dB	3.0 dB	0.0 dB
RVS_153_6kbps_RX	153.6	18.50 dB	0 dB	3.0 dB	0.0 dB
RVS_9.6 kbps_TX	9.6	3.75 dB	0 dB	3.0 dB	3.0 dB
RVS_19.2 kbps_TX	19.2	6.75 dB	0 dB	3.0 dB	3.0 dB
RVS_38.4 kbps_TX	38.4	9.75 dB	0 dB	3.0 dB	3.0 dB
RVS_76.8 kbps_TX	76.8	13.25 dB	0 dB	3.0 dB	3.0 dB
RVS_153.6 kbps_TX	153.6	18.50 dB	0 dB	3.0 dB	3.0 dB

3.4.3 1xEV-DO forward idle slot

When the FWD_Idle waveform pattern is selected, a CDMA2000 1xEV-DO forward idle slot modulation signal is output after IQ mapping is performed for that signal, in conformance with 3GPP2 C.S0024. This output signal has a pilot channel and forward MAC channel multiplexed. Figure 3.4.3-1 shows a block diagram of 1xEV-DO forward idle slot.

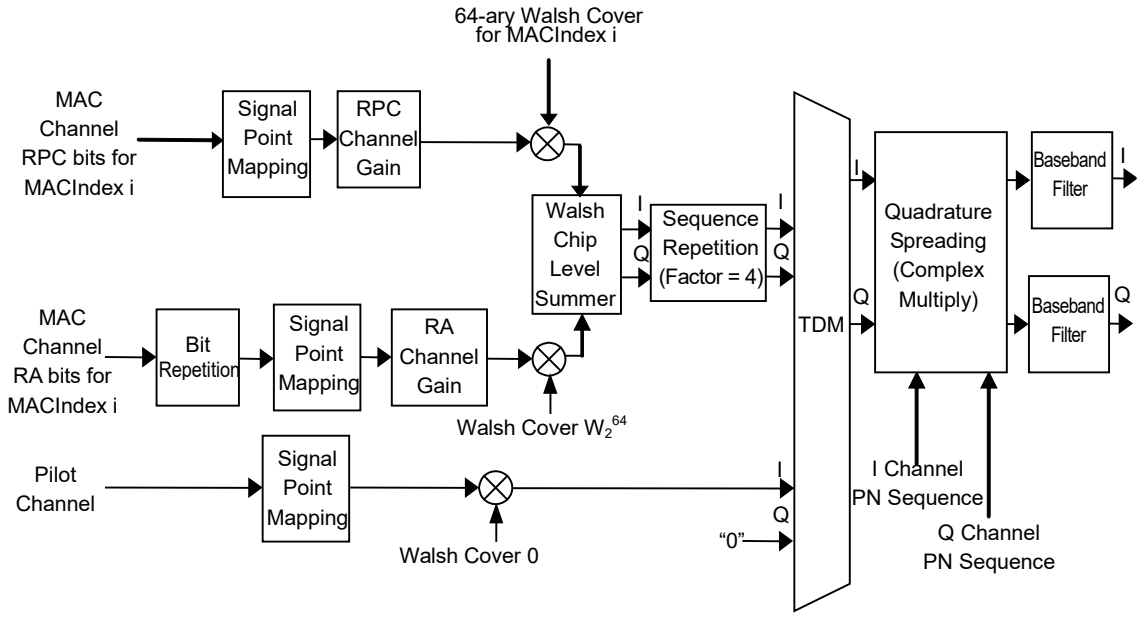


Figure 3.4.3-1 Block diagram of 1xEV-DO forward idle slot

Figure 3.4.3-2 shows the format of 1xEV-DO forward idle slot and Table 3.4.3-1 lists the MAC channel parameters of the 1xEV-DO forward idle slot.

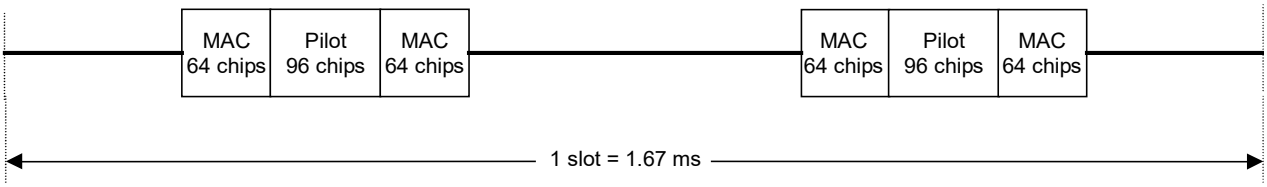


Figure 3.4.3-2 Format of 1xEV-DO forward idle slot

Table 3.4.3-1 MAC channel parameters of 1xEV-DO forward idle slot

MAC Index	RA Bit	RPC Bit	RA Channel Gain	RPC Channel Gain
4 (RA Channel), 5 to 17 (RPC Channel)	Random	Random	–12.04 dB*	–11.42 dB*

*: Value relative to the pilot channel.

3.5 WLAN Waveform Pattern

IEEE802.11a, IEEE802.11b, and IEEE802.11g waveform patterns are provided as WLAN waveform patterns. They are listed in Tables 3.5-1, 3.5-2, and 3.5-3, respectively.

Table 3.5-1 List of IEE802.11a waveform patterns

Waveform Pattern Name	Data rate (Mbits/s)	Modulation	Coding Rate	Coding Bits per Subcarrier	Coding Bits per OFDM Symbol	Data Bits per OFDM Symbol
11a_OFDM_6Mbps	6	BPSK	1/2	1	48	24
11a_OFDM_9Mbps	9	BPSK	3/4	1	48	36
11a_OFDM_9Mbps_PN9*1	9	BPSK	3/4	1	48	36
11a_OFDM_12Mbps	12	QPSK	1/2	2	96	48
11a_OFDM_18Mbps	18	QPSK	3/4	2	96	72
11a_OFDM_18Mbps_PN9*1	18	QPSK	3/4	2	96	72
11a_OFDM_24Mbps	24	16-QAM	1/2	4	192	96
11a_OFDM_36Mbps	36	16-QAM	3/4	4	192	144
11a_OFDM_36Mbps_PN9*1	36	16-QAM	3/4	4	192	144
11a_OFDM_48Mbps	48	64-QAM	2/3	6	288	192
11a_OFDM_54Mbps	54	64-QAM	3/4	6	288	216
11a_OFDM_54Mbps_PN9*1	54	64-QAM	3/4	6	288	216
11a_OFDM_54Mbps_ACP*2	54	64-QAM	3/4	6	288	216

*1: Waveform pattern having continuous PN9 data. For the waveform patterns without *1 affixed, the PN9 data does not have continuity. A gap period of 4 samples is secured at the start of the waveform pattern, followed by a PLCP preamble. When using an external trigger, set the trigger delay to –4 samples to match the rising of the external trigger and the starting point of the PLCP preamble.

*2: Waveform pattern having improved ACPR with spectrum sidelobes cut down.

Table 3.5-2 List of IEE802.11b waveform patterns

Waveform Pattern Name	Spreading and Coding	Modulation
11b_DSSS_1Mbps	DSSS, 11 chip Barker Code	DBPSK
11b_DSSS_2Mbps	DSSS, 11 chip Barker Code	DQPSK
11b_DSSS_2Mbps_PN9*1, *3	DSSS, 11 chip Barker Code	DQPSK
11b_CCK_5_5Mbps	CCK	DQPSK
11b_CCK_11Mbps	CCK	DQPSK
11b_CCK_11Mbps_PN9*1	CCK	DQPSK
11b_CCK_11Mbps_ACP*2	CCK	DQPSK

In the above waveform patterns, the ramp rises at the start of the waveform pattern. The frame clock also rises at the same timing. When using an external trigger, set the trigger delay to –88 samples to match the rising of the external trigger and the starting point of the PLCP preamble.

*1: Waveform pattern having continuous PN9 data. For the waveform patterns without *1 affixed, the PN9 data does not have continuity.

*2: Waveform pattern having improved ACPR with spectrum sidelobes cut down.

*3: For MS2830A or MS2840A: ARB Memory Upgrade 256 Msamples (option 027) must be installed to use this waveform pattern.

Table 3.5-3 List of IEE802.11g waveform patterns

Waveform Pattern Name	Data rate (Mbits/s)	Modulation	Coding Rate	Coding Bits per Subcarrier	Coding Bits per OFDM Symbol	Data Bits per OFDM Symbol
11g_DSSS_OFDM_6Mbps	6	BPSK	1/2	1	48	24
11g_DSSS_OFDM_9Mbps	9	BPSK	3/4	1	48	36
11g_DSSS_OFDM_12Mbps	12	QPSK	1/2	2	96	48
11g_DSSS_OFDM_18Mbps	18	QPSK	3/4	2	96	72
11g_DSSS_OFDM_24Mbps	24	16-QAM	1/2	4	192	96
11g_DSSS_OFDM_36Mbps	36	16-QAM	3/4	4	192	144
11g_DSSS_OFDM_48Mbps	48	64-QAM	2/3	6	288	192
11g_DSSS_OFDM_54Mbps	54	64-QAM	3/4	6	288	216

In the above waveform patterns, the ramp rises at the start of the waveform pattern. The frame clock also rises at the same timing. When using an external trigger, set the trigger delay to –60 samples to match the rising of the external trigger and the starting point of the PLCP preamble.

When a WLAN waveform pattern is output, a marker signal shown in Table 3.5-4 is output from the AUX connector on the rear panel.

Table 3.5-4 Marker output data

Marker Signal	Output Data
Marker 1	Frame Clock
Marker 2	RF Gate
Marker 3	–

3.5.1 IEEE802.11a

The IEEE802.11a waveform patterns conform to the MAC and physical layer specifications defined in IEEE802.11 and IEEE802.11a.

Table 3.5.1-1 lists the parameters commonly used by each waveform pattern.

Table 3.5.1-1 Common parameters

Parameter	Setting Value
PSDU Length	1000 bytes
PSDU Data	PN9fix or PN9*
Sampling Rate	40 MHz

*: PN9fix is PN9 data that is reset for every PSDU. Therefore, PN data is not continuous between PSDUs; however, continuity of PN data is retained for waveform patterns whose name ends with _PN9, since such waveform patterns have 511 frame cycles.

Figure 3.5.1-1 shows the PPDU frame format.

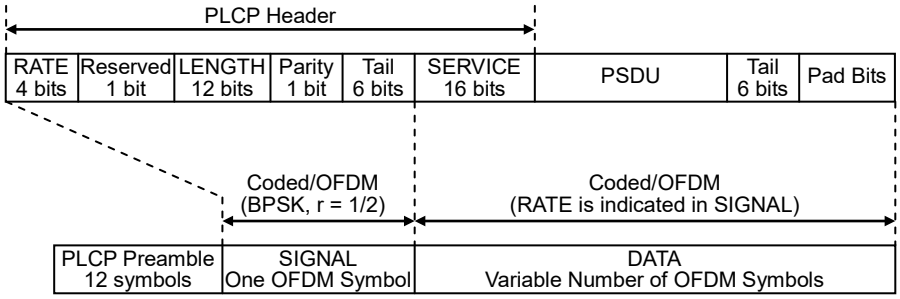


Figure 3.5.1-1 Format of IEEE802.11a PPDU frame

The MAC frame shown in Figure 3.5.1-2 is used in PSDU of the PPDU frame format. A MAC frame consists of Frame Body (transmission data), MAC header, and FCS.

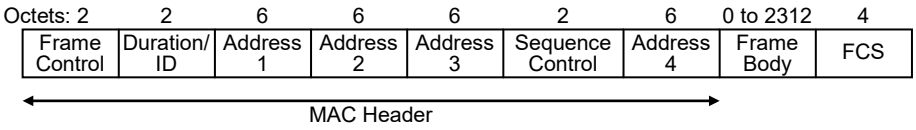


Figure 3.5.1-2 Format of IEEE802.11a MAC frame

The frame control field in the MAC header consists of the bits listed in Table 3.5.1-2 and the data below are used.

Table 3.5.1-2 Frame control field

Field	Bit	Data
Protocol Version	B0 and B1	00
Type	B2 and B3	01
Subtype	B4 to B7	0000
To DS	B8	0
From DS	B9	0
More Flag	B10	0
Retry	B11	0
Power Management	B12	00
More Data	B13	0
WEP	B14	0
Order	B15	0

The MAC frame data other than the frame control field is listed in Table 3.5.1-3.

Table 3.5.1-3 MAC header (Other than frame control)

Field	Data
Duration/ID	0000_H
Address 1	FFFF FFFF $FFFF_H$*
Address 2	0000 0000 0000_H
Address 3	0000 0000 0000_H
Sequence Control	0000_H
Address 4	0000 0000 0000_H

*: All “1s” in Address 1 (destination address in Adhoc mode) indicates a broadcast address.

3.5.2 IEEE802.11b

The IEEE802.11b waveform patterns conform to the MAC and physical layer specifications described in IEEE802.11 and IEEE802.11b.

Table 3.5.2-1 lists the parameters commonly used by each waveform pattern.

Table 3.5.2-1 Common parameters

Parameter	Setting Value
PSDU Length	1024 bytes
PSDU Data	PN9fix or PN9*
Sampling Rate	44 MHz

*: PN9fix is PN9 data that is reset for every PSDU. Therefore, PN data is not continuous between PSDUs; however, continuity of PN data is retained for waveform patterns whose name ends with _PN9, since such waveform patterns have 511 frame cycles.

Figure 3.5.2-1 shows the Long PLCP PPDU frame format.

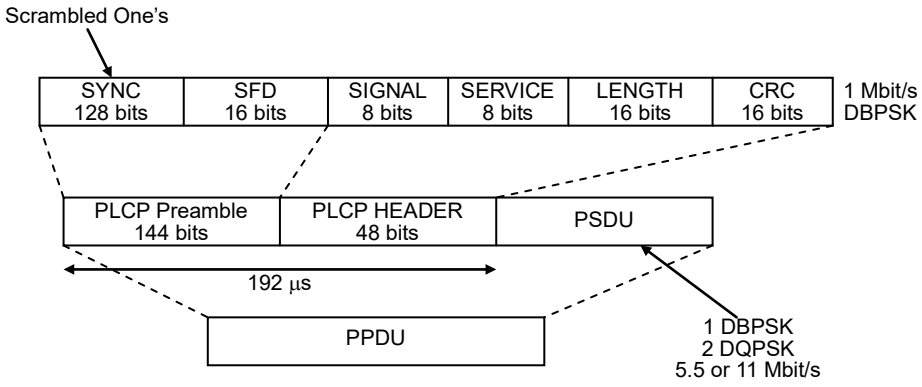


Figure 3.5.2-1 Format of IEEE802.11b Long PLCP PPDU frame

The same MAC frame as the one described in Section 3.5.1 "IEEE802.11a" is used in PSDU of the Long PLCP PPDU frame format.

3.5.3 IEEE802.11g

The IEEE802.11g waveform patterns conform to the MAC and physical layer specifications described in IEEE802.11 and IEEE802.11g.

Table 3.5.3-1 lists the parameters commonly used by each waveform pattern.

Table 3.5.3-1 Common parameters

Parameter	Setting Value
PSDU Length	1000 bytes
PSDU Data	PN9fix*
Sampling Rate	44 MHz

*: PN9fix is PN9 data that is reset for every PSDU. Therefore, PN data is not continuous between PSDUs.

Figure 3.5.3-1 shows the Long preamble PPDU frame format.

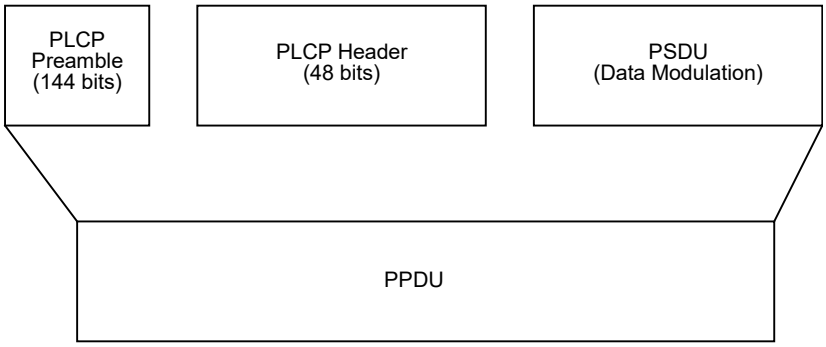


Figure 3.5.3-1 Format of IEEE802.11g Long preamble PPDU frame

3.6 Digital Broadcasting Waveform Pattern

Table 3.6-1 lists the provided digital broadcasting waveform patterns.

Table 3.6-1 List of digital broadcasting waveform patterns

Waveform Pattern Name	Parameter	Application
BS_1ch	Roll-off rate: 0.35 Nyquist bandwidth: 28.86 MHz Modulation: QPSK	Digital BS broadcasting (ISDB-S) physical layer waveform used for device test
CS_1ch	Roll-off rate: 0.35 Nyquist bandwidth: 21.096 MHz Modulation: QPSK	Digital CS broadcasting (DVB-S) physical layer waveform used for device test
CATV_AnnexC_1ch	Roll-off rate: 0.13 Nyquist bandwidth: 5.274 MHz Modulation: 64QAM	CATV (ITU-T J83 AnnexC) physical layer waveform used for device test
ISDBT_1layer_1ch	Mode: 3, GI: 1/8 Layer A: 13seg, 64QAM	ISDB-T physical layer waveform used for device test
ISDBT_2layer_1ch	Mode: 3, GI: 1/8 Layer A: 1seg, QPSK Layer B: 12seg, 64QAM	ISDB-T physical layer waveform used for device test
ISDBT_2layer_Coded	Mode: 3, GI: 1/8 Layer A: 1seg, QPSK, CR = 2/3, TI = 2 Layer B: 12seg, 64QAM, CR = 7/8, TI = 2	ISDB-T partial reception waveform mainly used for simplified BER measurement. The waveform length is four frames.
ISDBT_QPSK_1_2	Mode: 3, GI: 1/8 Layer A: 1seg, QPSK, CR = 1/2, TI = 0 Layer B: 12seg, 64QAM, CR = 7/8, TI = 1	ISDB-T partial reception waveform mainly used for simplified BER measurement. The waveform length is four frames.
ISDBT_QPSK_2_3	Mode: 3, GI: 1/8 Layer A: 1seg, QPSK, CR = 2/3, TI = 0 Layer B: 12seg, 64QAM, CR = 7/8, TI = 1	
ISDBT_16QAM_1_2	Mode: 3, GI: 1/8 Layer A: 1seg, 16QAM, CR = 1/2, TI = 0 Layer B: 12seg, 64QAM, CR = 7/8, TI = 1	
ISDBT_QPSK_2_3_TI4	Mode: 3, GI: 1/8 Layer A: 1seg, QPSK, CR = 2/3, TI = 4 Layer B, 12seg, 64QAM, CR = 3/4, TI = 2	

Table 3.6-1 List of digital broadcasting waveform patterns (Cont'd)

Waveform Pattern Name	Parameter	Application
ISDBTsb_QPSK_1_2	Transmission of concatenated eight segments consisting of Seg#1 to Seg#5 (1-segment format) and Seg#6 to Seg#8 (3-segment format) Mode: 3, GI: 1/8 Layer A: QPSK, CR = 1/2, TI = 0 Layer B: QPSK, CR = 1/2, TI = 0	ISDB-Tsb partial reception waveform mainly used for simplified BER measurement. The waveform length is four frames.
ISDBTsb_QPSK_2_3	Transmission of concatenated eight segments consisting of Seg#1 to Seg#5 (1-segment format) and Seg#6 to Seg#8 (3-segment format) Mode: 3, GI: 1/8 Layer A: QPSK, CR = 2/3, TI = 0 Layer B: QPSK, CR = 2/3, TI = 0	
ISDBTsb_16QAM_1_2	Transmission of concatenated eight segments consisting of Seg#1 to Seg#5 (1-segment format) and Seg#6 to Seg#8 (3-segment format) Mode: 3, GI: 1/8 Layer A: 16QAM, CR = 1/2, TI = 0 Layer B: 16QAM, CR = 1/2, TI = 0	

Table 3.6-2 lists the parameters commonly used by each waveform pattern.

Table 3.6-2 Common parameters

Parameter	Setting Value
Data	PN23fix*: (Digital BS, Digital CS, CATV, ISDB-T, and ISDB-Tsb)
Sampling Rate	Digital BS: 144.3 Msps Digital CS: 147.62 Msps CATV: 42.192 Msps ISDB-T: 16.253968 Msps ISDB-Tsb: 8.12698417Msps

*: The PN sequence is not continuous between tail and head of waveform patterns.

3.6.1 Frame configuration

BS_1ch, CS_1ch, CATV_AnnexC_1ch

Digital BS, Digital CS, and CATV waveform patterns consist of continuous PN23 data, and do not have a frame configuration as shown below.

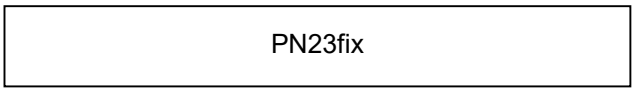


Figure 3.6.1-1 Data Configuration of Digital BS, Digital CS and CATV waveform patterns

ISDBT_1layer_1ch, ISDBT_2layer_1ch

ISDB-T waveform patterns are generated as shown in Figure 3.6.1-2. Table 3.6.1-1 lists the modulation parameters.

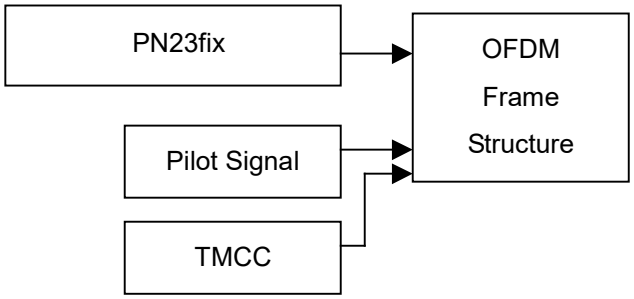


Figure 3.6.1-2 ISDB-T waveform pattern generation

Table 3.6.1-1 Modulation parameters

Pattern Name / Parameter	ISDBT_1layer_1ch	ISDBT_2layer_1ch	
Layer	Layer A	Layer A	Layer B
Mode	Mode3	Mode3	
Guard interval	1/8	1/8	
Partial reception	OFF	ON	
Emergency broadcasting	OFF	OFF	
Segment count	13	1	12
Modulation	64QAM	QPSK	64QAM

ISDBT_2layer_Coded

This waveform pattern is generated as shown below.

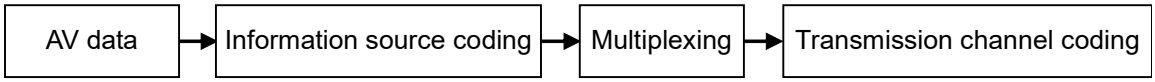


Figure 3.6.1-3 ISDB_2layer_Coded waveform pattern generation

This waveform pattern is generated through transmission channel coding in conformance with ARIB STD-B31. Table 3.6.1-2 lists the transmission channel coding parameters. This waveform pattern can be used for simplified BER measurement of the partial reception receiver.

Table 3.6.1-2 Transmission parameters for ISDBT_2layer_Coded waveform pattern

Pattern Name / Parameter	ISDBT_2layer_Coded	
Layer	Layer A	Layer B
Mode	Mode3	
Guard interval	1/8	
Partial reception	ON	
Emergency broadcasting	OFF	
Segment count	1	12
Modulation	QPSK	64QAM
Coding rate	2/3	7/8
Time interleave	2	2

ISDBT_QPSK_1_2, ISDBT_QPSK_2_3, ISDBT_16QAM_1_2, and ISDBT_QPSK_2_3_TI4

These waveform patterns are generated through transmission channel coding in conformance with ARIB STD-B31. Tables 3.6.1-3 and 3.6.1-4 list the transmission channel coding parameters for each pattern.

Table 3.6.1-3 Transmission parameters for ISDBT_QPSK_1_2 and ISDBT_QPSK_2_3 waveform patterns

Pattern Name / Parameter	ISDBT_QPSK_1_2		ISDBT_QPSK_2_3	
Layer	Layer A	Layer B	Layer A	Layer B
Mode	Mode3		Mode3	
Guard interval	1/8		1/8	
Partial reception	ON		ON	
Emergency broadcasting	OFF		OFF	
Segment count	1	12	1	12
Modulation	QPSK	64QAM	QPSK	64QAM
Coding rate	1/2	7/8	2/3	7/8
Time interleave	0	1	0	1

Table 3.6.1-4 Transmission parameters for ISDBT_16QAM_1_2 and ISDBT_QPSK_2_3_TI4 waveform patterns

Pattern Name / Parameter	ISDBT_16QAM_1_2		ISDBT_QPSK_2_3_TI4	
Layer	Layer A	Layer B	Layer A	Layer B
Mode	Mode3		Mode3	
Guard interval	1/8		1/8	
Partial reception	ON		ON	
Emergency broadcasting	OFF		OFF	
Segment count	1	12	1	12
Modulation	QPSK	64QAM	QPSK	64QAM
Coding rate	1/2	7/8	2/3	3/4
Time interleave	1	0	4	2

ISDBTsb_QPSK_1_2, ISDBTsb_QPSK_2_3, and ISDBTsb_16QAM_1_2

These waveform patterns are generated through transmission channel coding in conformance with ARIB STD-B29. Tables 3.6.1-5 to 3.6.1-7 list the transmission channel coding parameters for each pattern. Each of these waveform patterns consists of eight segments. Seg#1 to Seg#5 are 1-segment format and Seg#6 to Seg#8 are 3-segment format. These segments are concatenated and transmitted.

Table 3.6.1-5 Transmission parameters for ISDBTsb_QPSK_1_2 waveform pattern

Pattern Name / Parameter	ISDBTsb_QPSK_1_2						
Segment No.	Seg#1	Seg#2	Seg#3	Seg#4	Seg#5	Seg#6 to Seg#8	
Layer	Layer A	Layer A	Layer A	Layer A	Layer A	Layer A	Layer B
Mode	Mode3						
Guard interval	1/8						
Partial reception	OFF	OFF	OFF	OFF	OFF	ON	OFF
Emergency broadcasting	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Modulation	QPSK	QPSK	QPSK	QPSK	QPSK	QPSK	QPSK
Coding rate	1/2	1/2	1/2	1/2	1/2	1/2	1/2
Time interleave	0	0	0	0	0	0	0
Subchannel number at segment center	5	8	11	14	17	20/23/26	

Table 3.6.1-6 Transmission parameters for ISDBTsb_QPSK_2_3 waveform pattern

Pattern Name / Parameter	ISDBTsb_QPSK_2_3						
Segment No.	Seg#1	Seg#2	Seg#3	Seg#4	Seg#5	Seg#6 to Seg#8	
Layer	Layer A	Layer A	Layer A	Layer A	Layer A	Layer A	Layer B
Mode	Mode3						
Guard interval	1/8						
Partial reception	OFF	OFF	OFF	OFF	OFF	ON	OFF
Emergency broadcasting	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Modulation	QPSK	QPSK	QPSK	QPSK	QPSK	QPSK	QPSK
Coding rate	2/3	2/3	2/3	2/3	2/3	2/3	2/3
Time interleave	0	0	0	0	0	0	0
Subchannel number at segment center	5	8	11	14	17	20/23/26	

Table 3.6.1-7 Transmission parameters for ISDBTsb_16QAM_1_2 waveform pattern

Pattern Name / Parameter	ISDBTsb_16QAM_1_2						
Segment No.	Seg#1	Seg#2	Seg#3	Seg#4	Seg#5	Seg#6 to Seg#8	
Layer	Layer A	Layer A	Layer A	Layer A	Layer A	Layer A	Layer B
Mode	Mode3						
Guard interval	1/8						
Partial reception	OFF	OFF	OFF	OFF	OFF	ON	OFF
Emergency broadcasting	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Modulation	16QAM	16QAM	16QAM	16QAM	16QAM	16QAM	16QAM
Coding rate	1/2	1/2	1/2	1/2	1/2	1/2	1/2
Time interleave	0	0	0	0	0	0	0
Subchannel number at segment center	5	8	11	14	17	20/23/26	

3.7 *Bluetooth*® Waveform Pattern

Table 3.7-1 lists the provided *Bluetooth* waveform patterns.

Table 3.7-1 List of *Bluetooth* waveform patterns

Waveform Pattern Name	Data Rate (Mbits/s)	Modulation for Payload	Filter	Packet Type	Dirty, FM*8
DH1*1	1	GFSK*4	Gaussian*5	DH1	-
DH3*1	1	GFSK*4	Gaussian*5	DH3	-
DH5*1	1	GFSK*4	Gaussian*5	DH5	-
DH3_3SlotOff*1	1	GFSK*4	Gaussian*5	DH3	-
DH5_5SlotOff*1	1	GFSK*4	Gaussian*5	DH5	-
POLL	1	GFSK*4	Gaussian*5	POLL	-
2-DH1*1	2	π/4-DQPSK	Root Nyquist*6	2-DH1	-
2-DH3*1	2	π/4-DQPSK	Root Nyquist*6	2-DH3	-
2-DH5*1	2	π/4-DQPSK	Root Nyquist*6	2-DH5	-
2-DH3_3SlotOff*1	2	π/4-DQPSK	Root Nyquist*6	2-DH3	-
2-DH5_5SlotOff*1	2	π/4-DQPSK	Root Nyquist*6	2-DH5	-
3-DH1*1	3	8-DPSK	Root Nyquist*6	3-DH1	-
3-DH3*1	3	8-DPSK	Root Nyquist*6	3-DH3	-
3-DH5*1	3	8-DPSK	Root Nyquist*6	3-DH5	-
3-DH3_3SlotOff*1	3	8-DPSK	Root Nyquist*6	3-DH3	-
3-DH5_5SlotOff*1	3	8-DPSK	Root Nyquist*6	3-DH5	-
GFSK-PN9*2	1	GFSK*4	Gaussian*5	No packet format	-
GFSK-PN15*3	1	GFSK*4	Gaussian*5	No packet format	-
PI_4_DQPSK-PN9*2	2	π /4-DQPSK	Root Nyquist*6	No packet format	-
PI_4_DQPSK-PN15*3	2	π /4-DQPSK	Root Nyquist*6	No packet format	-
8DPSK-PN9*2	3	8DPSK	Root Nyquist*6	No packet format	-
8DPSK-PN15*3	3	8DPSK	Root Nyquist*6	No packet format	-

Table 3.7-1 List of *Bluetooth* waveform patterns (Continued)

Waveform Pattern Name	Data Rate (Mbits/s)	Modulation for Payload	Filter	Packet Type	Dirty, FM*8
DH1_dirty*1	1	GFSK*4	Gaussian*5	DH1	Dirty
DH3_dirty*1	1	GFSK*4	Gaussian*5	DH3	Dirty
DH5_dirty*1	1	GFSK*4	Gaussian*5	DH5	Dirty
2-DH1_dirty*1	2	π/4-DQPSK	Root Nyquist*6	2-DH1	Dirty
2-DH3_dirty*1	2	π/4-DQPSK	Root Nyquist*6	2-DH3	Dirty
2-DH5_dirty*1	2	π/4-DQPSK	Root Nyquist*6	2-DH5	Dirty
3-DH1_dirty*1	3	8-DPSK	Root Nyquist*6	3-DH1	Dirty
3-DH3_dirty*1	3	8-DPSK	Root Nyquist*6	3-DH3	Dirty
3-DH5_dirty*1	3	8-DPSK	Root Nyquist*6	3-DH5	Dirty
DH1_dirty_with FM*1	1	GFSK*4	Gaussian*5	DH1	Dirty, FM
DH3_dirty_with FM*1	1	GFSK*4	Gaussian*5	DH3	Dirty, FM
DH5_dirty_with FM*1	1	GFSK*4	Gaussian*5	DH5	Dirty, FM
2-DH1_dirty_with FM*1	2	π/4-DQPSK	Root Nyquist*6	2-DH1	Dirty, FM
2-DH3_dirty_with FM*1	2	π/4-DQPSK	Root Nyquist*6	2-DH3	Dirty, FM
2-DH5_dirty_with FM*1	2	π/4-DQPSK	Root Nyquist*6	2-DH5	Dirty, FM
3-DH1_dirty_with FM*1	3	8-DPSK	Root Nyquist*6	3-DH1	Dirty, FM
3-DH3_dirty_with FM*1	3	8-DPSK	Root Nyquist*6	3-DH3	Dirty, FM
3-DH5_dirty_with FM*1	3	8-DPSK	Root Nyquist*6	3-DH5	Dirty, FM
BLE*1	1	GFSK*9	Gaussian*5	BLE Reference Signal	-
BLE_dirty*1	1	GFSK*9	Gaussian*5	BLE Reference Signal	Dirty
BLE_Dirty_with FM*1	1	GFSK*9	Gaussian*5	BLE Reference Signal	Dirty, FM
BLE_CRC_corrupted*1 *7	1	GFSK*9	Gaussian*5	BLE Reference Signal	-
GMSK-PN15_BLE*3	1	GFSK*9	Gaussian*5	No packet format	-

*1: PN9 data is inserted into the payload field.

*2: PN9 data is inserted into all of the non-packet format fields.

*3: PN15 data is inserted into all of the non-packet format fields.

*4: Modulation index = 0.32

*5: Bandwidth Time (BT) = 0.5

*6: Roll-off rate β = 0.4

*7: Use in RF-PHY.TS/4.0.0 RCV-LE/CA/07/C (PER Report Integrity) with intentional CRC errors in every other packet is assumed.

*8: Refer to Section 3.7.4.

*9: Modulation index = 0.5

Figure 3.7-1 shows a timing chart of the waveform patterns with packet formats.

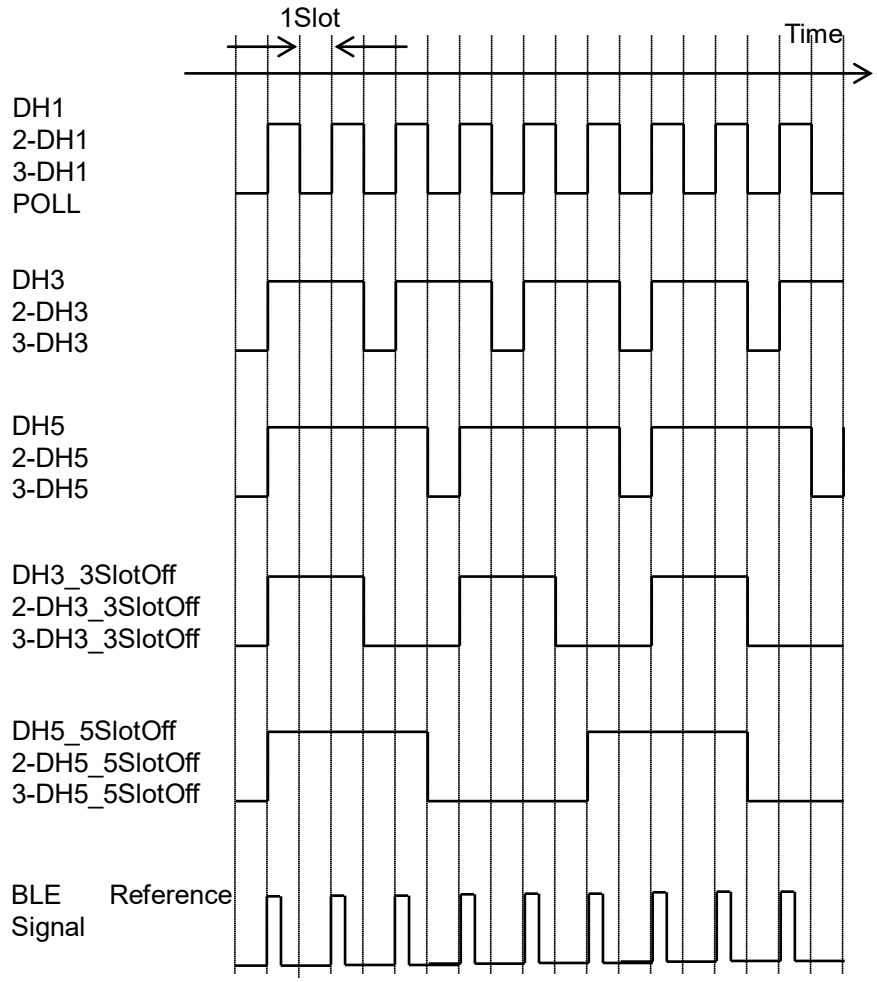


Figure 3.7-1 Timing chart of waveform patterns with packet format

When a *Bluetooth* waveform pattern having a packet configuration is output, a marker signal shown in Table 3.7-2 is output from the AUX connector on the rear panel.

Table 3.7-2 Marker output data

Marker Signal	Output Data
Marker 1	Packet Clock
Marker 2	RF Gate
Marker 3	–

3.7.1 Basic Rate packet configuration

When the DH1, DH3, DH5, DH3_3SlotOff, or DH5_5SlotOff waveform pattern is selected, data is output in the format shown in Figure 3.7.1-1. Table 3.7.1-1 lists the data length of the payload body.

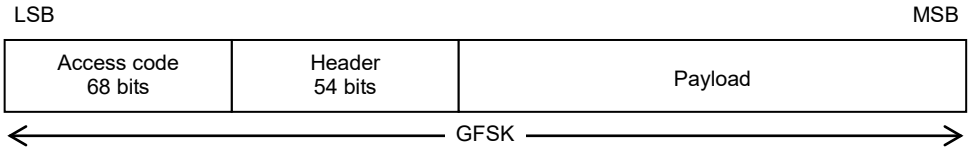


Figure 3.7.1-1 Basic Rate packet configuration

Table 3.7.1-1 BR payload body length

Packet Type	Payload Body (bytes)
DH1	27
DH3	183
DH5	339
POLL	None

3.7.1.1 Access code

The configuration of the access code field is shown below. For Sync Word, a value calculated with LAP = $9E8B33_H$, conforming to Sync Word Definition specified in Section 6.3.3 of Bluetooth specification Version 2.0 + EDR [vol3], is assigned. Preamble and trailer values are determined by the Sync Word value, conforming to the specifications defined in Sections 6.3.2 and 6.3.4 of Bluetooth specification Version 2.0 + EDR [vol3], respectively.

Access code

P	SW	T

P: Preamble 5_H (4 bits)
SW: Sync Word $475C58CC73345E72_H$ (64 bits)
T: Trailer A_H (4 bits)

3.7.1.2 Header

The configuration of the header field is shown below. For HEC, a value calculated conforming to HEC Generation specified in Section 7.1.1 of Bluetooth specification Version 2.0 + EDR [vol3] is assigned. Also, this 18-bit data becomes 54-bit data with FEC CODE: RATE 1/3, which is specified in Section 7.4 of Bluetooth specification Version 2.0 + EDR [vol3].

Header

LT_ADDR	TYPE	FLOW	ARQN	SEQN	HEC

LT_ADDR: Logical transport address 0_H (3 bits)
FLOW: Flow control 1_H (1 bit)
ARQN: Acknowledge indication 1_H (1 bit)
SEQN: Sequence number Alternate between 1_H and 0_H (1 bit)
HEC: Header error check (18 bits)

Table 3.7.1.2-1 Value of TYPE

Packet Type	Type Code
DH1	4_H
DH3	B_H
DH5	F_H

3.7.1.3 Payload

The configuration of the payload field is shown below. For CRC, a value calculated with UAP = 00_H, conforming to CRC Generation specified in Section 7.1.2 of Bluetooth specification Version 2.0 + EDR [vol3] is assigned.

Payload

LLID	FLOW	LENGTH	UNDEFINED	PAYLOAD BODY	CRC

LLID: Logical link indication 2_H (2 bits)
FLOW: Flow indication 1_H (1 bit)
LENGTH: Payload length indicator See Table 3.7.1.3-1.

Table 3.7.1.3-1 Value of LENGTH for BR packet

Packet Type	Data Length	Value
DH1	5 bits	27
DH3	9 bits	183
DH5	9 bits	339

3.7.2 Enhanced Data Rate packet configuration

When the 2-DH1, 2-DH3, 2-DH5, 3-DH1, 3-DH3, 3-DH5, 2-DH3_3SlotOff, 2-DH5_5SlotOff, 3-DH3_3SlotOff, or 3-DH5_5SlotOff waveform pattern is selected, data is output in the format shown in Figure 3.7.2-1. Table 3.7.2-1 lists the number of bits of Payload Body.

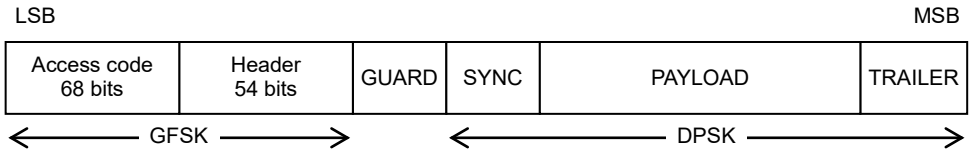


Figure 3.7.2-1 Enhanced Data Rate packet configuration

Table 3.7.2-1 EDR payload body length

Packet Type	Payload Body (bytes)
2-DH1	54
2-DH3	367
2-DH5	679
3-DH1	83
3-DH3	552
3-DH5	1021

3.7.2.1 Access code

The configuration of the access code field is the same as described in Section 3.7.1.1.

3.7.2.2 Header

The configuration of the header field is the same as described in Section 3.7.1.2. Table 3.7.2.2-1 lists the values assigned to TYPE.

Table 3.7.2.2-1 EDR output signal parameters

Packet Type	Type Code
2-DH1	4_H
2-DH3	B_H
2-DH5	F_H
3-DH1	4_H
3-DH3	B_H
3-DH5	F_H

3.7.2.3 Payload

The configuration of the payload field is the same as described in Section 3.7.1.3. Table 3.7.2.3-1 lists the data length and setting value of LENGTH.

Table 3.7.2.3-1 Value LENGTH for EDR packet

Packet Type	Data Length	Value
2-DH1	5 bits	54
2-DH3	10 bits	366
2-DH5	10 bits	678
3-DH1	5 bits	81
3-DH3	10 bits	549
3-DH5	10 bits	1017

3.7.2.4 Synchronous sequence

The synchronous sequence value for each EDR packet is shown below. Setting "0" to the head of a synchronous sequence initializes phases to 0 radians.

2-DH1, 2-DH3, and 2-DH5 packets: $0777D5_H$ (22 bits)
3-DH1, 3-DH3, and 3-DH5 packets: $0175D7E92_H$ (33 bits)

3.7.2.5 Trailer

The trailer value for each EDR packet is shown below.

2-DH1, 2-DH3, and 2-DH5 packets: 0_H (4 bits)
3-DH1, 3-DH3, and 3-DH5 packets: 00_H (6 bits)

3.7.3 Packet configuration for BLE

When waveform patterns of BLE, BLE_dirty, BLE_Dirty_withFM, and BLE_CRC_corrupted of Bluetooth Low Energy (BLE) waveform pattern are selected, the data is output in the format shown in Figure 3.7.3-1. Table 3.7.3-1 shows the payload body data length. Packet Interval is 1. 25 ms.

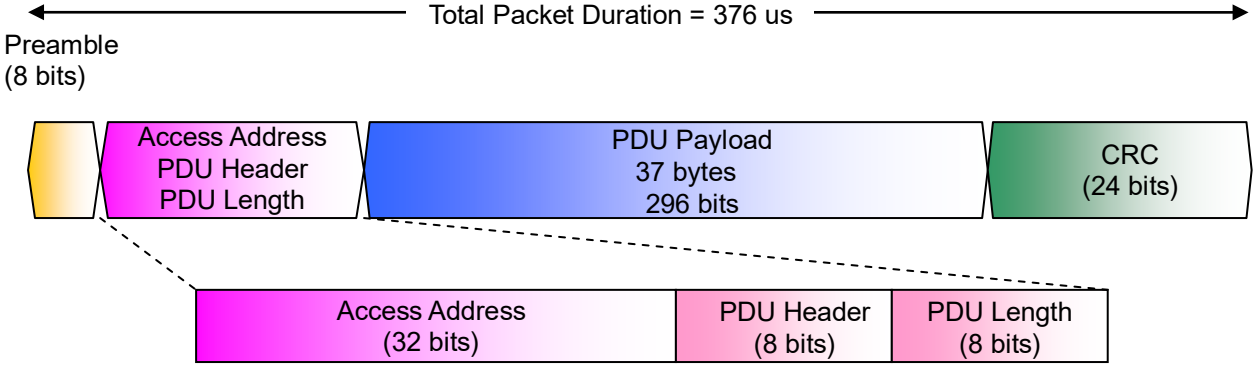


Figure 3.7.3-1 Packet Configuration for BLE Waveform

Table 3.7.3-1 BLE Payload Body Length

Packet type	Payload Body (bytes)
BLE Reference Signal	37

3.7.3.1 Preamble

Preamble is 8 bits of either one of 10101010 or 01010101 depending on LSB of Access Address as specified in Section 2.1.1, BLUETOOTH SPECIFICATION Version 4.0 [vol 6]. Because Access Address of BLE, BLE_dirty, BLE_Dirty_withFM, and BLE_CRC_corrupted is $0x94826E8E_H$, when LSB of Access Address is 1, the preamble is "10101010" (In this case, the first bit is assumed to be LSB due to the transmission order).

When LSB of Access Address is 1: 10101010b (8 bits)
When LSB of Access Address is 0: 01010101b (8 bits)

3.7.3.2 Access Address

Access Address is a bit string of 32 bits as specified in Section 2.1.2, BLUETOOTH SPECIFICATION Version 4.0 [vol 6]. Access Address of BLE, BLE_dirty, BLE_Dirty_withFM, and BLE_CRC_corrupted is $0x94826E8E_H$.

3.7.3.3 PDU Header, PDU Length

PDU Header and PDU Length are bit strings of 8 bits as specified in Section 2.4, BLUETOOTH SPECIFICATION Version 4.0 [vol 6] and Section 7.2.4, RF-PHY.TS/4.0.0 respectively.

3.7.3.4 PDU Payload,CRC

PDU Payload is payload data of 6 to 37 bytes as specified in Section 2.4, BLUETOOTH SPECIFICATION Version 4.0 [vol 6]. Payload data of BLE, BLE_dirty, BLE_Dirty_withFM, and BLE_CRC_corrupted is 37 bytes.In addition, CRC is 3 bytes.

3.7.4 Dirty Transmitter Signal

Dirty Transmitter Signal is specified as a signal used for a reception test in Section 5.1.18, Bluetooth Test Specification v1.2/2.0/2.0 + EDR/2.1/2.1 + EDR/3.0/3.0 + HS and Section 6.3.1, RF-PHY.TS/4.0.0. This Dirty Transmitter Signal changes the frequency offset, modulation index, and symbol timing error with every 50 packets. 10 combinations of these three parameters are specified, and outputs of Test Run 1 to 10 are repeated. Furthermore, the frequency drift of output signals is specified for the Dirty Transmitter Signal. The waveform patterns "Dirty" in Table 3.11-1 are waveform patterns with the addition of the frequency offset, modulation index fluctuation, and symbol timing error. In addition, the waveform patterns "Dirty, FM" are signals with the addition of the frequency offset, modulation index fluctuation, symbol timing error, and frequency drift.

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3.8 GPS Waveform Pattern

Table 3.8-1 lists the provided GPS waveform patterns.

Table 3.8-1 List of GPS waveform patterns

Waveform Pattern Name	Main Use	Data Summary
TLM	Sensitivity test	Consists of TLM, HOW, and default navigation data, formatted according to the subframe configuration that is prescribed in GLOBAL POSITIONING SYSTEM STANDARD POSITIONING SERVICE SIGNAL SPECIFICATION.
PN9	BER measurement	Consecutive PN9 data, not configured in a subframe format
PARITY	Parity detection	Configured in the Word format that is prescribed in GLOBAL POSITIONING SYSTEM STANDARD POSITIONING SERVICE SIGNAL SPECIFICATION. One Word consists of 24-bit PN9fix data and 6-bit parity bit data.
TLM_PARITY*1	Sensitivity test	Consists of TLM, HOW, and Nav Data, formatted according to the subframe configuration that is prescribed in GLOBAL POSITIONING SYSTEM STANDARD POSITIONING SERVICE SIGNAL SPECIFICATION. Random data is inserted into the Nav Data part of Word3 to Word10. One period is configured with 5 subframes.

*1: To use this waveform pattern on MS2830A or MS2840A, ARB Memory Upgrade 256 Msamples (option 027) is required.

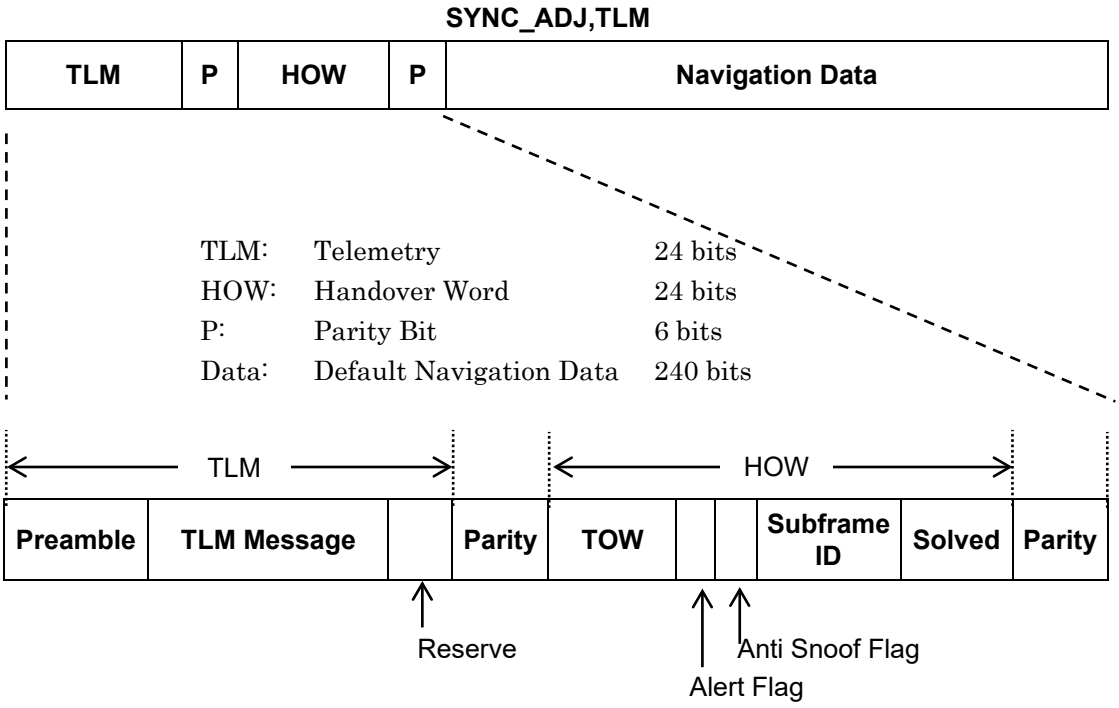
When outputting each TLM and PARITY waveform pattern, marker signals listed in the following table are output from the AUX connector at the rear panel of MS2690/MS2691/MS2692A, MS2830A or MS2840A.

Table 3.8-2 Marker output data and IQ output level

Marker Signal	Output Data
Marker1	Subframe Clock
Marker2	RF Gate
Marker3	——

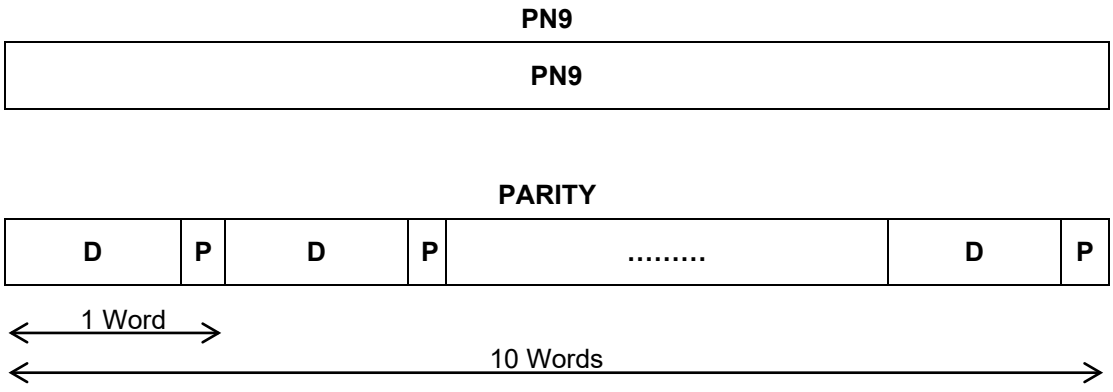
3.8.1 Waveform format

The following figures show the formats of the waveforms listed in Table 3.8-1 above. Each data is spread by the C/A code with Satellite ID Number 1. See Figure 3.8.1-1 for the C/A code generation.



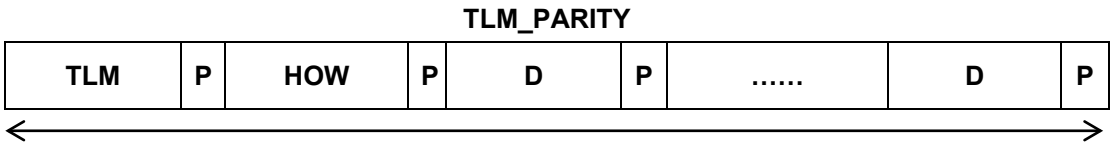
Preamble: $8B_H$ (8 bits)
TLM Message: 00_H (14 bits)
Reserved: 3_H (2 bits)
TOW (Time of Week): 00000_H (17 bits)
Alert Flag: 0_H (1 bit)
Anti Snoof Flag: 0_H (1 bit)
Subframe ID: 1_H (3 bits)
Solved: 1_H (2 bits)
Parity Bit: Parity Bit (6 bits)

Figure 3.8.1-1 Waveform format of SYNC_ADJ, TLM



D: Data 24 bits
P: Parity Bit 6 bits
PN9fix data is allocated to the Data part. Adjacent Word PN data is contiguous but the PN data is discontiguous at the 10th Word and the 1st Word of the next cycle.

Figure 3.8.1-2 Waveform format of PN9,PARITY



TLM: Telemetry 24 bits
HOW: Handover Word 24 bits
D: Data 24 bits
P: Parity Bit 6 bits
Random data is assigned to Data parts.

Figure 3.8.1-3 Waveform format of TLM_PARITY

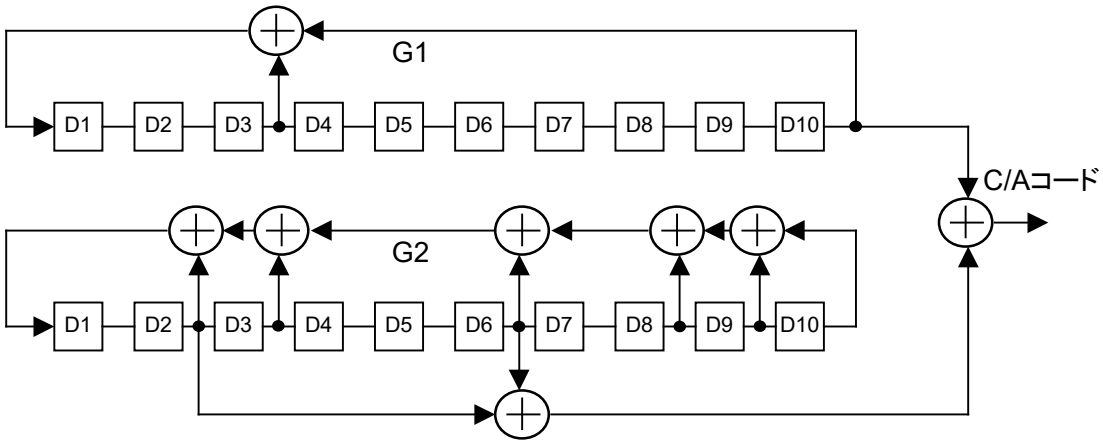


Figure 3.8.1-4 C/A code generation

3.9 GLONASS Waveform Pattern

The GLONASS waveform patterns shown in Table 3.9-1 are provided.

Table 3.9-1 GLONASS waveform patterns

Waveform Pattern Name	Main Use	Data Summary
15String _PN9	Sensitivity test Check bit Detection	It has String Navigation bit structure specified in GLOBAL NAVIGATION SATELLITE SYSTEM INTERFACE CONTROL DOCUMENT.
15String _Message	Sensitivity test Check bit Detection	It has String Navigation bit structure specified in GLOBAL NAVIGATION SATELLITE SYSTEM INTERFACE CONTROL DOCUMENT.
GLONASS_PN9	BER measurement	Consecutive PN9 data, not configured in a String, Frame format

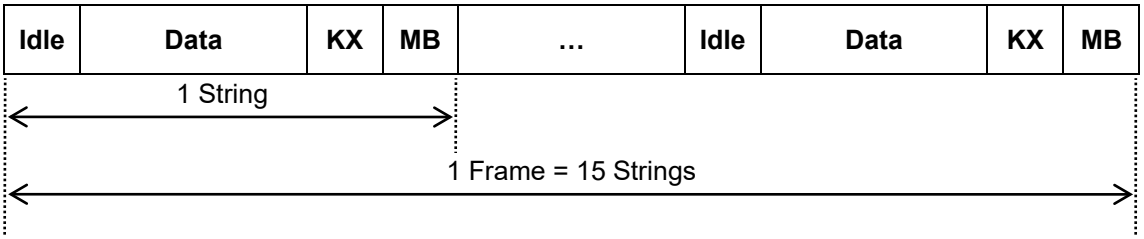
When outputting each DefaultNavData, PARITY and ENC waveform pattern, marker signals listed in the following table are output from the AUX connector at the rear panel of MS2690/MS2691/MS2692A, MS2830A or MS2840A.

Table 3.9-2 Marker output data and IQ output level

Marker Signal	Output Data
Marker1	Frame Clock
Marker2	String Clock
Marker3	——

3.9.1 Waveform format

The following figures show the formats of the waveforms listed in Table 3.9-1 above.

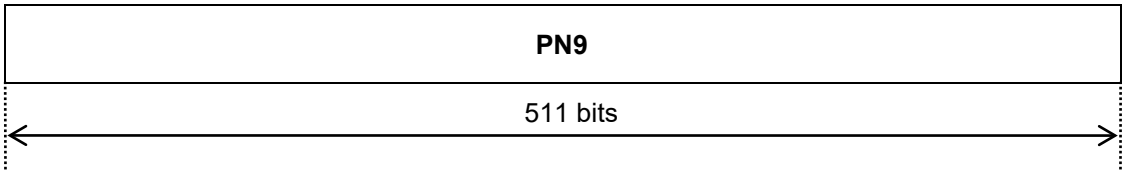


Idle:	Idle chip	1 bit	[50 bps]
Data:	Random data*1	76 bits	[50 bps]
KX:	Check bit	8 bits	[50 bps]
MB:	Time Mark*2	30 bits	[100 bps]

*1: PN9fix or Random data is assigned to Data parts.
Data is discontinuous, for it is reset every 1 frame.

*2: Generator polynomial of Time Mark
$g(x) = 1 + x^3 + x^5$

Figure 3.9.1-1 Waveform format of 15String _PN9 and 15String _Message



PN9:	PN9 data	511 bits	[100 bps]

Figure 3.9.1-2 Waveform format of GLONASS_PN9

3.10 QZSS Waveform Pattern

The QZSS waveform patterns shown in Table 3.10-1 are provided.

Table 3.10-1 List of QZSS waveform patterns

Waveform Pattern Name	Main Use	Data Summary
DefaultNavData	Sensitivity test	Consists of TLM, HOW, and default navigation data, formatted according to the subframe configuration that is prescribed in GLOBAL POSITIONING SYSTEM STANDARD POSITIONING SERVICE SIGNAL SPECIFICATION.
PARITY	Parity detection	Configured in the Word format that is prescribed in GLOBAL POSITIONING SYSTEM STANDARD POSITIONING SERVICE SIGNAL SPECIFICATION. One Word consists of 24-bit PN9fix data and 6-bit parity bit data.
ENC*1	Parity detection	Configured in the Word format that is prescribed in GLOBAL POSITIONING SYSTEM STANDARD POSITIONING SERVICE SIGNAL SPECIFICATION. One Word consists of 24-bit Random data and 6-bit parity bit data.
QZSS_PN9	BER measurement	Consecutive PN9 data, not configured in a subframe format

*1: To use this waveform pattern on MS2830A or MS2840A, ARB Memory Upgrade 256 Msamples (option 027) is required.

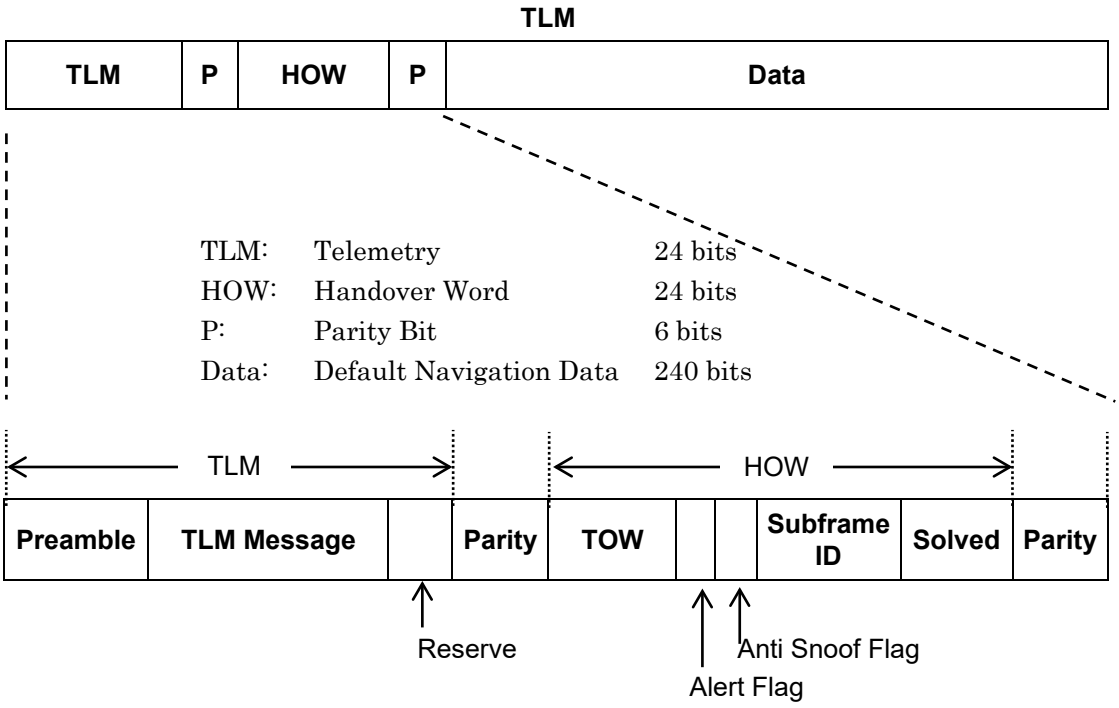
When outputting each DefaultNavData, PARITY and ENC waveform pattern, marker signals listed in the following table are output from the AUX connector at the rear panel of MS2690/MS2691/MS2692A, MS2830A or MS2840A.

Table 3.10-2 Marker output data and IQ output level

Marker Signal	Output Data
Marker1	Subframe Clock
Marker2	RF Gate
Marker3	——

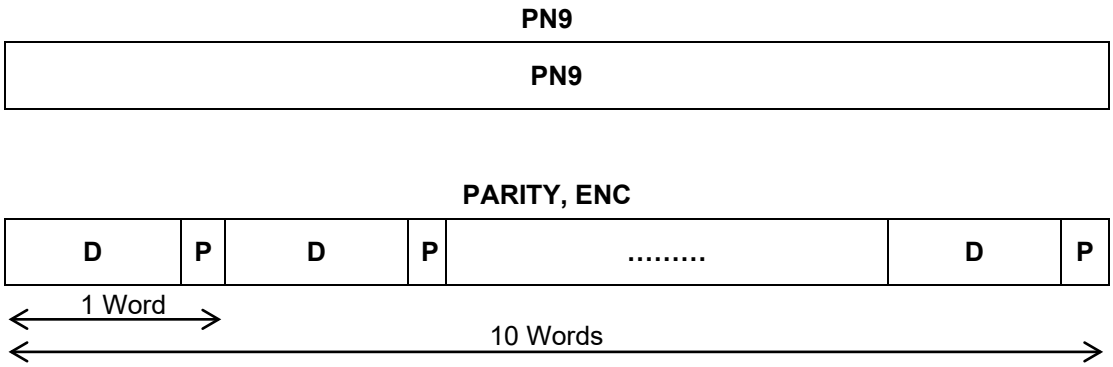
3.10.1 Waveform format

The following figures show the formats of the waveforms listed in Table 3.10-1 above. Each data is spread by the C/A code with Satellite ID Number 193. See Figure 3.10.1-3 for the C/A code generation.



Preamble:	$8B_H$ (8 bits)
TLM Message:	00_H (14 bits)
Reserved:	3_H (2 bits)
TOW (Time of Week):	00000_H (17 bits)
Alert Flag:	0_H (1 bit)
Anti Snoof Flag:	0_H (1 bit)
Subframe ID:	1_H (3 bits)
Solved:	1_H (2 bits)
Parity Bit:	Parity Bit (6 bits)

Figure 3.10.1-1 Waveform format of DefaultNavData



D: Data 24 bits
P: Parity Bit 6 bits

PN9fix data or Random data is allocated to the Data part. Adjacent Word PN data is contiguous but the PN data is discontiguous at the 10th Word and the 1st Word of the next cycle in PARITY waveform.

Figure 3.10.1-2 Waveform format of QZSS_PN9,PARITY,ENC

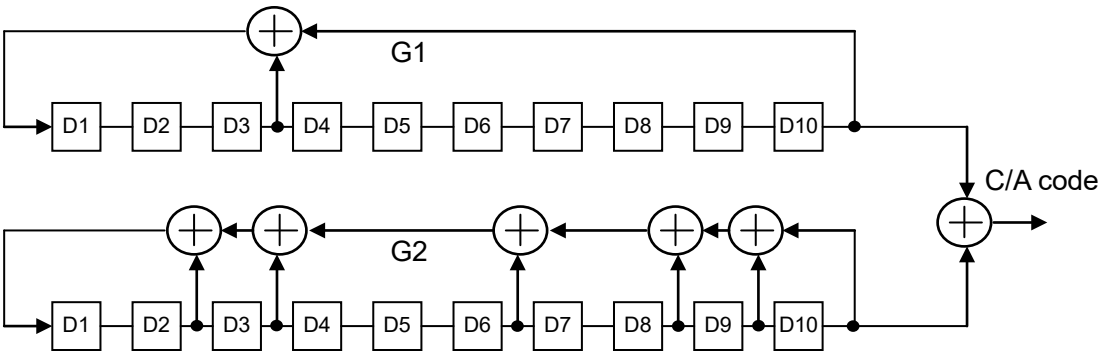


Figure 3.10.1-3 C/A code generation