Anritsu envision:ensure

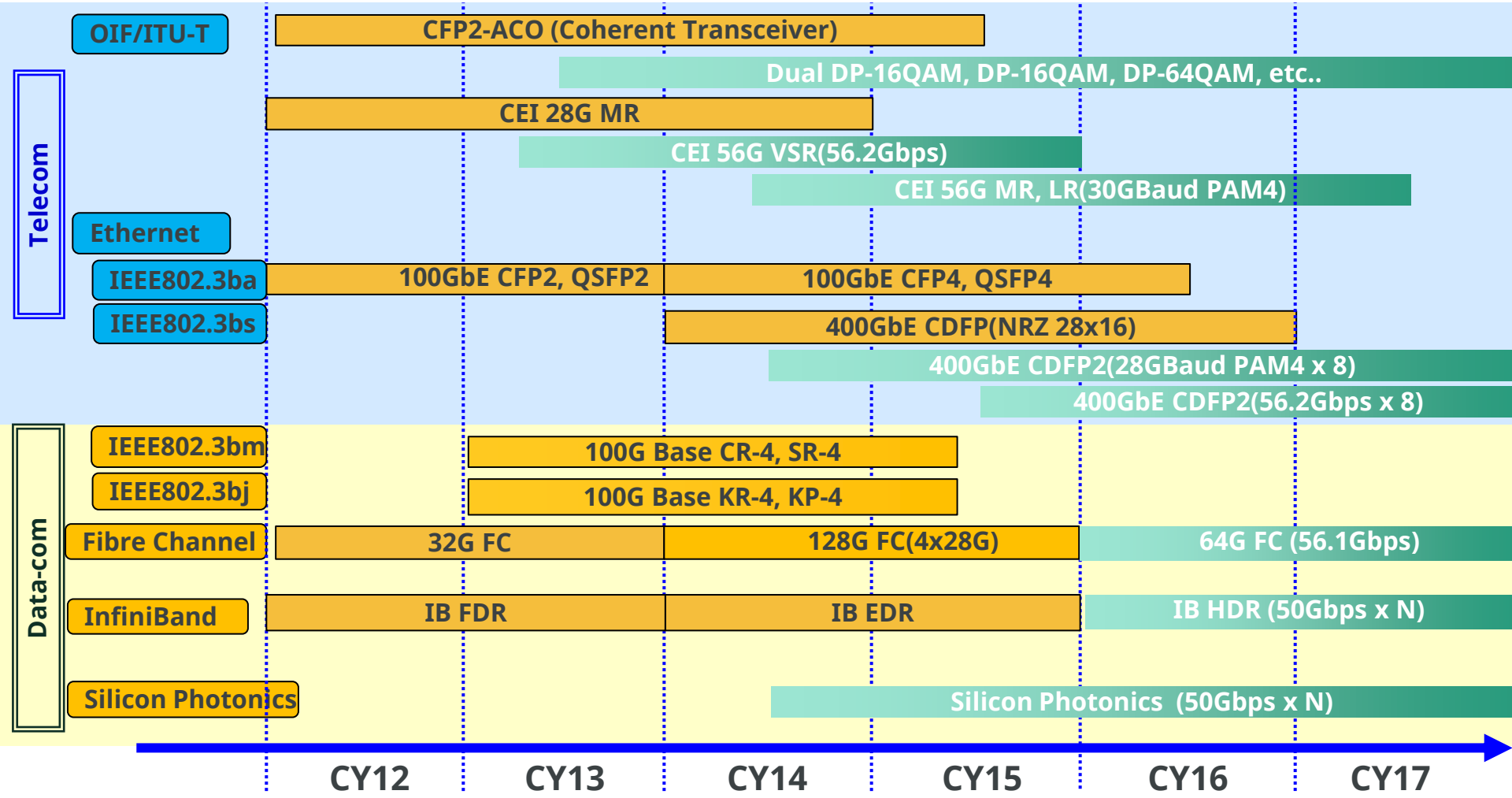
56G/64G Test Solution

56G/64G bit/s MUX MP1861A
56G/64G bit/s DEMUX MP1862A

Introduction

- Traffic volumes at data centers are exploding due to the spread of cloud computing services and new high-speed interface standards, such as 400GbE and CEI-56G, are being examined to speed-up communications between servers and network equipment.
- Jitter Tolerance of Receiver are key indices in evaluating the signal quality of PHY devices like SERDES used by these high-speed interfaces.
- The MP1861A MUX and MP1862A DEMUX are external cabinets for expanding the supported bit rate of the MP1800A from a 32G BERTs; connecting the high-quality waveform MUX and high-Rx sensitivity DEMUX to the MP1800A with installed PPG, ED and Jitter Modulation Source supports generation of NRZ Data up to 64.2 Gbit/s as well as BER measurements, injection of various jitter types, and Jitter Tolerance measurements.

Standards Trends



Increasing data traffic is leading to examination of transport methods such as PAM4 and 56G NRZ targeting 400GbE networks.

MP1861A/62A Target Standards

Market Trends 1/2

- Trends on Over 32G Market
  - ✓ IEEE802.3bs started discussions about 400GbE with a draft proposal in 2015 targeting new standards in 2016; currently the bit rate, modulation method (multiplier) and effect of the number of lanes are under discussion.

Distance / Fiber	Modulation Format
100 m/MMF (400GBASE-SR16)	MPO-16 Fiber Cable 25 Gbaud NRZ, 16ch parallel
500 m/SMF (400GBASE-DR4(T.B.D.))	100G data on each fiber 1λ 50Gbaud PAM4
2 km/SMF (400GBASE-FR8)	WDM 8λ WDM 25Gbaud PAM4
10 km/SMF (400GBASE-LR8)	WDM 8λ WDM 25Gbaud PAM4

  - ✓ Requirements for Short Distances (such as Data Centers)
    - ➢ High bit rates (56G)
    - ➢ PAM4
    - ➢ Multi-channel

Market Trends 2/2

- ✓ The OIF (Optical Internetworking Forum) is also discussing standards for interfaces between devices supporting 400GbE.

Standard	Interface	Distance	Coding	Symbol Rate Class	Target BER	Tx Jitter Components	Rx Jitter Tolerance
CEI-56G-USR	Die to Die	0 – 10mm	NRZ	39.8-57.8G	1E-15	TJ : 0.44UI BUJ : 0.25UI RJ:0.24UI	—
CEI-56G-XSR	Chip to Optical Engine	0 – 50mm	NRZ	39.8-57.8G	1E-15	TJ : 0.28UI BUJ : 0.15UI RJ:0.15UI	—
		0 – 50mm	PAM4	19.6-30.0G	1E-15	TJ : 0.48UI BUJ : 0.15UI RJ:0.15UI	—
CEI-56G-VSR	Chip to Pluggable Module	0 – 150mm	NRZ	39.0-56.2G	1E-15	TJ : 0.28UI BUJ : 0.15UI RJ:0.15UI	TSJ, UUGJ, UBHPJ
		0 – 100mm	PAM4	19.6-30.0G	1E-6	TJ : 0.28UI BUJ : 0.15UI RJ:0.15UI	SJ, UUGJ, UBHPJ
CEI-56G-MR	Chip to Chip	0 – 500mm	PAM4	19.6-30.0G	1E-6	—	SJ
CEI-56G-LR	Back plane, Cupper cable	0 – 1000mm	TBD	TBD	TBD	—	—

May be changed due to specification discussions by OIF working group.

Model Lineup 1/2

- 56G/64G bit/s MUX/DEMUX

MP1861A 56G/64G bit/s MUX

MP1862A 56G/64G bit/s DEMUX

- 56G/64G bit/s BERT Standard Configurations

MP1800A Max 6 slot

MP1861A

MP1862A

56G/64G Jitter BERT	56G/64G 2ch BERT	56G/64G 4ch BERT (2 box)	
32G PPG 2ch	32G PPG 4ch or 32G PPG 2ch x 2	32G PPG 4ch or 32G PPG 2ch x 2	32G ED 4ch or 32G ED 2ch x 2
32G ED 2ch			
Synthesizer (2 Slots)	32G ED 4ch or 32G ED 2ch x 2	32G PPG 4ch or 32GPPG 2ch x 2	32G ED 4ch or 32G ED 2ch x 2
Jitter Generator (2 Slots)	4Port Synthesizer (2 Slots)	4Port Synthesizer (2 Slots)	
64G MUX	64G MUX	64G MUX	64G DEMUX
64G DEMUX	64G MUX	64G MUX	64G DEMUX
	64G DEMUX	64G MUX	64G DEMUX
	64G DEMUX	64G MUX	64G DEMUX

Model Lineup 2/2

- MZ1854A Data Signal Combiner
- J1646A Passive Linear Equalizer 6 dB

MZ1854A Data Signal Combiner

J1646A Passive Equalizer 6dB(V connector)

- 56G/64G bit/s BERT Standard Configuration

56/64G 2ch BERT

MP1800A Max 6 slot

- 32G PPG 4ch or 32G PPG 2ch x 2
- 32G ED 4ch or 32G ED 2ch x 2
- 4Port Synthesizer (2 Slots)

MP1861A MP1862A

- 64G MUX → MZ1854A Data Signal Combiner
- 64G MUX → MZ1854A Data Signal Combiner
- 64G DEMUX ← J1646A
- 64G DEMUX ← J1646A

Features of New 64 Gbit/s Solution

Excellent Expandability: Maximizes Future-proof Investment

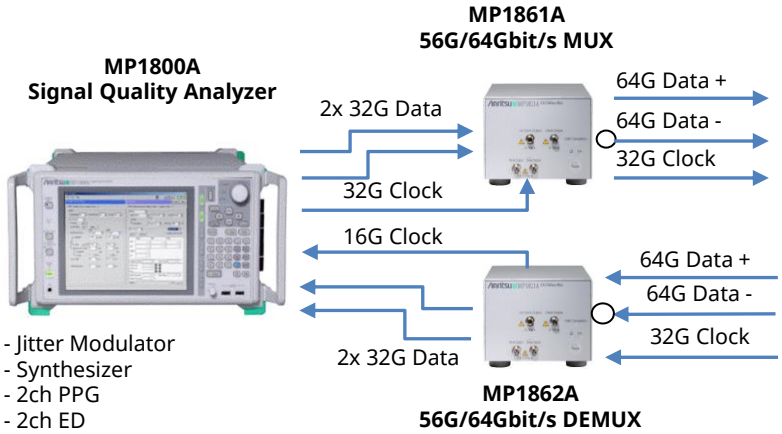
- MAX 4ch: Multi-Channel Sync pattern generation and simultaneous BER analysis

Excellent Signal Quality and Rx Sensitivity: High-accuracy Measurement of Semiconductor Chip Characteristics

- Low-intrinsic Jitter waveforms: RJ = 200 fs rms（typ.）
- Variable amplitude: 3.5 Vp-p Output max.
- High Input sensitivity: 25 mV (typ., single-end, EYE height)
- 2Tap Emphasis signal generation (57.8 Gbit/s, using MZ1854A, at MP1861A 2ch sync)
- PAM4 signal generation (43 Gbit/s BER measurement, using MZ1854A, at MP1861A 2ch sync)
- 56 Gbit/s signal EYE opening recovery (using J1646A)

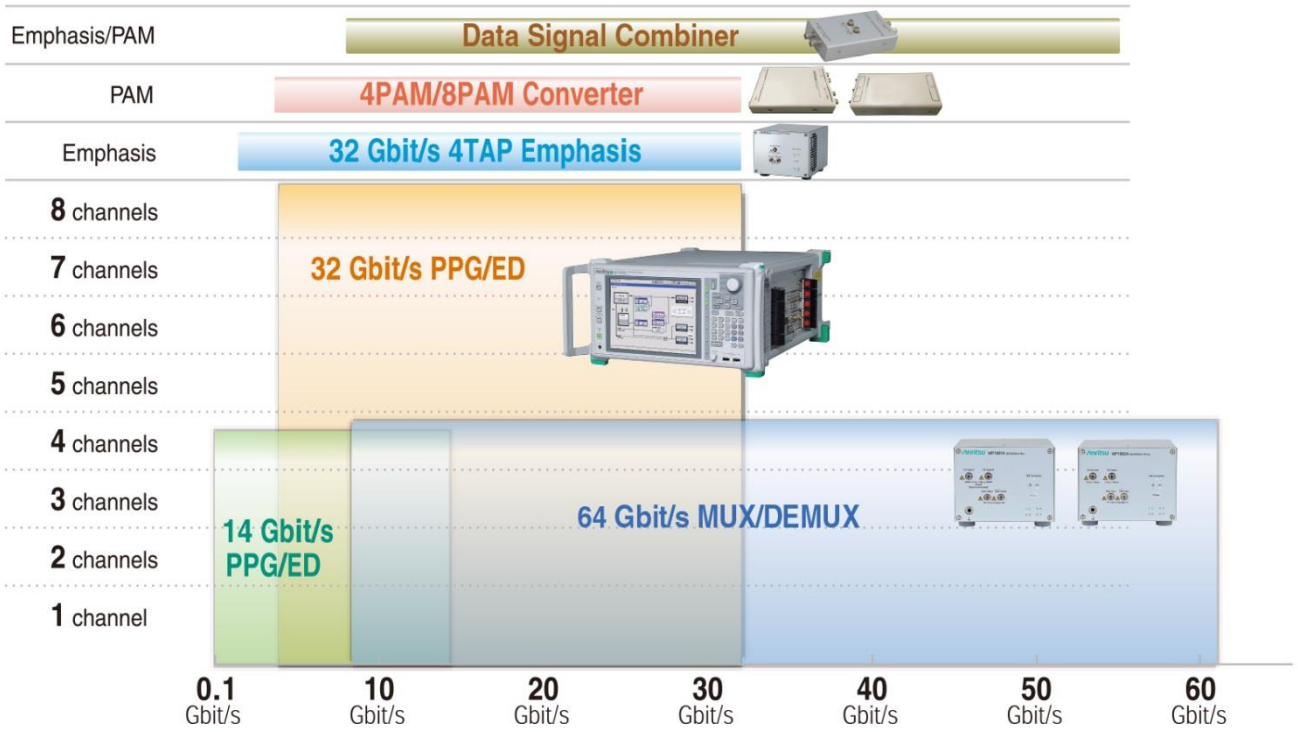
Versatile Signal Integrity Measurement Functions: Support CEI-56G and 400GbE

- TJ/DJ/RJ/Bathtub Jitter, EYE Diagram, EYE Margin auto-measurements
- Jitter Tolerance tests (using MU181500B): SJ, EJ, BUJ, SSC, Dual Tone SJ, Half Period Jitter (Even/Odd Jitter), wide amplitude SJ generation: 0.55UI @ fm 250 MHz
- Crosstalk tests using independently variable Data Skew for each channel



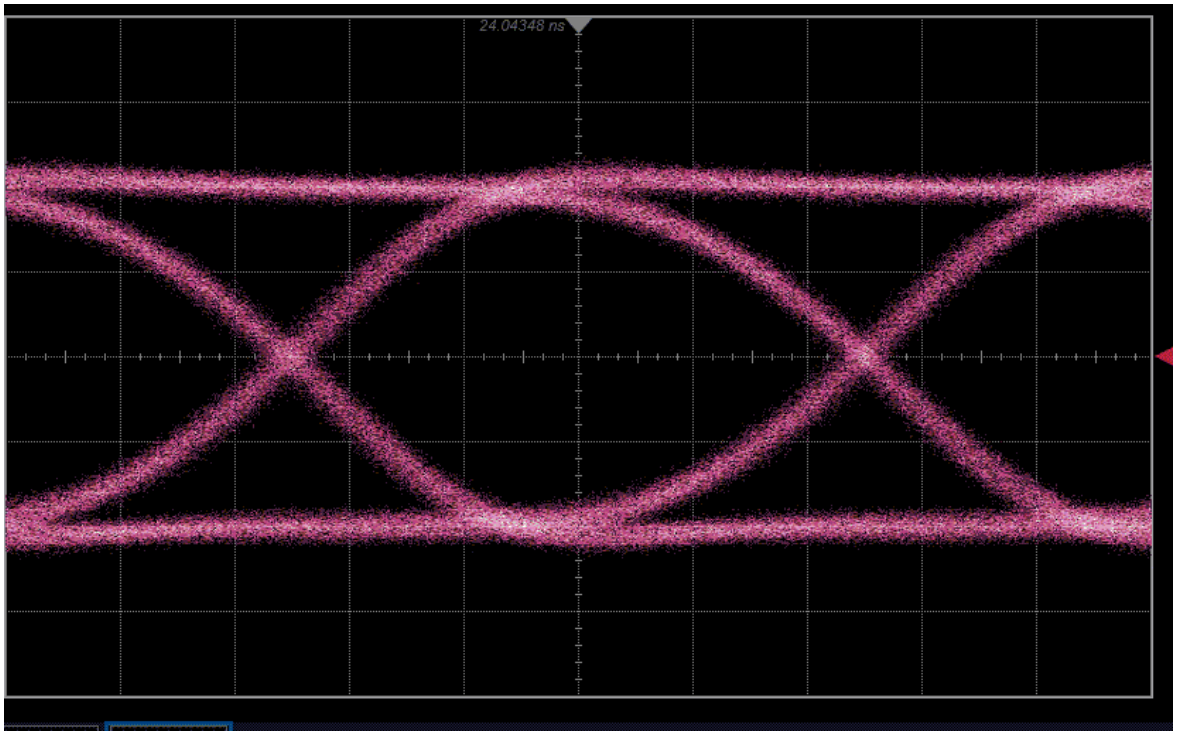
Features (1) Excellent Expandability

- Wideband bit rate from 8 Gbit/s to 64.2 Gbit/s.
- Max 4ch multi-channel 64.2 Gbit/s Sync pattern generation and simultaneous BER measurements.
- Easily expandable from 32G BERT using compact external cabinets.
- Emphasis and PAM signal generation using combination with MZ1854A.
- Supports world-first 64G signal integrity evaluation in combination with MU181500B Jitter Module.



Features (2) Excellent Signal Quality and Rx Sensitivity

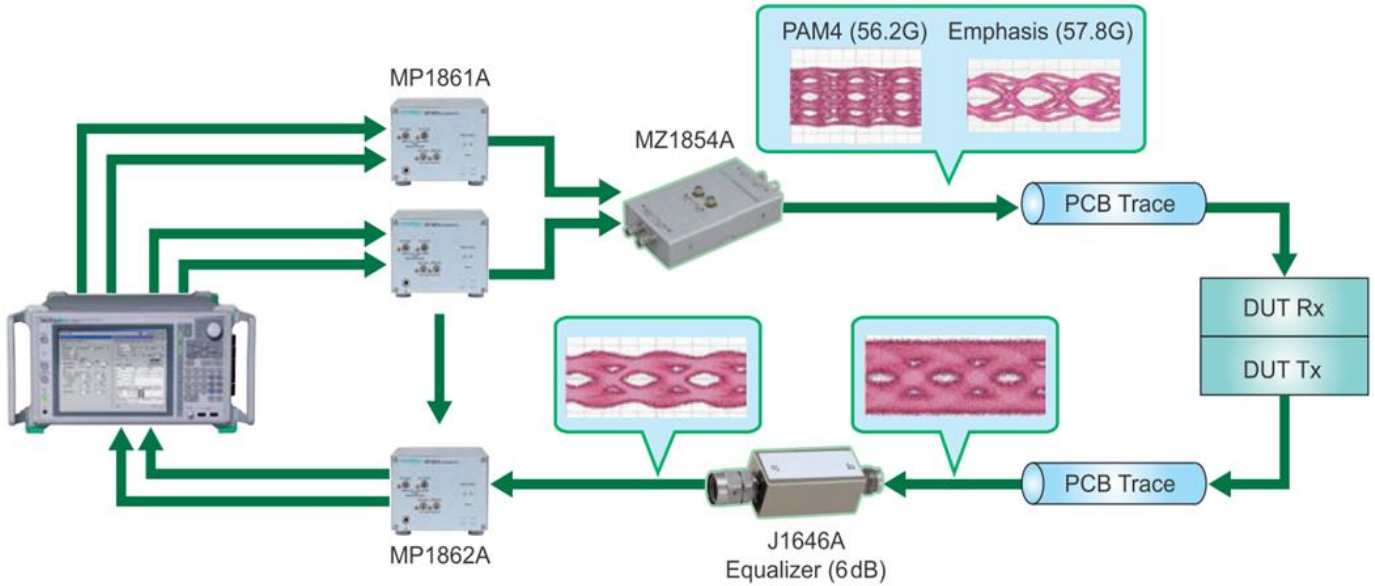
- Low-Jitter, High-quality Waveform MUX



50 Gbit/s, 3.5 Vp-p Output Waveform (MP1861A-013)

Features (3) Excellent Signal Quality and Rx Sensitivity

- High-sensitivity DEMUX
  - ✓ Sensitivity: 25 mV (typ.) (56.2 Gbit/s, single-end, EYE Height, PRBS31)
    ≤40 mV (56.2 Gbit/s, single-end, EYE Height, PRBS31)
    30 mV (typ.) (64.2 Gbit/s, single-end, EYE Height, PRBS31)
- Emphasis signal and generation
  - ✓ Combination with MZ1854A Combiner and two MP1861A units supports 2TAP Emphasis signal generation up to 57.8 Gbit/s.
- Passive equalizer
  - ✓ Inserting passive equalizer upstream of MP1862A 56/64G bit/s DEMUX supports correction of transmission path losses, recovery of EYE Opening and BER measurements of PHY devices with narrow EYE Opening, as well as Jitter Tolerance tests.

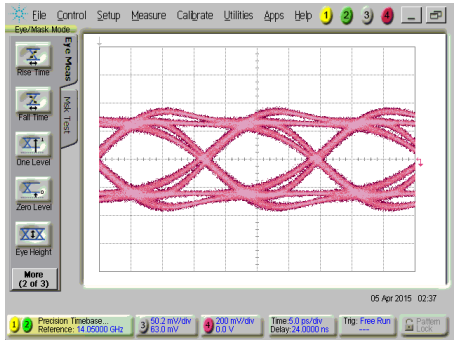


Measurement System using MP1861A, MP1862A, MZ1854A and J1646A

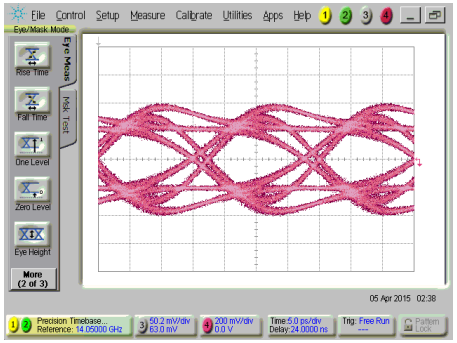
Features (4) Excellent Signal Quality and Rx Sensitivity

- MP1861A 2ch + MZ1854A Emphasis Reference Waveform: 2Tap Emphasis Output 57.8 Gbit/s optimized for CEI-56G Evaluations

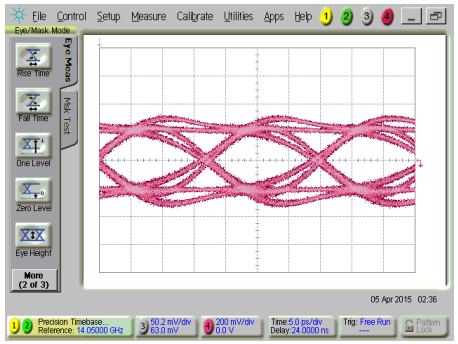
Eye Amplitude 0.48 V
Emphasis Gain 2.5 dB



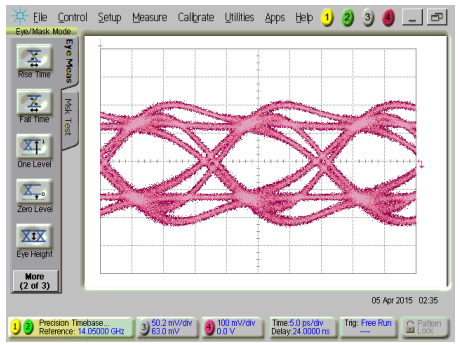
Eye Amplitude 0.40 V
Emphasis Gain 5.11 dB



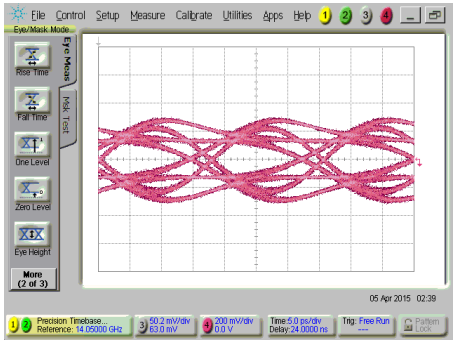
Eye Amplitude 0.40 V
Emphasis Gain 2.92 dB



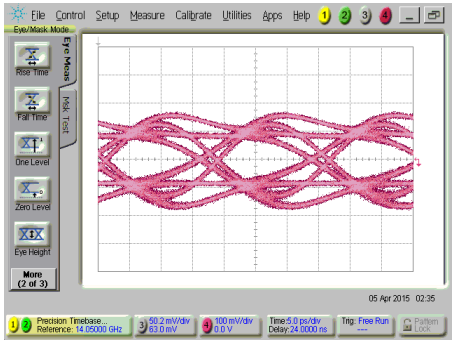
Eye Amplitude 0.23 V
Emphasis Gain 4.44 dB



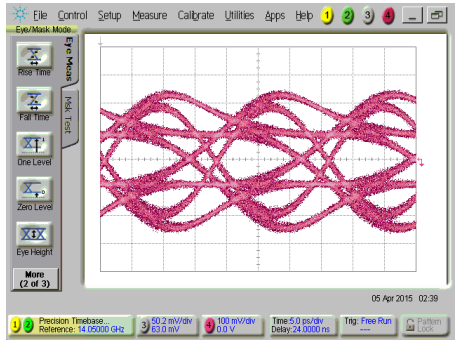
Eye Amplitude 0.24 V
Emphasis Gain 7.36 dB



Eye Amplitude 0.16 V
Emphasis Gain 6.02 dB



Eye Amplitude 0.16 V
Emphasis Gain 9.54 dB

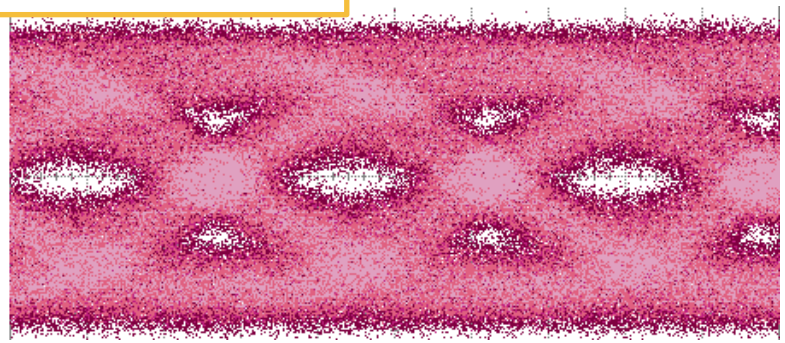


Measured with 41V-6 Attenuator and 86118A 70 GHz oscilloscope

Features (5) Excellent Signal Quality and Rx Sensitivity

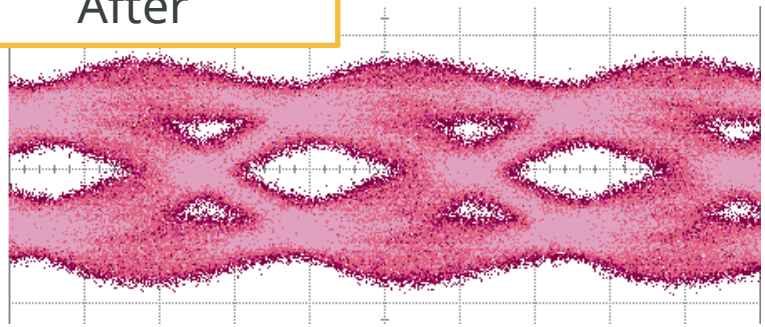
- Improved EYE opening using J1646A Passive Equalizer 6 dB: Corrects transmission path losses using 6-dB passive equalizer supporting 56 Gbit/s and improves EYE opening.

Before



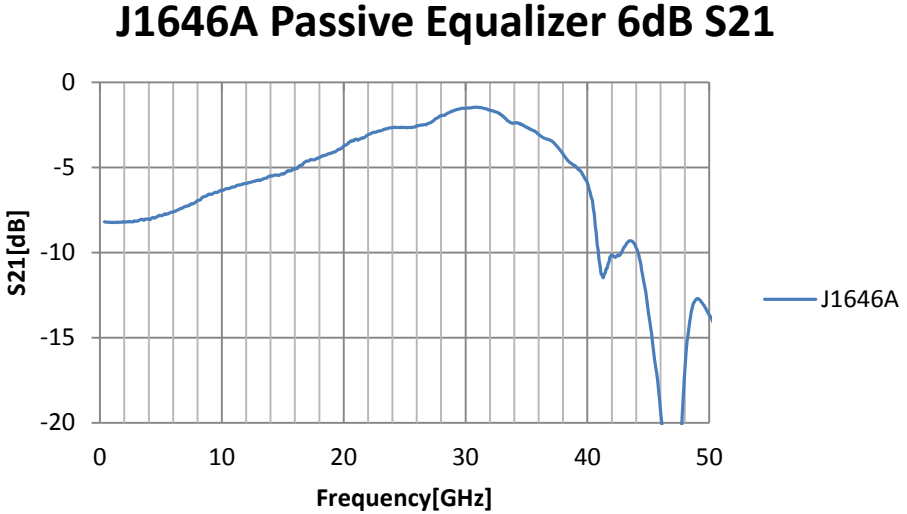
※70 mV/div

After



※50 mV/div

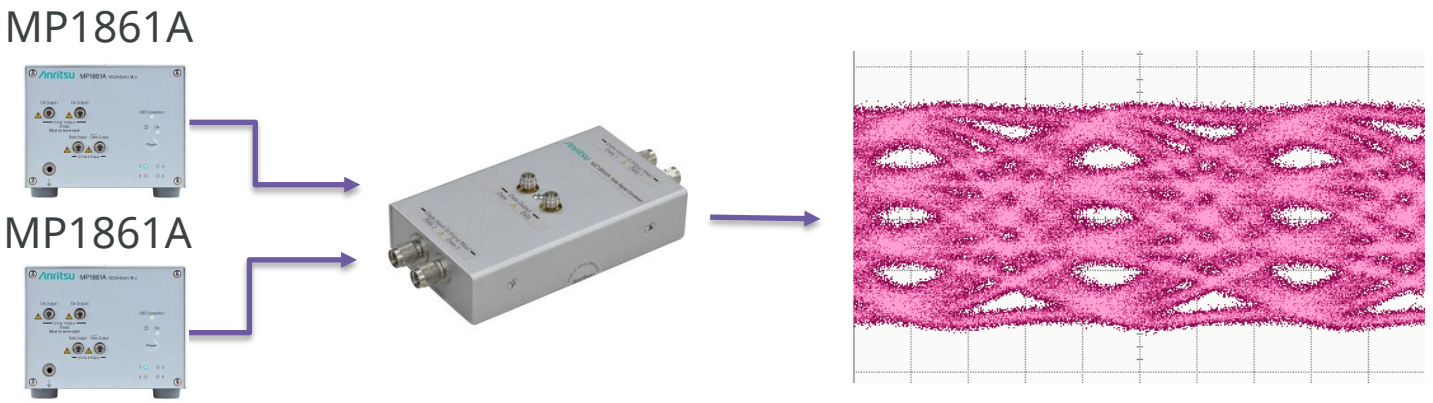
measured with 41V-6 attenuator and 86118A 70GHz oscilloscope



J1646A Frequency Characteristics (typical value)

Features (6) Excellent Signal Quality and Rx Sensitivity

- PAM4 Signal Generation and BER Measurements
  - ✓ Connecting high-quality waveforms from two MP1861A 56/64 Gbit/s MUX units via MZ1854A wideband passive type Combiner supports PAM4 signal generation.
  - ✓ PAM4 BER measurements supported up to 43 GBaud using high-sensitivity input of MP1862A 56G/64G bit/s DEMUX.

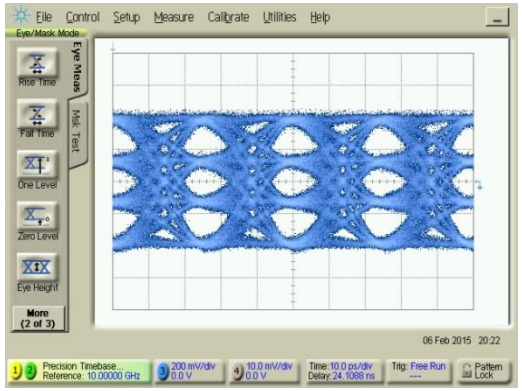


PAM4 signal waveform generation using 2ch sync, any bit delay and addition.

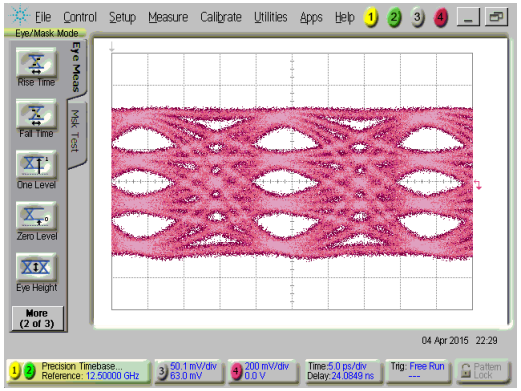
Features (7) MP1861A 2ch +MZ1854A PAM4 Reference Waveform

- PAM4 0.832 Vp-p (Data1 Input 3.5 V, Data2 Input 1.75 V)

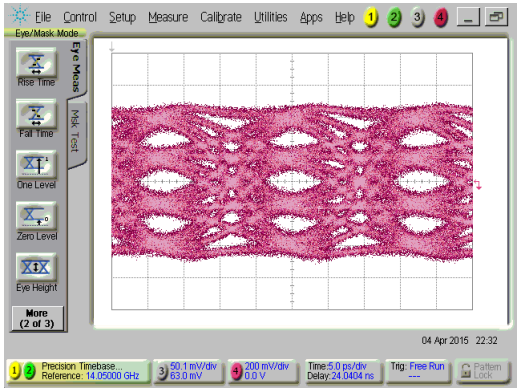
40 GBaud



50 GBaud

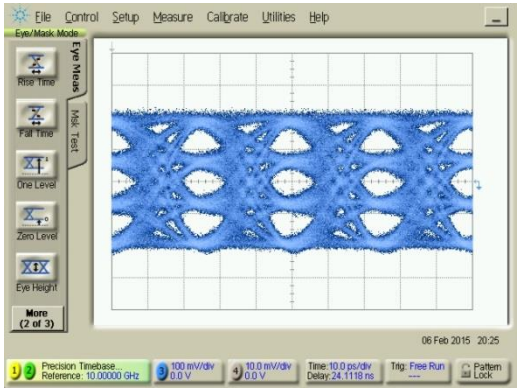


56.2 GBaud

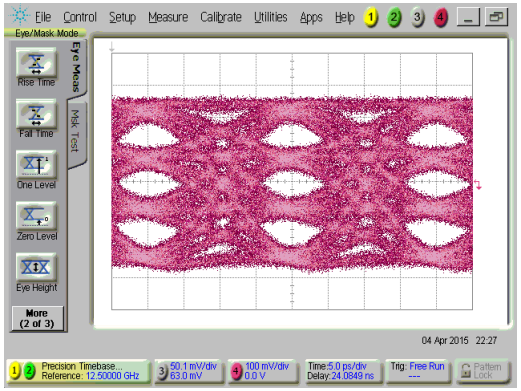


- PAM4 0.475 Vp-p (Data1 Input 2 V, Data2 Input 1 V)

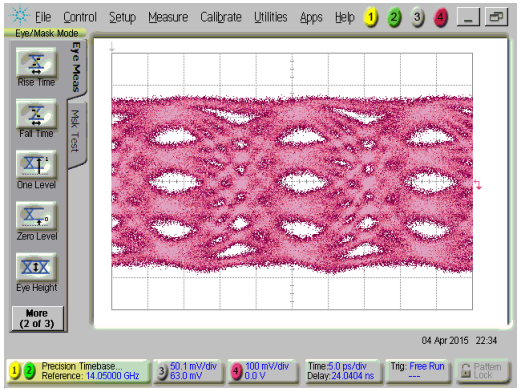
40 GBaud



50 GBaud



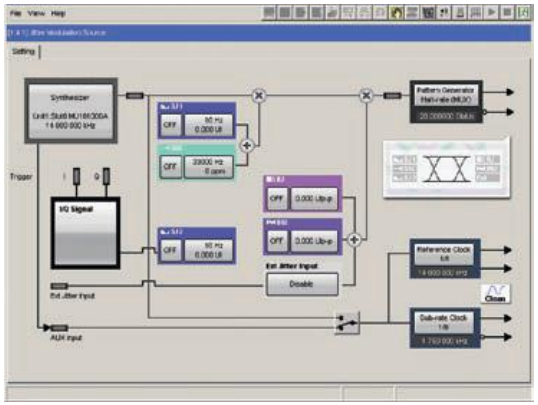
56.2 GBaud



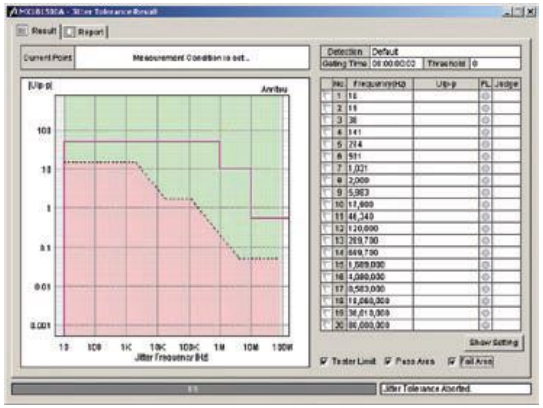
Measured with 41V-6 Attenuator and 86118A 70 GHz oscilloscope

Features (8) Versatile Signal Integrity Measurement Functions

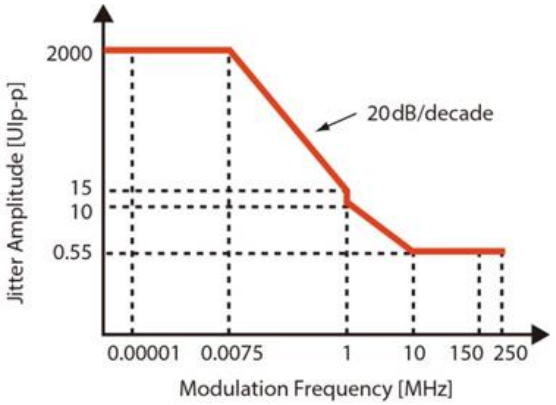
- **Versatile jitter generation including SJ, RJ, BUJ, SSC, Half Period Jitter (Even/Odd Jitter) and automatic tolerance measurements**
  - ✓ Generate SJ up to 2000 UI or 0.55 UI high-frequency SJ at 250 MHz (at 56.2G).
  - ✓ Low intrinsic jitter: 275 fs rms (nominal).
  - ✓ Inject Dual Tone SJ (two different frequencies), RJ, BUJ, and SSC independently and simultaneously.



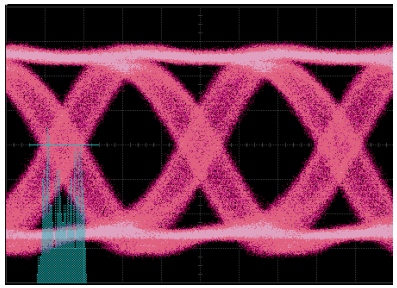
Generate Various Jitter Types



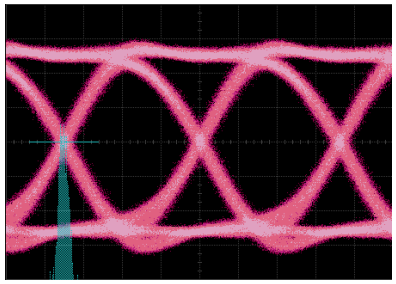
MX181500A Jitter/Noise Tolerance Test Software



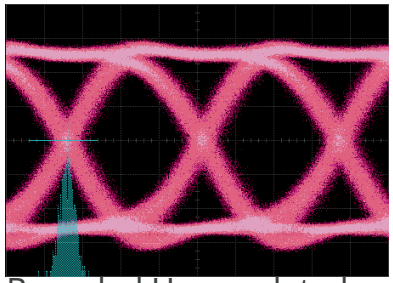
Jitter Generation Mask



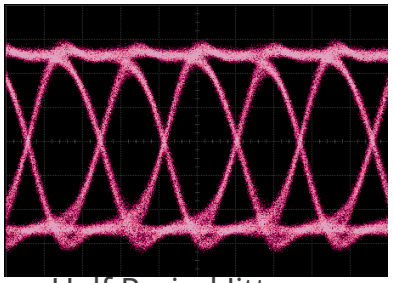
Sine Wave Jitter (SJ)



Random Jitter (RJ)



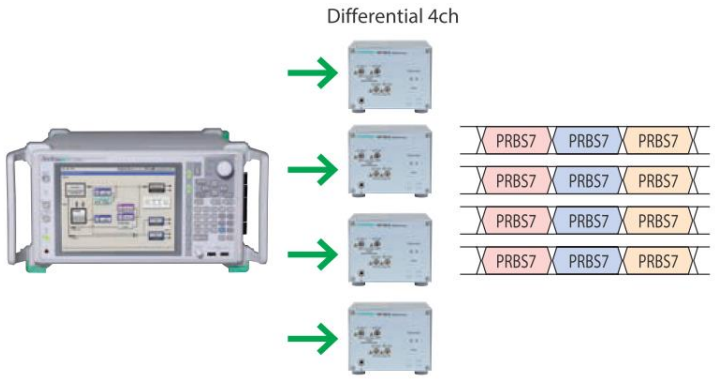
Bounded Uncorrelated Jitter (BUJ)



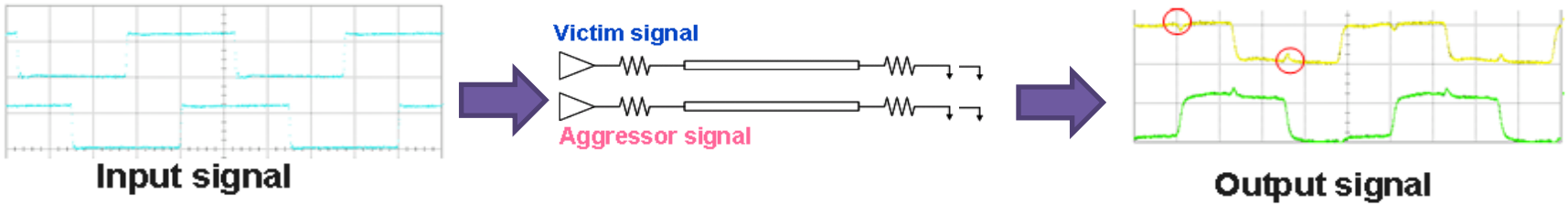
Half Period Jitter (Even/Odd Jitter)

Features (9) Versatile Signal Integrity Analysis Functions

- Max 4ch Sync
  - ✓ Using external MUX and DEMUX supports syncing for max 4ch by connection to PPG and ED modules installed in MP1800A.
  - ✓ Evaluation of D/A converters, crosstalk and skew tolerance all supported.



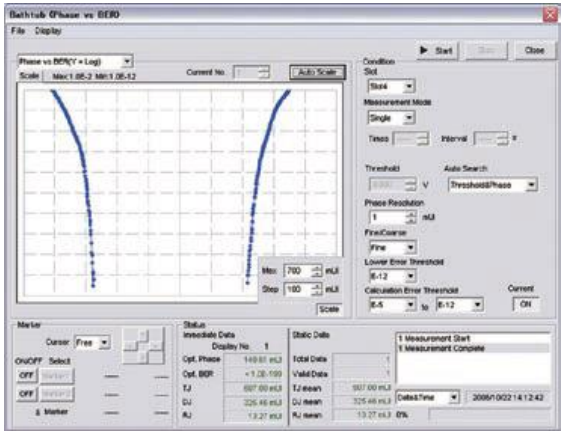
- Crosstalk Tests
  - ✓ Installing MUX Data Delay option offers independent phase control for each channel.
  - ✓ DUT crosstalk can be found with high accuracy using precision control in 4mUI steps.



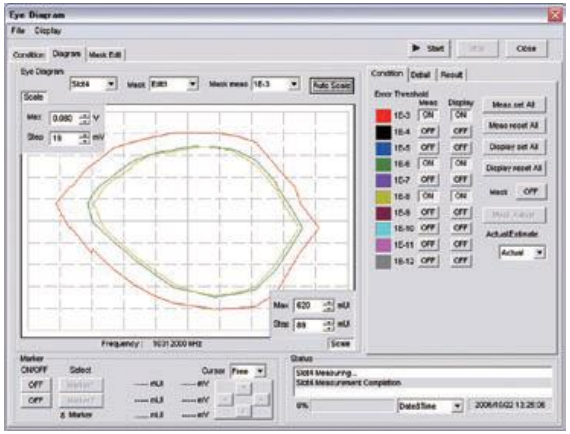
Features (10) Versatile Signal Integrity Analysis Functions

- TJ/DJ/RJ/Bathtub Jitter Auto-Measurements
  - ✓ Measures optimum BER based on changes in bit error rate relative to phase and analyzes Jitter (TJ, RJ, DJ)
- EYE Diagram Auto-Measurements
  - ✓ Captures BER contours linking specified BER points
- EYE Margin Auto-Measurements
  - ✓ Confirms data threshold and phase margins

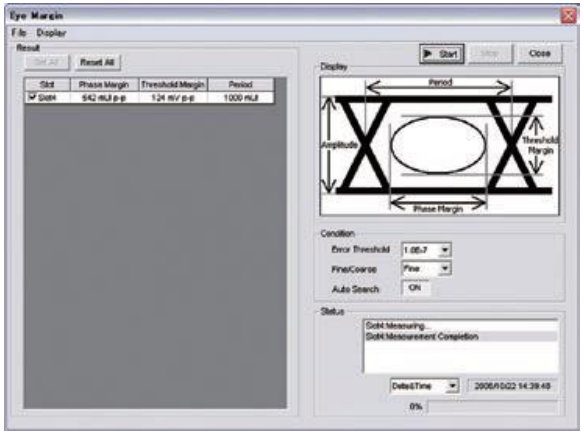
Bathtub Jitter Measurement



EYE Diagram Measurement



EYE Margin Measurement



Features (11) Supports Various Data Patterns

- Burst Signal Tests
  - ✓ Supports application evaluation using burst signals, such as optical loop test
    and transmission test using quantum noise technology
- Max 512 Mbit/ch Programmable Data Pattern
  - ✓ Generates any pattern for applications, such as CJTPAT, CJPAT, K28.5
  - ✓ 4PAM BER Measurement (three EYEs simultaneously) up to PRBS2 ^{20} -1
- Pseudorandom Patterns (PRBS)
  - ✓ 2 ^{n} $^{-1}$ (n = 7, 9 , 10 , 11 , 15 , 20 , 23 , 31)
- Zero Substitution Patterns
- Mixed Patterns

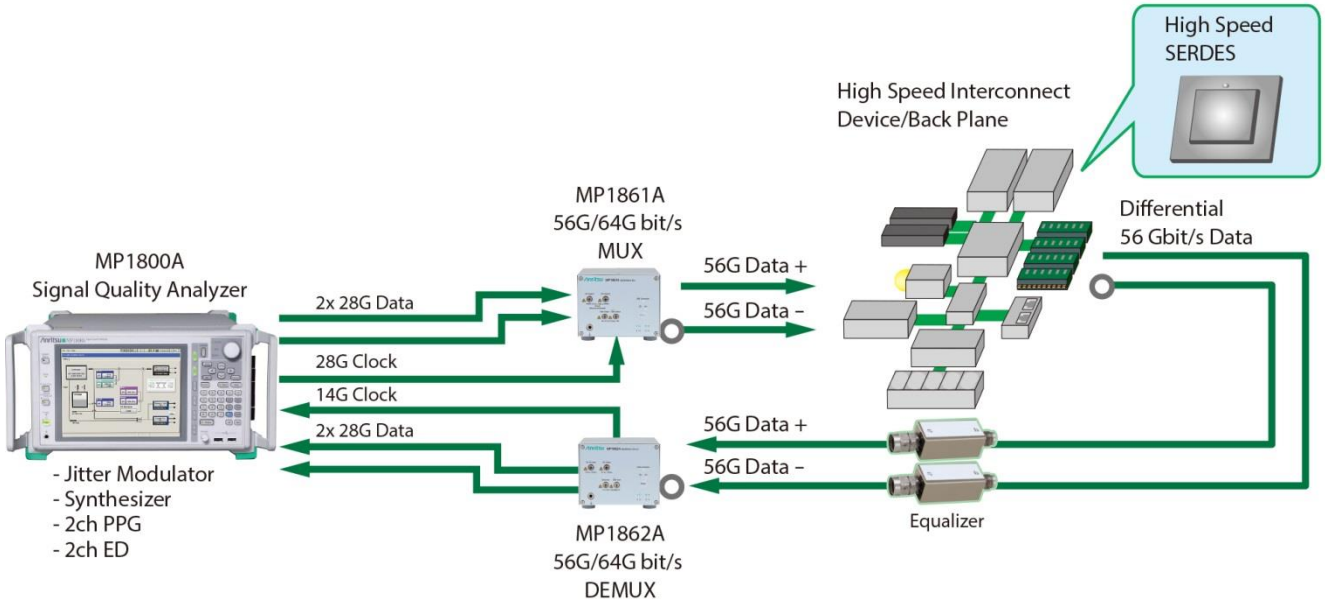
56G/64G bit/s MUX/DEMUX specification

MP1861A 56G/64G bit/s MUX	
Bit Rate	8 to 56.2 Gbit/s 8 to 64.2 Gbit/s (MP1861A-001)
No. of Channels	1ch, Up to 4ch parallel synchronization by connecting to MP1800A
Amplitude	0.5 to 2.5 Vp-p（≤56.2 Gbit/s, MP1861A-011） 1.0 to 2.5 Vp-p（>56.2 Gbit/s, MP1861A-011） 0.5 to 3.5 Vp-p（≤56.2 Gbit/s, MP1861A-013） 1.0 to 3.5 Vp-p（>56.2 Gbit/s, MP1861A-013）
Intrinsic Random Jitter	RJ = 200 fs rms（typ.）
Half Period Jitter	20 Steps

MP1862A 56G/64G bit/s DEMUX	
Bit Rate	8 to 56.2 Gbit/s 8 to 64.2 Gbit/s (MP1861A-001)
No. of Channels	1ch, Up to 4ch parallel synchronization by connecting to MP1800A
Amplitude	0.125 to 1.0 Vp-p
Sensitivity	25 mV (typ.), ≤40 mV (EYE height, PRBS31, single-ended)

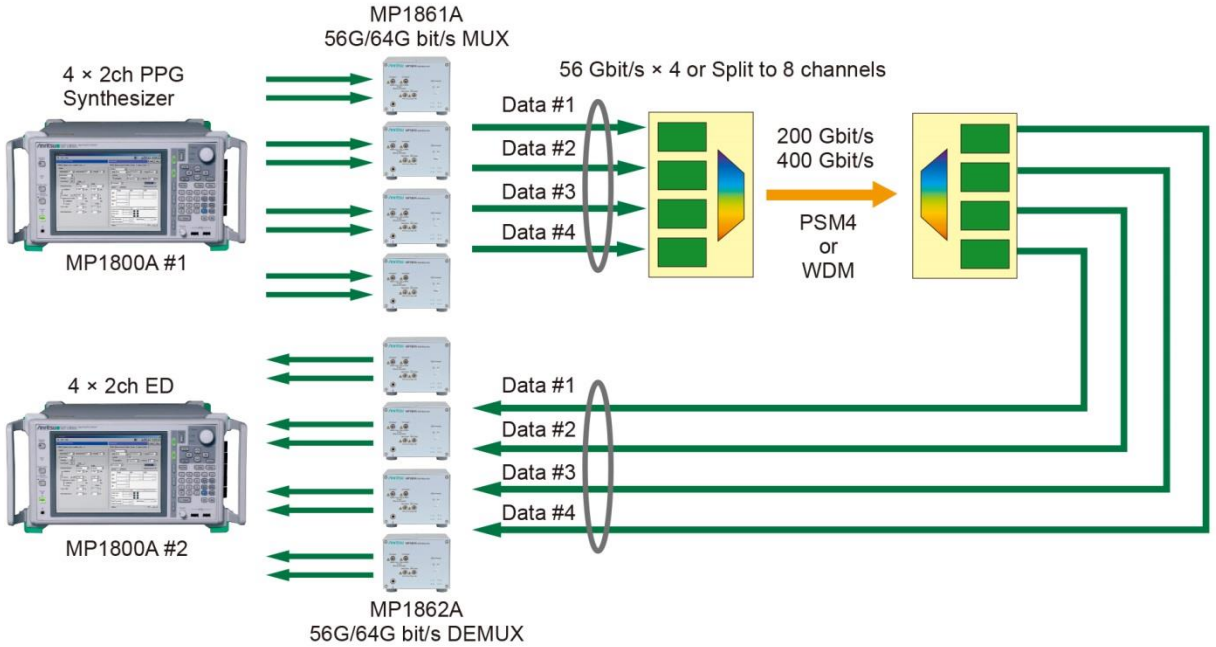
Main Applications (Interconnects)

- 56 Gbit/s Band High-Speed Semiconductor Chip Measurements



56 Gbit/s BER Measurements	→ BERT measurements for SERDES, Clock Data Recovery(CDR), etc.
Jitter Tolerance Tests	→ Supports SJ (two frequencies), RJ, BUJ, SSC, etc., Jitter Tolerance tests for CEI-56G
Input Sensitivity Tests	→ Device input sensitivity tests using wide variable amplitude range 0.5 to 3.5 Vpp (56G, with installed MP1861A-013 option)
Bathtub Jitter Measurements	→ Bathtub Jitter measurement using MP1862A Clean Clock during jitter addition

Main Applications (Transmitter)



400GbE, 56G × 4 Lane Evaluation → Supports EML and optical module evaluations for 400GbE now being examined by IEEE 802.3bs

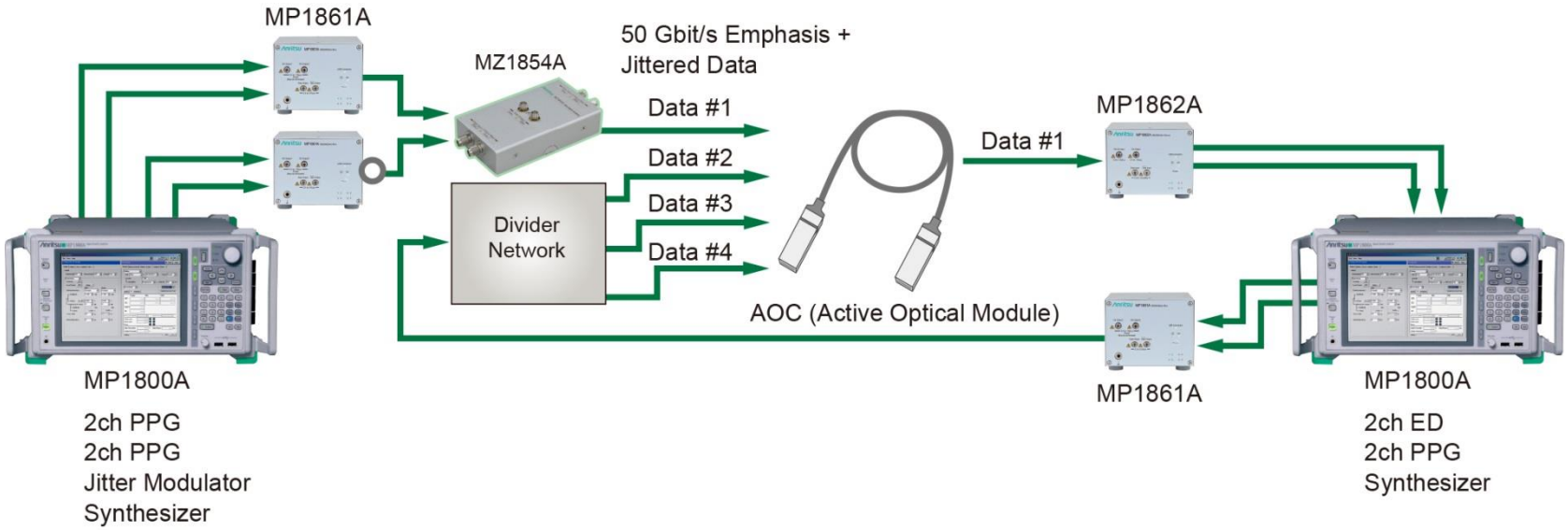
Optimum Signal Quality for EML Eval → Direct EML driving using variable output function up to 3.5 Vp-p

Confirming Skew and Crosstalk Effects → Pattern Sync and Variable Phase functions support easy verification of Rx device Skew Tolerance, Crosstalk effects

Built-in High Sensitivity/Auto Search Functions

→ Auto-tuning of Data and Clock phase differences and optimized voltage threshold using MP1862A Auto Search function

Main Applications (AOCs/Backplanes)



Emphasis Generation → MP1861A generates Emphasis signal using 2ch Sync function and MZ1854A Combiner

Jitter Tolerance Tests → Supports SJ (two frequencies), RJ, BUJ, SSC Jitter Tolerance tests for CEI-56G

Crosstalk Effects → Pattern Sync and Variable Phase functions support easy verification of Rx device Skew Tolerance, Crosstalk effects, etc.

Bathtub Jitter, EYE Diagram Analysis → Bathtub Jitter analysis (TJ, RJ, DJ) using built-in DEMUX Clock Delay function

Appendix

Configuration Guide

Category	Model Number	Model Name	28G 1ch Basic	High-speed Interconnects 32G 2ch + Jitter + Emphasis	InfiniBand QSFP 28G 8ch + Jitter	100 GbE/ Silicon Photonics 28G 4ch	DP-QPSK 32G 4ch PPG	4PAM	8PAM
Main Frame	MP1800A	Signal Quality Analyzer	1	1	2	1	1	1	1
	MP1800A-014	2-slot for PPG and/or ED	1	1			1	1	1
	MP1800A-015	4-slot for PPG and/or ED			2*	1*			
	MP1800A-016	6-slot for PPG and/or ED							
	MP1800A-032	32 Gbit/s PPG and/or ED Support	1	1	2	1	1	1	1
Synthesizer (Sinusoidal Jitter)	MU181000A	12.5 GHz Synthesizer	1	1	1	1	1	1	1
	MU181000A-001	Jitter Modulation		1	1				
Jitter Modulator SJ (2-tone)/RJ/ BUJ	MU181500B	Jitter Modulation Source		1	1				
28G/32G PPG 1ch/2ch	MU183020A	28G/32G bit/s PPG	1	1				1	
	MU183020A-001	32G bit/s Extension		1				1	
	MU183020A-012	1ch 2 V Data Output	1*						
	MU183020A-013	1ch 3.5 V Data Output							
	MU183020A-022	2ch 2 V Data Output		1*				1*	
	MU183020A-023	2ch 3.5 V Data Output							
	MU183020A-030	1ch Data Delay							
	MU183020A-031	2ch Data Delay		1				1	
28G/32G PPG 4ch	MU183021A	28G/32G bit/s 4ch PPG			2	1	1		1
	MU183021A-001	32G bit/s Extension					1		1
	MU183021A-012	4ch 2 V Data Output			2*	1*	1*		1*
	MU183021A-013	4ch 3.5 V Data Output							
	MU183021A-030	4ch Data Delay			2	1	1		1
28G/32G ED 1ch/2ch	MU183040B	28G/32G bit/s ED	1	1					
	MU183040B-001	32G bit/s Extension		1					
	MU183040B-010	1ch ED	1	1					
	MU183040B-020	2ch ED							
	MU183040B-022	2.4G to 28.1G bit/s Clock Recovery		1*					
	MU183040B-023	25.5G to 32.1G bit/s Clock Recovery							
28G/32G ED 4ch	MU183041B	28G/32G bit/s 4ch ED			2	1			
	MU183041B-001	32G bit/s Extension							
	MU183041B-022	2.4G to 28.1G bit/s Clock Recovery			1	1			
	MU183041B-023	25.5G to 32.1G bit/s Clock Recovery							
Emphasis	MP1825B	4Tap Emphasis		1					
	MP1825B-001	14 Gbit/s Operation							
	MP1825B-002	28 Gbit/s Operation		1					
	MP1825B-003	14 Gbit/s Variable Data Delay							
	MP1825B-004	28 Gbit/s Variable Data Delay							
	MP1825B-005	14.1 Gbit/s Extension							
	MP1825B-006	32.1 Gbit/s Extension		1					
Software	MX181500A	Jitter/Noise Tolerance Test Software		1	1				
PAM Signal Generation	MZ1834A	4PAM Converter						1	
	MZ1838A	8PAM Converter							1

*: Select any one

Category	Model Number	Model Name	56G 1ch Basic	64G 1ch Basic	High-Speed Semiconductor Chips	400G Modules	AOC Back Planes	Emphasis/ PAM4
56G/64G MUX	MP1861A	56G/64G bit/s MUX	1	1	1	4	3	2
	MP1861A-001	64G bit/s Extension	–	1	–	–	–	2
	MP1861A-011	Variable Data Output (0.5 to 2.5 Vp-p)	1*1	1*1	1*1	4*1	3*1	2*1
	MP1861A-013	Variable Data Output (0.5 to 3.5 Vp-p)						
	MP1861A-030	Variable Data Delay	–	–	1	4	3	2
56G/64G DEMUX	MP1862A	56G/64G bit/s DEMUX	1	1	1	4	1	2
	MP1862A-001	64G bit/s Extension	–	1	–	–	–	2
Main Frame	MP1800A	Signal Quality Analyzer	1	1	1	2	2	2
	MP1800A-014	2-Slot for PPG and/or ED	1	1	1*1	–	–	2*1
	MP1800A-015	4-Slot for PPG and/or ED	–	–		2*1	2*1	
	MP1800A-016	6-Slot for PPG and/or ED	–	–				
	MP1800A-032	32 Gbit/s PPG and/or ED Support	1	1	1	2	2	2
Synthesizer (Sinusoidal Jitter)	MU181000A	12.5 GHz Synthesizer	1	1	1	–	–	–
	MU181000A-001	Jitter Modulation	–	–	1	–	–	–
Synthesizer (Sinusoidal Jitter)	MU181000B	12.5 GHz 4port Synthesizer	–	–	–	1	1	1
	MU181000B-001	Jitter Modulation	–	–	–	–	1	–
Jitter Modulator SJ (2-tone)/RJ/BUJ	MU181500B	Jitter Modulation Source	–	–	1	–	1	1
28G/32G PPG 2ch	MU183020A	28G/32G bit/s PPG	1	1	1	4	3	2
	MU183020A-001	32G bit/s Extension	–	1	–	–	–	2
	MU183020A-022	2ch 2 V Data Output	1	1	1	4	3	2
	MU183020A-023	2ch 3.5 V Data Output	–	–	–	–	–	–
	MU183020A-031	2ch Data Delay*2	1	1	1	4	–	2
28G/32G ED 2ch	MU183040B	28G/32G bit/s High Sensitivity ED	1	1	1	4	1	2
	MU183040B-001	32G bit/s Extension	–	1	–	–	–	2
	MU183040B-020	2ch ED	1	1	1	4	1	2
Combiner	MZ1854A	Data Signal Combiner	–	–	–	–	1	1
Software	MX181500A	Jitter/Noise Tolerance Test Software	–	–	1	–	1	1

*1: Select any one
*2: Required when using 56G/64G bit/s MUX MP1861A

Anritsu

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