ANRITSU CORPORATION 5-1-1 Onna, Atsugi-shi, Kanagawa 243-8555 Japan

Anritsu - GRL

PCIe 3.0 CEM Rx Test Application

Release Note

Eleventh Edition

This software is released for PCIe CEM Rx Test.

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1. Released Software

The certificate software versions for Keysight / Tektronix Scope are shown in the table.

E 1'4'	GRL CEM Rx	Anritsu	Anritsu	Scope	
Edition	Test Application	MX190000A	MX183000A	Keysight	Tektronix
11	V1.0.75	V6.01.05	V6.00.05	DSAZ634A	DPO77002SX
				V06.60.00403	V10.11.0.30
10	V1.0.64	V5.01.00	V5.00.30	DSAZ634A	DPO77002SX
				V06.60.00403	V10.11.0.30
09	V1.0.59	V4.10.20	V4.10.05	DSAZ634A	DPO77002SX
				V06.55.00702	V10.1.0.34
08	V1.0.56	V4.09.50	V4.09.15	DSAZ634A	DPO77002SX
				V06.55.00702	V10.1.0.34
07	V1.0.54	V4.09.41	V4.09.15	DSAZ634A	DPO77002SX
				V06.55.00702	V10.1.0.34
06	V1.0.49	V4.03.12	V4.03.15	DSAZ634A	DPO75902SX
				V06.40.00714	V10.0.8.138
05	V1.0.49	V4.03.12	V4.03.15	DSAZ634A	DPO73304DX
				V06.40.00714	10.8.3 Build 3
	V1.0.49	V4.02.10	V4.02.10	DSAZ634A	DPO73304DX
				V06.40.00714	10.8.3 Build 3
	V1.0.49	V4.01.32	V4.00.08	DSAZ634A	DPO73304DX
				V06.40.00714	10.8.3 Build 3
04	V1.0.22	V3.01.10	V3.07.12	DSAZ634A	DPO73304DX
				V06.20.01101	10.8.3 Build 3
03	V1.0.22	V3.00.05	V3.06.16	DSAZ634A	DPO73304DX
				V06.20.01101	10.8.3 Build 3
02	V1.0.22	V2.05.08	V3.05.00	DSAZ634A	DPO73304DX
				V06.20.01101	10.8.3 Build 3
01	V1.0.11	V2.05.08	V3.05.00	DSAZ634A	DPO73304DX
				V06.20.01101	10.8.3 Build 3

2. Peripheral Devices

The peripheral devices of the application are shown in the table.

Model	Name
MP1900A	Signal Quality Analyzer-R
MU181000B	12.5GHz 4port Synthesizer (Option02 is required.)
MU181500B	Jitter Modulation Source
MU195020A or	21G/32G bit/s SI PPG or PAM4 PPG
MU196020A	
MU195040A	21G/32G bit/s SI ED
MU195050A	Noise Generator

For the installation position of the mainframe, refer to the Anritsu website (https://www.anritsu.com).

3. Added Functions

Edition	Function	Description		
11	All	Adds support for M.2 and U.2 Interface Types		
10	MOI	Updates MOI		
08	All	Turns OFF PPG output after completing tests and when changing ISI		
07	All	Supports MU196020A PAM4 PPG		
05	Auto Scale	This function turns off the Auto Scale function forScope to shorten the time required for Initial Tx EQand Tx LEQ response time test.When the function is set to True , input the amplitudeof the Data output of the DUT in the Vertical Range(scale of the vertical axis of Scope) with a valueequivalent to Differential Input.The recommended value for Vertical Range is 0.5Vpp because the Power Divider practicallyattenuates the data output of the DUT by 6 dB. Thissoftware may fail in waveform decoding if theamplitude is too small for the scale or beyond thescale.		

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Edition	Function	Description			
05	Auto DUT Reset	This function resets the DUT automatically during			
		Compliance Test.			
		To use this function, follow the steps below:			
		a. In the Auto DUT Reset box, select Internal			
		Power Cycle or Internal Power Reset.			
		b. Set up Anritsu Z2025A PCIe CBB Controller			
		according to the Z2025A Installation Guide.			
		c. In the Prompt Before Link EQ Training box,			
		select False.			
		Application Options License Windows Help			
		Configurations Image: Configuration (Configuration (Con			
		Auto DUT Reset: Internal Power Cycle Power Cycle Off Time(s): Power Reset Off Time(s): Post Reset WaitTime(s): BER Automation: PCle Link Training Prompt Before Link EQ Training: False			
		Power Cycle Off Time: Sets the time to turn off the CBB power.			
		Power Reset Off Time:			
		Sets the time to send the Power Reset signal to the			
		DUT.			
		Post Reset Wait Time:			
		Sets the time to wait after turning on Reset or			
		Cycle before Link Training is started.			
	Link Training Wait Time	This function sets the time to wait after Link Training			
		is ready to start before it is started.			
	Link Training CTLE Gain	Select a CTLE value option to set for SI ED. If the			
		DUT Tx Insertion Loss is large, adjust the value.			
	Log Link Training	This function saves an LTSSM Log file to the			
		following directory of MP1900A every time Link			
		Training is performed.			
		"C:¥PCIE_LTSSM_LOG"			

4. Bug Fixes

Edition	Item	Description		
09	PPG Final Preset setting issue	Fixes config "PPG Final Preset" not being applied when changed to fixed preset.		
	JTOL display issue	Updates framework to fix Jitter tolerance plot display incorrect JTOL line.		
05	Tx LEQ Response time test and Rx LEQ test failed occasionally.	Tx LEQ Response time test and Rx LEQ test failed occasionally.		
01	Sometimes, Preset calibration fails with Tektronix scope.	Calibration fails when attempting to execute Preset calibration. Bug occurs in GRL software version 1.00.11 and Tektronix scope software version 10.8.3.		

5. Remaining Known Bugs

None

6. Usage Notes

The precautions for using each version are described below.

6.1 How to shorten measurement time

- BER and Margin Test

Decrease Margin Test Measurement Time and Margin Test Max Steps.

Conf	figurations	
	Compliance BER Measurement Time(s): G3 Maximum Compliance Error:	
	Margin Test Measurement Time(s): Argin Test Max Steps: 5	
	Margin Test Step Size(%): 20 Maximum Margin Test Error: 1	
	Loopback Mode: Recovery	-

Set Retrain When Sj Frequency Changed to False.

	Margin Test Measurement Time(s):	5
	Margin Test Max Steps:	5
	Margin Test Step Size(%):	20
	Maximum Margin Test Error:	1
-	Loopback Mode: Reco	very 🔹
	Retrain When Sj Frequency Change	ed: False 🔹
L	MarginSearchLivePlot:	True
▲		

6.2 Note on Link EQ Response time test

Perform the **Tx EQ Response time (Preset)** test before running the **Tx EQ Response Time** (Cursor) test.

When starting the test with **Tx EQ Response Time (Preset)**, the cursor values corresponding to Preset are sent from the DUT and are saved in MP1900A. These values are required for testing **Tx**

EQ Response Time (Cursor).

Application Options License Windows Help		
Select Tests $2 \Rightarrow 0 \Rightarrow $?	
		3

To skip the test with Tx EQ Response time (Preset):

Perform link training by following the steps below to acquire cursor values from the DUT. When replacing the DUT to test **Tx EQ Response time (Cursor)**, it is required to go through these steps again.

- a. Launch MX183000A with PCIe Link Training application.
- b. Initialize the PCIe Link Training application.
- c. Set Specification to 3.0(8.0 GT/s).
- d. Click on LEQ Test Setting check box.

MX183000A - PCIe File Setup He							Operate MP1900A
Equipment Setu	p Link Trainin	g Run Test Gr	aph Report		Elect	rical Idle	
Specification 3.0/3.1(8.0 GT,	/s) 🔹 DUT	oint (AIC)	-	Nore results			Link Start
LTSSM State Linkup Speed			Received Use Preset PPG Final Pre	set		LEQ T	est 📄 Setting
8b10b SKP Count Symbol Err Current RD Err	Received	Transmitted	PPG Final Cur Pre-C Full Swing, Low Link, Lane Num	Frequency			Configure Measurement TSSM Log
Symbol Lock				PCIe 3	PCIe 4	Config	
	Received	Transmitted	Phase0 (Root)	PCIE 3	PLIE 4	Test Pa	ttern
SKP Count			Phase1			Compl	iance 🔻
DCBalance Sync Header Err			Phase2			MCP	-
1 ·			Phase3				
Parity Err Block Lock			ALL				Timeout Option
<u>[]</u>			,				Орион

e. Select **Rx LEQ** tab and click on **Apply** button.

MX183000A - PCIe Link Training		×
File Setup Help		Operate MP1900A
Equipment Setup Link Training Run Test Gr	aph Report Elect	trical Idle
Specification DUT 3.0/3.1(8.0 GT/s) DUT Endpoint (AIC)	More results	Link Start
LTSSM State Linkup Speed	Received Use Preset PPG Final Preset	LEQ Test 📝 Setting Rx LEQ
LEQ Test Rx LEQ Apply Rx LEQ I itial TX LEQ Tx LEQ Response	PPG Final Cursor Pre-Cursor Cursor Post-Cursor	Configure BER Measurement
Loopback Through: Recovery Link EQ: Preset Saved Cursor Lane: 0/8	Full Swing, Low Frequency Link, Lane Number	LTSSM Log Loopback through
Test Pattern: MCP (Modified Compliance Pattern)	PCIe 3 PCIe 4	Recovery Test Pattern
PPG Starting Preset: P7	Phase0 (Root)	Compliance •
DUT Initial Preset (Preset Hint Tx):	Phase2	MCP
DUT Target Preset (Change Preset):	ALL	Timeout
		Option

f. Click on **Option** button.

MX183000A - PCIe Link Training		×
File Setup Help		Operate MP1900A
Equipment Setup Link Training Run Test Gr	aph Report Elect	rical Idle
Specification DUT 3.0/3.1(8.0 GT/s) DUT Endpoint (AIC)	More results	Link Start
UTSSM State Linkup Speed LEQ Test Rx LEQ Apply Rx LEQ Initial TX LEQ Rx LEQ Initial TX LEQ Loopback Through: Recovery Link E: Preset Lane: 0/8	Received Use Preset PPG Final Preset PPG Final Cursor Pre-Cursor Cursor Cursor FutUssor FutUssor, Low Frequency Link, Lane Number	LEQ Test V Setting Rx LEQ BER Measurement LTSSM Log Loopback through Recovery V
Test Pattern: MCP (Modified Compliance Pattern) PPG Starting Preset: PT DUT Initial Preset (Preset Hint Tx): [PT v] DUT Target Preset (Change Preset): [PT v]	PCIe 3 PCIe 4 Phase0 (Root) Phase1 Phase2 Phase3 ALL	Test Pattern Compliance • MCP • Timeout

g. Set Algorithm to increment and set Repeat to 12 on Link EQ tab.

1 Option State Machine SKP Link EQ PPG/E	D Trigger	u u
Link EQ (Recovery Phase2,3) Try Algorithm Increment	▼ Repeat 12	PCIe 3.0/3.1
PCIe 3.0/3.1 Use Preset Preset Downstream Downstream (MP1900A) sends Starting Preset un Starting Preset Preset Hint (Rx)	ntil it receives preset from Upstream (AIC). Recovery.EQ.Phase2 Change Preset	Root Complex Downstream port Tx Rx
P7:-6.0, 3.5	P7:-6.0, 3.5 v	Rx Tx Upstream port
Downstream (MP1900A) requests these presets	to Upstream (AIC) Recovery.EQ.Phase3 Change Preset	End Point
Preset Hint (Tx) Preset Hint (Rx) P7: -6.0, 3.5 • -6 dB •	P7 : -6.0, 3.5	
		Close

h. Reset the DUT and click on Link Start button.



i. When LTSSM State is Loopback.Active.Lead, click on Saved Cursor button on LEQ Test window.

MX183000A - PCIe Link Training					×
File Setup Help					Operate MP1900A
Equipment Setup Link Training Run Test Gra	aph Report			Outp	outting Test Pattern
Specification DUT [3.0/3.1(8.0 GT/s) -	• M	lore results			Unlink
LTSSM State Loopback.Active.Master Linkup Speed 8.0 Gbps	Received Use Preset PPG Final Pres		PI	eset P7	LEQ Test V Setting
LEQ Test Rx LEQ Apply Rx LEQ Initial TX LEQ Tx LEQ Response	PPG Final Curr PPG Final Curr Pre-C	sor ursor Cursor	Post-C		Configure BER Measurement
Loopback Through: Recovery Link EQ: Preset Saved Cursor Lane: 0/8	Full Swing, Low Link, Lane Numb	Frequency	63 1	21	LTSSM Log Loopback through
Test Pattern: MCP (Modified Compliance Pattern) PPG Starting Preset: P7 UT Initial Preset (Preset Hint Tx): [P7 v]	Phase0 (Root) Phase1 Phase2 Phase3	PCIe 3 Complete Complete	PCIe 4 		Test Pattern Compliance
DUT Target Preset (Change Preset):	ALL	Complete	-		Timeout Option

					ed automati				
Г	Saved		PCIe 3.0		Saved		PCIe 4.0		
	Cursor	C-1	CO	C+1	Cursor	C-1	CO	C+1	
	V P0	0	47	16	🔽 РО	0	47	16	
	V P1	0	52	11	V P1	0	52	11	
	✓ P2	0	50	13	V P2	0	50	13	
	🗸 РЗ	0	55	8	🔽 РЗ	0	55	8	
	V P4	0	63	0	V P4	0	63	0	
	V P5	6	57	0	V P5	6	57	0	
	V P6	8	55	0	V P6	8	55	0	
	V P7	7	45	11	V P7	7	45	11	
	V P8	8	47	8	V P8	8	47	8	
	V P9	11	52	0	V P9	11	52	0	
	√ P10	0	42	21	V P10	0	42	21	

j. If all Saved Cursor checkboxes are ON, the steps are finished.

k. Launch GRL application and start Tx EQ Response time (Cursor).



6.3 Selecting Interface Types

The option to select between CEM, U.2, and M.2 Interface Types is located in the Setup Configuration page \rightarrow Setup Tab.

Setup Debug	Tool		
Device Typ	e:	Add In Card	\sim
Interface Ty	pe:	M.2 CEM U.2 M.2	~

7. Troubleshooting

If you encounter any errors during calibration or testing, check as follows.

7.1 Calibration

7.1.1 In case of an error when calibrating Amplitude, Preset, SJ and RJ

- Check the RF connections. Especially, the connection polarity (Pos/Neg) and the trigger connections (PPG Aux Out and Scope Aux In) are easy to mistake.
- Check the software version. A different version of software may cause an unexpected error.
- Check the SigTest version. SigTest version needs to be 3.2.0.3 for Gen3 or 4.0.51 for Gen4. Also, this should be installed to the directory C:¥Program Files (x86). Do not change the installation directory from the default setting.
- 7.1.2 In case of a SigTest error when performing Long Channel Calibration

A SigTest error message is displayed and SigTest has stopped working when calibrating SJ, RJ and EH/EW. Since this message has no effect on calibration results, click **Close the program** to continue the calibration.



To avoid this message:

- Close all applications except the GRL software, MX190000A, MX183000A and scope applications. Especially when VNC is running, SigTest may not work properly.
- If you see this message frequently despite not running other applications on the PC, use another PC with the GRL software installed.

7.1.3 When Final Eye calibration fails

- Use the PCIe 3.0 test fixture. It is recommended to use the calibration fixture distributed by the PCI-SIG.
- If any components (DC block, Power Divider, Attenuator and Adaptor) are attached to the Noise module output, remove them. These components may affect the waveform.



7.2 Tx and Rx LEQ test

- 7.2.1 When Tx LEQ Response cursor test cannot be started
 - Before starting Rx Test, complete all calibrations or load a calibrated session file.
- 7.2.2 In case of a Link Training error when testing Tx LEQ Response
 - Check the RF connections. Especially, the trigger connections (PPG Aux Out and Scope Aux In) are easy to mistake.
 - If DUT Tx has large insertion loss, adjust the MP1900A CTLE value in the MX183000A screen. Refer to Appendix C for adjusting CTLE.
- 7.2.3 In case of a decode error when testing Rx LEQ Reponses time
 - On the **Configurations** tab, set **CTLE Setting** to **Auto**.

🕅 Anritsu PCIe CEM 4.0 Rx Test	
Application Options License Windows Help	
Configurations	
CTLE Scan End EQ Gain(dB): T X Link EQ Tests T X Response Offline Mode: CTLE Setting: Capture Response Time Waveform Only: R X Tests BER Automation: PCIe Link Training R Tests	Set Default

7.3 Others

- 7.3.1 When a session file cannot be loaded
 - Close the folder where you installed the GRL software and saved PDF report file(s) because the loaded session file accesses and edits the folder.

Load Session	x
Incompatible file format or file is being used: Error in loading test session	
ок	

- While recalling the session file on CEM spec takes several minutes, it does not mean that the computer is frozen. Wait until the recalling is completed. This function recalls large waveform files which are acquired by Tx initial EQ and Tx LEQ Response time test.

Appendix

- A. Quick Startup Guide
 - 1. Connect instruments with Ethernet cables as shown below.
 - 2. Set the IP and GPIB addresses as shown below. These can be set in the Network and Sharing Center (Windows OS feature).
 - 3. Install all applications as shown below (Yellow letters).

Recommended connection



* TCP/IP cannot be used when the GRL software is installed on a Tektronix scope. Set the GPIB address as "GPIB8::1::INSTR".

- Optional connection



* TekVISA is needed to control Tektronix scopes. But, the PC on which TekVISA is installed cannot control Keysight scopes. Also, this configuration makes the remote control speed slower than the recommended configuration.

 Launch application and configure equipment settings. Enter the scope address as below, and click . If the setting and connection are correct, the button will turn green.

Tektronix Scope

When the GRL software is installed on the laptop: TCPIP0::192.168.2.110::inst0::INSTR When the GRL software is installed on the scope: GPIBX::1::INSTR*

* Tektronix scope cannot use TCP/IP when the GRL software is installed on it. In this case, GPIB VISA should be set. The address can be checked using the VISA instruments Manager.



Keysight Scope

When the GRL software is installed on the laptop: TCPIP0::192.168.2.110::inst0::INSTR When the GRL software is installed on the scope: TCPIP0::localhost::inst0::INSTR

MX190000A: TCPIP0::192.168.2.100::5001::SOCKET* MX183000A: TCPIP0::192.168.2.100::5000::SOCKET*

Port numbers should be set for MX190000A and MX183000A.

B. Before beginning Tx LEQ response time test

Before beginning Tx LEQ response time test, it is recommended to adjust the **CTLE Gain** value in MX183000A. This is especially efficient when DUT Tx has a large Insertion Loss like a System board. In case of a link training error and/or bit error, adjusting the **CTLE Gain** value is also recommended.

Note:

Though the following procedure uses the screenshots for PCIe 4.0, read PCIe 4.0 as PCIe 3.0 here. Set **Specification** to **3.0 (8 GT/s)**, and then adjust the **CTLE Gain** value according to the following procedure.

a. In MX183000A, display the LEQ test settings and BER Measurement screen.

File Setup Help	Operate MP1900A
Equipment Setup Link Training Run Test Graph Rep	Electrical Idle
Specification DUT	
4.0(16.0 GT/s) • Endpoint (AIC) PCIe 4	0 Preset P7 : -6.0, 3.5 Link Start
LTSSM State	CTLE Gain [dB]
Linkup Speed EC Three	shold 1 LEQ Test V Setting Tx LEQ Response
LEQ Test Tx LEQ Response Apply Pass/Fai	I 📝 Configure
Ry LEO, Unitial TY LEO, TX LEO, Response	BER Measurement

b. Set CTLE Gain to 0 (zero) on the BER Measurement panel.

File Setup Help			Operate MP1900A
Equipment Setup Link Training Run Test Gr	aph Report	Electrical	Idle
Specification DUT			
4.0(16.0 GT/s) • Endpoint (AIC)	PCle 4.0	Preset P7 : -6.0. 3.5 👻	Link Start
LTSSM State		CTLE Gain [dB] 0 🚔	
Linkup Speed	EC Threshold	1	LEQ Test 💟 Setting Tx LEQ Response
LEQ Test Tx LEQ Response Apply	Pass/Fail		Configure
Rx LEQ Initial TX LEQ Tx LEQ Response			BER Measurement

c. On the **Tx LEQ Response** tab of the LEQ test pane, set **PPG Starting Preset** to **7**, **DUT Initial Preset** to **7** and **Target Preset** to **P4**.

File Setup Help			Operate MP1900A
Equipment Setup Link Training Run Test Gr	aph Report	Electrica	Ildie
Specification DUT 4.0(16.0 GT/s) DUT Endpoint (AIC)	PCle 4.0	Preset P7 : -6.0, 3.5 🗸	Link Start
	PCIE 4.0	CTLE Gain [dB]	to Reset to Power Cycled 👻
Linkup Speed	EC Threshold	1	LEQ Test 📝 Setting Tx LEQ Response
LEQ Test Tx LEQ Response Apply	Pass/Fail		Configure
Rx LEQ Initial TX LIQ Tx LEQ Response Loopback Through: Recovery Link EQ: Preset Saved Cursor	Cycle Gating Time	Single ▼ 63 ★ [s]	EER Measurement
Lane: 0/8 Test Pattern: CP (Compliance Pattern)	Switch To Manual BER Test	Error Addition	ecovery 👻
PPG Starting Preset:	Total BER	0.0000E-11	st Pattern ompliance -
DUT Initial Preset (Preset Hint Tx):	Total Error Count	0 5.3760E11	CP 🔻
DUT Target Preset (Change Preset)	Current BER	0.0000E-09	Timeout
P4 🔻	Sync Loss 🔳	Clock Loss 🔳	Option

- d. Click Link Start.
- e. If the following error conditions are met, adjust the **CTLE Gain** value by proceeding to the next step.
 - LTSSM State is not Loopback.Active.Lead.
 - Sync Header Err is greater than 0 (zero).

If there is no error, this procedure is assumed to be completed.

Equipment Setu	p Link Tra	aining	Run Test G	raph Report	Outputti	ng Test Pattern
Specification		DUT				
4.0(16.0 GT/s)		Endpo	int (AIC)	PCIe 4.0	Preset P7 : -6.0, 3.5 🔹 👻	Unlink to Reset
LTSSM State		oonbac	k.Active.Master	-	CTLE Gain [dB] 0 🚔	to Power Cycled 👻
Linkup Speed			16.0 Gbps	EC Threshold	1	LEQ Test 📄 Setting
Linkup speed				20 micshold	- <u>v</u>	Tx LEQ Response
8b10b	Received	т	ransmitted	Pass/Fail		Configure
SKP Count						Stop
Symbol Err	•			Cycle	Single 👻	LTSSM Log
Current RD Err				Gating Time	63 🔶 [s]	
Symbol Lock						opback through
				Switch To	Error Addition	ecovery 👻
128b130b	Received	т	fransmitted	Manual BER Test		st Pattern
SKP Count		0	0	Total BER		ompliance 🔹
DCBalance		0	18	Total Error Count		СР
Sync Header Err	105	57603		Total Bits		UP 👻
Parity Err		0		Current BER		Timeout
Block Lock	Ali	gned				- meour
				Sync Loss 📕	Clock Loss 🔳	Option

f. Increment the CTLE Gain value and run Link Training again until Sync Header Err becomes 0 (zero) and Total Error Count becomes 0 (zero). In this case, it is considered to be error free with -6 dB.



- g. Repeat steps d to f with DUT target Preset P7.
- h. After adjusting the CTLE Gain value, close the MX183000A application and return to the selector screen. The CTLE Gain value is stored on the MX183000A. Start GRL Tx LEQ response time test again.