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Anritsu - GRL

PCIe 4.0 BASE Rx Test Application

Release Note

Seventh Edition

This software is released for PCIe BASE Rx Test.

Table of Contents

1. Released Software

The certificate software versions for Keysight / Tektronix Scope are shown in the table.

Edition	GRL BASE Rx Test Application	Anritsu MX190000A	Scope	
			Keysight	Tektronix
07	V1.5.127	V4.09.50	DSAZ634A V06.55.00702	DPO77002SX V10.1.0.34
06	V1.5.126	V4.09.41	DSAZ634A V06.55.00702	DPO77002SX V10.1.0.34
05	V1.5.123	V4.03.12	DSAZ634A V06.40.00714	DPO75902SX V10.0.8.138
04	V1.5.114	V4.03.12	DSAZ634A V06.40.00714	DPO75902SX V10.0.8.138
03	V1.5.105	V4.03.12 V4.02.10	DSAZ634A V06.40.00714	DPO73304DX 10.8.3 Build 3
02	V1.5.105	V3.00.05	DSAZ634A V06.20.01101	DPO73304DX 10.8.3 Build 3
01	V1.5.105	V2.05.08	DSAZ634A V06.20.01101	DPO73304DX 10.8.3 Build 3

2. Peripheral Devices

The peripheral devices of the application are shown in the table.

Model	Name
MP1900A	Signal Quality Analyzer-R
MU181000B	12.5GHz 4port Synthesizer (Option02 is required.)
MU181500B	Jitter Modulation Source
MU195020A or MU196020A	21G/32G bit/s SI PPG or PAM4 PPG
MU195040A	21G/32G bit/s SI ED
MU195050A	Noise Generator

For the installation position of the mainframe, refer to the Anritsu website (https://www.anritsu.com).

3. Added Functions

Version	Description
V1.5.127	Turns OFF PPG output after testing complete and when changing test configuration
V1.5.126	Supports Keysight UXR scope
V1.5.123	Added the 'System Defined' option to use the Vendor-specific method(Tektronix DPOJET or Keysight EZ-JIT Plus software) for low SJ frequency calibration and the SigTest method for high SJ frequency and RJ calibration.
V1.5.114	Supports MU196020A PAM4 PPG

4. Bug Fixes

None

5. Remaining Known Bugs

None

6. Usage Notes

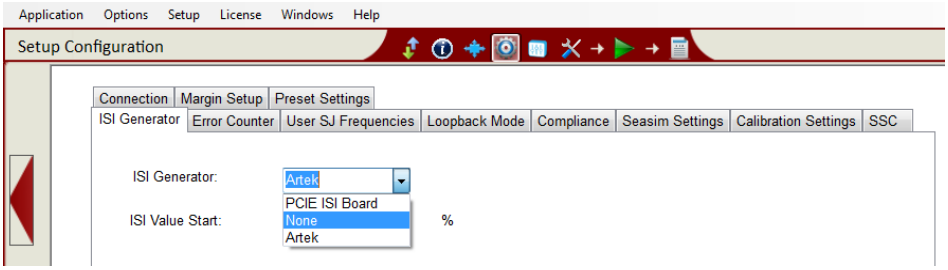
The precautions for using each version are described below.

6.1 ISI Generator explanation

ISI Generator can be selected from the following three options:

-None
-Artek
-PCIE ISI Board

This section explains these three options.



6.1.1 None (Recommended):
27, 28 and 30 dB Insertion Loss channels (e.g., PCIe Gen4 CEM Fixtures) calibrated by VNA should be used for this setting. User fixtures would be acceptable if they meet the specifications.

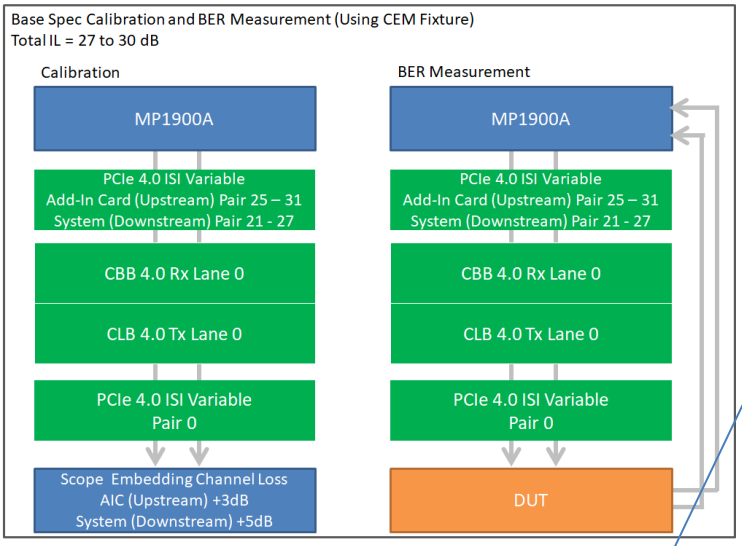


Table 8-9: Calibration Channel IL Limits

Data Rate	$F_{LOW-IL-MIN}$	$F_{LOW-IL-MAX}$	$F_{HIGH-IL-MIN}$	$F_{HIGH-IL-MAX}$
2.5 GT/s	4.5 dB @ 1 GHz	5.0 dB @ 1 GHz	4.7 dB @ 1.25 GHz	5.2 dB @ 1.25 GHz
5.0 GT/s	4.5 dB @ 1 GHz	5.0 dB @ 1 GHz	10.0 dB @2.5 GHz	11.0 dB @2.5 GHz
8.0 GT/s	5 dB @ 1 GHz	8 dB @ 1 GHz	~20 dB @ 4 GHz	~22 dB @ 4 GHz
16.0 GT/s Root Port Long	4.2 dB @ 1 GHz	5.2 dB @ 1 GHz	~22.5 dB @ 8 GHz	~23.5 dB @ 8 GHz
16.0 GT/s Non-Root Port Long	4.2 dB @ 1 GHz	5.2 dB @ 1 GHz	~24.5 dB @ 8 GHz	~25.5 dB @ 8 GHz

Note: Calibration channel plus Rx package is 28 dB nominally (informative) for 16.0 GT/s.

Note: Different reference packages are defined for devcies containing Root Ports and all other device types at 16.0 GT/s.

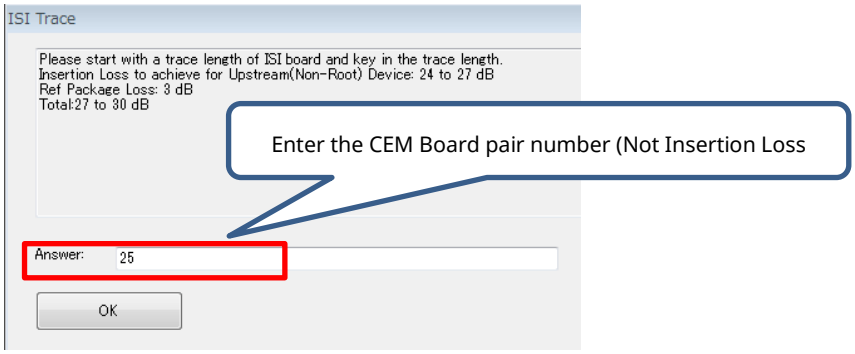
Note: It is recommeded that some validation be done with shorter channels at 16.0 GT/s.

6.1.2 PCIE ISI Board (Optional):
This is an optional method to calibrate the Insertion Loss value (from 27.5 to 29.5 dB) using Step response of Seasim. If the Insertion Loss value of ISI Fixtures already calibrated by VNA, **None** must be selected and **PCIE ISI Board** should not be selected.

When you see the following message, enter the number printed on the CEM Board. For example,

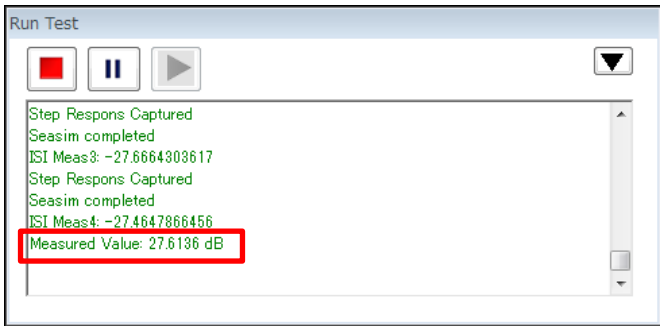
CEM Board (Pair): 25

Artek ISI (%): 23



The Insertion Loss value equivalent to the label is automatically recorded by the software.

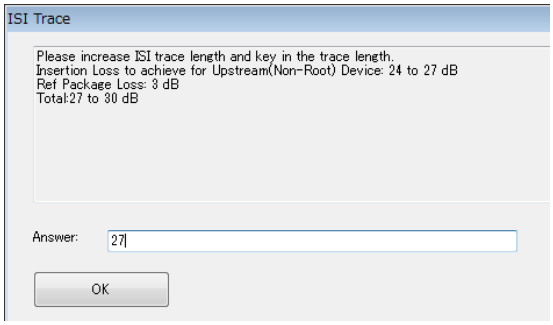
The following value is recorded in this case.



When you see the following message, increase a physical insertion loss trace and type the label (numerical). For example,

CEM Board (Pair): 27

Artek ISI (%): 26

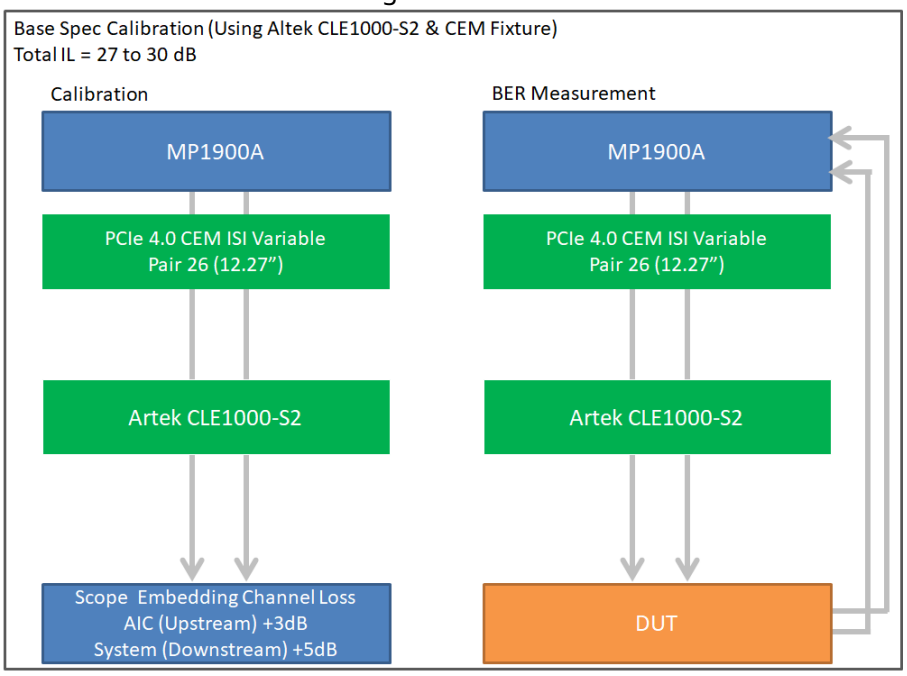


Repeatedly increase (or decrease) physical insertion loss trace until the calibration is

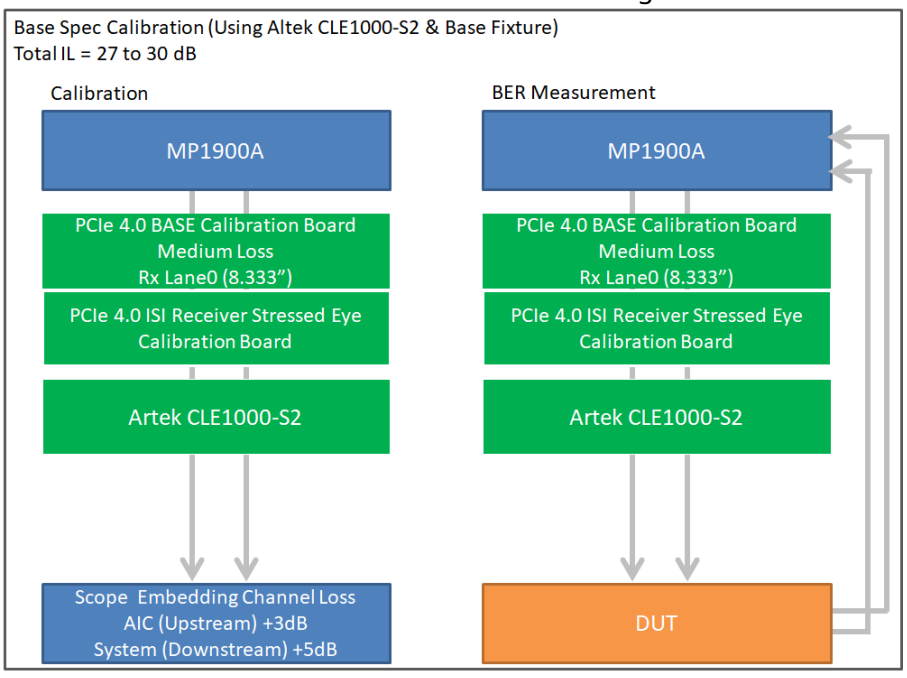
complete.

6.1.3 Artek (Optional):
This is an optional method to automate calibration sequence. This method also calibrates the Insertion Loss using Step Response of Seasim instead of VNA.
Artek CLE1000-S2 (Not A2) and PCIe 4.0 CEM ISI Variable or PCIe 4.0 Base Calibration Board are required for this setting.

PCIe 4.0 CEM ISI Variable configuration



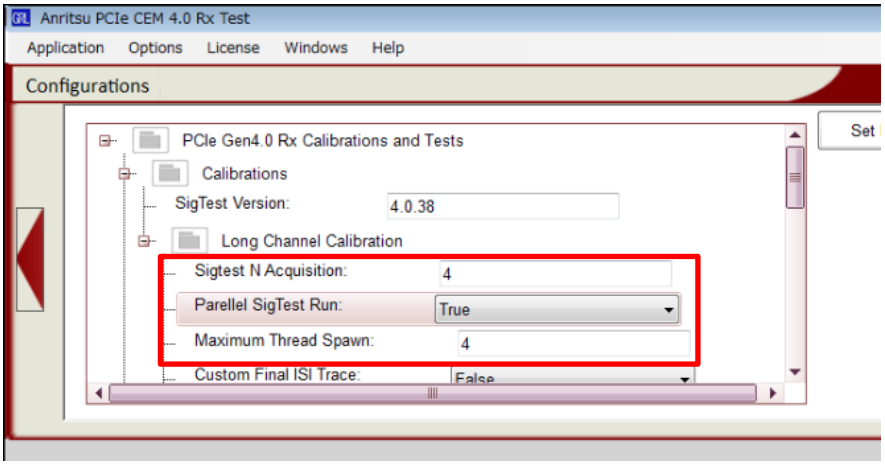
PCIe 4.0 Base Calibration Board Medium Loss configuration



6.2 How to shorten measurement time

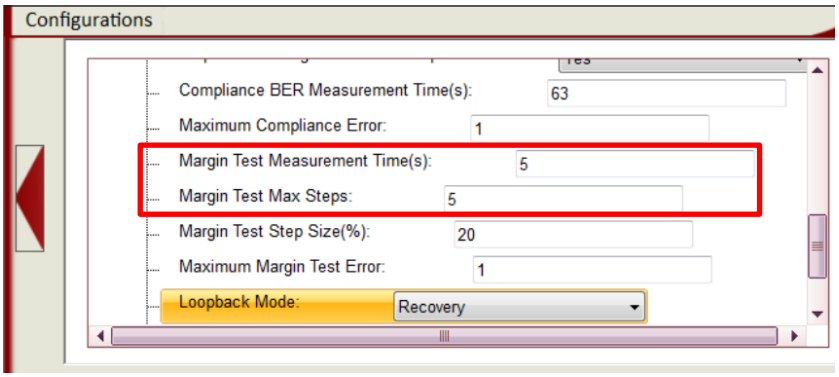
- EH / EW Calibration

Set **Sigtest N Acquisition** (basically set to **7** to comply with the test) to **4** or less. Also, set **Parallel SigTest Run** and **Maximum Thread Spawn** to **True** and **4**. In order to operate with these settings, CPU with at least CORE i5 and 4 cores is necessary. If the CPU has higher performance than this, it can process even more numbers in parallel. If a set value is larger than the number that can be processed by the CPU, a SigTest error may occur.

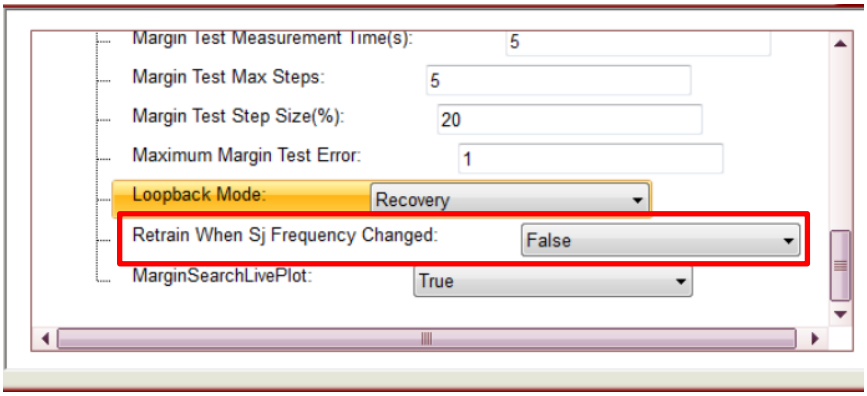


- BER and Margin Test

Decrease **Margin Test Measurement Time** and **Margin Test Max Steps**.



Set **Retrain When Sj Frequency Changed** to **False**.



6.3 Note on Apply Embedding

Basically, in order to comply with the PCIe standard:

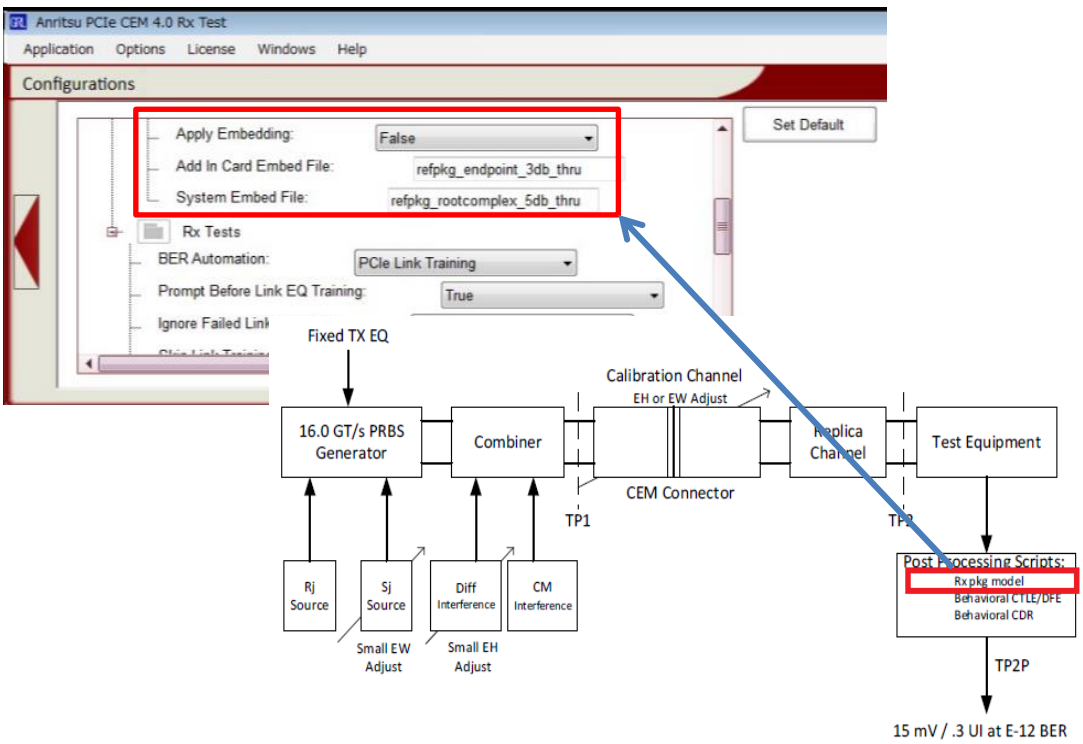
- Use a scope with the Embedded function installed.
- With the GRL software, set **Apply Embedding** (3 dB for AIC, 5 dB for System on the scope) to **True**.

This section explains an alternative (optional) procedure for performing calibration when using a scope without the Embedded function installed.

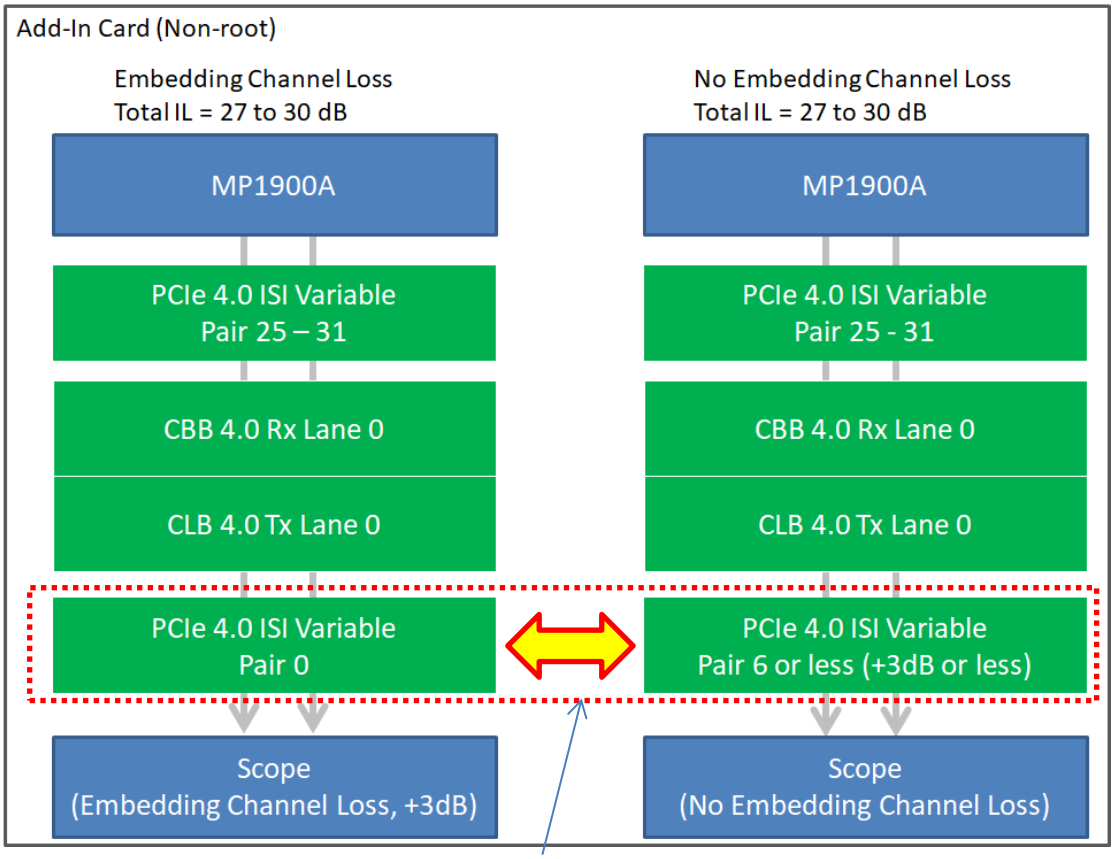
In order to use the Embed function, the InfiniiSim waveform transformation toolset (Option N5465A InfiniiSim) is required on the Keysight scope. If the option is not installed on the scope, set the parameter to **False**. Note that no option is required for Tektronix scopes.

Also, if the parameter is set to **False**, the IL value needs to be added on the physical loss board*. Specifically, for Add-in Card (Upstream, Non-root) calibration, Pair 6 or less* should be used instead of Pair 0. For System (Downstream, Root) calibration, Pair 26 should be used instead of Pair16 or less*. The connection diagrams are shown in Figure 6.3-1 and Figure 6.3-2.

*As pair number increases by 1, insertion Loss increases by 0.5 dB at 8 GHz. So Pair 6 insertion loss is 3 dB bigger than Pair 0. But, embedding loss and physical loss have different effects on actual EH/EW. If EH/EW calibration is failed, reduce Pair number. Note that this method is optional, and use of the embedding function is official procedure based on the PCIe standard.


Anritsu PCIe CEM 4.0 Rx Test
Application
Options
License
Windows
Help
Configurations
Set Default
Apply Embedding:
False
Add In Card Embed File:
refpkg_endpoint_3db_thru
System Embed File:
refpkg_rootcomplex_5db_thru
Rx Tests
BER Automation:
PCIe Link Training
Prompt Before Link EQ Training:
True
Fixed TX EQ
Calibration Channel
EH or EW Adjust
16.0 GT/s PRBS Generator
Combiner
Replica Channel
Test Equipment
CEM Connector
TP1
TP2
Rj Source
Sj Source
Diff Interference
CM Interference
Small EW Adjust
Small EH Adjust
Post Processing Scripts:
Rx pkg model
Behavioral CTLE/DFE
Behavioral CDR
TP2P
15 mV / .3 UI at E-12 BER

- Difference of connection between Embedding and No Embedding Channel Loss when calibrating EH/EW (Add-In Card).

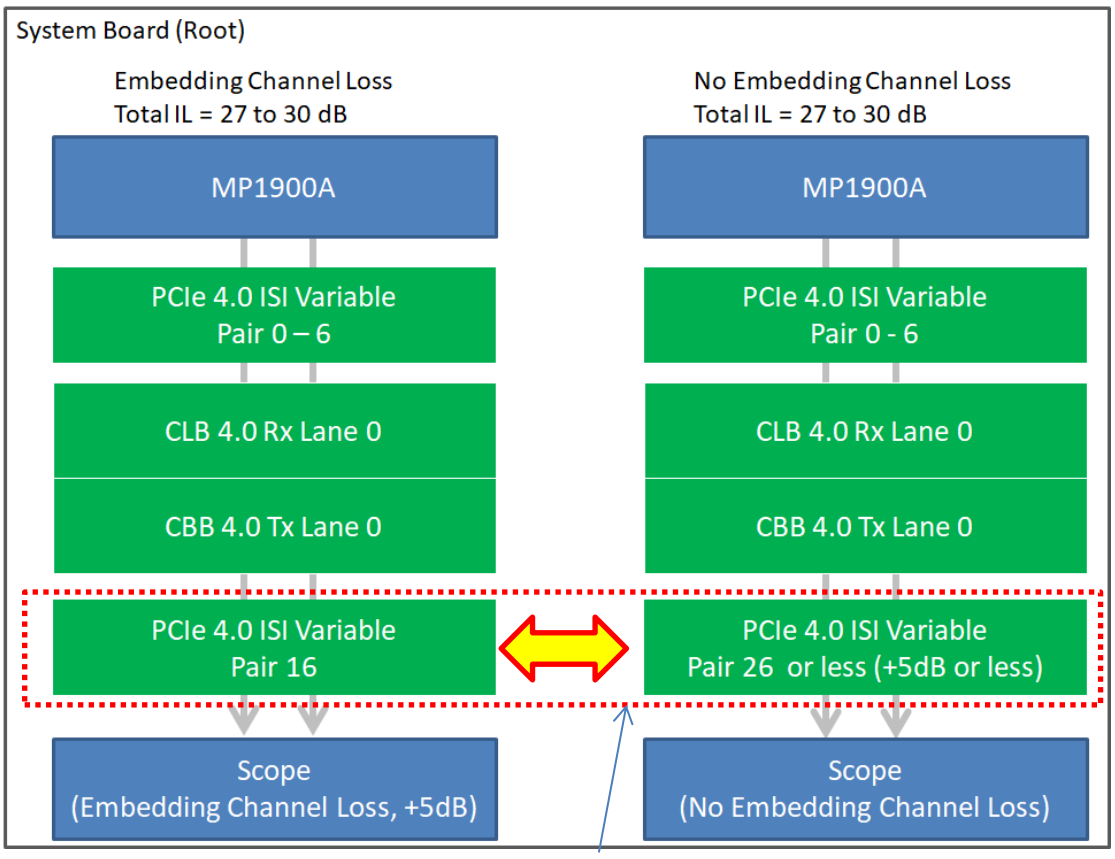


When operating with “No Embedding”, the physical IL (Insertion Loss) must be added on here.

Figure 6.3-1 Connection Diagram for Add-in Card (Non-root) Calibration

When measuring BER, the DUT is connected to CBB 4.0, so CLB 4.0 and later fixtures are not used. Therefore, by increasing/decreasing the Pair number of “PCIe 4.0 ISI Variable Pair 0” instead of “PCIe 4.0 ISI Variable Pair 25 - 31", it is possible to match the condition with the Embedding Channel Loss set on the scope.

- Difference of connection between Embedding and No Embedding Channel Loss when calibrating EH/EW (System Board).
- Note that this is setup for Base spec not CEM spec; therefore, the equipment connection is different from CEM spec.



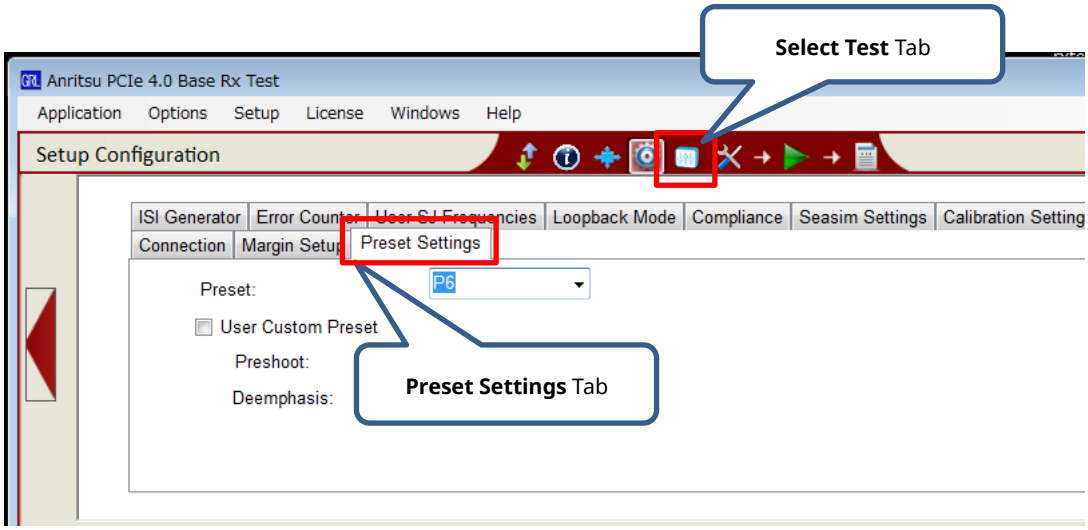
When operating with “No Embedding”, the physical IL (Insertion Loss) must be added on here.

Figure 6.3-2 Connection Diagram for System (Root) Calibration

6.4 Note on Apply Stress Voltage Param

To set all calibrated values to MP1900A, select **Apply Stress Voltage Param** on the **Select Test** tab.

To set only a desired value to MP1900A, select a value for **Preset** on the **Preset Settings** tab. In the case shown below, the calibrated value of only P6 will be set to MP1900A.



7. Troubleshooting

If you encounter any errors during calibration or testing, check as follows.

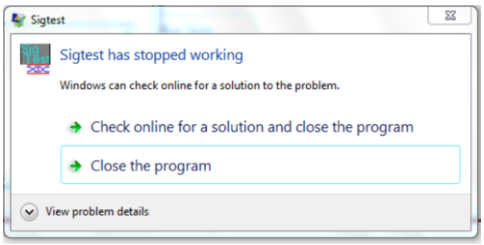
7.1 Calibration

7.1.1 In case of an error when calibrating **Amplitude**, **Preset**, **SJ** and **RJ**

- Check the RF connections. Especially, the connection polarity (Pos/Neg) and the trigger connections (PPG Aux Out and Scope Aux In) are easy to mistake.
- Check the software version. A different version of software may cause an unexpected error.
- Check the SigTest version. SigTest version needs to be 3.2.0 for Gen3 or 4.0.38 for Gen4. Also, this should be installed to the directory C:¥Program Files (x86). Do not change the installation directory from the default setting.

7.1.2 In case of a SigTest error when performing Long Channel Calibration

A SigTest error message is displayed and SigTest has stopped working when calibrating SJ, RJ and EH/EW. Since this message is no effect on calibration results, click **Close the program** to continue the calibration.



To avoid this message:

- Close all applications except the GRL software, MX190000A, MX183000A and scope applications. Especially when VNC is running, SigTest may not work properly.
- If you see this message frequently despite not running other applications on the PC, use another PC with the GRL software installed.

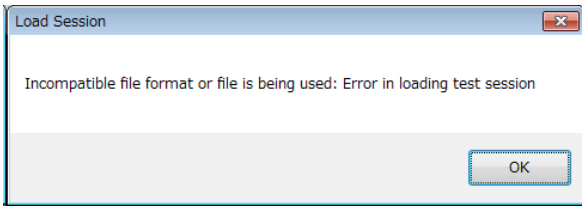
7.1.3 When Final Eye calibration cannot be succeeded

- Use the ISI Trace properly calibrated to 27 to 30 dB. It is recommended to use the calibration fixture distributed by the PCI-SIG.
- If any components (DC block, Power Divider, Attenuator and Adaptor) are attached to the Noise module output, remove them. These components may affect the waveform.

7.2 Others

7.2.1 When a session file cannot be loaded

- Close the folder where you installed the GRL software and saved PDF report file(s) because the loaded session file accesses and edits the folder.

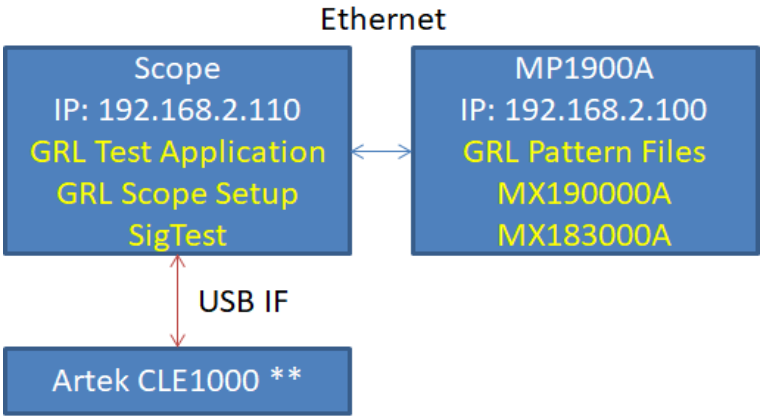


Appendix

A. Quick Startup Guide

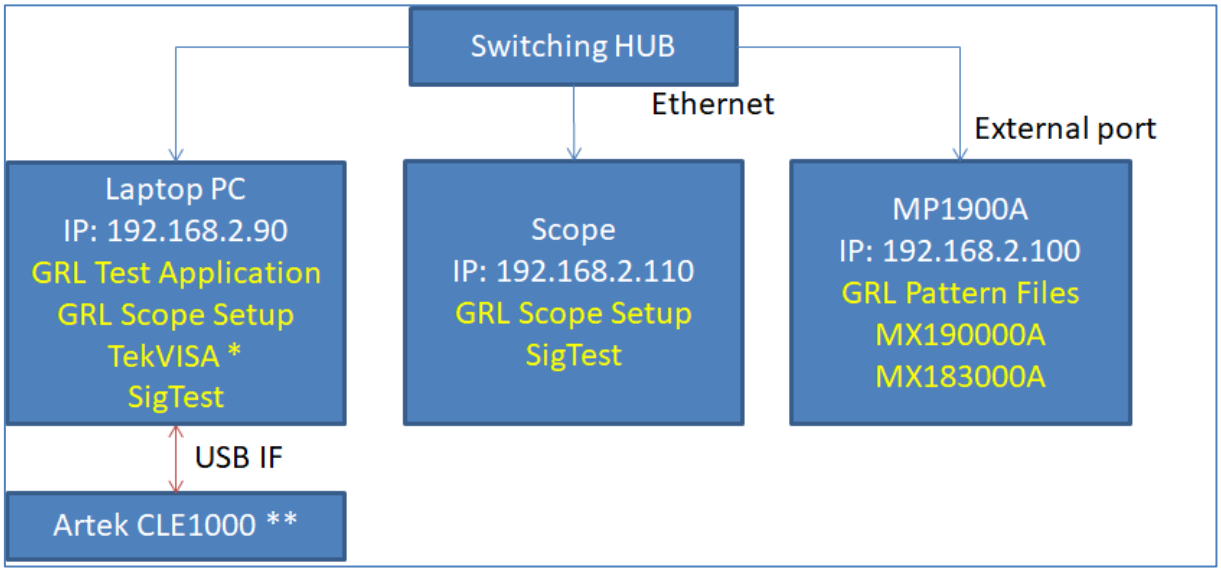
1. Connect instruments with Ethernet cables as shown below.
2. Set the IP addresses as shown below. These can be set in the Network and Sharing Center (Windows OS feature).
3. Install all applications as shown below (Yellow letters).

- Recommended connection



* Artek CEL1000 ISI Variable is not mandatory.

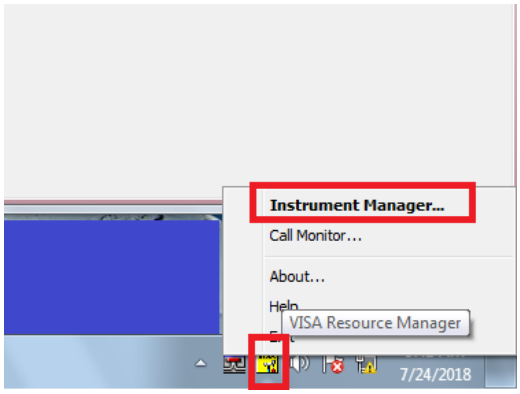
- Optional connection

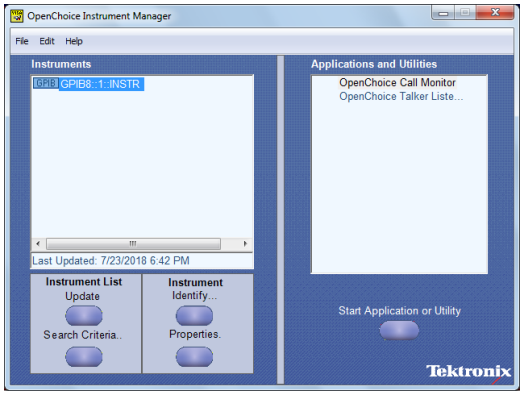


* TekVISA is needed to control Tektronix scopes. But, the PC on which TekVISA is installed cannot control Keysight scopes. Also, this configuration makes the remote control speed slower than the recommended configuration.
* Artek CEL1000 ISI Variable is not mandatory.

4. Launch application and configure equipment settings.
   Enter the scope address as below, and click . If the setting and connection are correct, the button will turn green.

Tektronix Scope
When the GRL software is installed on the laptop:
TCPIP0::192.168.2.110::inst0::INSTR
When the GRL software is installed on the scope: GPIBX::1::INSTR*
* Tektronix scope cannot use TCP/IP when the GRL software is installed on it. In this case, GPIB VISA should be set. The address can be checked using the VISA instruments Manager.





Keysight Scope
When the GRL software is installed on the laptop:
TCPIP0::192.168.2.110::inst0::INSTR
When the GRL software is installed on the scope: TCPIP0::localhost::inst0::INSTR

MX190000A: TCPIP0::192.168.2.100::5001::SOCKET*
MX183000A: TCPIP0::192.168.2.100::5000::SOCKET*
* Port numbers should be set for MX190000A and MX183000A.

ISI Generator: COM4*
* Enter the COM number which can be checked by the CLE-1000 software.
* The CLE1000 software must be closed when controlled by the GRL Software.