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Anritsu - GRL

PCIe 4.0 CEM Rx Test Application

Release Note

19th Edition

This software is released for PCIe CEM Rx Test.

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1. Released Software

The certificate software versions for Keysight / Tektronix Scope are shown in the table.

Edition	GRL CEM Rx Test Application	Anritsu MX190000A	Anritsu MX183000A	Scope	
				Keysight	Tektronix
19	V1.08.12	V8.03.14	V8.03.13	DSAZ634A V06.60.00403	DPO77002SX V10.11.0.30
18	V1.08.00	V8.03.00	V8.03.02	DSAZ634A V06.60.00403	DPO77002SX V10.11.0.30
17	V1.08.00	V8.03.00	V8.03.00	DSAZ634A V06.60.00403	DPO77002SX V10.11.0.30
16	V1.08.00	V8.02.00	V8.01.31	DSAZ634A V06.60.00403	DPO77002SX V10.11.0.30
15	V1.08.00	V8.01.31	V8.01.31	DSAZ634A V06.60.00403	DPO77002SX V10.11.0.30
14	V1.08.00	V8.00.30	V8.00.30	DSAZ634A V06.60.00403	DPO77002SX V10.11.0.30
13	V1.0.132	V8.00.30	V8.00.30	DSAZ634A V06.60.00403	DPO77002SX V10.11.0.30
12	V1.0.130	V7.02.30	V7.02.30	DSAZ634A V06.60.00403	DPO77002SX V10.11.0.30
11	V1.0.130	V5.01.00	V5.00.30	DSAZ634A V06.60.00403	DPO77002SX V10.11.0.30
10	V1.0.118	V4.10.20	V4.10.05	DSAZ634A V06.55.00702	DPO77002SX V10.1.0.34
09	V1.0.115	V4.09.50	V4.09.15	DSAZ634A V06.55.00702	DPO77002SX V10.1.0.34
08	V1.0.113	V4.09.41	V4.09.15	DSAZ634A V06.55.00702	DPO77002SX V10.1.0.34
07	V1.0.110	V4.03.12	V4.03.15	DSAZ634A V06.40.00714	DPO75902SX V10.0.8.138
06	V1.0.86	V4.03.12	V4.03.15	DSAZ634A V06.40.00714	DPO75902SX V10.0.8.138
05	V1.0.86	V4.03.12	V4.03.15	DSAZ634A V06.40.00714	DPO73304DX 10.8.3 Build 3
	V1.0.86	V4.02.10	V4.02.10	DSAZ634A V06.40.00714	DPO73304DX 10.8.3 Build 3
	V1.0.86	V4.01.32	V4.00.08	DSAZ634A V06.40.00714	DPO73304DX 10.8.3 Build 3
04	V1.0.27	V3.01.10	V3.07.12	DSAZ634A V06.20.01101	DPO73304DX 10.8.3 Build 3
03	V1.0.27	V3.00.05	V3.06.16	DSAZ634A V06.20.01101	DPO73304DX 10.8.3 Build 3
02	V1.0.27	V2.05.08	V3.05.00	DSAZ634A V06.20.01101	DPO73304DX 10.8.3 Build 3
01	V1.0.23	V2.05.08	V3.05.00	DSAZ634A V06.20.01101	DPO73304DX 10.8.3 Build 3

2. Peripheral Devices

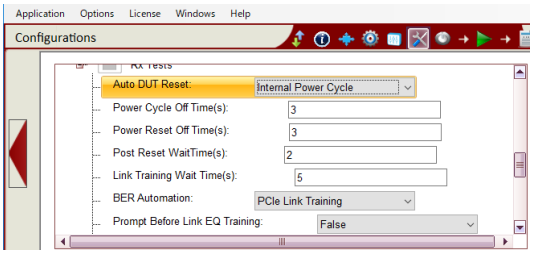
The peripheral devices of the application are shown in the table.

Model	Name
MP1900A	Signal Quality Analyzer-R
MU181000B	12.5GHz 4port Synthesizer (Option02 is required.)
MU181500B	Jitter Modulation Source
MU195020A or MU196020A	21G/32G bit/s SI PPG or PAM4 PPG
MU195040A	21G/32G bit/s SI ED
MU195050A	Noise Generator

For the installation position of the mainframe, refer to the Anritsu website (https://www.anritsu.com).

3. Added Functions

Edition	Function	Description
19	Calibration Tx Link EQ Tests	Adds parameters for DM Optimization Adds "Skip if waveform exist" to allow efficiency in retesting without recapturing all preset waveforms
11	Calibration MOI	Adds "Preset Scan on ISI Calibration". The default configuration is 'True'. Select 'True' to enable rescan of presets to be performed for each ISI trace that has been changed. Or, select 'False' to enable the "Preset EQ Optimization" calibration option in the calibration/test list. Defaults the CTLE scan range to 8.5 – 10.5. Updates MOI.
10	Calibration	Defaults "CTLE Scan For ISI Calibration" to "On" Defaults "ISI Start Trace" to "30" and "ISI End Trace" to "27" dB
09	All Calibration	Turns OFF PPG output after testing complete and when changing ISI Supports ISI scan method both ascending and descending.
08	All	Supports MU196020A PAM4 PPG
07	Tx EQ response time test	Updates MOI and software to reflect pass/fail based on electrical timing only.
05	DM Measurement	A DM (Differential Mode Noise) calibration mode is added, which converts DM from Vrms to Vpp. Normally use with set to **Vrms to Vpp**. In Edition 04 or earlier, recalibration of already-calibrated DM is not necessary because the Final EH / EW values are not affected.

	Auto Scale	This function turns off the Auto Scale function for Scope to shorten the time required for Initial Tx EQ and Tx LEQ response time test. When the function is set to **True**, input the amplitude of the Data output of the DUT in the Vertical Range (scale of the vertical axis of Scope) with a value equivalent to Differential Input. The recommended value for Vertical Range is 0.5 Vpp because the Power Divider practically attenuates the data output of the DUT by 6 dB. This software may fail in waveform decoding if the amplitude is too small for the scale or beyond the scale.
	Auto DUT Reset	This function resets the DUT automatically during Compliance Test. To use this function, follow the steps below: a. In the **Auto DUT Reset** box, select **Internal Power Cycle** or **Internal Power Reset**. b. Set up Anritsu Z2025A PCIe CBB Controller according to the Z2025A Installation Guide. c. In the **Prompt Before Link EQ Training** box, select **False**.  Power Cycle Off Time: Sets the time to turn off the CBB power. Power Reset Off Time: Sets the time to send the Power Reset signal to the DUT. Post Reset Wait Time: Sets the time to wait after turning on Reset or Cycle before Link Training is started.
	Link Training Wait Time	This function sets the time to wait after Link Training is ready to start before it is started.
	Link Training CTLE Gain	Select a CTLE value option to set for SI ED. If the DUT Tx Insertion Loss is large, adjust the value.
	Apply CM and CM calibration	The Apply CM function sets whether to apply CM (Common Mode Noise) to Rx LEQ Test. CM Calibration is added as an option for Long Channel Calibration and needs to be performed before using the Apply CM function.

	Log Link Training	This function saves an LTSSM Log file to the following directory of MP1900A every time Link Training is performed. "C:¥PCIE_LTSSM_LOG"
	CTLE and Preset optimization step	This function sets the CTLE range, from 6 to 12 dB in 0.25 dB steps, when performing calibration for searching for an optimum CTLE value.
		The following change has been made to the order of increasing ISI Channel (Insertion Loss) when searching for an optimum CTLE value. Before: 27dB -> 28dB -> 30dB After: 27 dB -> 27.5 dB -> 28 dB -> --- -> 29.5 dB -> 30 dB

4. Bug Fixes

Edition	Item	Description
10	PPG Final Preset setting issue	Fixes config "PPG Final Preset" not being applied when changed to fixed preset.
	JTOL display issue	Updates framework to fix Jitter tolerance plot display incorrect JTOL line.
05	Tx LEQ Response time test and Rx LEQ test failed occasionally.	Tx LEQ Response time test and Rx LEQ test failed occasionally.
01	Sometimes, Preset calibration fails with Tektronix scope.	Calibration fails when attempting to execute Preset calibration. Bug occurs in GRL software version 1.00.23 and Tektronix scope software version 10.8.3.

5. Remaining Known Bugs

None

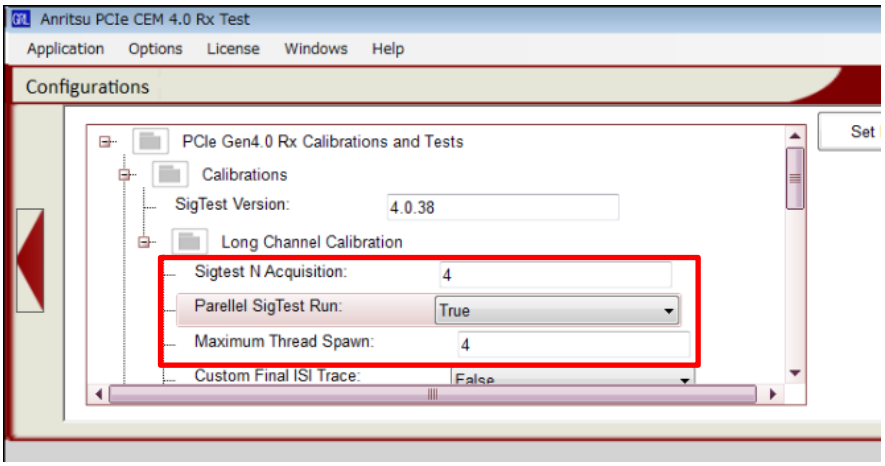
6. Usage Notes

The precautions for using each version are described below.

6.1 How to shorten measurement time

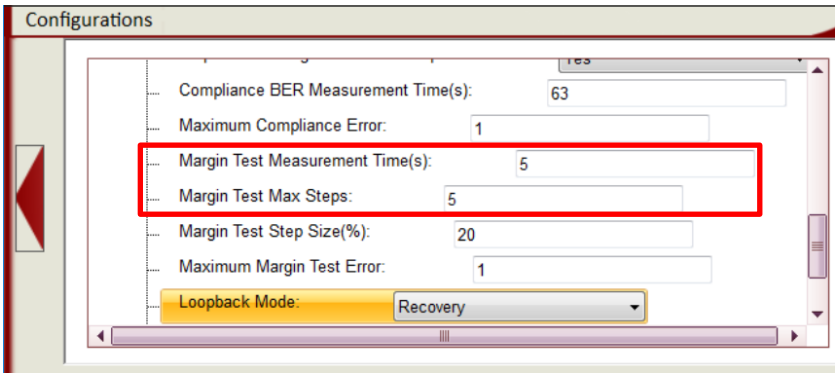
- EH / EW Calibration

Set **Sigtest N Acquisition** (basically set to **7** to comply with the test) to **4** or less. Also, set **Parallel SigTest Run** and **Maximum Thread Spawn** to **True** and **4**. In order to operate with these settings, CPU with at least CORE i5 and 4 cores is necessary. If the CPU has higher performance than this, it can process even more numbers in parallel. If a set value is larger than the number that can be processed by the CPU, a SigTest error may occur.

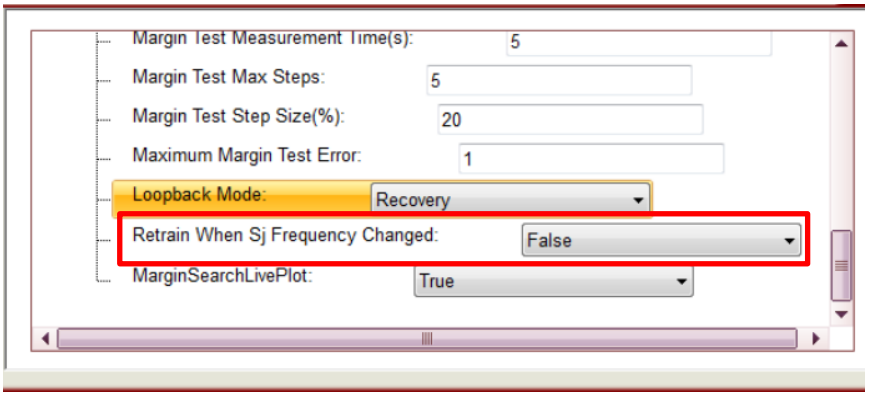


- BER and Margin Test

Decrease **Margin Test Measurement Time** and **Margin Test Max Steps**.



Set **Retrain When Sj Frequency Changed** to **False**.



6.2 Note on Apply Embedding

Basically, in order to comply with the PCIe standard:

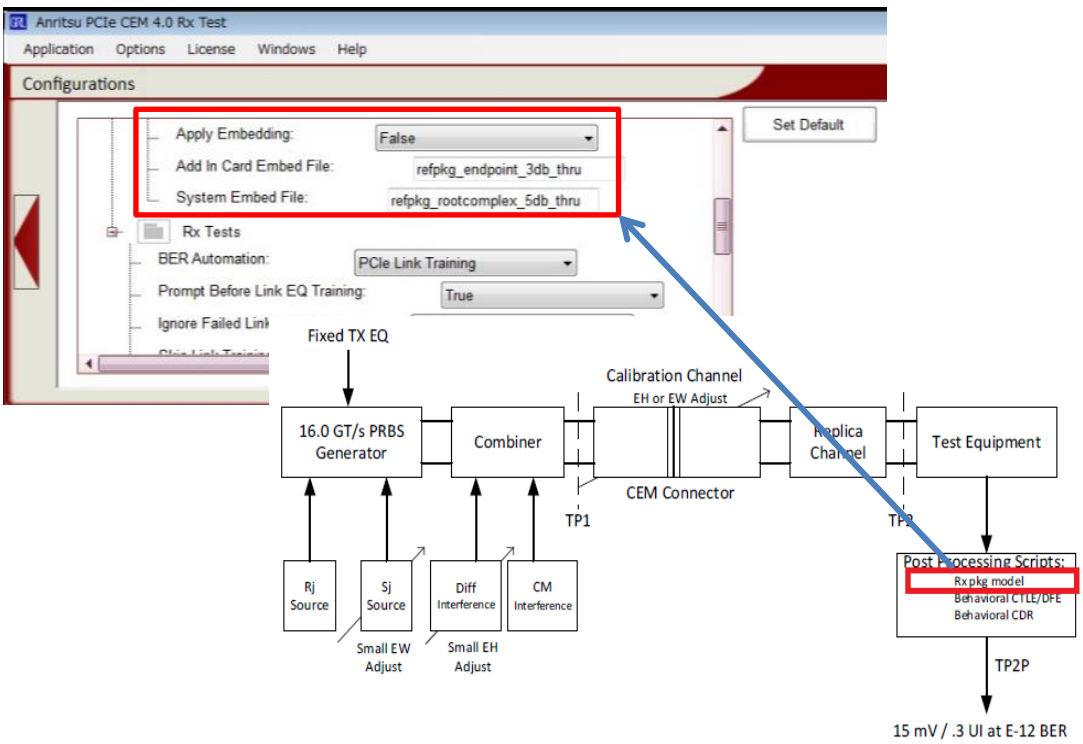
- Use a scope with the Embedded function installed.
- With the GRL software, set **Apply Embedding** (3 dB for AIC, 5 dB for System on the scope) to **True**.

This section explains an alternative (optional) procedure for performing calibration when using a scope without the Embedded function installed.

In order to use the Embed function, the InfiniiSim waveform transformation toolset (Option N5465A InfiniiSim) is required on the Keysight scope. If the option is not installed on the scope, set the parameter to **False**. Note that no option is required for Tektronix scopes.

Also, if the parameter is set to **False**, the IL value needs to be added on the physical loss board*. Specifically, for Add-in Card (Upstream, Non-root) calibration, Pair 6 or less* should be used instead of Pair 0. For System (Downstream, Root) calibration, Pair 26 should be used instead of Pair16 or less*. The connection diagrams are shown in Figure 6.2-1 and Figure 6.2-2.

*As pair number increases by 1, insertion Loss increases by 0.5 dB at 8 GHz. So Pair 6 insertion loss is 3 dB bigger than Pair 0. But, embedding loss and physical loss have different effects on actual EH/EW. If EH/EW calibration is failed, reduce Pair number. Note that this method is optional, and use of the embedding function is official procedure based on the PCIe standard.


Anritsu PCIe CEM 4.0 Rx Test
Application
Options
License
Windows
Help
Configurations
Set Default
Apply Embedding:
False
Add In Card Embed File:
refpkg_endpoint_3db_thru
System Embed File:
refpkg_rootcomplex_5db_thru
Rx Tests
BER Automation:
PCIe Link Training
Prompt Before Link EQ Training:
True
Fixed TX EQ
Calibration Channel
EH or EW Adjust
16.0 GT/s PRBS Generator
Combiner
Replica Channel
Test Equipment
CEM Connector
TP1
TP2
Rj Source
Sj Source
Diff Interference
CM Interference
Small EW Adjust
Small EH Adjust
Post Processing Scripts:
Rx pkg model
Behavioral CTLE/DFE
Behavioral CDR
TP2P
15 mV / .3 UI at E-12 BER

- Difference of connection between Embedding and No Embedding Channel Loss when calibrating EH/EW (Add-In Card).

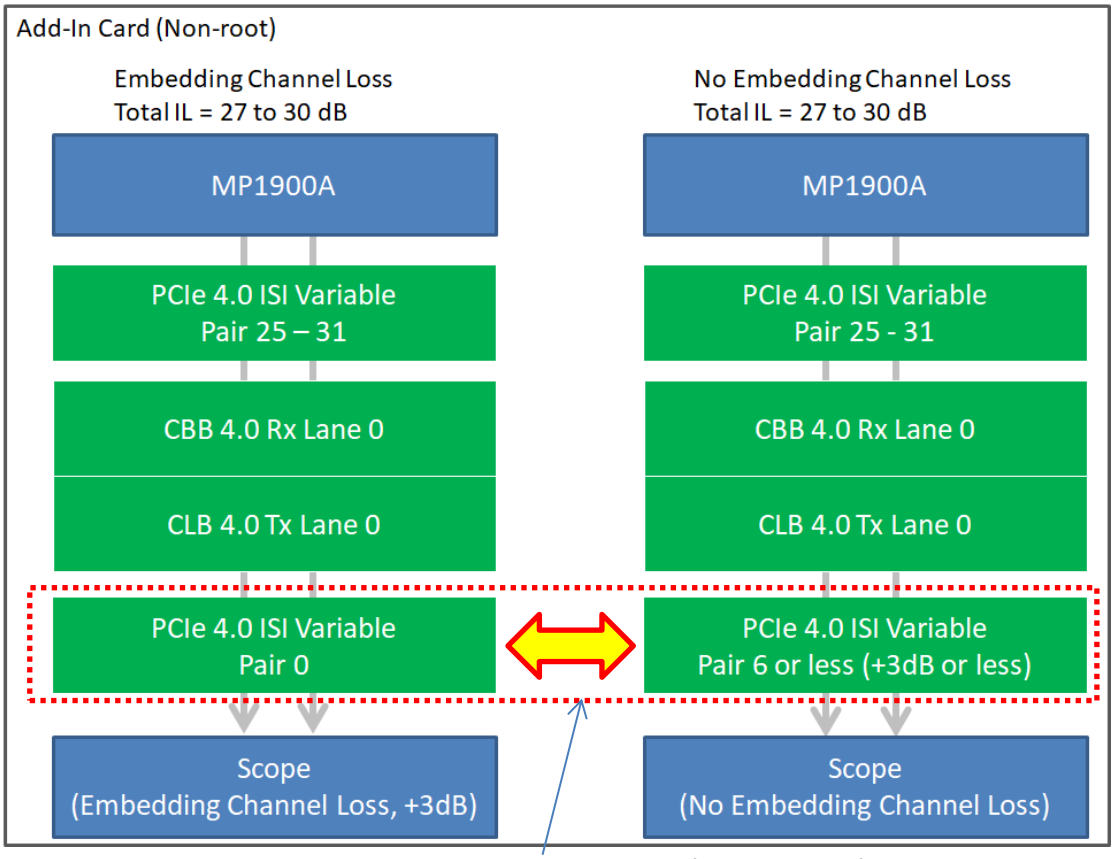
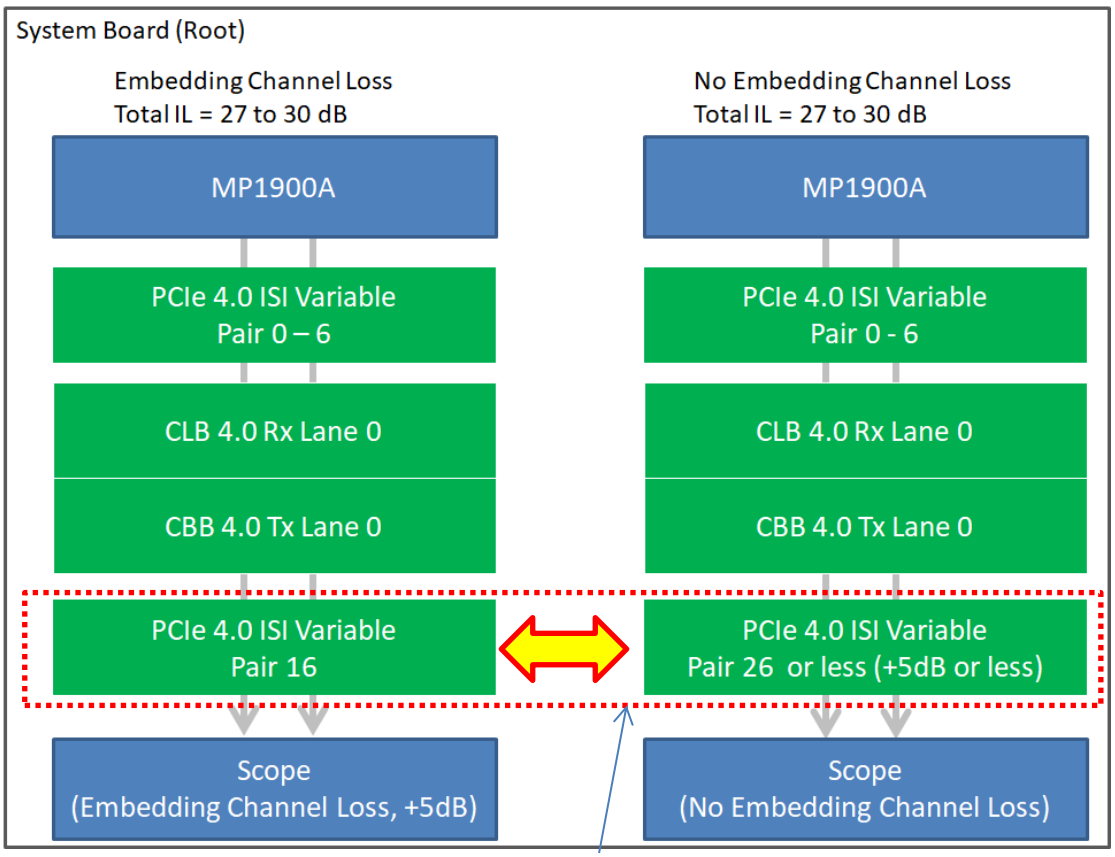


Figure 6.2-1 Connection Diagram for Add-in Card (Non-root) Calibration

When measuring BER, the DUT is connected to CBB 4.0, so CLB 4.0 and later fixtures are not used. Therefore, by increasing/decreasing the Pair number of “PCIe 4.0 ISI Variable Pair 0” instead of “PCIe 4.0 ISI Variable Pair 25 - 31", it is possible to match the condition with the Embedding Channel Loss set on the scope.

- Difference of connection between Embedding and No Embedding Channel Loss when calibrating EH/EW (System Board).

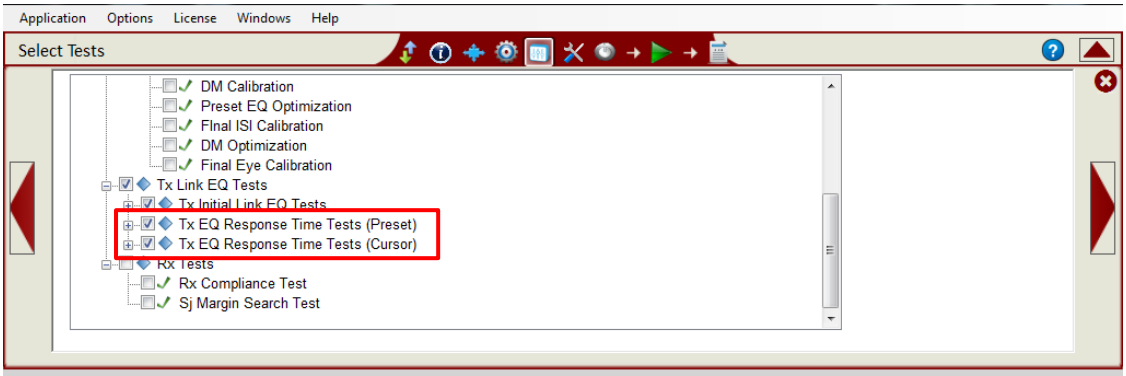


When operating with “No Embedding”, the physical IL (Insertion Loss) must be added on here.

Figure 6.2-2 Connection Diagram for System (Root) Calibration

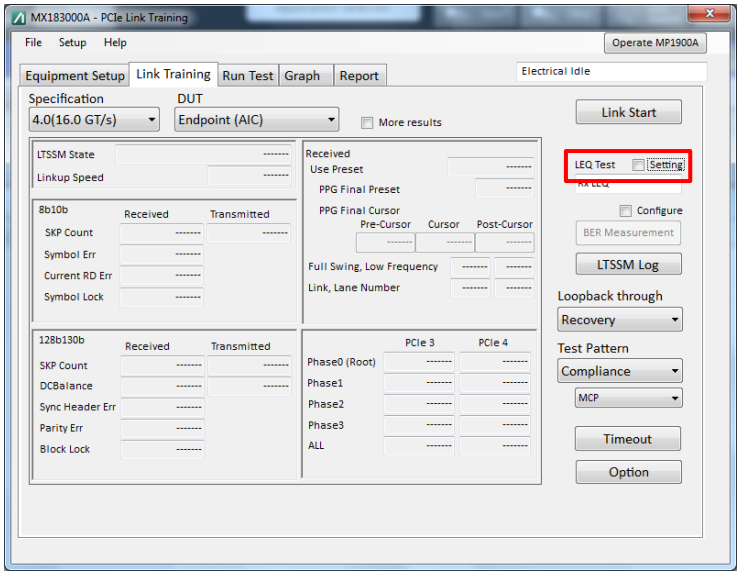
6.3 Note on Link EQ Response time test

Perform a test with **Tx EQ Response time (Preset)** first and then perform it with **Tx EQ Response Time (Cursor)**.
When starting the test with **Tx EQ Response Time (Preset)**, the cursor values corresponding to Preset are notified from a DUT, and they are saved in MP1900A.
These values are required for testing with **Tx EQ Response Time (Cursor)**.

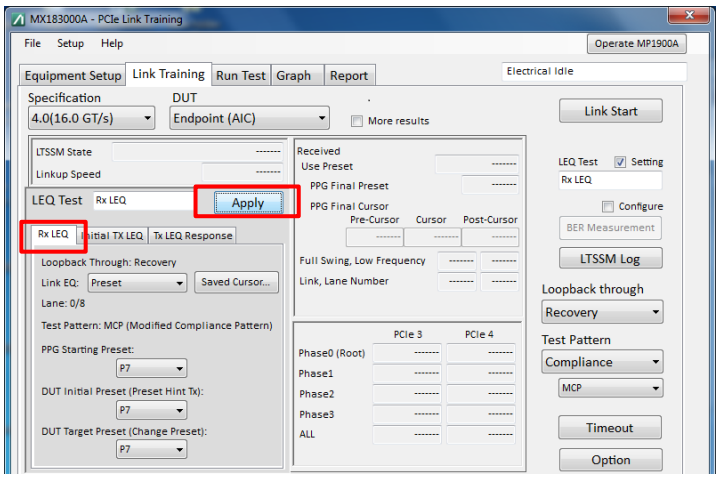


To skip the test with **Tx EQ Response time (Preset)**:
Perform link training follow the below steps to acquire cursor values from a DUT.
When replace the DUT to test **Tx EQ Response time (Cursor)**, the steps are required again.

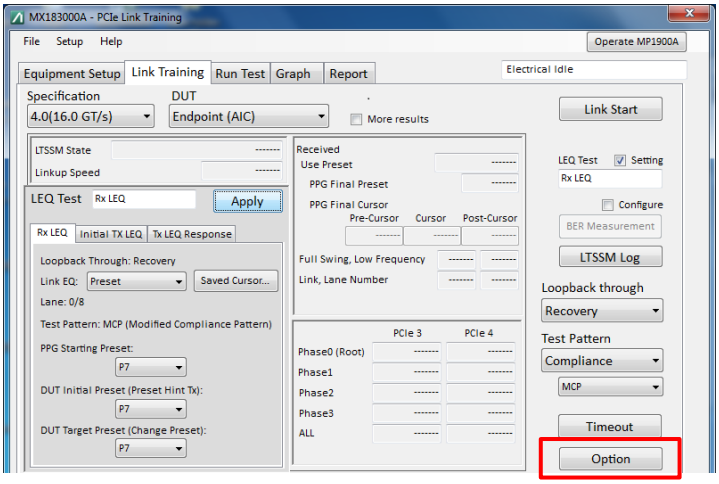
a. Launch MX183000A with PCIe Link Training application.
b. Initialize the PCIe Link Training application.
c. Click on **LEQ Test Setting** check box.



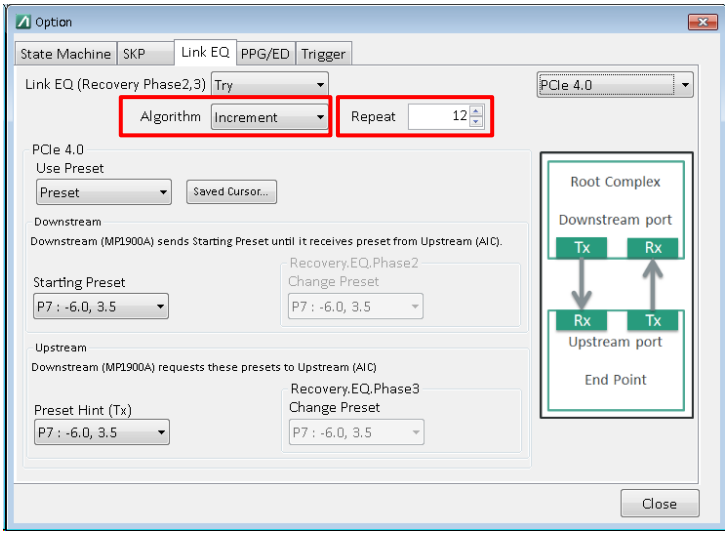
d. Select **Rx LEQ** tab and click on **Apply** button.



e. Click on **Option** button.

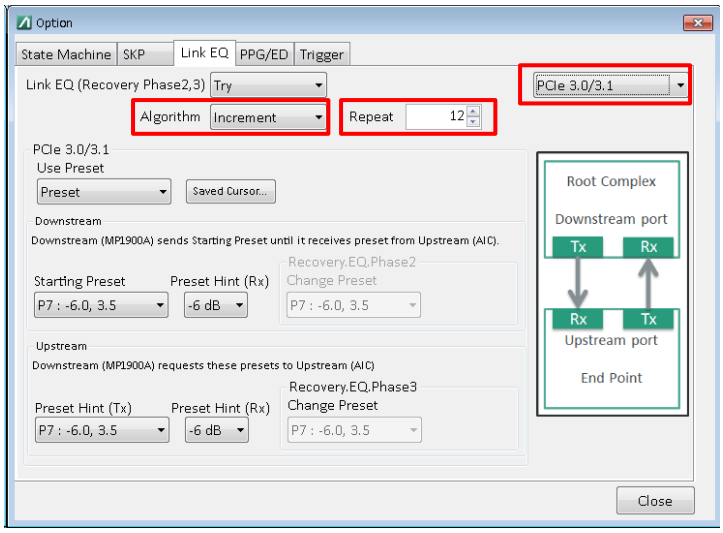


f. Set **Algorithm** to **increment** and set **Repeat** to **12** on Link EQ tab.

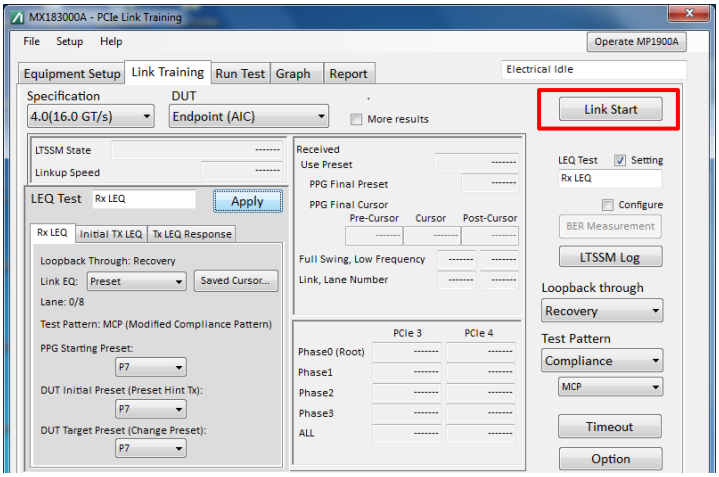


g. Set specification to **PCIe 3.0/3.1** on **Link EQ tab.**

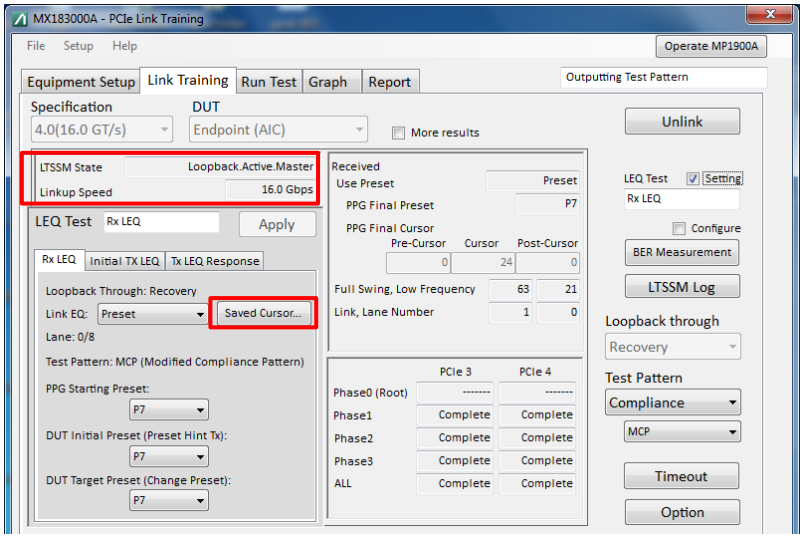
h. Set **Algorithm** to **increment** and set **Repeat** to **12** on Link EQ tab.



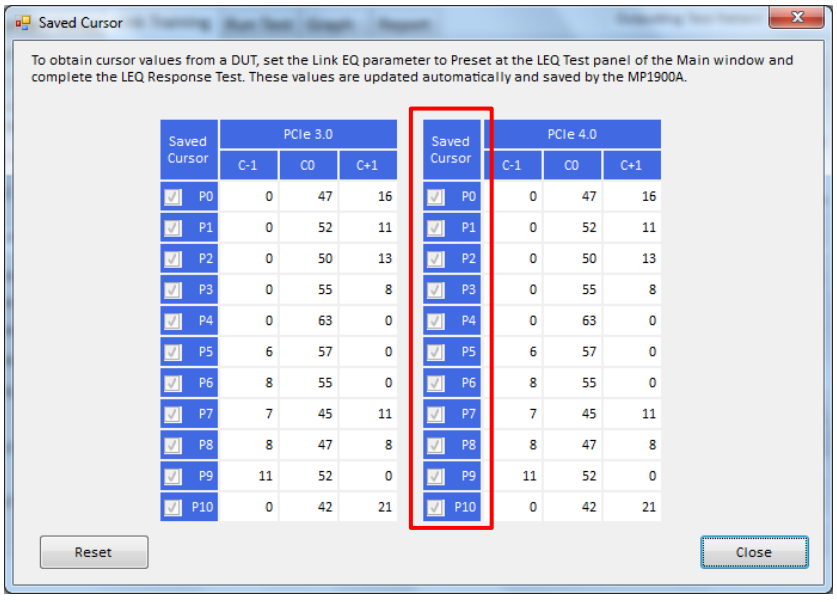
i. Reset DUT and click on **Link Start** button.



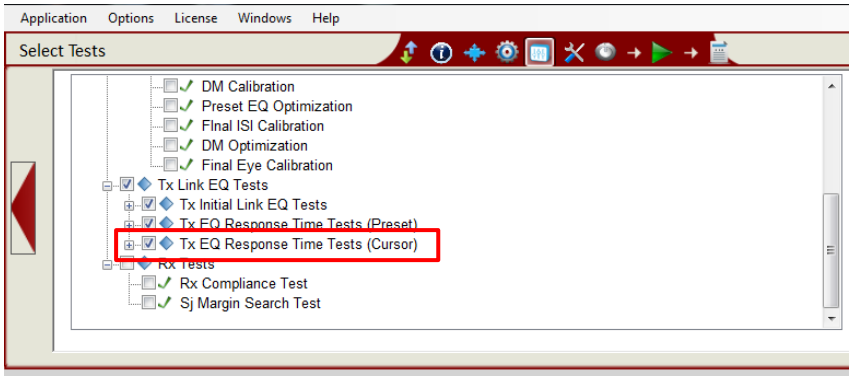
j. When **LTSSM State** is **Loopback.Active.Master**, click on **Saved Cursor** button on LEQ Test window.



k. If All **Saved Cursor check boxes** are **ON**, the steps are finished.



l. Launch GRL application and start **Tx EQ Response time (Cursor)**.



7. Troubleshooting

If you encounter any errors during calibration or testing, check as follows.

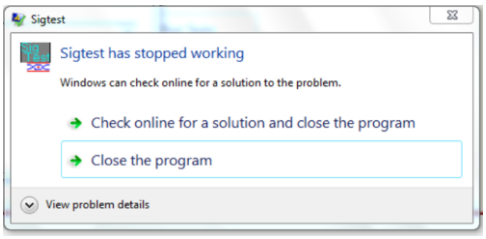
7.1 Calibration

7.1.1 In case of an error when calibrating **Amplitude**, **Preset**, **SJ** and **RJ**

- Check the RF connections. Especially, the connection polarity (Pos/Neg) and the trigger connections (PPG Aux Out and Scope Aux In) are easy to mistake.
- Check the software version. A different version of software may cause an unexpected error.
- Check the SigTest version. SigTest version needs to be 3.2.0.3 for Gen3 or 4.0.51 for Gen4. Also, this should be installed to the directory C:¥Program Files (x86). Do not change the installation directory from the default setting.

7.1.2 In case of a SigTest error when performing Long Channel Calibration

A SigTest error message is displayed and SigTest has stopped working when calibrating SJ, RJ and EH/EW. Since this message is no effect on calibration results, click **Close the program** to continue the calibration.



To avoid this message:

- Close all applications except the GRL software, MX190000A, MX183000A and scope applications. Especially when VNC is running, SigTest may not work properly.
- If you see this message frequently despite not running other applications on the PC, use another PC with the GRL software installed.

7.1.3 When Final Eye calibration cannot be succeeded

- Use the ISI Trace properly calibrated to 27 to 30 dB. It is recommended to use the calibration fixture distributed by the PCI-SIG.
- If any components (DC block, Power Divider, Attenuator and Adaptor) are attached to the Noise module output, remove them. These components may affect the waveform.

7.2 Tx and Rx LEQ test

7.2.1 When Tx LEQ Response cursor test cannot be started

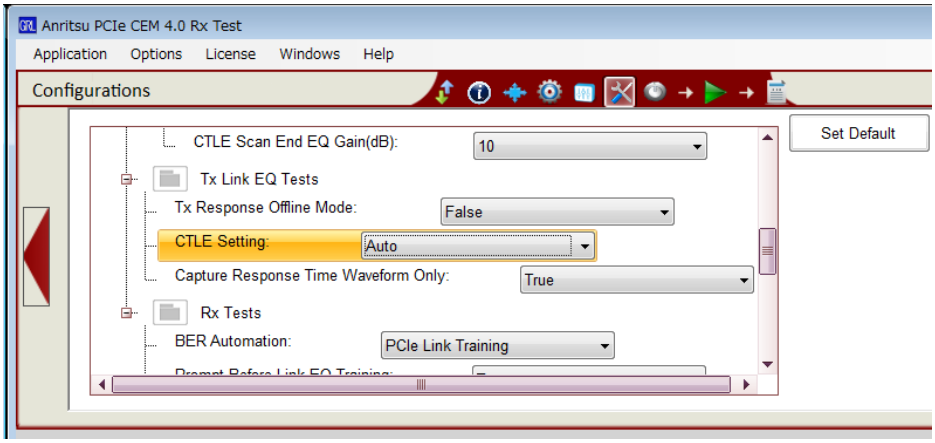
- Before starting Rx Test, complete all calibrations or load a calibrated session file.

7.2.2 In case of a Link Training error when testing Tx LEQ Response

- Check the RF connections. Especially, the trigger connections (PPG Aux Out and Scope Aux In) are easy to mistake.
- If DUT Tx has large insertion loss, adjust the MP1900A CTLE value in the MX183000A screen. Refer to Appendix C for adjusting CTLE.

7.2.3 In case of a decode error when testing Tx LEQ Reponses time

- On the **Configurations** tab, set **CTLE Setting** to **Auto**.

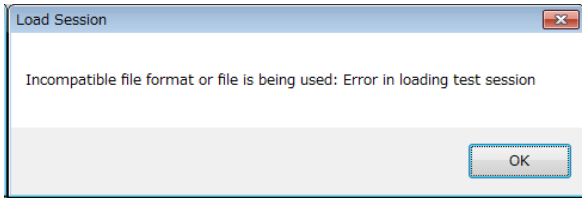


- When DUT Tx has large insertion loss, a decode error sometimes occurs because the Eye is completely closed on the scope even if the CTLE and DFE functions are applied.

7.3 Others

7.3.1 When a session file cannot be loaded

- Close the folder where you installed the GRL software and saved PDF report file(s) because the loaded session file accesses and edits the folder.



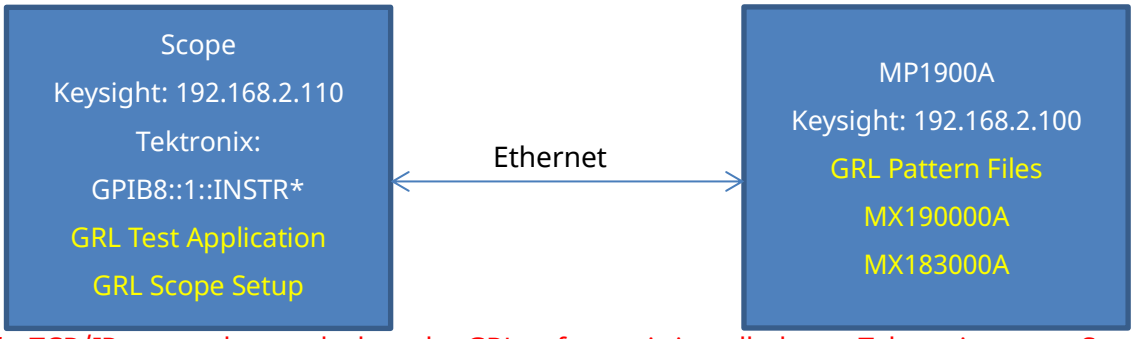
- While recalling the session file on CEM spec takes several minutes, it does not mean that the computer is frozen. Wait until the recalling is completed. This function recalls large waveform files which are acquired by Tx initial EQ and Tx LEQ Response time test.

Appendix

A. Quick Startup Guide

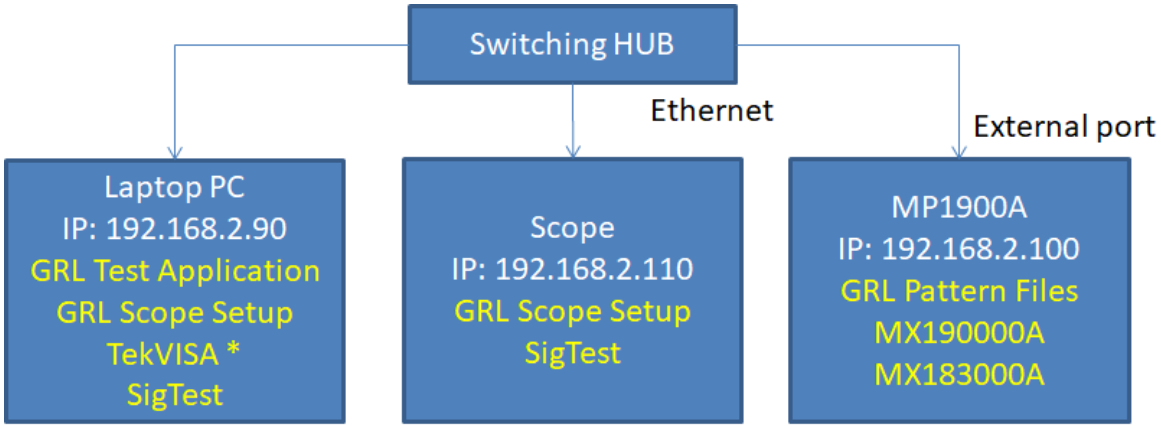
1. Connect instruments with Ethernet cables as shown below.
2. Set the IP and GPIB addresses as shown below. These can be set in the Network and Sharing Center (Windows OS feature).
3. Install all applications as shown below (Yellow letters).

- Recommended connection



* TCP/IP cannot be used when the GRL software is installed on a Tektronix scope. Set the GPIB address as “GPIB8::1::INSTR”.

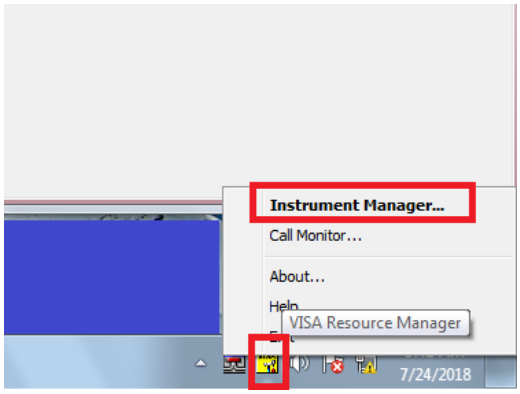
- Optional connection

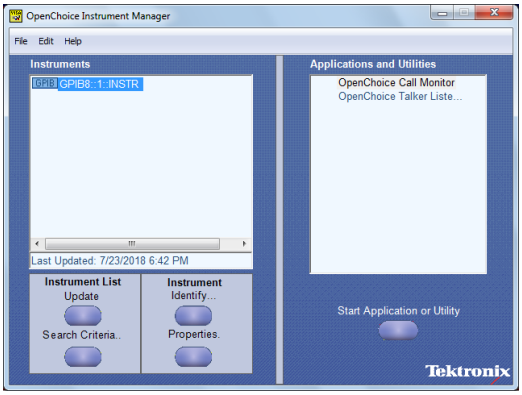


* TekVISA is needed to control Tektronix scopes. But, the PC on which TekVISA is installed cannot control Keysight scopes. Also, this configuration makes the remote control speed slower than the recommended configuration.

4. Launch application and configure equipment settings.
   Enter the scope address as below, and click . If the setting and connection are correct, the button will turn green.

Tektronix Scope
When the GRL software is installed on the laptop:
TCPIP0::192.168.2.110::inst0::INSTR
When the GRL software is installed on the scope: GPIBX::1::INSTR*
* Tektronix scope cannot use TCP/IP when the GRL software is installed on it. In this case, GPIB VISA should be set. The address can be checked using the VISA instruments Manager.





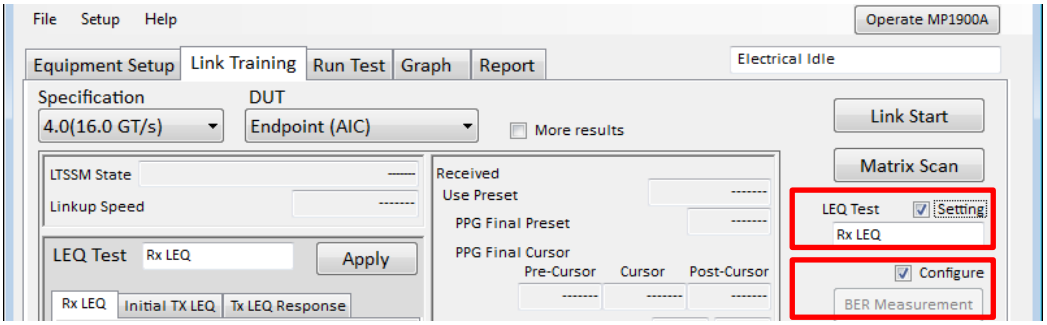
Keysight Scope
When the GRL software is installed on the laptop:
TCPIP0::192.168.2.110::inst0::INSTR
When the GRL software is installed on the scope: TCPIP0::localhost::inst0::INSTR

MX190000A: TCPIP0::192.168.2.100::5001::SOCKET*
MX183000A: TCPIP0::192.168.2.100::5000::SOCKET*
* Port numbers should be set for MX190000A and MX183000A.

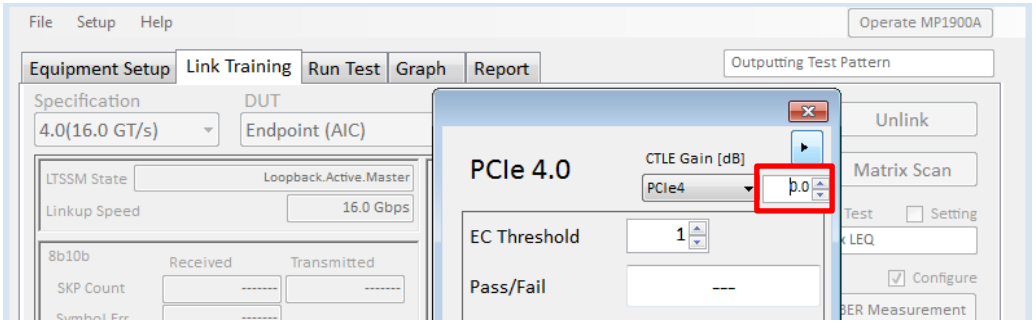
B. Before beginning Tx LEQ response time test

Before beginning Tx LEQ response time test, it is recommended to adjust the **CTLE Gain** value in MX183000A. Especially, this is efficient when DUT Tx has a large Insertion Loss like a System board.
Also, in case of a link training error and/or bit error, adjust the **CTLE Gain** value.

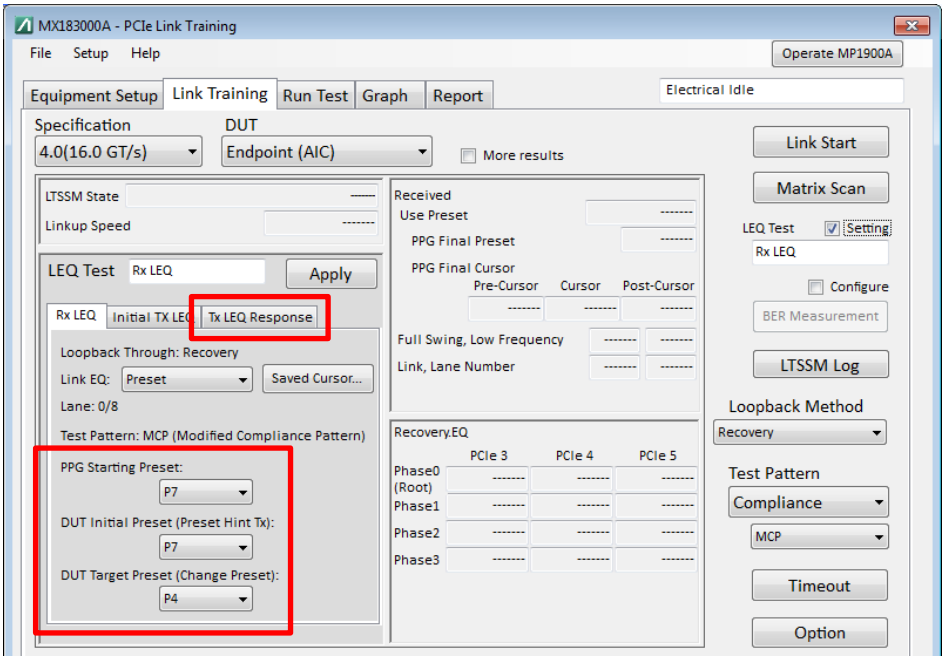
a. In MX183000A, display the LEQ test settings and BER Measurement screen.



b. Set **CTLE Gain** to **0** (zero) on the BER Measurement panel.

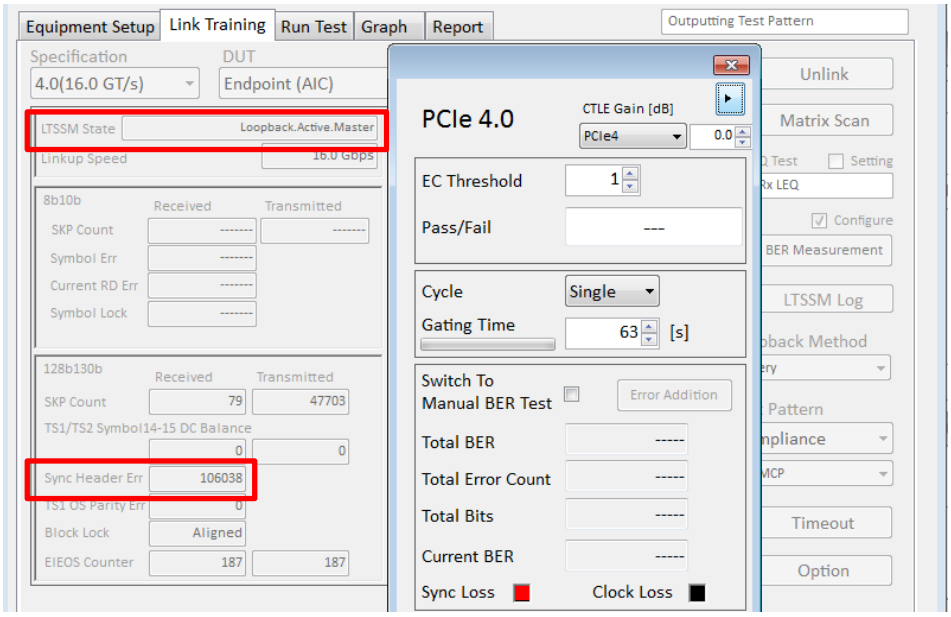


c. On the **Tx LEQ Response** tab of the LEQ test pane, set **PPG Starting Preset** to **7**, **DUT Initial Preset** to **7** and **Target Preset** to **P4**.

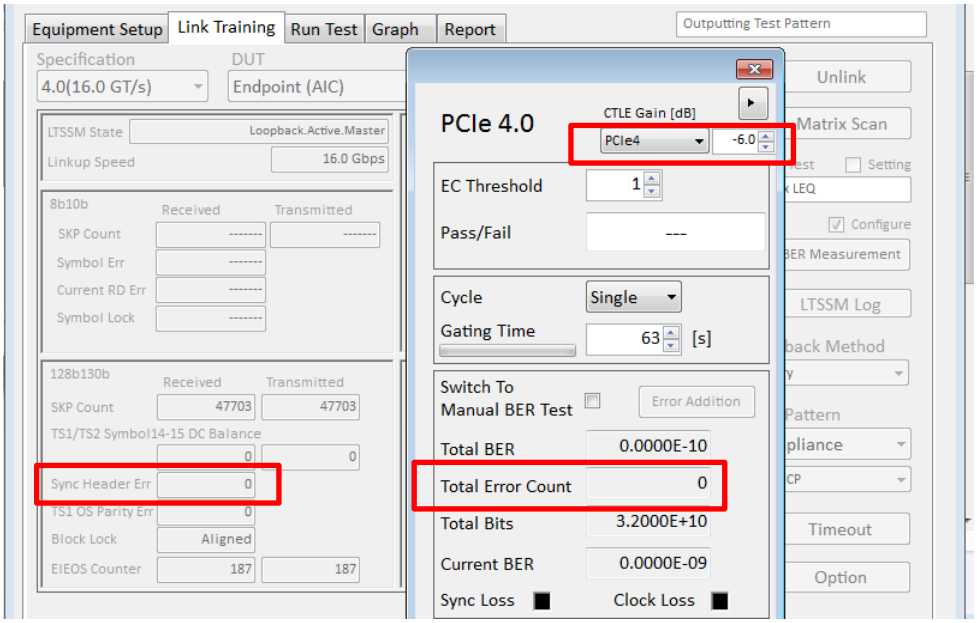


d. Click **Link Start**.

e. If the following conditions are met, adjust the **CTLE Gain** value. If there is no error, this procedure is assumed already to be done, so proceed to step h.
- **LTSSM State** is not **Loopback.Active.Master**.
- **Sync Header Err** is other than **0** (zero).



f. Increment the **CTLE Gain** value, and run Link Training again until **Sync Header Err** becomes **0** (zero) and **Total Error Count** becomes **0** (zero). In this case, it is considered to be error free with -6 dB.



g. Repeat steps d to f with DUT target **Preset P7**.

h. After adjusting the **CTLE Gain** value, close the MX183000A application and return to the selector screen. The **CTLE Gain** value is stored on the MX183000A. And, start GRL Tx LEQ response time test again.