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Anritsu - GRL

PCIe 3.0 CEM Rx Test Application

Release Note

20th Edition

This software is released for PCIe CEM Rx Test.

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1. Released Software

The certificate software versions for Keysight / Tektronix Scope are shown in the table.

	GRL CEM Rx	Anritsu	Anritsu	Scope	-
Edition	Test Application	MX190000A	MX183000A	Keysight	Tektronix
20	V1.10.00	V9.00.01	V9.00.00	DSAZ634A	DPS77004SX
				V06.60.00403	V10.11.0.30
19	V1.08.00	V8.03.14	V8.03.13	DSAZ634A	DPS77004SX
18	V1.08.00	V8.03.00	V8.03.02	V06.60.00403 DSAZ634A	V10.11.0.30 DPS77004SX
10	v1.08.00	vo.05.00	V8.03.02	V06.60.00403	V10.11.0.30
17	V1.08.00	V8.03.00	V8.03.00	DSAZ634A	DPS77004SX
				V06.60.00403	V10.11.0.30
16	V1.08.00	V8.02.00	V8.01.31	DSAZ634A	DPS77004SX
				V06.60.00403	V10.11.0.30
15	V1.08.00	V8.01.31	V8.01.31	DSAZ634A	DPS77004SX
	N/4 00 00	N/0.00.00	N/0.00.00	V06.60.00403	V10.11.0.30
14	V1.08.00	V8.00.30	V8.00.30	DSAZ634A	DPS77004SX
13	V1.0.75	V8.00.30	V8.00.30	V06.60.00403 DSAZ634A	V10.11.0.30 DPS77004SX
15	V1.0.75	vo.uu.su	V8.00.50	V06.60.00403	V10.11.0.30
12	V1.0.75	V7.02.30	V7.02.30	DSAZ634A	DPS77004SX
		1102100	1,102.00	V06.60.00403	V10.11.0.30
11	V1.0.75	V6.01.05	V6.00.05	DSAZ634A	DPO77002SX
				V06.60.00403	V10.11.0.30
10	V1.0.64	V5.01.00	V5.00.30	DSAZ634A	DPO77002SX
				V06.60.00403	V10.11.0.30
09	V1.0.59	V4.10.20	V4.10.05	DSAZ634A	DPO77002SX
08	V1.0.56	V4.09.50	V4.09.15	V06.55.00702	V10.1.0.34 DPO77002SX
08	V1.0.50	V4.09.50	V4.09.15	DSAZ634A V06.55.00702	V10.1.0.34
07	V1.0.54	V4.09.41	V4.09.15	DSAZ634A	DP077002SX
07	V1.0.01	1.05.11	1.05.15	V06.55.00702	V10.1.0.34
06	V1.0.49	V4.03.12	V4.03.15	DSAZ634A	DPO75902SX
				V06.40.00714	V10.0.8.138
05	V1.0.49	V4.03.12	V4.03.15	DSAZ634A	DPO73304DX
				V06.40.00714	10.8.3 Build 3
	V1.0.49	V4.02.10	V4.02.10	DSAZ634A	DPO73304DX
	N/1 0 40	N/4 04 22	N/4 00 00	V06.40.00714	10.8.3 Build 3
	V1.0.49	V4.01.32	V4.00.08	DSAZ634A V06.40.00714	DPO73304DX 10.8.3 Build 3
04	V1.0.22	V3.01.10	V3.07.12	DSAZ634A	DPO73304DX
	v 1.0.22	• 5.01.10	¥3.07.12	V06.20.01101	10.8.3 Build 3
03	V1.0.22	V3.00.05	V3.06.16	DSAZ634A	DP073304DX
				V06.20.01101	10.8.3 Build 3
02	V1.0.22	V2.05.08	V3.05.00	DSAZ634A	DPO73304DX
				V06.20.01101	10.8.3 Build 3
01	V1.0.11	V2.05.08	V3.05.00	DSAZ634A	DPO73304DX
				V06.20.01101	10.8.3 Build 3

2. Peripheral Devices

The peripheral devices of the application are shown in the table.

Model	Name
MP1900A	Signal Quality Analyzer-R
MU181000B	12.5GHz 4port Synthesizer (Option02 is required.)
MU181500B	Jitter Modulation Source
MU195020A or MU196020A	21G/32G bit/s SI PPG or PAM4 PPG
MU195040A	21G/32G bit/s SI ED
MU195050A	Noise Generator

For the installation position of the mainframe, refer to the Anritsu website (<u>https://www.anritsu.com</u>).

3. Added Functions

Edition	Function	Description
11	All	Adds support for M.2 and U.2 Interface Types
10	MOI	Updates MOI
08	All	Turns OFF PPG output after completing tests and when changing ISI
07	All	Supports MU196020A PAM4 PPG
05	Auto Scale	This function turns off the Auto Scale function for Scope to shorten the time required for Initial Tx EQ and Tx LEQ response time test. When the function is set to True , input the amplitude of the Data output of the DUT in the Vertical Range (scale of the vertical axis of Scope) with a value equivalent to Differential Input. The recommended value for Vertical Range is 0.5 Vpp because the Power Divider practically attenuates the data output of the DUT by 6 dB. This software may fail in waveform decoding if the amplitude is too small for the scale or beyond the scale.

Edition	Function	Description
05	Auto DUT Reset	 This function resets the DUT automatically during Compliance Test. To use this function, follow the steps below: a. In the Auto DUT Reset box, select Internal Power Cycle or Internal Power Reset. b. Set up Anritsu Z2025A PCIe CBB Controller according to the Z2025A Installation Guide. c. In the Prompt Before Link EQ Training box, select False.
		 Power Cycle Off Time: Sets the time to turn off the CBB power. Power Reset Off Time: Sets the time to send the Power Reset signal to the DUT. Post Reset Wait Time: Sets the time to wait after turning on Reset or Cycle before Link Training is started.
	Link Training Wait Time	This function sets the time to wait after Link Training is ready to start before it is started.
	Link Training CTLE Gain	Select a CTLE value option to set for SI ED. If the DUT Tx Insertion Loss is large, adjust the value.
	Log Link Training	This function saves an LTSSM Log file to the following directory of MP1900A every time Link Training is performed. "C:¥PCIE_LTSSM_LOG"

4. Bug Fixes

Edition	Item	Description
20	Calibration with Keysight UXR scope	Fixes Preset calibration failure with Keysight UXR scope. Fixes RJ and SJ calibration failure with Keysight UXR EZJIT application.
09	PPG Final Preset setting issue	Fixes config "PPG Final Preset" not being applied when changed to fixed preset.
	JTOL display issue	Updates framework to fix Jitter tolerance plot display incorrect JTOL line.
05	Tx LEQ Response time test and Rx LEQ test failed occasionally.	Tx LEQ Response time test and Rx LEQ test failed occasionally.
01	Sometimes, Preset calibration fails with Tektronix scope.	Calibration fails when attempting to execute Preset calibration. Bug occurs in GRL software version 1.00.11 and Tektronix scope software version 10.8.3.

5. Remaining Known Bugs

None

6. Usage Notes

The precautions for using each version are described below.

6.1 How to shorten measurement time

- BER and Margin Test

Decrease Margin Test Measurement Time and Margin Test Max Steps.

figurations		
	Compliance BER Measurement Time(s): 63 Maximum Compliance Error: 1	
	Margin Test Max Steps: 5 Margin Test Max Steps: 5	
	Margin Test Step Size(%): 20 Maximum Margin Test Error: 1	
	Loopback Mode: Recovery	+
		Compliance BER Measurement Time(s): G3 Maximum Compliance Error: 1 Margin Test Measurement Time(s): S Margin Test Max Steps: 5 Margin Test Step Size(%): 20 Maximum Margin Test Error: 1

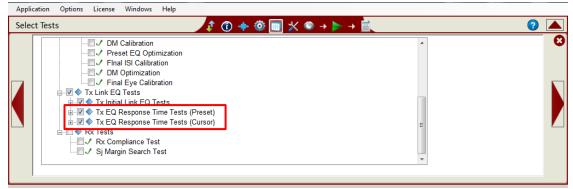
Set Retrain When Sj Frequency Changed to False.

	Margin Test Max Steps:	
Γ	Margin Test Max Steps.	5
-	Margin Test Step Size(%):	20
L	Maximum Margin Test Error:	1
-	Loopback Mode: Rec	overy 🗸
-	Retrain When Sj Frequency Chang	ged: False ·
L	MarginSearchLivePlot:	True

6.2 Note on Link EQ Response time test

Perform the **Tx EQ Response time (Preset)** test before running the **Tx EQ Response Time (Cursor)** test.

When starting the test with **Tx EQ Response Time (Preset)**, the cursor values corresponding to Preset are sent from the DUT and are saved in MP1900A. These values are required for testing **Tx EQ Response Time (Cursor)**.



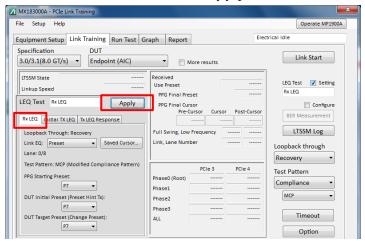
To skip the test with **Tx EQ Response time (Preset)**:

Perform link training by following the steps below to acquire cursor values from the DUT. When replacing the DUT to test **Tx EQ Response time (Cursor)**, it is required to go through these steps again.

- a. Launch MX183000A with PCIe Link Training application.
- b. Initialize the PCIe Link Training application.
- c. Set Specification to 3.0(8.0 GT/s).
- d. Click on **LEQ Test Setting** check box.

Equipment Setup Link Training Run Test Graph Report Electrical Idle 3.0/3.1(8.0 GT/5) DUT Inkup Speed Inku	1 MX183000A - PCIe Link Training File Setup Help		Operate MP1900A
Linkup Speed Use Preset Bb10b Received Symbol Err PPG Final Preset Current RD Err PILI Swing, Low Frequency Symbol Lock Init, Lane Number Liz80130b Received SkP Count Phase0 (Root) Sync Header Err Phase3 Phase3 MCP Block Lock ALL	Specification	Graph Report	
SKP Count Pre-Cursor Cursor Post-Cursor BER Measurement Symbol Err Full Swing, Low Frequency Italian Italian Symbol Lock Italian Pre-Cursor Cursor Post-Cursor 1280130b Received Transmitted Full Swing, Low Frequency Italian 1280130b Received Transmitted Preceire Italian Sync Header Err Phase1 Italian MCP Phase3 Italian Timeout	Linkup Speed	Use Preset PPG Final Preset	
128b130b Received Transmitted PCIe 3 PCIe 4 SKP Count	SKP Count	Pre-Cursor Cursor Post-Cursor Full Swing, Low Frequency	BER Measurement LTSSM Log Loopback through
	Received Transmitted SKP Count DCBalance Sync Header Err Parity Err	Phase0 (Root) Phase1 Phase2 Phase3	Test Pattern Compliance

e. Select **Rx LEQ** tab and click on **Apply** button.



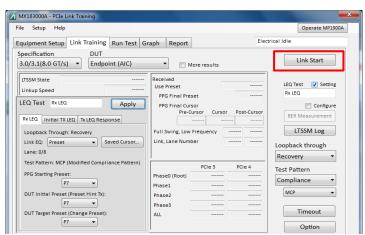
f. Click on **Option** button.

MX183000A - PCIe Link Training		×
File Setup Help		Operate MP1900A
Equipment Setup Link Training Run Test Gra	aph Report Elect	trical Idle
Specification DUT 3.0/3.1(8.0 GT/s) DUT Endpoint (AIC)	More results	Link Start
UTSSM State Linkup Speed LEQ Test Rx LEQ Apply Rx LEQ Initial TX LEQ Saved Cursor Lane: 0/8	Received Use Preset PPG Final Preset PPG Final Cursor Pre-Cursor Cursor Pre-Cursor Cursor Full Swing, Low Frequency Link, Lane Number	LEQ Test V Setting Rx LEQ ER Measurement LTSSM Log Loopback through Recovery V
Test Pattern: MCP (Modified Compliance Pattern) PPG Starting Preset: P7 UT Initial Preset (Preset Hint Tx): P7 UT Target Preset (Change Preset): P7 V	PCIe 3 PCIe 4 Phase0 (Root) Phase1 Phase2 Phase3 ALL	Test Pattern Compliance • MCP • Timeout

g. Set **Algorithm** to **increment** and set **Repeat** to **12** on **Link EQ** tab.

Option	
State Machine SKP Link EQ PPG/ED Trigger	
Link EQ (Recovery Phase2,3) Try	PCIe 3.0/3.1 🔹
Algorithm Increment 🔹 Repeat 12	
PCle 3.0/3.1 Use Preset Preset Saved Cursor	Root Complex
Downstream Downstream (MP1900A) sends Starting Preset until it receives preset from Upstream (AIC).	Downstream port
Recovery,EQ,Phase2 Starting Preset P7 : -6.0, 3.5	Tx Rx
Upstream	Upstream port
Downstream (MP1900A) requests these presets to Upstream (AIC) Recovery, EQ, Phase3	End Point
Preset Hint (Tx) Preset Hint (Rx) Change Preset P7 : -6.0, 3.5 ▼ -6 dB ▼ P7 : -6.0, 3.5 ▼	
	Close

h. Reset the DUT and click on Link Start button.



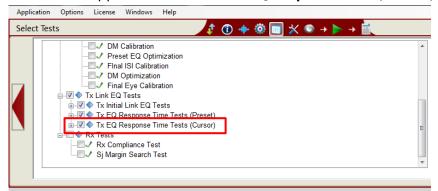
i. When **LTSSM State** is **Loopback.Active.Lead**, click on **Saved Cursor** button on LEQ Test window.

MX183000A - PCIe Link Training		×
File Setup Help		Operate MP1900A
Equipment Setup Link Training Run Test Gra	aph Report	Outputting Test Pattern
Specification DUT 3.0/3.1(8.0 GT/s) -	More results	Unlink
LTSSM State Loopback.Active.Master Linkup Speed 8.0 Gbps	Received Use Preset	Preset LEQ Test V Setting
LEQ Test Rx LEQ Apply Rx LEQ Initial TX LEQ Tx LEQ Response	PPG Final Cursor	t-Cursor 0 BER Measurement
Loopback Through: Recovery Link EQ: Preset Vaved Cursor Lane: 0/8	Full Swing, Low Frequency 63 Link, Lane Number 1	21 LTSSM Log 0 Loopback through Recovery
Test Pattern: MCP (Modified Compliance Pattern) PPG Starting Preset: P7 ▼ DUT Initial Preset (Preset Hint Tx): p7 ▼ DUT Target Preset (Change Preset):	PCle 3 PCl Phase0 (Root) Phase1 Complete Phase2 Complete Phase3 Complete	e 4 Compliance • MCP • Timeout
P7	ALL Complete	Option

 Response Te	st. mest	e values a	are update	ed auto	matic	ally and s	aved by t	ne MP19	JUA.
Saved		PCIe 3.0		Sav	ed.		PCIe 4.0		
Cursor	C-1	CO	C+1	Cur		C-1	CO	C+1	
🗾 РО	0	47	16	\checkmark	PO	0	47	16	
V P1	0	52	11	\checkmark	P1	0	52	11	
V P2	0	50	13	\checkmark	P2	0	50	13	
📝 РЗ	0	55	8	\checkmark	P3	0	55	8	
🗸 Р4	0	63	0	\checkmark	P4	0	63	0	
V P5	6	57	0	\checkmark	P5	6	57	0	
📝 P6	8	55	0	\checkmark	P6	8	55	0	
V P7	7	45	11	\checkmark	P7	7	45	11	
V P8	8	47	8	\checkmark	P8	8	47	8	
🔽 Р9	11	52	0	\checkmark	P9	11	52	0	
V P10	0	42	21	∇	P10	0	42	21	

j. If all **Saved Cursor checkboxes** are **ON**, the steps are finished.

k. Launch GRL application and start **Tx EQ Response time (Cursor)**.



6.3 Selecting Interface Types

The option to select between CEM, U.2, and M.2 Interface Types is located in the **Setup Configuration** page \rightarrow **Setup** Tab.

Setup	Debug Tool		
D	evice Type:	Add In Card	~
	erface Type:		v
	endee Type.	M.2 CEM U.2	~
		M.2	

7. Troubleshooting

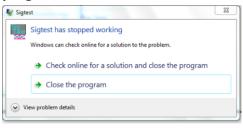
If you encounter any errors during calibration or testing, check as follows.

7.1 Calibration

7.1.1 In case of an error when calibrating Amplitude, Preset, SJ and RJ

- Check the RF connections. Especially, the connection polarity (Pos/Neg) and the trigger connections (PPG Aux Out and Scope Aux In) are easy to mistake.
- Check the software version. A different version of software may cause an unexpected error.
- Check the SigTest version. SigTest version needs to be 3.2.0.3 for Gen3 or 4.0.51 for Gen4. Also, this should be installed to the directory C:¥Program Files (x86). Do not change the installation directory from the default setting.
- 7.1.2 In case of a SigTest error when performing Long Channel Calibration

A SigTest error message is displayed and SigTest has stopped working when calibrating SJ, RJ and EH/EW. Since this message has no effect on calibration results, click **Close the program** to continue the calibration.



To avoid this message:

- Close all applications except the GRL software, MX190000A, MX183000A and scope applications. Especially when VNC is running, SigTest may not work properly.
- If you see this message frequently despite not running other applications on the PC, use another PC with the GRL software installed.

7.1.3 When Final Eye calibration fails

- Use the PCIe 3.0 test fixture. It is recommended to use the calibration fixture distributed by the PCI-SIG.
- If any components (DC block, Power Divider, Attenuator and Adaptor) are attached to the Noise module output, remove them. These components may affect the waveform.



7.2 Tx and Rx LEQ test

- 7.2.1 When Tx LEQ Response cursor test cannot be started
 - Before starting Rx Test, complete all calibrations or load a calibrated session file.
- 7.2.2 In case of a Link Training error when testing Tx LEQ Response
 - Check the RF connections. Especially, the trigger connections (PPG Aux Out and Scope Aux In) are easy to mistake.
 - If DUT Tx has large insertion loss, adjust the MP1900A CTLE value in the MX183000A screen. Refer to Appendix C for adjusting CTLE.
- 7.2.3 In case of a decode error when testing Rx LEQ Reponses time

- On the **Configurations** tab, set **CTLE Setting** to **Auto**.

M Anritsu PCIe CEM 4.0 Rx Test
Application Options License Windows Help
Configurations 2 $(1) + (2) = 12$ $(2) + (2) = 12$
CTLE Scan End EQ Gain(dB): 10 Tx Link EQ Tests Tx Response Offline Mode: False CTLE Setting: Auto Capture Response Time Waveform Only: True Rx Tests BER Automation: PCIe Link Training Present Before Link EO Tenining

7.3 Others

- 7.3.1 When a session file cannot be loaded
 - Close the folder where you installed the GRL software and saved PDF report file(s) because the loaded session file accesses and edits the folder.

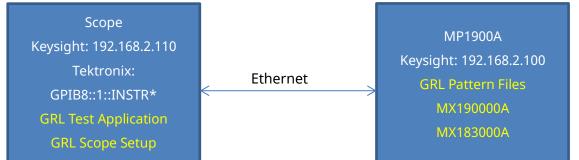
ſ	Load Session
	Incompatible file format or file is being used: Error in loading test session
	ОК

- While recalling the session file on CEM spec takes several minutes, it does not mean that the computer is frozen. Wait until the recalling is completed. This function recalls large waveform files which are acquired by Tx initial EQ and Tx LEQ Response time test.

Appendix

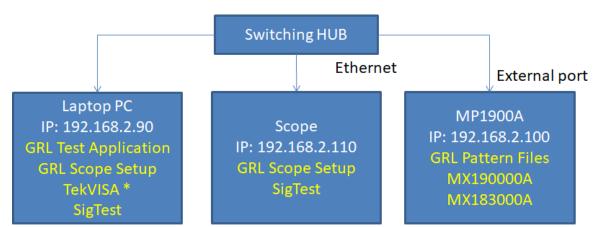
- A. Quick Startup Guide
 - 1. Connect instruments with Ethernet cables as shown below.
 - 2. Set the IP and GPIB addresses as shown below. These can be set in the Network and Sharing Center (Windows OS feature).
 - 3. Install all applications as shown below (Yellow letters).

Recommended connection



* TCP/IP cannot be used when the GRL software is installed on a Tektronix scope. Set the GPIB address as "GPIB8::1::INSTR".

• Optional connection



* TekVISA is needed to control Tektronix scopes. But, the PC on which TekVISA is installed cannot control Keysight scopes. Also, this configuration makes the remote control speed slower than the recommended configuration.

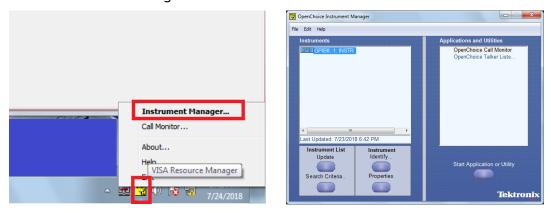
Tektronix Scope

When the GRL software is installed on the laptop:

TCPIP0::192.168.2.110::inst0::INSTR

When the GRL software is installed on the scope: GPIBX::1::INSTR*

* Tektronix scope cannot use TCP/IP when the GRL software is installed on it. In this case, GPIB VISA should be set. The address can be checked using the VISA instruments Manager.



Keysight Scope

When the GRL software is installed on the laptop:

TCPIP0::192.168.2.110::inst0::INSTR

When the GRL software is installed on the scope: TCPIP0::localhost::inst0::INSTR

MX190000A: TCPIP0::192.168.2.100::5001::SOCKET*

MX183000A: TCPIP0::192.168.2.100::5000::SOCKET*

* Port numbers should be set for MX190000A and MX183000A.

B. Before beginning Tx LEQ response time test

Before beginning Tx LEQ response time test, it is recommended to adjust the **CTLE Gain** value in MX183000A. This is especially efficient when DUT Tx has a large Insertion Loss like a System board.

In case of a link training error and/or bit error, adjusting the **CTLE Gain** value is also recommended.

Note:

Though the following procedure uses the screenshots for PCIe 4.0, read PCIe 4.0 as PCIe 3.0 here. Set **Specification** to **3.0 (8 GT/s)**, and then adjust the **CTLE Gain** value according to the following procedure.

a. In MX183000A, display the LEQ test settings and BER Measurement screen.

File Setup Help			Operate MP1900A
Equipment Setup Link Training Run Test Gr	aph Report	Electrical	Idle
Specification DUT			
4.0(16.0 GT/s) • Endpoint (AIC)	PCIe 4.0	Preset P7 : -6.0, 3.5 🔷 🔻	Link Start
LTSSM State		CTLE Gain [dB] 0 🚔	
Linkup Speed	EC Threshold	1	LEQ Test 📝 Setting Tx LEQ Response
LEQ Test Tx LEQ Response Apply	Pass/Fail		Configure
Rx LEQ Initial TX LEQ Tx LEQ Response			BER Measurement

b. Set CTLE Gain to 0 (zero) on the BER Measurement panel.

File Setup Help			Operate MP1900A
Equipment Setup Link Training Run Test Gr	aph Report	Electrical	Idle
Specification DUT			
4.0(16.0 GT/s) • Endpoint (AIC)	PCIe 4.0	Preset P7:-6.0.3.5 🗸	Link Start
LTSSM State		CTLE Gain [dB]	
Linkup Speed	EC Threshold	1	LEQ Test 🛛 Setting
			Tx LEQ Response
LEQ Test Tx LEQ Response Apply	Pass/Fail		Configure
Rx LEQ Initial TX LEQ Tx LEQ Response			BER Measurement

c. On the **Tx LEQ Response** tab of the LEQ test pane, set **PPG Starting Preset** to **7**, **DUT Initial Preset** to **7** and **Target Preset** to **P4**.

File Setup Help			Operate MP1900A
Equipment Setup Link Training Run Test Gr	aph Report	Electrica	lldle
Specification DUT			
4.0(16.0 GT/s) • Endpoint (AIC)	PCle 4.0	Preset P7 : -6.0, 3.5 🔹	Link Start
LTSSM State		CTLE Gain [dB] 0 🚔	to Power Cycled 👻
Linkup Speed	EC Threshold	1	LEQ Test 👿 Setting Tx LEQ Response
LEQ Test Tx LEQ Response Apply	Pass/Fail		Configure
Rx LEQ Initial TX LEQ Tx LEQ Response	Cycle	Single 🔻	LTSSM Log
Link EQ: Preset Saved Cursor	Gating Time	63 🛓 [s]	opback through
Lane: 0/8 Test Pattern: CP (Compliance Pattern)	Switch To Manual BER Test	Error Addition	ecovery 🔻
PPG Starting Preset:	Total BER	0.0000E-11	st Pattern
	Total Error Count	0	ompliance
DUT Initial Preset (Preset Hint Tx):	Total Bits	5.3760E11	
DUT Target Preset (Change Preset)	Current BER	0.0000E-09	Timeout
P4 •	Sync Loss 🔳	Clock Loss 🔳	Option

- d. Click Link Start.
- e. If the following error conditions are met, adjust the **CTLE Gain** value by proceeding to the next step.
 - LTSSM State is not Loopback.Active.Lead.
 - Sync Header Err is greater than **0** (zero).

If there is no error, this procedure is assumed to be completed.

Equipment Setup	Link Training	Run Test	Graph	Report	Outputti	ng Test Pattern
Specification	DUT		_			Unlink
4.0(16.0 GT/s)	Endpoint	oint (AIC)	PCI	e 4.0	Preset P7 : -6.0, 3.5 👻	o Reset
LTSSM State	Loopba	ck.Active.Mast	er		CTLE Gain [dB] 0 🚔	to Power Cycled 👻
Linkup Speed		16.0 Gbj	ps EC	Threshold		LEQ Test Setting Tx LEQ Response
8b10b	Received	Transmitted	Pas	ss/Fail		Configure
SKP Count			-			Stop
Symbol Err			Сус	cle	Single 👻	LTSSM Log
Current RD Err			Ga	ting Time	63 🚊 [s]	
Symbol Lock				1. L. T.		opback through
128b130b				itch To Inual BER Test	Error Addition	ecovery 🔻
		Transmitted	Tot	al BER		st Pattern
SKP Count	0		<u> </u>			ompliance 🔹
Sync Header Err	1057603			al Error Count		CP 👻
Parity Err	0		Tot	al Bits		
Block Lock	Aligned		Cu	rrent BER		Timeout
			Syr	nc Loss 📕	Clock Loss 🔳	Option

f. Increment the **CTLE Gain** value and run Link Training again until **Sync Header Err** becomes **0** (zero) and **Total Error Count** becomes **0** (zero). In this case, it is considered to be error free with -6 dB.

quipment Setu		g Run Test G	raph Report		
pecification 4.0(16.0 GT/s)		oint (AIC)	PCle 4.0	Preset P7 : -6.0, 3.5 🗸	Unlink o Reset
LTSSM State	Loopb	ack.Active.Master		CTLE Gain [dB] -6 🚔	to Power Cycled 👻
Linkup Speed		16.0 Gbps	EC Threshold	1	LEQ Test Setting Tx LEQ Response
8b10b	Received	Transmitted	Pass/Fail		Configure
SKP Count Symbol Err Current RD Err			Cycle Gating Time	Single ▼ 63 <mark>↓</mark> [s]	Stop
Symbol Lock			Switch To Manual BER Test	Error Addition	ecovery 👻
128b130b SKP Count	Received 0	Transmitted 0	Total BER	0.0000E-11	st Pattern
DCBalance	0	18	Total Error Count	0	
Sync Header Err	0		Total Bits	1.0720E11	<u> </u>
Parity Err Block Lock	0 Aligned	-	Current BER	0.0000E-09	Timeout
L. L. LOUN	Anglica		Sync Loss 🔳	Clock Loss 🔳	Option

- g. Repeat steps d to f with DUT target **Preset P7**.
- h. After adjusting the CTLE Gain value, close the MX183000A application and return to the selector screen. The CTLE Gain value is stored on the MX183000A.
 Start GRL Tx LEQ response time test again.