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Anritsu - GRL

PCIe 3.0 CEM Rx Test Application

Release Note

20th Edition

This software is released for PCIe CEM Rx Test.

Table of Contents

1. Released Software

The certificate software versions for Keysight / Tektronix Scope are shown in the table.

Edition	GRL CEM Rx Test Application	Anritsu MX190000A	Anritsu MX183000A	Scope	
				Keysight	Tektronix
20	V1.10.00	V9.00.01	V9.00.00	DSAZ634A V06.60.00403	DPS77004SX V10.11.0.30
19	V1.08.00	V8.03.14	V8.03.13	DSAZ634A V06.60.00403	DPS77004SX V10.11.0.30
18	V1.08.00	V8.03.00	V8.03.02	DSAZ634A V06.60.00403	DPS77004SX V10.11.0.30
17	V1.08.00	V8.03.00	V8.03.00	DSAZ634A V06.60.00403	DPS77004SX V10.11.0.30
16	V1.08.00	V8.02.00	V8.01.31	DSAZ634A V06.60.00403	DPS77004SX V10.11.0.30
15	V1.08.00	V8.01.31	V8.01.31	DSAZ634A V06.60.00403	DPS77004SX V10.11.0.30
14	V1.08.00	V8.00.30	V8.00.30	DSAZ634A V06.60.00403	DPS77004SX V10.11.0.30
13	V1.0.75	V8.00.30	V8.00.30	DSAZ634A V06.60.00403	DPS77004SX V10.11.0.30
12	V1.0.75	V7.02.30	V7.02.30	DSAZ634A V06.60.00403	DPS77004SX V10.11.0.30
11	V1.0.75	V6.01.05	V6.00.05	DSAZ634A V06.60.00403	DPO77002SX V10.11.0.30
10	V1.0.64	V5.01.00	V5.00.30	DSAZ634A V06.60.00403	DPO77002SX V10.11.0.30
09	V1.0.59	V4.10.20	V4.10.05	DSAZ634A V06.55.00702	DPO77002SX V10.1.0.34
08	V1.0.56	V4.09.50	V4.09.15	DSAZ634A V06.55.00702	DPO77002SX V10.1.0.34
07	V1.0.54	V4.09.41	V4.09.15	DSAZ634A V06.55.00702	DPO77002SX V10.1.0.34
06	V1.0.49	V4.03.12	V4.03.15	DSAZ634A V06.40.00714	DPO75902SX V10.0.8.138
05	V1.0.49	V4.03.12	V4.03.15	DSAZ634A V06.40.00714	DPO73304DX 10.8.3 Build 3
	V1.0.49	V4.02.10	V4.02.10	DSAZ634A V06.40.00714	DPO73304DX 10.8.3 Build 3
	V1.0.49	V4.01.32	V4.00.08	DSAZ634A V06.40.00714	DPO73304DX 10.8.3 Build 3
04	V1.0.22	V3.01.10	V3.07.12	DSAZ634A V06.20.01101	DPO73304DX 10.8.3 Build 3
03	V1.0.22	V3.00.05	V3.06.16	DSAZ634A V06.20.01101	DPO73304DX 10.8.3 Build 3
02	V1.0.22	V2.05.08	V3.05.00	DSAZ634A V06.20.01101	DPO73304DX 10.8.3 Build 3
01	V1.0.11	V2.05.08	V3.05.00	DSAZ634A V06.20.01101	DPO73304DX 10.8.3 Build 3

2. Peripheral Devices

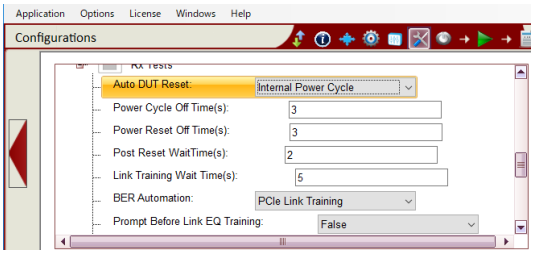
The peripheral devices of the application are shown in the table.

Model	Name
MP1900A	Signal Quality Analyzer-R
MU181000B	12.5GHz 4port Synthesizer (Option02 is required.)
MU181500B	Jitter Modulation Source
MU195020A or MU196020A	21G/32G bit/s SI PPG or PAM4 PPG
MU195040A	21G/32G bit/s SI ED
MU195050A	Noise Generator

For the installation position of the mainframe, refer to the Anritsu website (https://www.anritsu.com).

3. Added Functions

Edition	Function	Description
11	All	Adds support for M.2 and U.2 Interface Types
10	MOI	Updates MOI
08	All	Turns OFF PPG output after completing tests and when changing ISI
07	All	Supports MU196020A PAM4 PPG
05	Auto Scale	This function turns off the Auto Scale function for Scope to shorten the time required for Initial Tx EQ and Tx LEQ response time test. When the function is set to **True**, input the amplitude of the Data output of the DUT in the Vertical Range (scale of the vertical axis of Scope) with a value equivalent to Differential Input. The recommended value for Vertical Range is 0.5 Vpp because the Power Divider practically attenuates the data output of the DUT by 6 dB. This software may fail in waveform decoding if the amplitude is too small for the scale or beyond the scale.

Edition	Function	Description
05	Auto DUT Reset	This function resets the DUT automatically during Compliance Test. To use this function, follow the steps below: a. In the **Auto DUT Reset** box, select **Internal Power Cycle** or **Internal Power Reset**. b. Set up Anritsu Z2025A PCIe CBB Controller according to the Z2025A Installation Guide. c. In the **Prompt Before Link EQ Training** box, select **False**.  Power Cycle Off Time: Sets the time to turn off the CBB power. Power Reset Off Time: Sets the time to send the Power Reset signal to the DUT. Post Reset Wait Time: Sets the time to wait after turning on Reset or Cycle before Link Training is started.
	Link Training Wait Time	This function sets the time to wait after Link Training is ready to start before it is started.
	Link Training CTLE Gain	Select a CTLE value option to set for SI ED. If the DUT Tx Insertion Loss is large, adjust the value.
	Log Link Training	This function saves an LTSSM Log file to the following directory of MP1900A every time Link Training is performed. "C:¥PCIE_LTSSM_LOG"

4. Bug Fixes

Edition	Item	Description
20	Calibration with Keysight UXR scope	Fixes Preset calibration failure with Keysight UXR scope. Fixes RJ and SJ calibration failure with Keysight UXR EZJIT application.
09	PPG Final Preset setting issue	Fixes config "PPG Final Preset" not being applied when changed to fixed preset.
	JTOL display issue	Updates framework to fix Jitter tolerance plot display incorrect JTOL line.
05	Tx LEQ Response time test and Rx LEQ test failed occasionally.	Tx LEQ Response time test and Rx LEQ test failed occasionally.
01	Sometimes, Preset calibration fails with Tektronix scope.	Calibration fails when attempting to execute Preset calibration. Bug occurs in GRL software version 1.00.11 and Tektronix scope software version 10.8.3.

5. Remaining Known Bugs

None

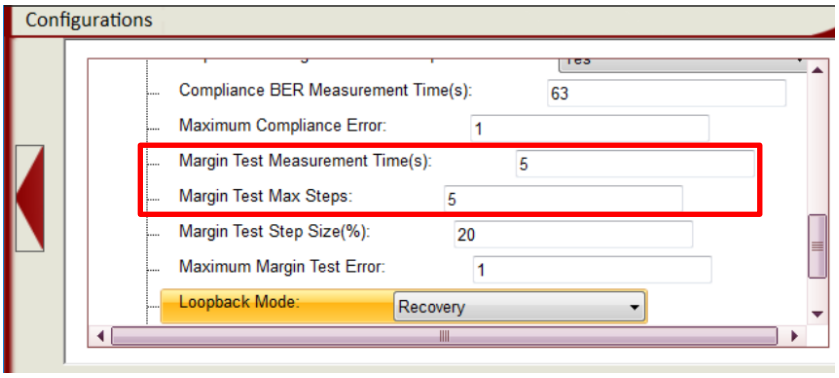
6. Usage Notes

The precautions for using each version are described below.

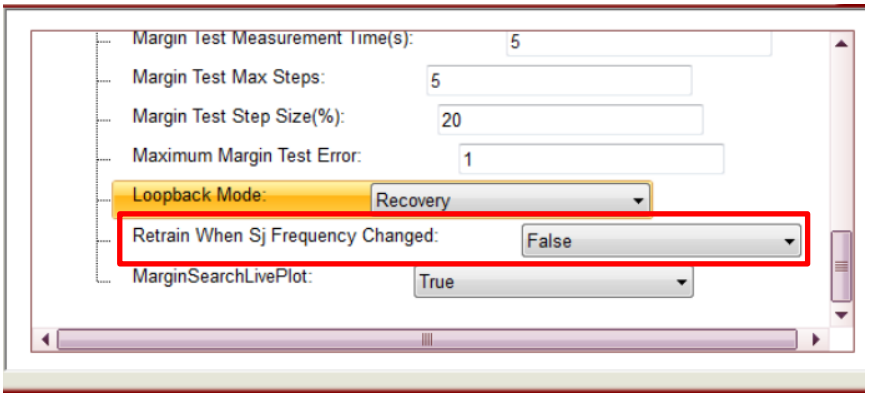
6.1 How to shorten measurement time

- BER and Margin Test

Decrease **Margin Test Measurement Time** and **Margin Test Max Steps**.

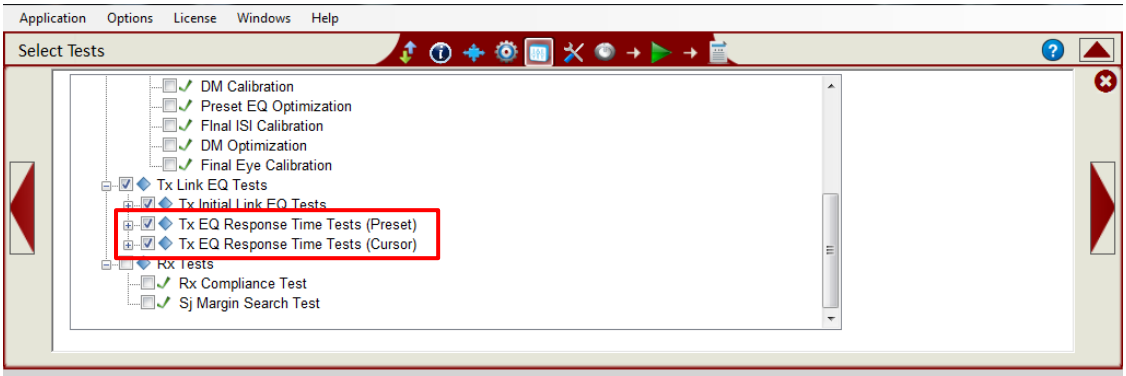


Set **Retrain When Sj Frequency Changed** to **False**.



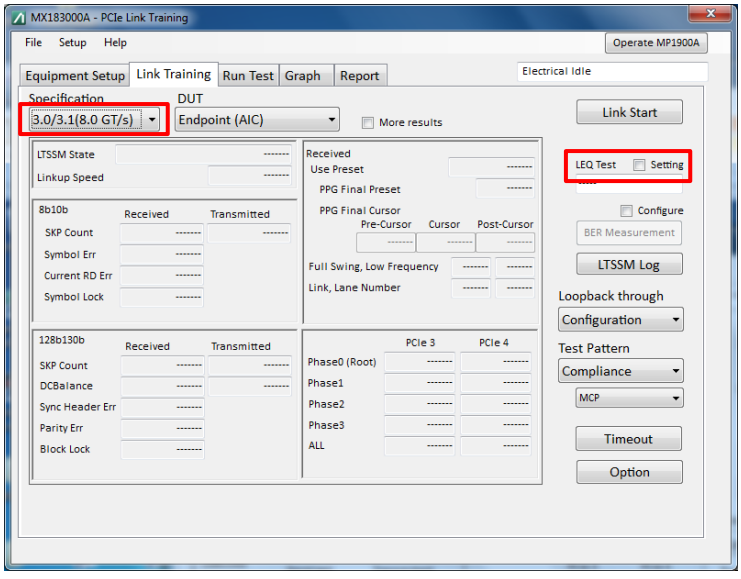
6.2 Note on Link EQ Response time test

Perform the **Tx EQ Response time (Preset)** test before running the **Tx EQ Response Time (Cursor)** test.
When starting the test with **Tx EQ Response Time (Preset)**, the cursor values corresponding to Preset are sent from the DUT and are saved in MP1900A. These values are required for testing **Tx EQ Response Time (Cursor)**.

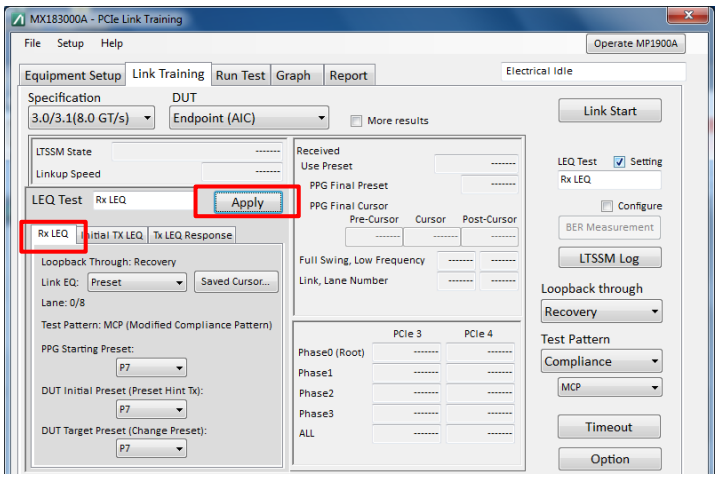


To skip the test with **Tx EQ Response time (Preset)**:
Perform link training by following the steps below to acquire cursor values from the DUT. When replacing the DUT to test **Tx EQ Response time (Cursor)**, it is required to go through these steps again.

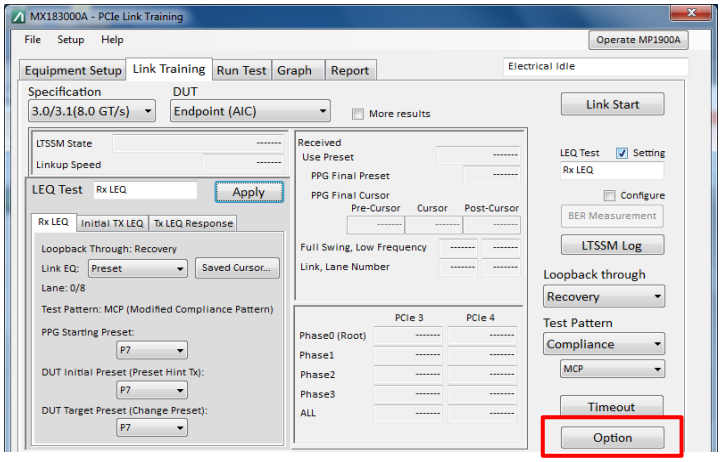
a. Launch MX183000A with PCIe Link Training application.
b. Initialize the PCIe Link Training application.
c. Set **Specification** to **3.0(8.0 GT/s)**.
d. Click on **LEQ Test Setting** check box.



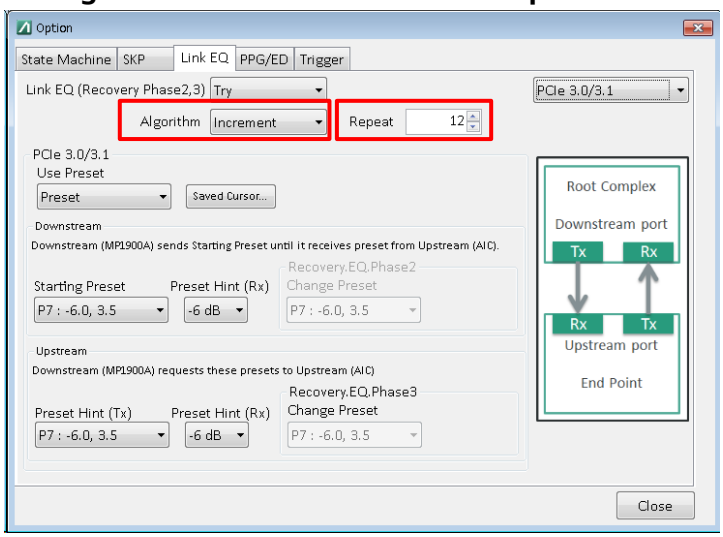
e. Select **Rx LEQ** tab and click on **Apply** button.



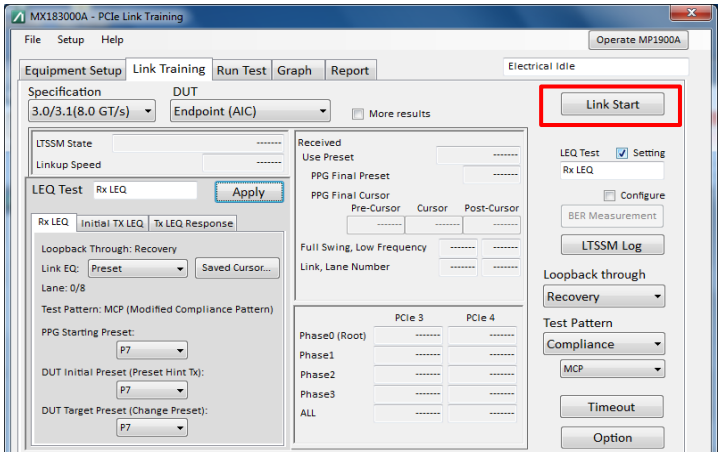
f. Click on **Option** button.



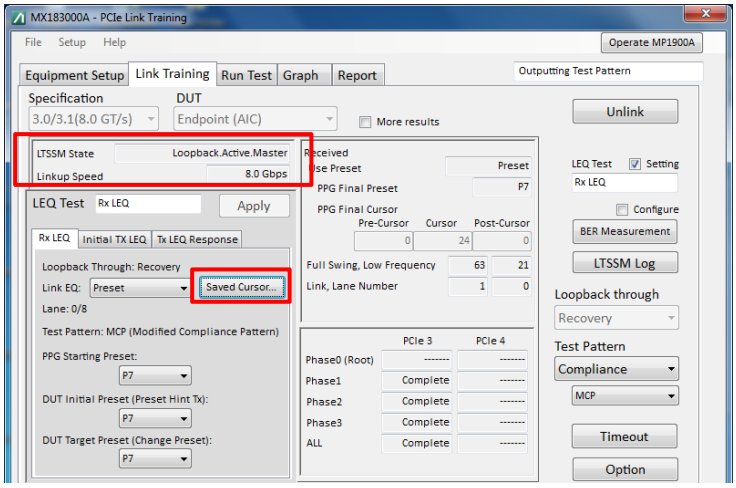
g. Set **Algorithm** to **increment** and set **Repeat** to **12** on **Link EQ** tab.



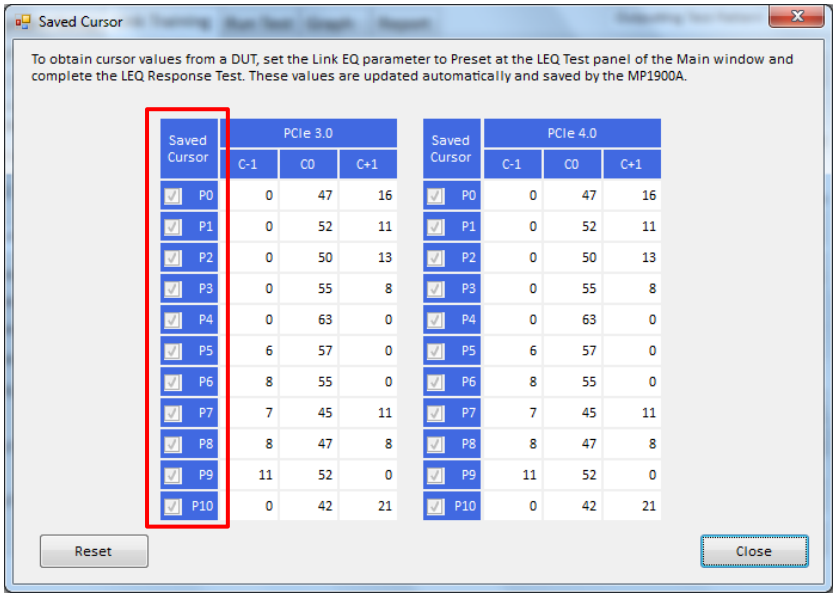
h. Reset the DUT and click on **Link Start** button.



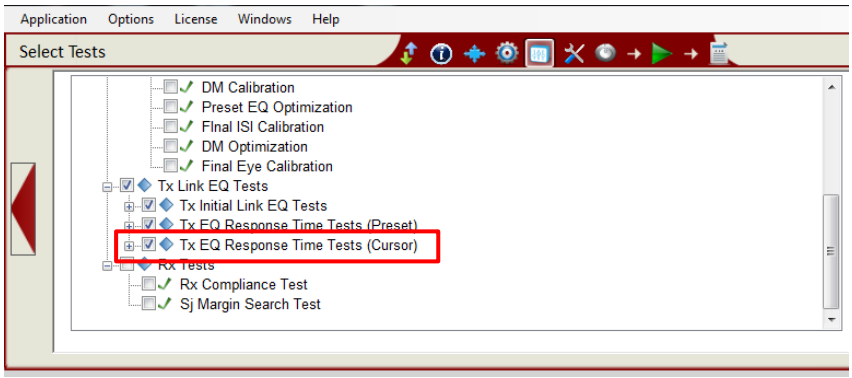
i. When **LTSSM State** is **Loopback.Active.Lead**, click on **Saved Cursor** button on LEQ Test window.



j. If all **Saved Cursor checkboxes** are **ON**, the steps are finished.

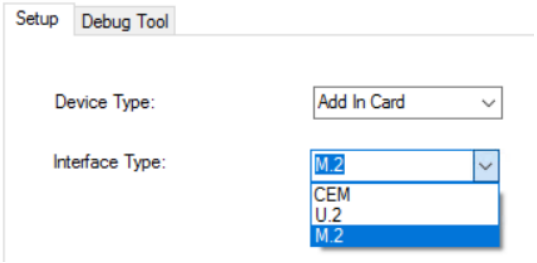


k. Launch GRL application and start **Tx EQ Response time (Cursor)**.



6.3 Selecting Interface Types

The option to select between CEM, U.2, and M.2 Interface Types is located in the **Setup Configuration** page →**Setup** Tab.



7. Troubleshooting

If you encounter any errors during calibration or testing, check as follows.

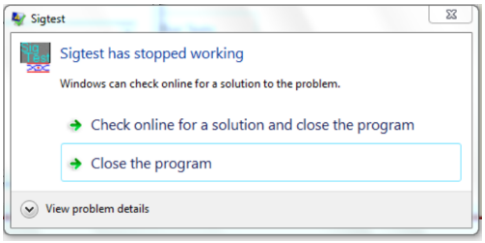
7.1 Calibration

7.1.1 In case of an error when calibrating **Amplitude**, **Preset**, **SJ** and **RJ**

- Check the RF connections. Especially, the connection polarity (Pos/Neg) and the trigger connections (PPG Aux Out and Scope Aux In) are easy to mistake.
- Check the software version. A different version of software may cause an unexpected error.
- Check the SigTest version. SigTest version needs to be 3.2.0.3 for Gen3 or 4.0.51 for Gen4. Also, this should be installed to the directory C:¥Program Files (x86). Do not change the installation directory from the default setting.

7.1.2 In case of a SigTest error when performing Long Channel Calibration

A SigTest error message is displayed and SigTest has stopped working when calibrating SJ, RJ and EH/EW. Since this message has no effect on calibration results, click **Close the program** to continue the calibration.



To avoid this message:

- Close all applications except the GRL software, MX190000A, MX183000A and scope applications. Especially when VNC is running, SigTest may not work properly.
- If you see this message frequently despite not running other applications on the PC, use another PC with the GRL software installed.

7.1.3 When Final Eye calibration fails

- Use the PCIe 3.0 test fixture. It is recommended to use the calibration fixture distributed by the PCI-SIG.
- If any components (DC block, Power Divider, Attenuator and Adaptor) are attached to the Noise module output, remove them. These components may affect the waveform.

7.2 Tx and Rx LEQ test

7.2.1 When Tx LEQ Response cursor test cannot be started

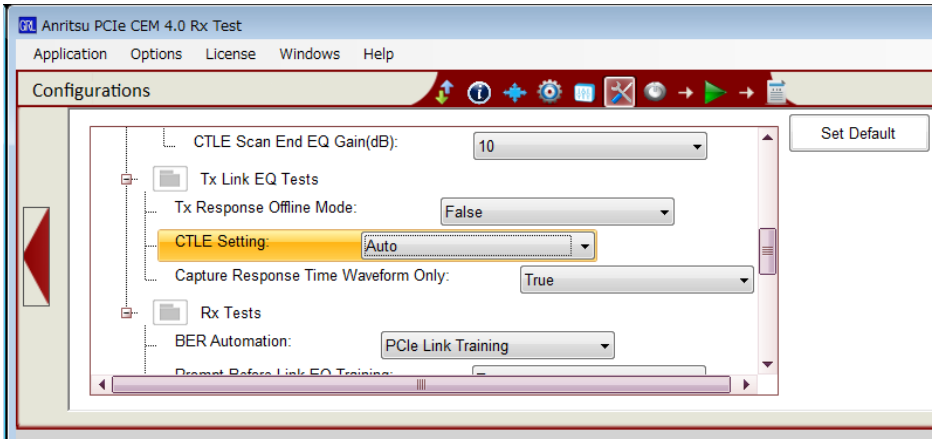
- Before starting Rx Test, complete all calibrations or load a calibrated session file.

7.2.2 In case of a Link Training error when testing Tx LEQ Response

- Check the RF connections. Especially, the trigger connections (PPG Aux Out and Scope Aux In) are easy to mistake.
- If DUT Tx has large insertion loss, adjust the MP1900A CTLE value in the MX183000A screen. Refer to Appendix C for adjusting CTLE.

7.2.3 In case of a decode error when testing Rx LEQ Reponses time

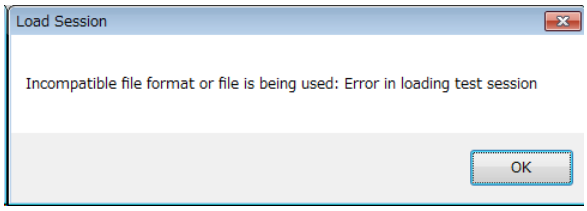
- On the **Configurations** tab, set **CTLE Setting** to **Auto**.



7.3 Others

7.3.1 When a session file cannot be loaded

- Close the folder where you installed the GRL software and saved PDF report file(s) because the loaded session file accesses and edits the folder.



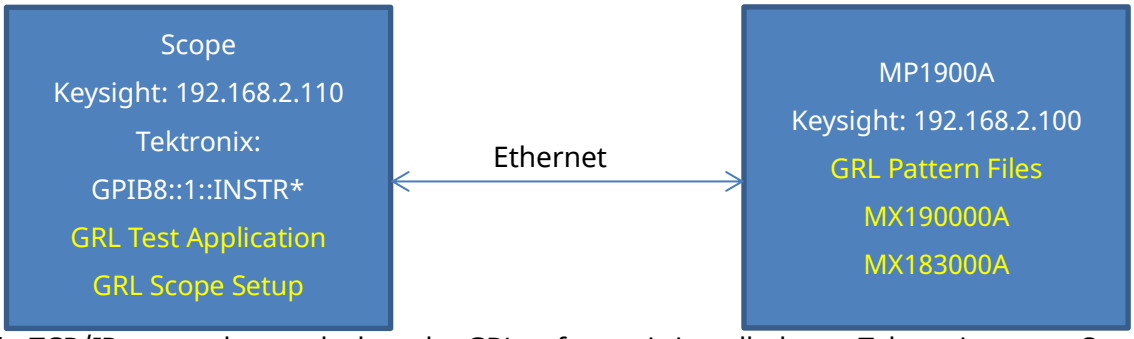
- While recalling the session file on CEM spec takes several minutes, it does not mean that the computer is frozen. Wait until the recalling is completed. This function recalls large waveform files which are acquired by Tx initial EQ and Tx LEQ Response time test.

Appendix

A. Quick Startup Guide

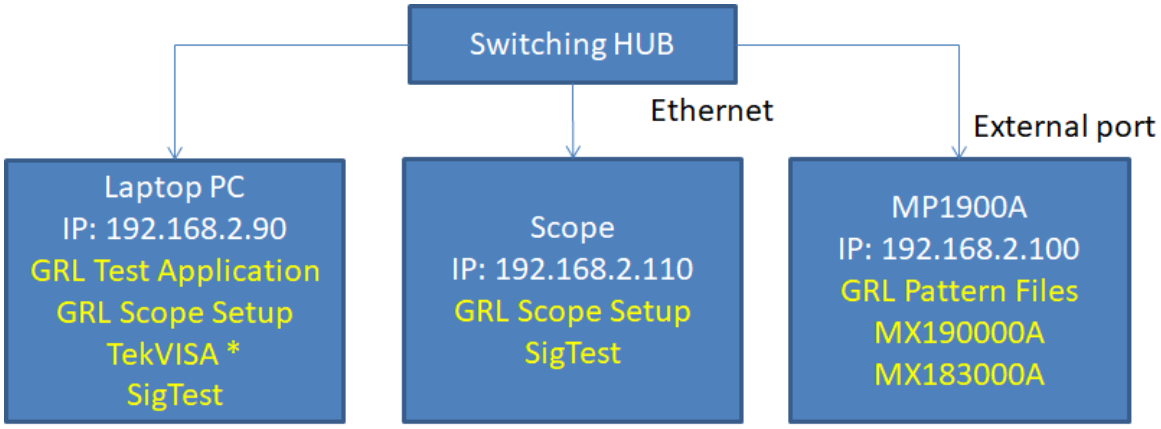
1. Connect instruments with Ethernet cables as shown below.
2. Set the IP and GPIB addresses as shown below. These can be set in the Network and Sharing Center (Windows OS feature).
3. Install all applications as shown below (Yellow letters).

- Recommended connection



* TCP/IP cannot be used when the GRL software is installed on a Tektronix scope. Set the GPIB address as “GPIB8::1::INSTR”.

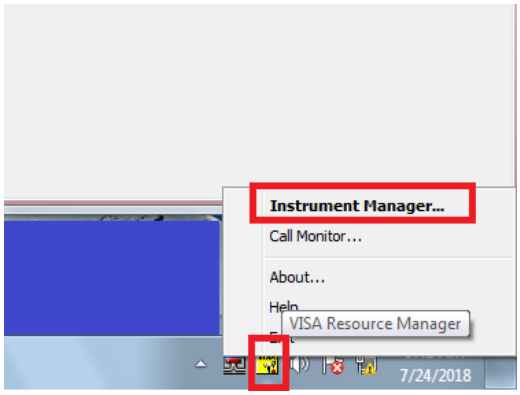
- Optional connection

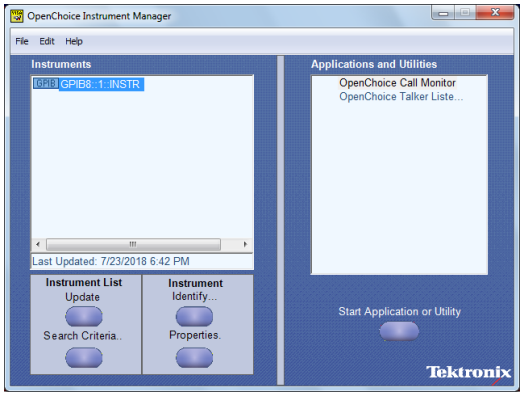


* TekVISA is needed to control Tektronix scopes. But, the PC on which TekVISA is installed cannot control Keysight scopes. Also, this configuration makes the remote control speed slower than the recommended configuration.

4. Launch application and configure equipment settings.
   Enter the scope address as below, and click . If the setting and connection are correct, the button will turn green.

Tektronix Scope
When the GRL software is installed on the laptop:
TCPIP0::192.168.2.110::inst0::INSTR
When the GRL software is installed on the scope: GPIBX::1::INSTR*
* Tektronix scope cannot use TCP/IP when the GRL software is installed on it. In this case, GPIB VISA should be set. The address can be checked using the VISA instruments Manager.





Keysight Scope
When the GRL software is installed on the laptop:
TCPIP0::192.168.2.110::inst0::INSTR
When the GRL software is installed on the scope: TCPIP0::localhost::inst0::INSTR

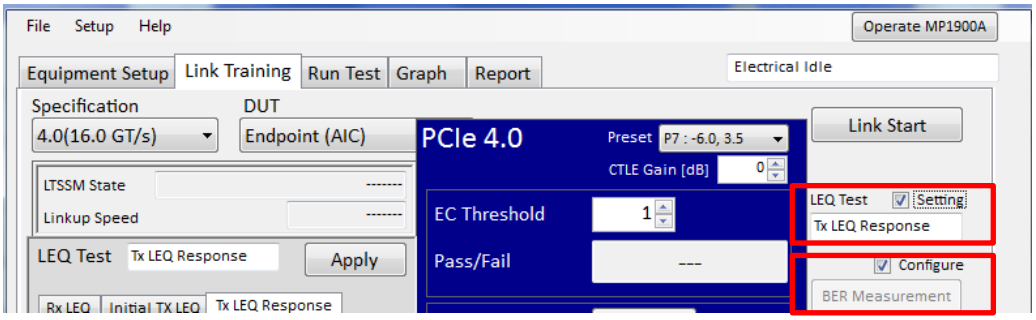
MX190000A: TCPIP0::192.168.2.100::5001::SOCKET*
MX183000A: TCPIP0::192.168.2.100::5000::SOCKET*
* Port numbers should be set for MX190000A and MX183000A.

B. Before beginning Tx LEQ response time test

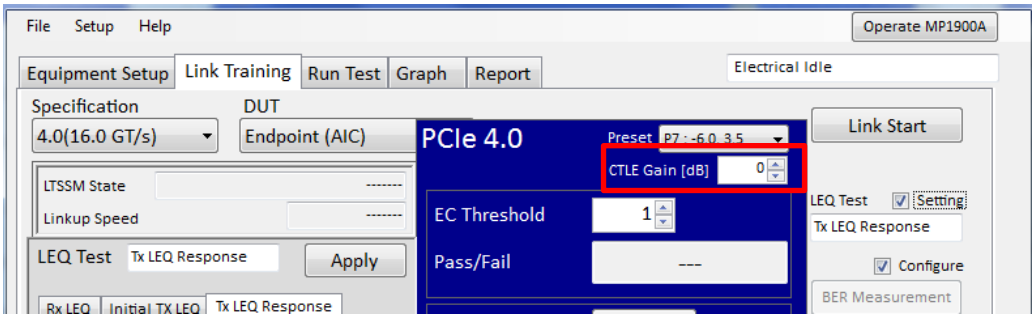
Before beginning Tx LEQ response time test, it is recommended to adjust the **CTLE Gain** value in MX183000A. This is especially efficient when DUT Tx has a large Insertion Loss like a System board.
In case of a link training error and/or bit error, adjusting the **CTLE Gain** value is also recommended.

Note:
Though the following procedure uses the screenshots for PCIe 4.0, read PCIe 4.0 as PCIe 3.0 here. Set **Specification** to **3.0 (8 GT/s)**, and then adjust the **CTLE Gain** value according to the following procedure.

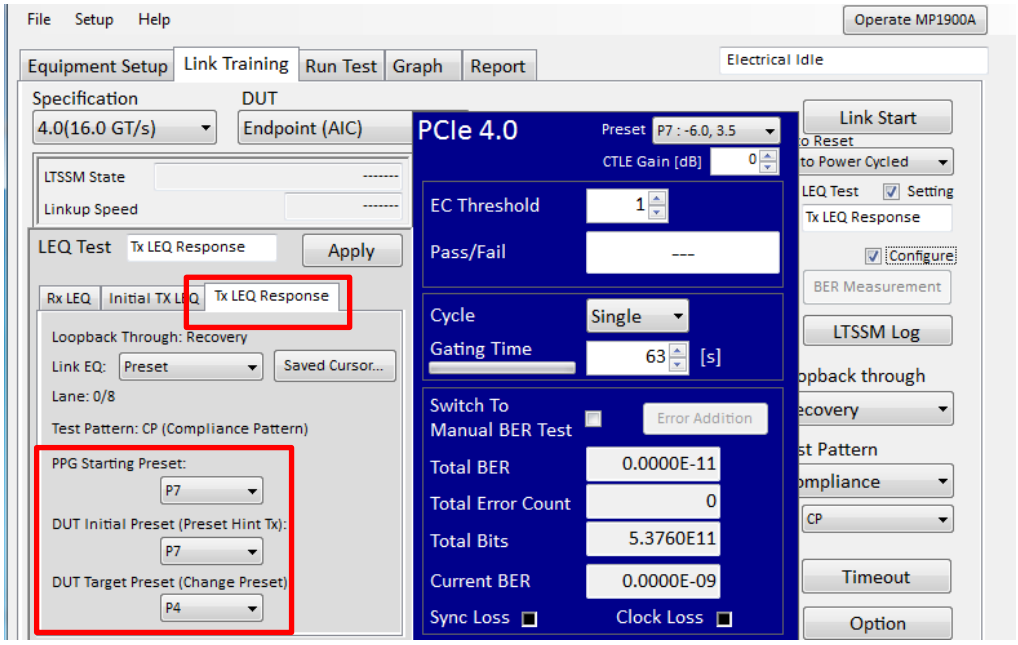
a. In MX183000A, display the LEQ test settings and BER Measurement screen.



b. Set **CTLE Gain** to **0** (zero) on the BER Measurement panel.



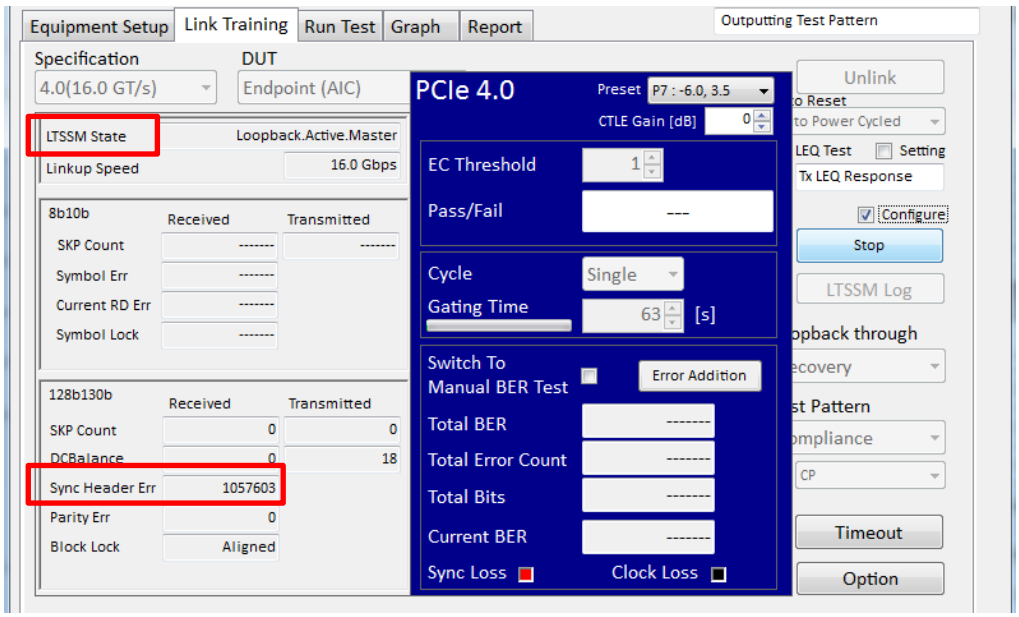
c. On the **Tx LEQ Response** tab of the LEQ test pane, set **PPG Starting Preset** to **7**, **DUT Initial Preset** to **7** and **Target Preset** to **P4**.



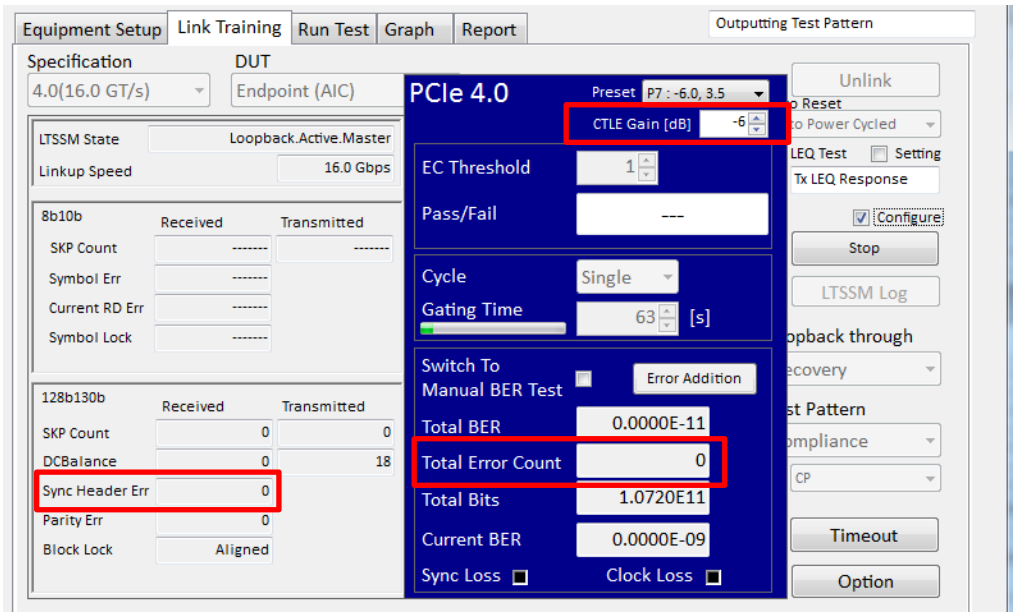
d. Click **Link Start**.

e. If the following error conditions are met, adjust the **CTLE Gain** value by proceeding to the next step.
- **LTSSM State** is not **Loopback.Active.Lead**.
- **Sync Header Err** is greater than **0** (zero).

If there is no error, this procedure is assumed to be completed.



f. Increment the **CTLE Gain** value and run Link Training again until **Sync Header Err** becomes **0** (zero) and **Total Error Count** becomes **0** (zero). In this case, it is considered to be error free with -6 dB.



g. Repeat steps d to f with DUT target **Preset P7**.

h. After adjusting the **CTLE Gain** value, close the MX183000A application and return to the selector screen. The **CTLE Gain** value is stored on the MX183000A. Start GRL Tx LEQ response time test again.