Development of MP2100B 12.5 Gbit/s 4ch Bit Error Rate Tester

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[Summary] We developed the all-in-one MP2100B with built-in 12.5 Gbit/s 4ch Bit Error Rate Tester (BERT) and sampling oscilloscope supporting performance tests of 4ch optical transceivers expected to see increased future demand. The BERT combines an in-house wideband amplifier with a commercially available high-speed transceiver to offer both high performance and low cost. In optical transceiver optical Rx sensitivity tests, the MP2100B achieved 0.7-dB better performance than its predecessor model.

1 Introduction

Data-center traffic volumes are exploding due to the spread of cloud computing services, which is forcing an increase in transfer speeds between servers and network equipment. As a result, optical interfaces are being adopted between data center servers and network equipment, which is driving increased demand for optical transceivers. In particular, there is high demand for SFP+ modules for 10GbE, and QSFP+ modules for 40GbE (10 Gbit/s \times 4)^{1) to 3)}. Development and manufacturing of optical transceivers requires a Bit Error Rate Tester (BERT) and a sampling oscilloscope for EYE pattern analysis⁴⁾. The BERT is composed of a Pulse Pattern Generator (PPG) as a signal source and an Error Detector (ED) for measuring bit errors. A conventional BERT and sampling oscilloscope configuration uses separate units, incurring higher capital equipment costs and occupying more bench space. To solve these issues, Anritsu had released the MP2100A incorporating a 2ch BERT and 2ch sampling oscilloscope in an all-in-one unit⁵⁾.

However, supporting QSFP+ modules for 40GbE applications requires a 4ch BERT⁶⁾. Since two MP2100A units are needed for this, an upgrade is required from the aspects of holding-down costs and space requirements. To this end, we have developed the new MP2100B with a 4ch BERT in the same cabinet size as its predecessor MP2100A. As a result, the all-in-one MP2100B supports BER measurements of 40GbE QSFP+ modules without any increase in required bench space.

In developing the MP2100B, the previous sampling oscilloscope from the predecessor MP2100A was used as is and only the BERT was updated. This article describes the technologies developed to extend the BERT from 2ch to 4ch support.

2 Basic Configuration

2.1 MP2100B Structure

Figure 1 shows an external view of the MP2100B. It has a 12.1-inch touch-panel LCD displaying the BERT and sampling oscilloscope operation screen and measurement results. With the same cabinet size $(341H \times 221.5W \times 180D \text{ mm})$ as its predecessor MP2100A and a mass of less than 7 kg, the MP2100B retains excellent compactness and portability.



Figure 1 External View of MP2100B

Figure 2 shows the MP2100B block diagram. The BERT is composed of a 4ch PPG and a 4ch ED. The BERT Clock can be switched between internal and external sources. The sampling oscilloscope has both electrical and optical channels.



Figure 2 MP2100B Block Diagram

2.2 BERT Configuration

Figure 3 shows the BERT block diagram. After the 12.5-Gbit/s NRZ signal generated by the Field Programmable Gate Array (FPGA) is re-timed by a commercial high-speed transceiver IC to improve the jitter characteristics, the signal is amplified by a Tx amplifier and output as a 0.1 to 0.8 Vp-p signal. The input signal to the ED is amplified by the Rx amplifier to improve the sensitivity characteristics. The BERT Clock can be switched between external and internal sources and synchronization with an external Clock is also supported. The low-phase-noise Clock generated in the Reference Clock section is supplied to high-speed transceiver ICs.



Figure 3 BERT Block Diagram

3 Design Concept

3.1 Multi-channel BERT

The BERT design was changed from the previous 2ch design to that shown in Figure 3 to increase the number of channels to four while retaining the same compact cabinet size. The earlier MP2100A used one high-speed transceiver IC for each channel of the PPG and ED, whereas the MP2100B uses one high-speed transceiver IC for two channels of the PPG and ED. This solution cuts the parts count, enabling the upgrade to 4ch while keeping the same cabinet size.

3.2 High-Performance Low-Cost PPG

The low-jitter characteristics of PPG output waveform are a key item determining the BERT performance. The high-speed transceiver ICs used this time incorporate an Emphasis function for correcting attenuation of the signal level and quality degradation. The low-jitter output waveform is implemented by optimizing adjustment of this function. However, with high-speed transceiver ICs, it is necessary to add a commercial amplifier to compensate for the inadequate output amplitude, which does not satisfy the low-jitter performance requirement from the target cost aspect. To overcome this issue, we developed a new dedicated gallium arsenide (GaAs) compound semiconductor in-house. Moreover, we added an equalizer circuit to improve the waveform by suppressing output waveform overshoot^{7), 8)}.

Figure 4 shows the PPG block diagram. An RC equalizer is connected to each of the positive and negative outputs of the Tx amplifier. The Rx equalizer equivalent circuit is shown in Figure 5. The synthetic impedance Z of this circuit is found by Eq. 1.

$$Z = Z_1 + Z_0 \tag{1}$$

where, Z_1 is synthetic impedance of the resistance R and the capacitance C found as follows:

$$\frac{1}{Z_1} = \frac{1}{R} + \frac{1}{\frac{1}{j\omega c}} \quad (\omega = 2\pi f)$$
(2)
$$|Z_1| = \frac{R}{\sqrt{1 + (2\pi f C R)^2}}$$
(3)

where, $Z_0 = 50 \ \Omega$. In this design, since components below 0.1 GHz are a cause of overshoot, the resistance $R = 20 \ \Omega$, and the capacitance C = 10 pF. Figure 6 shows the combined impedance Z versus the frequency characteristics f. At less than 0.1 GHz, impedance is high (70 Ω), and above 10 GHz it is closer to 50 Ω . Based on this result, the system is functioning as an equalizer at less than 0.1 GHz to decrease amplitude.



Figure 5 RC Equalizer Equivalent Circuit



Figure 6 Combined Impedance Zvs Frequency Characteristics f

These resistance and capacitance chips are surface mounted on the PC board for excellent cost performance but their physical size has a large adverse impact on the circuit impedance characteristics.

To counter this issue, we developed an upgraded surface mount method shown in Figure 7. Figure 7a shows the previous mounting method with the chip resistor and chip capacitor mounted parallel on the PC board. In this case, 50 Ω cannot be maintained due to the drop in the impedance characteristics of the transmission line at the division, so the waveform is disturbed by reflections. However, stacking the resistor on the capacitor as shown in Figure 7b eliminates the division in the transmission line, which maintains the impedance characteristics at 50 Ω while incorporating the equalizer function.

Since the Tx and Rx amplifiers are high-speed ICs, they have low ability to withstand ESD and there is a risk of damage to circuits because users frequently touch the input



MF2100B 6.25 GDIt/s

and output connectors. As a countermeasure, we strengthened the ESD performance by adding protection diodes to the Tx and Rx amplifiers (Figure 4).



a) Previous Mounting Method (Parallel)





Figure 7 Improved Equalizer Implementation

4 Performance Evaluation 4.1 PPG Output Waveform

Figure 8 shows the PPG output waveforms with a comparison of the newly developed MP2100B and the previous MP2100A. The RMS Jitter of the MP2100B is 0.99 ps at 12.5 Gbit/s compared to 2.53 ps at 12.5 Gbit/s for the MP2100A, decrease to less than 50%, and showing a high-quality waveform with no baseline ringing.

The main specifications of the MP2100B are listed in Table 1. The ED Rx sensitivity is 10 mVp-p (typ.) at 12.5 Gbit/s, or five times better than the MP2100A ED Rx sensitivity of 50 mVp-p at 12.5 Gbit/s.



d) MP2100A 6.25 Gbit/s



Table 1 MP2100B Key Specifications

| Item | Value |
|------------------------|---|
| BERT | |
| Number of channel | 4 |
| Bitrates | 125 Mbit/s to $12.5~\mathrm{Gbit/s}$ |
| Test Pattern | PRBS: 2 ⁷ -1, 2 ⁹ -1, 2 ¹⁵ -1, 2 ²³ -1, 2 ³¹ -1 (Inverted On/Off) User data: 1.3 Mbits |
| Data Output | |
| Amplitude | 0.1 Vp-p to 0.8 Vp-p |
| Tr/Tf | 24 ps (20 to 80%, typ.) |
| RMS Jitter | 1 ps (typ.) |
| Intrinsic RJ (RMS) | 600 fs (typ.) |
| Data Input Sensitivity | 10 mVp-p (typ.)@12.5 Gbit/s |
| Sampling Oscilloscope | |
| Power Input | 150 ksample/s (max.) |
| Sampling Speed | |
| Bandwidth (–3 dB) | DC to 25 GHz (typ.) |
| Flatness | ±1 dB (typ.) |
| Optical Input | 750 nm to 1650 nm |
| Wavelength | |
| Bandwidth (–3 dB) | DC to 9.0 GHz (typ.) |

4.2 Optical Transceiver Optical Rx Sensitivity Test

The optical Rx sensitivity test is used widely as an index of optical transceiver performance^{4), 9)}. Figure 9 shows the measurement block diagram for the optical Rx sensitivity test. As the DUT optical transceiver optical output signal is attenuated by a variable optical attenuator, the error rate increases vs the optical RX signal power. The optical Rx sensitivity test expresses this relationship. To minimize size and power consumption, commercially available SFP+ optical transceiver modules for 10GbE and QSFP+ modules for 40GbE commonly do not have a built-in clock recovery circuit. In this case, in addition to the optical transceiver itself, the analog performance, such as noise and jitter of the measuring instrument, has an impact on the measurement results. Consequently, achieving high-accuracy measurement requires a higher-quality PPG output waveform and a higher-sensitivity ED.

Figure 10 shows a comparison of the optical Rx sensitivity test results for an SFP+ optical transceiver as an example. The improved MP2100B performance is apparent not just for the 40GbE QSFP+ module but is also effective in increasing the 10GbE SFP+ measurement accuracy. To demonstrate this, we compared the results of an optical Rx sensitivity test for an SFP+ as DUT using the MP2100B, MP2100A, and Anritsu MP1800A with high-performance BERT. At an error rate of 1×10^{-11} , the optical Rx sensitivity of the MP2100B was -19.0 dBm while that of the predecessor MP2100A was -18.3 dBm, an improvement of 0.7 dB for the new model. This test result is less than the performance difference (5 times Rx sensitivity) when the PPG electrical signal was input directly to the ED as shown in section 4.1 because the input signal to the ED is affected by noise generated by the optical transceiver. Figure 11 shows each waveform for the MP2100B SFP+ optical Rx optical sensitivity test. The effect of noise increases relatively as the input optical signal power (amplitude) decreases, and the error rate worsens as the waveform degrades.



Figure 9 Optical Rx Sensitivity Test Measurement Block Diagram



Figure 10 Optical Transceiver SFP+ Optical Rx Sensitivity Test Results Comparison as an example (10.3125 Gbit/s, PRBS31)





4.3 Solved Problems

The newly developed MP2100B extends the BERT of the previous MP2100A to 4ch while retaining the same cabinet size and now supports all-in-one QSFP+ module tests. Additionally, the MP2100B ED Rx sensitivity is five times better than the MP2100A, and the optical transceiver optical Rx sensitivity test achieves a 0.7 dB better sensitivity than the MP2100A.

5 Conclusion

Optical interfaces are being deployed between servers and network equipment in data centers to cope with the explosive increase in traffic. This is increasing demand for optical transceivers, such as SFP+ for 10GbE and QSFP+ for 40GbE applications. We developed the all-in-one MP2100B with built-in 4ch 12.5 Gbit/s BERT and sampling oscilloscope to meet these test needs. By designing a compact 4ch BERT, the new MP2100B retains the same size as its predecessor MP2100A with 2ch BERT. From the performance aspect, both the PPG output waveform quality and ED sensitivity have been improved to produce 0.7-dB better optical transceiver optical Rx sensitivity test results than the MP2100A.

We expect to provide the best solution for BER and EYE pattern evaluations and to play a key role in improving development, manufacturing and quality evaluations of optical transceivers supporting future deployment of high-speed broadband communications infrastructure.

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