Development of Functional Modules using High-Performance InP DHBT for Measuring High-Speed Communications Systems

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[Summary] We developed functional modules for measuring high-speed communications systems required at transmission tests of next-generation technologies. The ICs in these modules were fabricated using InP Double Hetero-junction Bipolar Transistors (DHBT) offering excellent high speed and reliability. This article introduces the developed InP DBHT process technology and the 64 Gbaud 2-bit DAC, 64 Gbit/s 2:1 MUX, and 1:2 DEMUX modules fabricated from ICs using the developed InP DHBT technology.

1 Introduction

The spread of cloud computing services and smartphones requires faster data transmissions between servers and core networks. Consequently, standards bodies such as OIF, IEEE, etc., and leading research organizations are testing next-generation communications methods using Quadrature Amplitude Modulation (QAM) transmission and Non Retern to Zero (NRZ) transmission technologies. These transmission tests require bit error rate measurements. Transmission test systems for R&D into these next-generation transmission technologies can be configured using Anritsu's Signal Quality Analyzer MP1800A and functional modules for measuring high-speed communications systems. Functional modules used for measuring high-speed communications systems require high-speed, high-reliability integrated circuits (ICs) that are not generally available. As a result, we have developed InP Double Hetero-junction Bipolar Transistor (DHBT) process technologies for fabricating devices with excellent speed and reliability[1]. Various ICs using this process technology have been developed for functional modules for measuring high-speed communications systems.

This article begins by explaining this InP DHBT process technology and then introduces various developed functional modules for measuring high-speed communications systems.

2 InP DHBT Fabrication Technology

2.1 Required Device Performance and Fabrication

Functional modules incorporating fast and high-performance custom ICs help strengthen and extend the basic performance of instruments for measuring high-speed communications systems. In recent years, ICs have become more highly integrated and transistors comprising the basic element of devices must be both fast and have high uniformity. The speed of the InP/InGaAs/InP DHBT can be increased due to the excellent material characteristics of InP. Moreover, the characteristics are more uniform than the Field Effect Transistor (FET) and a high breakdown voltageis more easily secured. Consequently, the InP DHBT is considered to be an ideal basic device for use in functional modules for measuring high-speed communications systems.

Generally, to assure reliability, GaAs HBTs use a ridge structure leaving a depleted thin emitter layer around the emitter. On the other hand, since the etching controllability is lower for an InP DHBT, the ridge thickness is more variable, making formation of uniform transistors difficult. Consequently, we used a novel layer structure with an Etching Stop Layer (ESL) inserted into the InP emitter layer[1]. Inserting an extremely thin InGaAs layer of about 2 nm as the ESL using the wet etching method made it possible to fabricate the ridge. Figure 1 shows a cross-section of the developed InP DHBT with a stable ridge formed around the emitter.

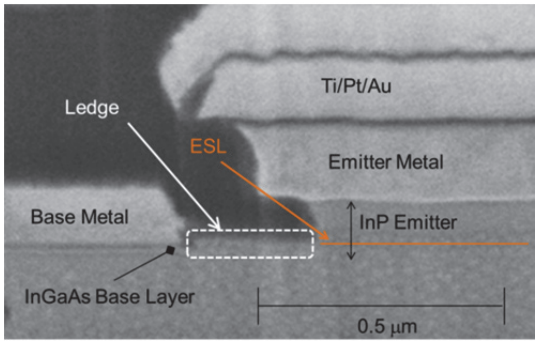


Figure 1 InP DHBT Cross Section

2.2 Device Characteristics

Figure 2 shows the *I-V* characteristics of the developed InP DHBT. The emitter size is 1 × 5 μm². This figure also shows that the characteristics are good with a breakdown voltage of better than 6 V. Moreover, the wafer-level variation of the DHBT current gain h_{FE} is sufficiently small at 1.5% max. with excellent uniformity due to the ESL. Next, Figure 3 shows the defendence of cutoff frequency f_T and maximum oscillation frequency f_{max} on collector current I_C. The value of f_T/f_{max} is 229/408 GHz when I_C = 10 mA, which is a sufficiently good value for implementing a functional module for measuring high-speed communications systems. Last, Figure 4 shows the Arrhenius plot for the Mean Time To Failure (MTTF) evaluation results as an index of reliability. With an MTTF of 1.5 × 10⁷ at a DHBT junction temperature T_J of 125°C derived from operating temperature tests, the InP DHBT has sufficient reliability for the intended application.

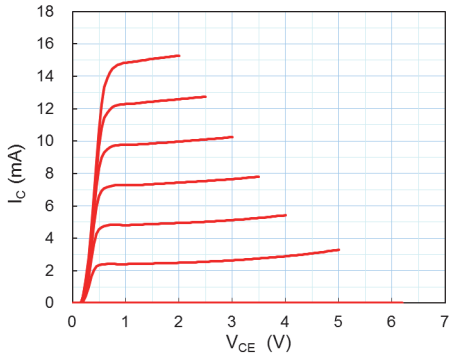


Figure 2 *I-V* Characteristics

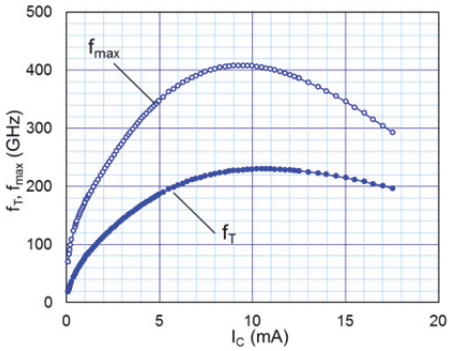


Figure 3 Dependence of f_T and f_{max} on I_C

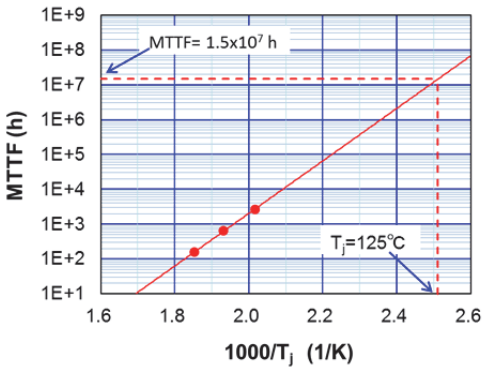


Figure 4 MTTF Arrhenius Plot

3 Functional Modules for Measuring High-speed Communications Systems

We designed and fabricated various types of IC using the developed InP DHBT process. We also developed various functional modules packaged in metal cases for measuring high-speed communications systems using these ICs.

A low-sheet resistance InP semiconductor-layer resistor, high-sheet resistance WSiN resistor and Metal-Insulator-Metal (MIM) capasitor were used as passive elements.

Either two- or three-layer interconnects was used for each IC, depending on the complexity of the circuit configuration. In addition, via holes were used to stabilize the IC thermal radiation and circuit operation.

Connections between the IC and module coaxial connectors were made using a Grounded Coplanar Waveguide (G-CPW) with excellent high-frequency characteristics. Coaxial V-connectors were used for ultra-high-speed connections, and coaxial K-connectors were used for other connections.

The following sections introduce the various functional modules developed under these conditions for measuring high-speed communications systems.

3.1 64 Gbaud 2-bit DAC with MUX (G0361A)

This module is a digital to analog converter (DAC) that can generate the 4-level Pulse Amplitude Modulation (PAM4) signal required by the latest high-speed interface standard. Figure 5 shows the DAC block diagram. The DAC is composed of a Clock buffer, two half-rate 2:1 multiplexers (MUX) and a DAC core. The two MUXes in the IC make it possible to output a high-speed PAM4 signal when driven by the MP1800A. Additionally, the DAC core uses a method to suppress PAM4 signal waveform distortion[2]. Figure 6 shows a photograph of the DAC chip. The IC has a transis-

tor count of 282. And the chip size is 2 × 3 mm^2. Figure 7 shows a photograph of the module which outputs a differential PAM4 signal by being input four Data signals and one Clock signal from the MP1800A to the module. The maximum operation baud rate is 64 Gbaud. The power consumption and power supply voltage are 2.1 W and –3.7 V, respectively. Figures 8 (a) and (b) show the PAM4 signal output waveform when operating at 56 and 64 Gbaud, respectively; the output amplitude is 800 mV.

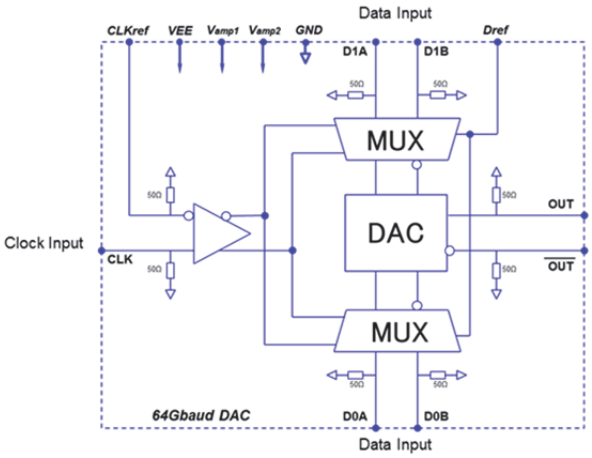


Figure 5 DAC Block Diagram

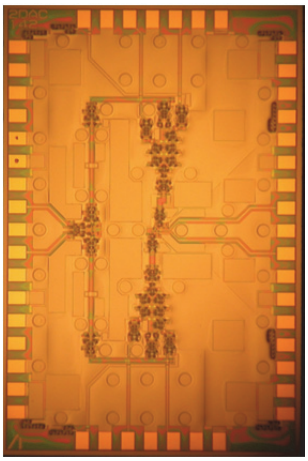
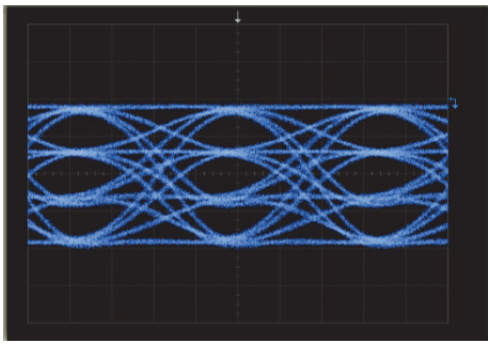
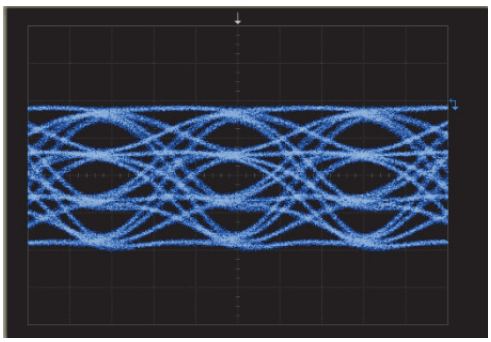


Figure 6 DAC Chip

Figure 7 DAC Module



(a) 56 Gbaud



(b) 64 Gbaud

Figure 8 PAM4 Signal Output Waveform (200 mV/div., 5 ps/div.)

3.2 64 Gbit/s 2:1 MUX (AH64175)

This module is a MUX for converting two external input NRZ signals to a high-speed NRZ signal. Figure 9 shows the block diagram of this MUX, which is composed of two Data buffers, Clock buffer, MUX core, and output buffer. The IC design emphasizes speed using Clock Signal Distribution (CSD) method[3]. Figure 10 shows a photograph of the MUX chip. The IC has a transistor count of 122. And the chip size is 2 × 2 mm^2. Figure 11 shows a photograph of the module which outputs a differential NRZ signal by being input two Data signals and one Clock signal from the MP1800A to the module. The maximum operation baud rate is 64 Gbaud. The power consumption and power supply voltage are 1.2 W and –3.5 V, respectively. Figures 12 (a) and (b) show the NRZ output waveform when operating at 56 and 64 Gbaud, respectively. The output amplitude and Jitter rms when operating at 56 Gbit/s are 427 mV and 260 fs, respectively. At 64 Gbit/s operation, the figures are 402 mV and 349 fs, respectively.

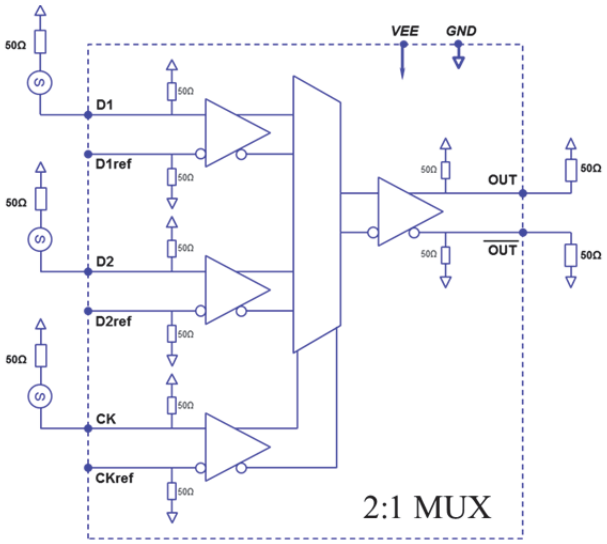


Figure 9 MUX Block Diagram

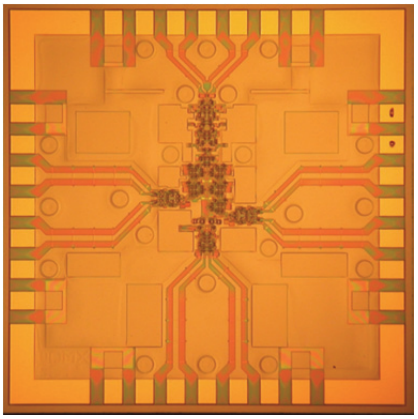


Figure 10 MUX Chip

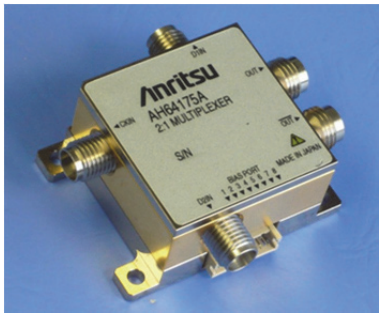
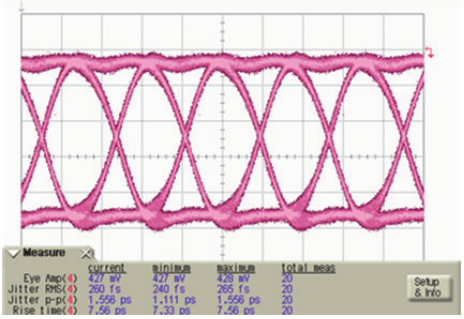
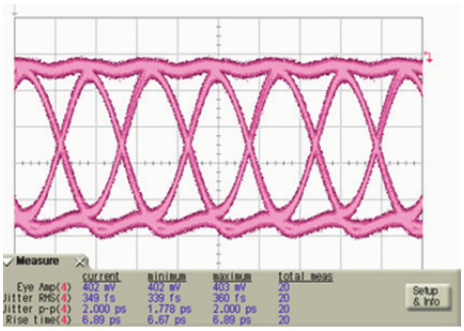


Figure 11 MUX Module



(a) 56 Gbit/s



(b) 64 Gbit/s

Figure 12 MUX Module Output Waveform

3.3 64 Gbit/s 1:2 DEMUX (AH64176A)

This module is a demultiplexer (DEMUX) for dividing an external output high-speed NRZ signal into two half-rate NRZ signals. Figure 13 shows the DEMUX block diagram. This DEMUX is composed of a Data buffer, Clock buffer, DEMUX core, and two output buffers. Like the MUX, the IC design emphasizes high speed using Clock Signal Distribution (CSD) method. Additionally, the pattern layout has been considered to simplify the module[4]. Figure 14 shows a photograph of the DEMUX chip. The IC has a transistor count of 124. And the chip size is 2 × 2 mm^2. Figure 15 shows a photograph of the module which outputs two half-rate NRZ signals by being input a high-speed NRZ signal and a Clock signal to the module. The maximum operation baud rate is 64 Gbaud. The power consumption and power supply voltage are 1.5 W and –3.5 V, respectively. Figure 16 shows the 10 and 32 Gbit/s output waveforms at input of 20 and 64 Gbit/s signals. The output amplitude and Jitter rms at 20 Gbit/s operation are 349 mV and 257 fs, respectively. The figures for 64 Gbit/s operation are 339 mV and 366 fs, respectively.

Using a combination of the MP1800A, 64 Gbit/s 2:1 MUX and 64 Gbit/s 1:2 DEMUX supports bit error rate measurements for NRZ signals up to 64 Gbit/s.

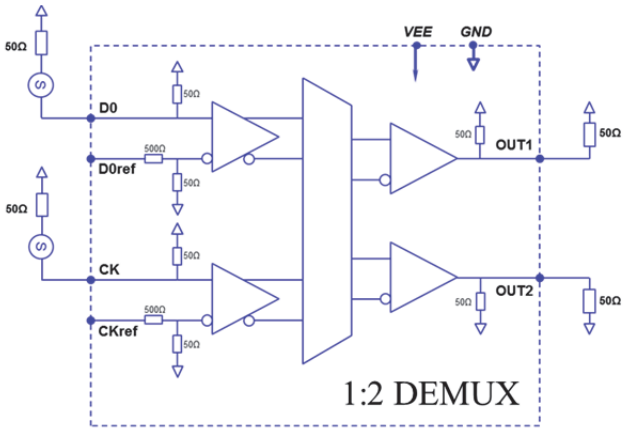


Figure 13 DEMUX Block Diagram

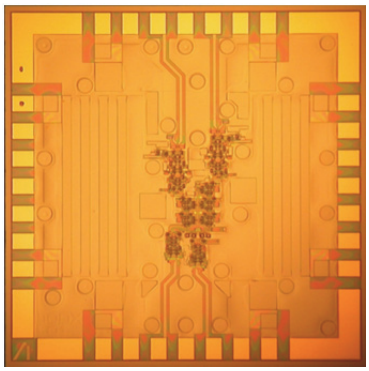


Figure 14 DEMUX Chip

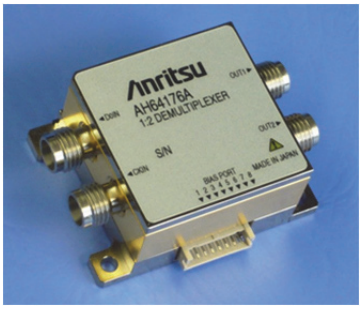
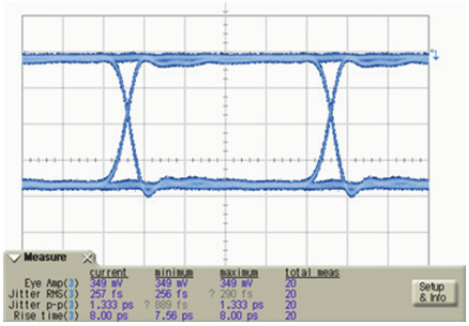
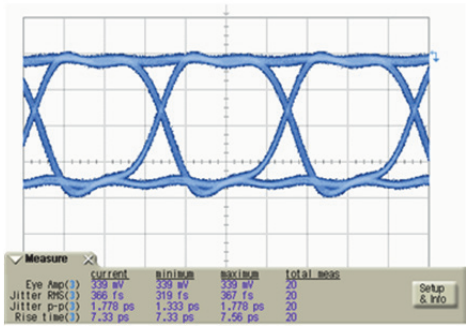


Figure 15 DEMUX Module



(a) 20 Gbit/s Input, 10 Gbit/s Output



(b) 64 Gbit/s Input, 32 Gbit/s Output

Figure 16 DEMUX Module Output Waveform

3.4 Differential Branch Amplifier (AH54172A)

When multiple signals are required, such as at bit error rate measurement, generally the Clock signal is divided using a power divider. However, since a power divider has a loss of 6 dB, there are issues with a drop in output level. The solution is to divide the Clock signal using an active element. This amplifier module divides a Clock signal into two differential signals. Figure 17 shows the amplifier block diagram. This amplifier is composed of an input buffer, signal distribution section, and two output buffers. Figure 18 shows a photograph of the amplifier chip. The IC transistor count is 42. And the chip size is 1.5 × 2 mm^2. Figure 19 shows a photograph of the module and Figure 20 shows the transmission characteristics (S21). The dc gain is 17 dB and the 3-dB bandwidth is 40 GHz. The power consumption and power supply voltage are 0.6 W and –3.5 V, respectively. Figure 21 shows the output waveforms at input of 10 and 30 GHz Clock signals. The output amplitudes at Clock signals of 10 and 30 GHz are 850 and 780 mV, respectively.

This module has excellent characteristics at division of a 32 GHz Clock signal and is ideal for supplying clocks to the 64 Gbaud DAC and 64 Gbit/s MUX/DEMUX modules.

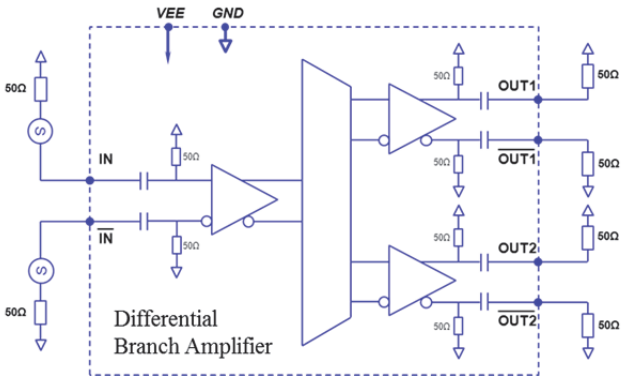


Figure 17 Differential Branch Amplifier Block Diagram

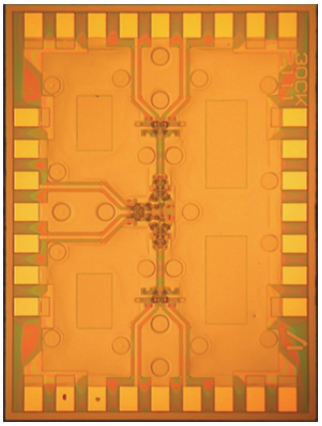


Figure 18 Differential Branch Amplifier Chip

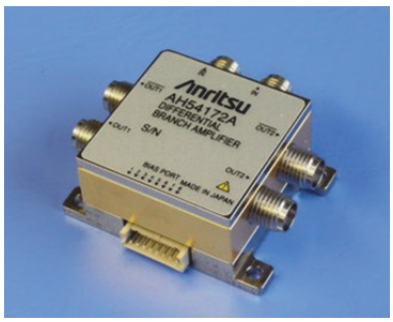


Figure 19 Differential Branch Amplifier Module

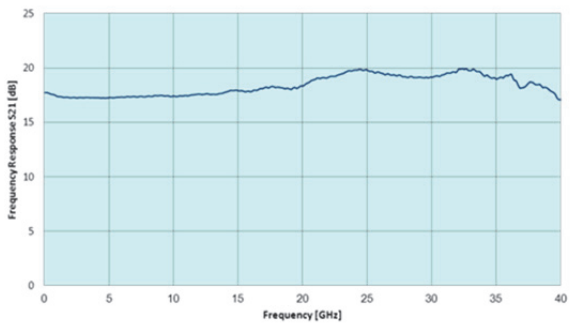
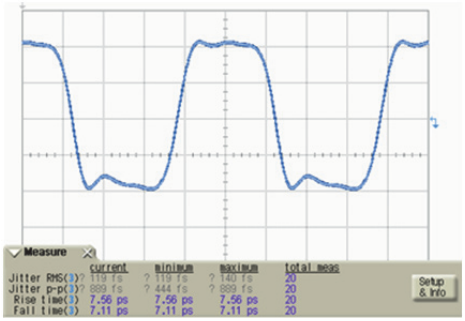
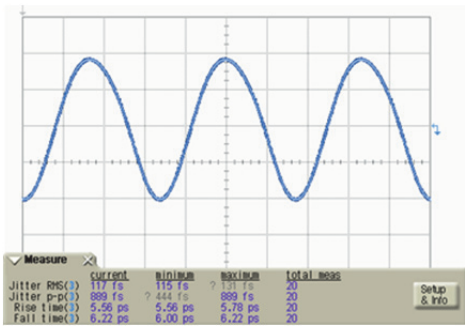


Figure 20 Transmission Characteristics of Differential Branch Amplifier



(a) 10 GHz



(b) 30 GHz

Figure 21 Differential Branch Amplifier Module Output Waveform

4 Conclusion

We have developed an InP DHBT with high speed and excellent reliability. This InP DHBT was used to develop various functional modules for measuring high-speed communications systems including using a signal quality analyzer to measure bit error rates at various high-speed transmission tests. Each of the developed functional modules is suitable for leading-edge high-speed transmission tests.

References

1) Y. Matsuoka, Y. Ohkubo, T. Matsumoto, T. Koji, Y. Amano, and A. Takagi, “On the Emitter Resistance of High-Performance GaAs- and InP-Based Heterojunction Bipolar Transistors”, Jpn. J. Appl. Phy. Vol. 47, pp. 4441- 4447, June 2008

2) Y. Arayashiki, M. Ikeda, Y. Amano, “80 GBd 6-bit DAC in InP DHBT for arbitrary waveform generator,” IET, Electronics letters, Vol. 52, No.23, pp. 1937-1938, 2016

3) Y. Arayashiki, Y. Ohkubo, T. Matsumoto, Y. Amano, A. Takagi, and Y. Matsuoka, “A 120-Gbit/s 1.27 W 520-mVpp 2:1 Multiplexer IC using Self-Aligned InP/InGaAs/InP DHBTs with Emitter Mesa Passivation,” IEICE, Trans. Electron. Vol. E93-C, pp. 1273-1278, August 2010

4) Y. Arayashiki, T. Kamizono, Y. Ohkubo, T. Matsumoto, Y. Amano, and Y. Matsuoka, "High-Bitrate-Measurement-System-Oriented Lower-Jitter 113-Gbit/s 2:1 Multiplexer and 1:2 Demultiplexer Modules Using 1-μm InP/InGaAs/InP Double Heterojunction Bipolar Transistors," IEICE, Trans. Electron. Vol. E96-C, pp. 912-919, June 2013

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