Development of Signal Quality Analyzer-R MP1900A for PCIe Gen4

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[Summary] The speed of interfaces in data-center equipment is being increased to cope with rising date-center traffic. Most importantly, interfaces using Rev. 1.0 of the PCI Express (PCIe hereafter) Gen4 standard released in October 2017 are expected to see future growth. We have developed the MP1900A with link training function to support early evaluation of the PCIe Gen4 physical layer, which will help with deployment of faster interfaces required by the growing Datacom market.

1 Introduction

Due to the increase in data traffic as a result of the popularity of smartphones and mobile terminals, Ethernet network interfaces in data centers are being upgraded to speeds of 200 and 400 Gbps. Moreover, the speed of communications equipment bus interfaces is being increased to PCIe Gen4 (16.0 GT/s). The Peripheral Component Interconnect (PCI) serial bus was created mainly as a fast internal bus for computers starting with Gen1 supporting a speed of 2.5 GT/s in 2002. Subsequently, Gen2 (5 GT/s) and Gen3 (8.0 GT/s) were released in 2006 and 2010, respectively, to solve speed bottlenecks. Standardization of Gen4 (16.0 GT/s) was completed in 2017 and release of new specifications, such as test procedures, is expected.

The PCIe standards are defined by the PCI-SIG standards organization, with participation by chipset vendors, Intellectual Property (IP) vendors, and measuring-instrument makers. In the compliance test for interconnectivity, not only the testing method but also measuring instruments and fixtures to be used are specified. Although release of the final Gen4 Standard was delayed by about 1 year from the expected release. This delay is said to have been caused by unexpected difficulties in implementing the higher speed of 16.0 GT/s. Currently, standardizing Gen5 for speeds of 32.0 GT/s has started but it is expected to involve and even higher degree of difficulty.

We have already released the Signal Quality Analyzer MP1800A (SQA hereafter) to support the increasing demand for quality analysis and management of optical modules, high-speed devices, etc., supporting 10, 25, and 100 GbE. However, when performing PCIe jitter tolerance tests, unlike current SQA tests, link training must be performed between the Device Under Test (DUT) and measuring instrument prior to measurement, requiring transition of the DUT to the loopback condition.

We have now developed the successor Signal Quality Analyzer-R MP1900A (SQA-R hereafter) with the following features to support PCIe testing.

- Link Training and Status State Machine (LTSSM) offering link training function with DUT
- 21G/32G bit/s SI PPG MU195020A Pulse Pattern Generator (SI PPG hereafter) supporting high-speed Emphasis switching required for PCIe measurement
- 21G/32G bit/s SI ED MU195040A Error Detector (SI ED hereafter) with high-accuracy Continuous Time Linear Equalizer (CTLE)
- Noise Generator MU195050A (Noise Gen hereafter) for Injecting various types of noise for stress testing
- PCIe Link Training MX183000A-PL021 software for controlling link training with DUT

Furthermore, in addition to supporting the Compliance Test, the SQA-R has an LTSSM analysis and trigger generation function for troubleshooting problems at the early development stage. These functions can shorten design time. Additionally, capital equipment costs are held down by future support for the Gen5 standard using software updates.

This article explains the SQA-R development concept, LTSSM function, other key functions, measurement examples, etc., for supporting PCIe measurements.

2 Development Concept

Until PCIe Gen3, physical layer evaluation methods were established by other makers' measuring instruments. Although Anritsu's SQA had the functions and performance for

physical layer evaluations at the Gen4 development stage, it did not support the Compliance Test required for mass production. Moreover, evaluation also required two noise generation sources in addition to the SQA as well as a complex procedure for coordination between instruments. Since no physical layer evaluation method has been established yet for PCIe Gen4, instrument makers and DUT vendors have been holding workshops since the Revision 1.0 release to establish measurement methods while performing measurements. In order to participate in the PICe workshop and establish the measurement method of PCIe Gen 4. We have developed the SQA-R as an all-in-one Bit Error Rate (BER) measuring instruments supporting PCIe Gen4 physical layer evaluation measurements.

3 Built-in LTSSM

Transitioning the DUT to the loopback state is managed by a state machine in the DUT called LTSSM, which is defined in the PCIe Base Specification[1]. Link training is performed between the DUT and measuring instrument to perform measurement by transitioning the DUT state (LTSSM) to the loopback state. LTSSM is built into the Field-Programmable Gate Array (FPGA) of SI PPG and SI ED to perform link training with the DUT.

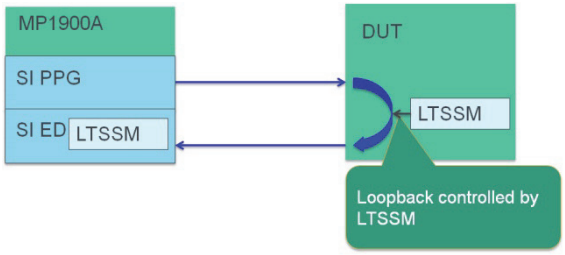


Figure 1 LTSSM Loopback Operation

3.1 Transition to Loopback State

There are two DUT loopback measurement methods for PCIe Gen4. The first method performs the transition using the Configuration State route. Since this method only uses simple link training, there are only a few transition states, making loopback easy. However, adjustment of both the output waveform and Rx equalizer is not possible. The second method performs the transition using the Recovery State route. This method has many transition states and link training is difficult, but both the output waveform and Rx equalizer can be adjusted to optimize the signal quality. The developed LTSSM supports both link trainings and

Figure 2 shows the transition flow to the loopback state at LTSSM.

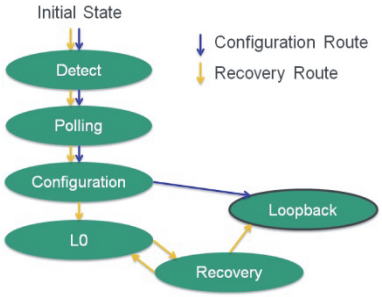


Figure 2 Transition to Loopback State using LTSSM

3.2 LTSSM Link Training Contents

Link training uses patterns called the Training Sequence Ordered Set (TS OS hereafter). Sending and receiving the TS OS are establish the bit alignment and symbol alignment, and exchanges physical layer parameters between the DUT and SQA-R. In addition, during link training, the Electrical Idle Ordered Set (EIOS hereafter) is sent, indicating the transmitter transition to the electrical idle state, and the Electrical Idle Exit Ordered Set (EIEOS hereafter) used for block alignment indicating transition from the electrical idle state.

The contents executed at each LTSSM state are explained below.

(1) Detect State

Detects electrical idle state and whether opposite device can connect or not

(2) Polling State

Exchanges TS OS and establishes bit alignment and symbol alignment

(3) Configuration State

Exchanges TS OS and negotiates link speed, lane width, and lane number; transitions to loopback state when loopback required

(4) L0 State

Normal operation state; transitions to Recovery state when negotiation establishes higher speed than Configuration State

(5) Recovery State

Changes bit rates for configured lanes and re-establishes bit alignment, symbol alignment, and block alignment; exchanges TS OS at this time to adjust both output waveform and Rx equalizer. Recovery state Gen4 (16.0 GT/s) is not reached by one

transition. Transitions through Recovery Gen1 (2.5 GT/s) → Gen3 (8.0 GT/s) → L0 → Recovery Gen3 (8.0 GT/s) → Gen4 (16.0 GT/s) path are required. Transit to loopback state when loopback required after changing to Gen4 (16.0 GT/s)

(6) Loopback State

Exchanges TS OS to perform loopback negotiation; after transition from Configuration State, changes bit rate from Gen1 (2.5 GT/s) to Gen4 (16.0 GT/s)

When establishing link training, the test pattern sent from SI PPG is looped-back in the DUT and can be received by SI ED.

3.3 LTSSM Block Structure

The LTSSM block in the FPGA is not just for performing link training; it also has PHY layer functions, log functions, functions for SI PPG control, and functions for control of high-speed Front End devices. Figure 3 shows the LTSSM block diagram and the functions of each block are explained below.

(1) SI ED PHY Block

Establishes bit synchronization, symbol synchronization, block synchronization for encodings (8b/10b, 128b/130b) used by PCIe and unscrambles and decodes TS OS; removes Skip Ordered Set (SKP OS) included in pattern

(2) LTSSM Log Block

Saves contents of link training as LTSSM log

(3) SI PPG Control Block

Directs creation of TS OS for link training for SI PPG Pattern Generator block; directs creation of test pattern after loopback. SI PPG PHY block automatically generates, EIOS, EIEOS, and SKP OS

(4) High-Speed Front End Control Block

Switches SI ED high-speed front end device to negotiated bit rate; switching Emphasis setting changes SI PPG output waveform to waveform trained in Recovery State

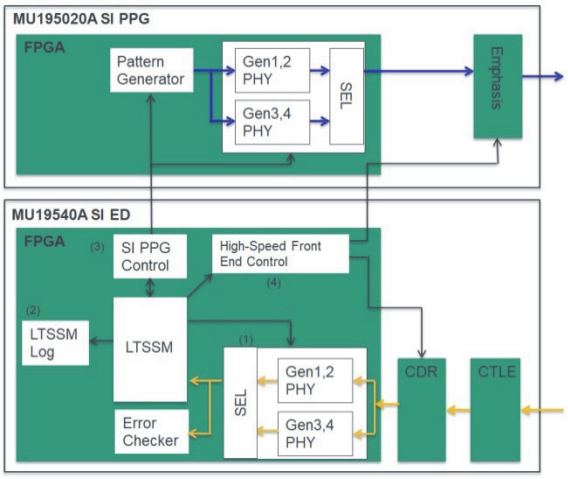


Figure 3 LTSSM Blocks

4 Built-in 10Tap Emphasis Function

Since digital high-frequency signal components become more attenuated as they pass through the printed circuit board pattern, the Eye pattern becomes closed. In typical interconnect interfaces such as PCIe, the open Eye pattern is maintained by previously performing compensation of this attenuation amount at the Tx side using a transfer technology called Emphasis. The Emphasis technology uses a Finite Impulse Response (FIR) filter to improve the waveform on the time axis by strengthening high-frequency components. When a degraded waveform is observed, applying a pre-optimized Emphasis gain maintains an open Eye pattern.

By using the above-described Emphasis technology, it is possible to simulate waveforms after passage through various devices and channels suffering degradation on the time axis due to attenuation of high-frequency components. For interconnect interfaces such as PCIe, up to three FIR filter taps (3Tap) are required to apply the necessary Emphasis. However, to simulate various attenuation-degraded waveforms, it is useful to have more taps and we have implemented a 10Tap (world's largest) Emphasis function in the SI PPG.

4.1 PCIe Emphasis Requirement

With PCIe Gen4, the Emphasis function required by the physical layer of the transmitter side has a De-emphasis function for strengthening the rising edge of the transferred waveform and a Pre-shoot function for strengthening the falling edge. Table 1 lists the 11 Preset settings defined by the PCIe Base Specification at a bit rate of 16 Gbit/s[1]. Since

De-emphasis and Pre-shoot are both required simultaneously by presettings P7 and P8, the minimum required tap count setting is 3Tap.

Table 1 Tx Preset Ratios

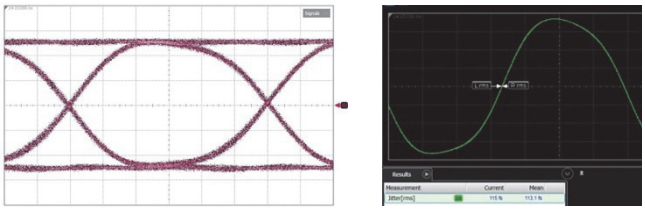
Preset	Pre-shoot	De-emphasis
P4	0.0	0.0
P1	0.0	−3.5 ±1 dB
P0	0.0	−6.0 ±1.5 dB
P9	3.5 ±1 dB	0.0
P8	3.5 ±1 dB	−3.5 ±1 dB
P7	3.5 ±1 dB	−6.0 ±1.5 dB
P5	1.9 ±1 dB	0.0
P6	2.5 ±1 dB	0.0
P3	0.0	−2.5 ±1 dB
P2	0.0	−4.4 ±1.5 dB
P10	0.0	Boost limit

4.2 Implemented Functions and Performance

Table 2 and Figure 4 show the main SI PPG performance.

Table 2 SI PPG Typical Specifications

Item	Specifications
Operation Bit Rate	2.4 to 21 Gbit/s or 32.1 Gbit/s
No of Channels	1 or 2
Output Amplitude	0.1 to 1.3 Vp-p (Single-end) 0.2 to 2.6 Vp-p (Differential)
Emphasis	10Tap (6post-Tap, 1main-Tap, 3pre-Tap) −20 to +20 dB
Tr/Tf (20 to 80%)	12 ps (typ.)
RJ	115 fs rms (typ.)



28.1 Gbit/s PRBS $2^{31}-1$
Typical Output Waveform

Low Intrinsic RJ 115 fs rms

Figure 4 SI PPG Output Waveform

As shown in Figure 4, the SI PPG has both fast rise (Tr) and fall times (Tf) as well as low jitter.

The SI PPG Emphasis function has the presets listed in Table 1. Choosing the required preset switches the applied Emphasis in less than 500 ns, and the user can set up to 16 preset values. As well as the Emphasis function, waveform simulating Inter-Symbol Interference (ISI) loss can also be generated using 10Tap Emphasis. Figure 5 shows a waveform adjustment example.

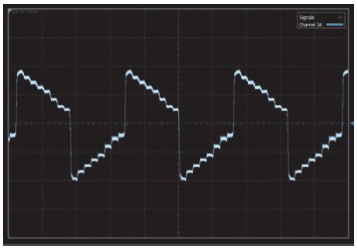


Figure 5 Waveform Adjusted with 10Tap Emphasis

4.3 PPG HIC

The SI PPG Data signal output section uses a Hybrid Integrated Circuit (HIC) structure composed of a thin-film substrate, bare IC chips, and peripheral circuits. The material of the thin-film substrate transmission path is quartz with a Grounded Coplanar Waveguide (GCPW) for excellent transfer characteristics from DC to high frequencies. Additionally, we used our own unique InP Heterojunction Bipolar Transistor (HBT) process to develop a dedicated Multiplexer Integrated Circuit (MUX IC) for impressing 10Tap Emphasis. This IC achieves high-quality output waveforms with low jitter and fast Tr/Tf at rates up to 32.1 Gbit/s.

4.4 Features and Advantages

The SI PPG can output high-quality waveforms at bit rates up to 32.1 Gbit/s, and features a built-in 10Tap Emphasis function. This all-in-one module supports all Emphasis settings required by interconnect interfaces such as PCIe. Moreover, it can simulate the output of waveforms degraded by passage through various devices and channels and also supports ISI estimates, helping play a role in efficient design verification of various devices.

5 Built-in CTLE

The CTLE is an equalizer function for attenuating low-frequency components at the Rx side to match the attenuation of high-frequency components. Balancing attenuation at low and high frequencies improves the Eye pattern opening.

5.1 PCIe Gen4 CTLE Requirements

The CTLE transfer function for PCIe Gen4 at 8.0 and 16.0 GT/s is defined as:

$$H(s) = \omega_{p2}\frac{s + \omega_{p1} * A_{DC}}{(s + \omega_{p1}) * (s + \omega_{p2})} \quad \text{--- (a)}$$

where, ω_{p1} is the low-frequency pole, ω_{p2} is the high-frequency pole, and A_{DC} is the adjustable DC gain. By substituting each value shown in Table 3 into Eq (a), we obtain the frequency characteristics plotted as shown in Figure 6.

Table 3 PCIe Gen4 CTLE Parameters

Parameter	8.0 GT/s	16.0 GT/s
ω_{p1} [rad/s]	2π*2 GHz	2π*4 GHz
ω_{p2} [rad/s]	2π*8 GHz	2π*16 GHz
A_{DC} [dB]	−6 to −12 dB	

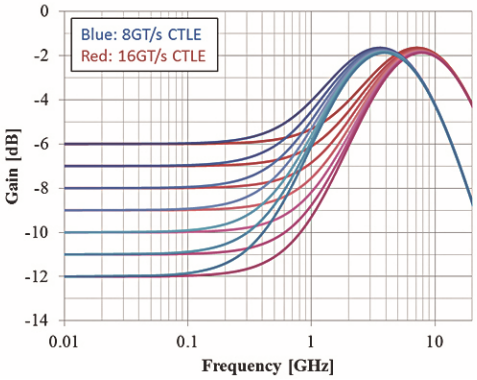


Figure 6 PCIe Gen4 CTLE Specifications

In other words, satisfying the requirements of the PCIe Gen4 standard requires:

(1) Variable low gain

(2) Frequency characteristics satisfying the defined transfer function

(3) Support for both 8.0 GT/s and 16.0 GT/s

5.2 Outline of Implemented Multiband CTLE

Using our unique InP HBT process, we developed a multiband CTLE Monolithic Microwave Integrated Circuit (MMIC) meeting the PCIe requirements. The CTLE block diagram is shown in Figure 7. This CTLE is composed of three CTLE blocks and one amplifier. In addition to CTLE support for both 8.0 GT/s and 16.0 GT/s, it also has the built-in CTLE supporting the 28.0 GT/s rate standardized by CEI28G-VSR of the Optical Internetworking Forum (OIF). Furthermore, the CTLE OFF route with no equalizer has a built-in amplifier extending the flatness to 40 GHz for implementing high-accuracy measurement supporting future equipment types. Switching each of these CTLE supports measurement of different bit rates.

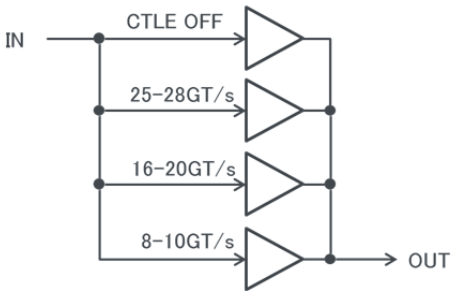
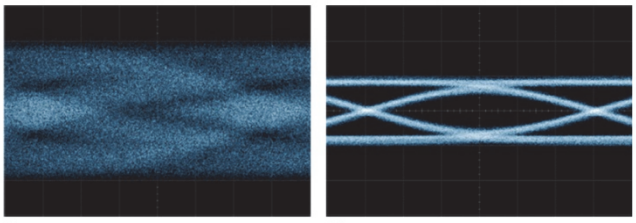


Figure 7 CTLE MMIC Block Diagram

5.3 Loss Compensation using CTLE MMIC

Figure 8(a) shows the waveform of the 400-mVp-p, 16.0-GT/s Data signal generated using the SI PPG after passage through a transmission path with 12 dB of loss at 8 GHz which is the Nyquist frequency. The plotted waveform points are widespread and spread across the center and the entire Eye pattern is blurred. Figure 8(b) shows the waveform after loss compensation using the developed CTLE MMIC. The waveform is plotted in the same position repeatedly, there are no plots near the center, and the form of the Eye is open and good, confirming the good loss compensation performance.

The CTLE MMIC shown above is built into the SI ED, supporting BER measurement even when the Eye pattern is closed as a result of transmission path losses.



(a) Waveform After Passage Through −12 dB at 8 GHz Channel (b) Waveform After Calibration Using CTLE

Figure 8 CTLE MMIC Loss Calibration Evaluation Example (16 GT/s)

6 Implemented Noise Generator

At the PCIe Gen4 receiver stressed Eye test, as well as injecting fixed values of Random Jitter (RJ) and Common Mode Interference (CMI) on the Data signal, Sinusoidal Jitter (SJ), Inter Symbol Interference (ISI), and Differential Mode Interference (DMI) are also injected[1]. Table 4 lists the parameters for the PCIe Gen4 16.0 GT/s stressed Eye standard.

Table 4 PCIe Gen4 16.0 GT/s Stressed Eye Parameters

Parameter	Specification
Eye Width (EW)	0.30 UI (18.25 to 19.25 ps)
Eye Height (EH)	15 mV (13.5 to 16.5 mV)
Long Rx Calibration Channel (ISI)	27 to 30 dB @ 8 GHz
Generator Launch Voltage	800 mVp-p Adjustment Range: 720 to 800 mVp-p
Swept Sinusoidal Jitter (SJ)	6.25 ps (6.25 to 6.75 ps) @ 100 MHz Adjustment Range: 5 to 10 ps p-p with Jitter Tolerance Mask
Random Jitter (RJ)	1.0 ps rms (fixed value)
Differential Mode Interference (DMI)	14 mVp-p (12 to 14 mV) @ 2.1 GHz Adjustment Range: 10 to 25 mVp-p
Common Mode Interference (CMI)	150 mVp-p @ 120 MHz (fixed value)

Here, EW and EH are obtained by fine-adjusting the Generator Launch Voltage, SJ, and DMI in the adjustment range shown in Table 4.

Noise Gen can inject the CMI and DMI required by the PCIe Gen4 receiver stressed Eye test simultaneously on the SI PPG output signal. The outline specifications for Noise Gen are listed in Table 5.

Table 5 Noise Gen Outline Specifications

Item	Specification
Data Input/Output Loss	−3.0 dB +1/−2.5 dB −3.3 dB (typ.) (U-shaped semi-rigid cable)
Differential Mode Interference (DMI)	4 to 200 mVp-p/1 mV Step (Differential)
	2 GHz to 10 GHz/10 MHz Step
Common Mode Interference (CMI)	10 to 250 mVp-p/2 mV Step (Single-ended)
	Low Band: 100 MHz to 1 GHz/ 1 MHz Step
	High Band:1 GHz to 6 GHz/ 10 MHz Step

Adding the maximum DMI amplitude of 25 mVp-p (Table 4) at the DUT connector requires an amplitude of about 79 mVp-p at the Noise Gen connector due to loss of about 10 dB at the Long Rx Calibration Channel of 2.1 GHz. Moreover, adding the CMI amplitude of 150 mVp-p (Table 4) at the DUT connector requires an amplitude of about 190 mVp-p at the Noise Gen connector due to loss of about 2 dB at 120 MHz. As shown in Table 5, Noise Gen has a sufficient amplitude and frequency setting range for both DMI and CMI for PCIe Gen4 evaluation.

To inject the CMI and DMI on the SI PPG Data signal, Noise Gen uses a Pickoff-Tee combiner designed to the latest specifications to minimize degradation of the SI PPG output waveform. Figure 9 shows the typical SI PPG 16-Gbit/s waveform after passage through Noise Gen. A similar waveform to that shown in Figure 4 is obtained. Additionally, Figure 10 shows the typical waveform with CMI and DMI noise injected on the Data signal by Noise Gen. As shown from Figures 9 and 10, Noise Gen causes very little waveform degradation due to passage through the module and can inject the required CMI and DMI.

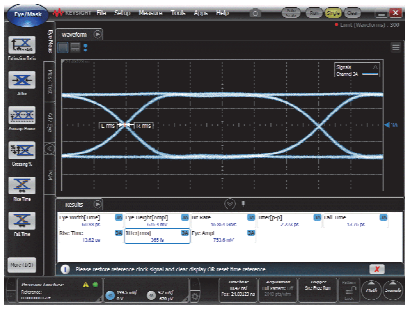


Figure 9 SI PPG 16-Gbit/s Waveform After Passing Noise Gen

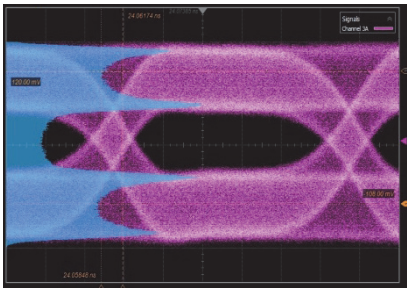


Figure 10 Typical Waveform with the injected CMI and DMI

Figure 11 shows the window for controlling Noise Gen using the SQA-R control software. The window is designed to give users an intuitive understanding of the setting conditions by visualizing the CMI and DMI signal, etc., flow based on the Noise Gen internal block diagram.

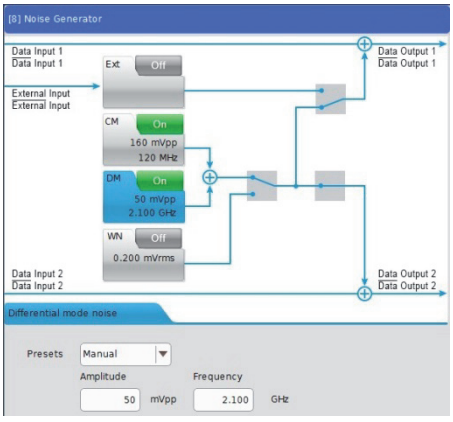


Figure 11 Noise Gen Control Window

7 Development of Link Training Software

At PCIe link training, the optimum Preset and CTLE values between the DUT and measuring instrument are determined, the DUT is transitioned to the Loopback.Active state and processing called Link Equalization is performed. Here, Link Equalization is executed at Recovery.Equalization, which is one of the LTSSM states, with the aim of determining dynamically the optimum Preset and CTLE values used at sending and receiving. This processing can often cause communication problems because many DUT parameters must be managed at high speed while requiring many complex state transitions at the same time. One problem with PCIe is allowing the DUT itself to perform state transitions using link training. To overcome this problem, the link training software not only has functions required for the Compliance test but also has a full range of functions for troubleshooting.

7.1 Link Training Tab

Figure 12 shows the Link Training tab at the Link Training window. If the DUT link training is unsuccessful, useful debugging information can be confirmed at the Link Training window. For example, it is possible to confirm the Tx and Rx SKP OS counts required for balancing-out frequency differences between Root complex and Endpoint, as well as the success or failure of Link Equalization. The Tx SKP OS count and Link Equalization parameters can also be changed easily at the Option window.

When linking is achieved successfully, the Compliance Test BER measurements and optional Jitter Tolerance Test can be executed.

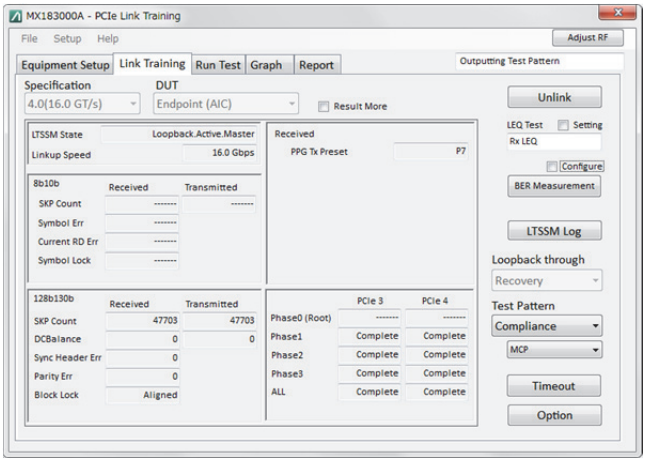


Figure 12 Link Training Tab

7.2 Link Training Log Viewer Function

Figure 13 shows the Link Training Log Viewer window. There is a logic analyzer to examine complex LTSSM state transitions, but this is difficult to test under the condition that the desired stress is applied to the data like the BERT system. Whereas using this application with built-in LTSSM Log function makes it easy to list LTSSM state transitions during link training. As a result, testing can be performed close to the logic layer in an actual stressed environment.

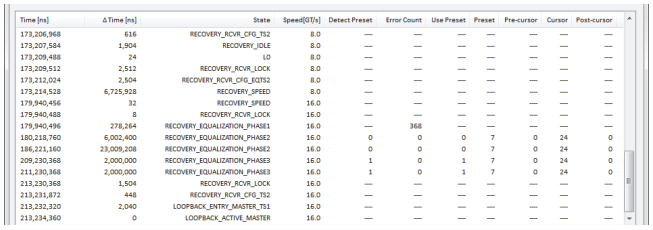


Figure 13 LTSSM Log Viewer

Using the above logs, it is possible to determine the state when the DUT has timed-out and the TRx parameters. Injecting or removing stress on the Data in these conditions enables analog-like debugging of DUT weaknesses and logic problems, helping cut DUT troubleshooting costs.

7.3 LTSSM Trigger Function

Figure 14 shows the LTSSM Trigger window. LTSSM Trigger is a function for outputting a pulse signal (trigger) from the SQA-R when transitioning to a specified state during link training. Combining this function with a real-time oscilloscope can capture Data waveforms at the pulse-signal timing. Unlike the previously described LTSSM Log state information, the actual data exchange before and after the specified state can be analyzed to strengthen debugging. Figure 14 shows the trigger setting screen and Figure 15 shows the pulse-signal Data waveform captured before and after the DUT presets change during Link Equalization.

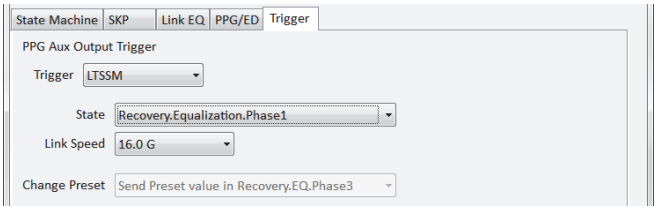


Figure 14 LTSSM Trigger

Figure 15 Link Equalization Output Waveform

8 PCIe Gen4 Phy Layer Rx Test Example

As an example of a PCIe Gen4 physical layer test using the SQA-R, Figure 16 shows the Rx test setup when using a PCIe Gen4 Add-in Card as the DUT.

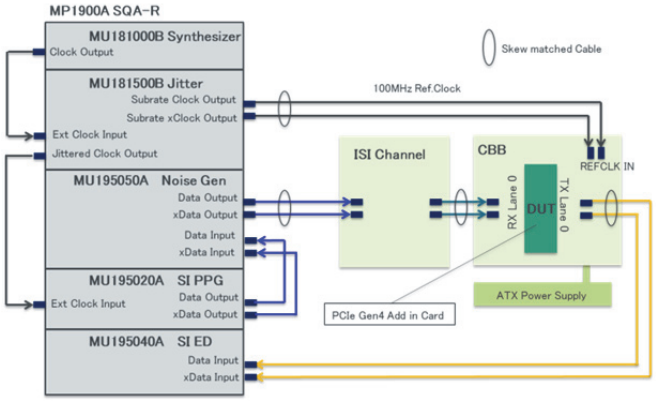


Figure 16 PCIe Gen4 Add-in-Card Rx Test Example

The Jitter module generates a Clock signal with added SJ and RJ, which is used by the SI PPG to generate the Data signal. The SI PPG output signal is connected to the Noise Gen module, which injects the DMI and CMI.

The Compliance Base Board (CBB) and ISI Channel are test fixtures supplied by PCI-SIG. CBB is for extracting the DUT signal and supplying the Clock and power. The test is executed using a common Clock and supplies a 100-MHz reference clock from the Jitter module to the CBB. ISI Channel is used to make a transmission path with a nominal loss of 28 dB at 8 GHz which is the Nyquist frequency of 16.0 GT/s and calibrate the Eye diagram of the signal input to the DUT to the standert value. Stressed signals at the CBB (DUT) input connector are captured by the real-time oscilloscope and the degree of the Eye pattern opening is calculated using the Sigtest dedicated PCIe waveform analysis tool for calibration. The procedure from adjusting the amount of applied stress and amplitude to calculating the parameters EW and EH is repeated for input to the standard values required by PCIe Gen4 16.0 GT/s listed in Table 4.

After calibration, link training is performed using LTSSM, and the DUT transitions to the loopback state. The Gen4 Modified Compliance Pattern is used as the test pattern after loopback. The DUT must achieve a BER of 10^{-12} in this state.

Figure 17 shows the SQA-R measurement results. Confirming the BER of 10^{-12} required about 63 s. A large PASS or FAIL evaluation result display when measurement is completed makes it easy to confirm the result.

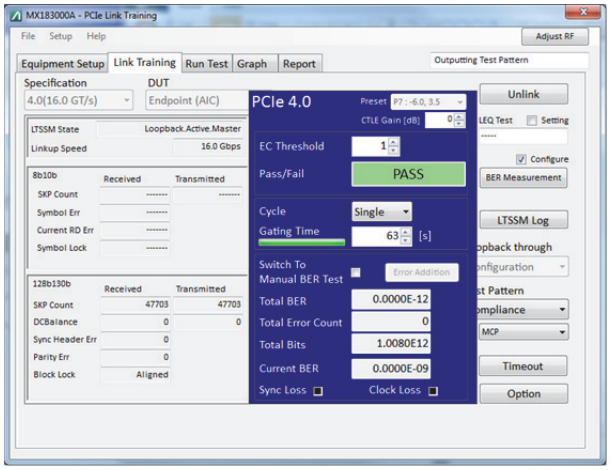


Figure 17 Rx Test Results Window

9 Conclusion

We have developed the MP1900A SQA-R to support evaluation of the PCIe Gen4 physical layer which will help increase interface speeds as required by the growing Datacom market. The all-in-one SQA-R for PCIe testing is easy to operate and will play a key role in evaluating the PCIe Gen4 physical layer through future links with PCI-SIG and workshops.

In addition, planning for the new PCIe Gen5 (32.0 GT/s) standard has started and the SQA-R has been designed with futureproof performance and features supporting Gen5 in mind. Anritsu continues its efforts to support the new measurement needs of the growing Datacom market.

References

1) PCI-SIG, “PCI Express Base Specification, Rev. 4.0 Version 1.0”, PCI Express Base Specification, Rev. 4.0 Version 1.0, pp.287, pp.1022, pp.1053-1061, (September 27, 2017)

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