# **Development of Sampling Oscilloscope MP2110A**

#### Takashi Murakami, Yuki Yokoyama, Takashi Kamizono, Fumihito Hirabayashi

[Summary] We developed the MP2110A with built-in 25 Gbit/s 4ch Bit Error Rate Tester and sampling oscilloscope to support all-in-one performance tests of optical transceivers for 100GbE networks expected to see increasing future demand. The sampling oscilloscope uses a newly designed 40-GHz O/E module as well as new sampler modules and high-accuracy trigger system. Evaluation results confirm high-accuracy Mask Margin measurements of -13.6 dBm and excellent jitter performance of 174 fs rms.

#### 1 Introduction

Due to the explosive increase in data traffic caused by the spread of cloud computing services, the transfer capacity of servers and network equipment in data centers needs urgent increase<sup>1) to 3)</sup>. Interfaces between servers and network equipment in data centers are being converted to optical technology, creating rapidly increasing demand for optical transceivers. In particular, the demand for SFP28 form-factor modules for 25GbE (25 Gigabit Ethernet) and for QFSP28 form-factor modules for 100GbE (25 Gbit/s  $\times$  4 lanes) is expected to grow rapidly after 2016. Development and manufacturing of optical transceivers requires a Bit Error Rate Tester (BERT) and sampling oscilloscope for Eye pattern analysis<sup>4)</sup>. Anritsu released its all-in-one MP2100B with built-in 4ch BERT and sampling oscilloscope for the R&D and manufacturing markets in 2015<sup>5)</sup>. However, the MP2100B is limited to a maximum measurable bit rate of 12.5 Gbit/s, and does not support measurement of optical transceivers for 25GbE and 100GbE. Consequently, we have developed the all-in-one MP2110A with built-in 4ch BERT and sampling oscilloscope supporting bit rates up to 25 Gbit/s and enabling both BER measurements and measurements of optical output waveforms of SFP28 and QSFP28 optical transceiver modules.

To observe 25-Gbit/s signals, the overall design of the sampling oscilloscope in the developed MP2110A has been changed. In concrete terms, to widen the analog input band, we designed a new 40-GHz optical band optical-to-electrical (O/E) conversion module as well as a 40-GHz electrical band sampler module. Furthermore, a new trigger system has been adopted and intrinsic jitter generated within the measuring instrument has been reduced to an average of 200 fs rms. This article explains the key points in designing these fundamental technologies.

# 2 Basic Configuration 2.1 MP2110A Configuration

Figure 1 shows an external view of the developed MP2110A incorporating both a BERT and sampling oscilloscope (oscilloscope hereafter) in one cabinet. As seen from the front panel, the oscilloscope is located above the BERT. Since a display for the Graphical User Interface (GUI) is not commonly required on optical transceiver production lines, an external display can be connected when necessary.



Figure 1 External View of MP2110A

Figure 2 shows the MP2110A block diagram. The BERT is composed of a 4ch Pulse Pattern Generator (PPG) and 4ch Error Detector (ED) and outputs a Clock signal synchronized with the PPG at the Clock Output connector. The Sync Output connector outputs a Clock signal synchronized with the pulse pattern. The oscilloscope has Data input connectors for two channels (Ch A Input, Ch B Input) and a Trigger Clock Input connector. The user can choose either electrical or optical channels for the Data input connectors.



Figure 2 MP2110A Block Diagram

#### 2.2 Oscilloscope Configuration

Figure 3 shows the oscilloscope block diagram. In this diagram, Ch A is the electrical channel, and Ch B is the optical channel. In the Ch A electrical channel, the input signal is input to the sampler module. In the Ch B optical channel, the input signal is converted to an electrical signal by the O/E converter module (O/E module hereafter) before input to the sampler module in the same way as the electrical channel. The sampler module samples Ch A or Ch B based on a timing signal from the trigger system. The level of the signal output from the sampler module is converted to digital data by the Analog to Digital Converter (ADC) after amplification by the Intermediate Frequency (IF) circuit. The digitally converted data is analyzed by software processing using the Field-Programmable Gate Array (FPGA) and CPU before final display of Eye pattern analysis results.

A Clock signal synchronized with the Ch A or Ch B input signal is input to the Trigger Clock Input connector. This Clock signal is controlled by the trigger circuit and a signal of several 100 kHz is supplied to the sampler module and FPGA as a low-speed timing signal.



Figure 3 Oscilloscope Block Diagram

#### 3 Design Requirements

#### 3.1 Optical Signal Sampling System

The IEEE802.3 standard defines the optical Tx waveform Eye pattern using a standard Eye Mask to assure interoperability between optical transceivers. This standard requires the oscilloscope analog input band (3 dB) for Eye pattern observation to be equal to 75% of the observed signal bit-rate frequency. For example, when the bit rate is 25.78125 Gbit/s, a 3-dB bandwidth of 19.34 GHz is required.

Separate from the interoperability test, when analyzing the accuracy of the tansition time of the Tx waveform and overshoot at development and production of optical modules, the oscilloscope requires a sufficiently wider input band than the observed signal bit-rate frequency. For example, when the bit rate is 25.78125 Gbit/s, an input band of three times the reference frequency, or 40 GHz, is required.

When using the MP2110A, the oscilloscope optical channel analog input band is determined by the O/E module and sampler module shown in Figure 3. To implement high-sensitivity wideband characteristics for up to 40 GHz, we designed a new O/E module and sampler module for the MP2110A.

#### 3.1.1 Wideband O/E Module Development

Figure 4 shows the block diagram of the developed O/E module, which is composed of a photodiode (PD), trans-impedance amplifier (TIA) and equalizer. Figure 5 shows and example of the frequency characteristics for an O/E module composed of PD and TIA only (without equalizer dotted line in graph). In this example, the PD and TIA-only configuration is attenuated by about 3 dB at 17.5 GHz, which does not meet the required band. Consequently, we designed a wider bandwidth O/E module by correcting the attenuation using an equalizer. The solid line in Figure 5 shows an example of the O/E module characteristics with built- in equalizer, confirming an improvement in the 3-dB band characteristics up to 40 GHz.



Figure 4 O/E Module Block Diagram



Figure 5 Developed O/E Module Characteristics (1310-nm band)

In addition to wideband performance, both wavelength range and sensitivity are also important O/E module performance requirements. The 100GbE standard requires two wavebands of 1310 nm and 850 nm. Analysis of two wavebands is supported by using a PD supporting both wavebands. However, since the Rx sensitivity (A/W units) of this type of PD is tuned to be maximum at wavebands around 1000 nm, there is a problem with optical Rx sensitivity not being high at either the 1310<sup>-</sup> or 850<sup>-</sup>nm band. To obtain the maximum optical Rx sensitivity at each wavelength, the MP2110A uses a separate PD for each 1310<sup>-</sup> and 850<sup>-</sup>nm band. The Rx switching method is used in the MP2110A to switch the two O/E modules for the wavelength bands.

#### 3.1.2 Coupling with Wideband Sampler Module

The developed 40-GHz band O/E module does not have a function for adjusting the 3-dB band. Consequently, implementing the 3-dB band for 19.34 GHz required for compatible connectivity described in section 3.1, requires a low pass filter (LPF) function at the downstream stage. This LPF is implemented in the MP2110A using the sampler modules. Figure 6 shows the developed sampler module internal block diagram. Two sampling diodes are connected to the electrical signal input ports of the sampler module and terminated to ground (GND) via a  $50-\Omega$  resistance.

A reverse-bias voltage is impressed on each sampling diode so that it does not operate usually. In other words, the sampling diode is normally in the non-conductive state. However, when a strobe pulse is impressed from the trigger circuit, the sampling diode switches to the conductive state for the duration of the impressed strobe pulse. The sampling capacitor is charged in accordance with the input signal level during this time interval. The sampling diode returns to the non-conductive state when the strobe pulse is no longer impressed, but the sampling capacitor holds its charged state. The charge voltage is read until impression of the next strobe pulse to sample and process the Eye pattern waveform.



Figure 6 Sampler Module Block Diagram

The sampler module 3-dB bandwidth is determined by the time when the sampling diode changes to the conductive state<sup>6)</sup>. If the conductive state time can be controlled accordingly, the sampling module band can be changed. As described above, usually a reverse-bias is impressed on the sampling diode. The diode conductive time becomes shorter when the strobe pulse is impressed in the high reverse-bias condition. Conversely, the diode conductive time becomes longer when the strobe pulse is impressed in the low reverse-bias condition. In other words, the sampler module bandwidth can be adjusted by controlling the reverse-bias voltage. Figure 7 outlines the changes in the sampler module frequency response when the reverse-bias voltage is adjusted. In the new sampler module design, the sampling diode operation frequency is extended to 40 GHz, and the 3-dB band can be changed from 17 to 40 GHz.



Figure 7 Relationship between Reverse Bias Voltage and Bandwidth

### 3.2 Trigger System

Figure 8 shows the MP2110A trigger system block diagram.



Figure 8 Trigger System Block Diagram

The trigger system is composed of a frequency divider, Direct Digital Synthesizer (DDS), and BPF. The first-stage frequency divider adjusts the supplied trigger Clock frequency to the DDS input range. When the trigger Clock frequency is smaller than the DDS input range, it is multiplied using a Phase Locked Loop (PLL). The further DDS-divided Clock signal is connected to a downstream BPF where unwanted components, such as image and harmonic components appearing in the DDS output, are removed. Finally, another frequency divider is used to convert the signal to a frequency that can be used by the sampler module. Next, a step recovery diode (SRD) driver converts the signal to the voltage level required to operate the sampler module which is output as the signal for driving the sampler module. The trigger system frequency division operation is expressed as follows:

Frigger System Output Frequency 
$$= \frac{B}{S} \times \frac{1}{P} \times \frac{N}{M} \times \frac{1}{L}$$
  
 $= \frac{B \times N}{S \times P \times M \times L}$  (1)

Where *B* is the measured signal rate, *S* is the supplied synchronous Clock division, *P* is the first-stage frequency divider division, *N/M* is the DDS division, and *L* is the last-stage division. Additionally, *S*, *P*, *N*, *M*, and *L* are all positive values. The trigger system output signal synchronization is expressed as the reciprocal of Eq (1):

Trigger System Output Period = 
$$\frac{S \times P \times M \times L}{B \times N}$$
 (2)

Since 1/B is equivalent to UI (Unit Interval), Eq (2) can be expressed as:

Trigger System Output Period = 
$$\frac{S \times P \times M \times L}{N}$$
 [U1] (3)

When the numerator and denominator in Eq (3) have a relative prime relationship, when a trigger occurs N times, phase shift occur only  $S \times P \times M \times L$  [*UI*] relative to the input signal, and  $S \times P \times M \times L$  becomes a positive value due to the preconditions. As a result, in this trigger system, sampling is possible by sweeping the in-bit phase for N samples based on the value of N set at the DDS.

To suppress intrinsic jitter generated by the trigger system, the MP2110A has a new built-in, precision trigger option. The system block diagram for this precision trigger function is shown in Figure 9. The basic configuration is the same as Figure 8 but the BPF output signal passes to the sampler module via a delay circuit for jitter correction. The sampler module for jitter correction is driven by the output of the final stage SRD driver. Consequently, the sampler module for jitter correction samples the signal output from the delay (called Reference Clock) at this division timing.



Figure 9 Precision Trigger System Block Diagram

This state is explained in Figure 10. The delay is adjusted so that sampling is performed at center timing of the reference clock rising edge. Due to the division relationship between Ref. Clock and Strobe Signal, the sample data series (Sampled Data) is almost a constant value. When the sampler module internal noise is sufficiently small, minute voltage fluctuations generated in Sampled Data at each sample are caused by the difference between the Ref. Clock timing drift (called Reference Clock Jitter) and the Strobe Signal timing drift (called Sampling Jitter). When the Reference Clock Jitter is relatively small compared to Sampling Jitter, changes in the Sampled Data voltage are expressed as changes in Sampling Jitter. In other words, Sampling Jitter generated in the trigger system is detected by the sampler module for jitter correction.



Figure 10 Jitter Calibration at High-Sensitivity Trigger

Similarly, the DUT signal sampler module shown at the top of Figure 9 is affected by Sampling Jitter included in the trigger signal. However, the effect can be suppressed when drawing the Eye pattern of the DUT signal by subtracting Sampling Jitter detected by the sampler module for correction. Notwithstanding this, internal noise and Reference Clock Jitter are not removed by passage through the sampler module for removing Sampled Jitter and remain unsuppressed in the signal. The MP2110A has been designed to hold intrinsic jitter to 200 fs rms or less by using low-noise sampler modules and a DDS system generating a high-purity Reference Clock.

#### 4 Performance Evaluation

# 4.1 Optical Signal Waveform and Sensitivity Performance

Figure 11 shows the observed waveform for an LN modulator at 25.78125 Gbit/s using a PRBS2<sup>31</sup>-1 pattern with an extinction ratio of 10 dB and an average input power of -2dBm. The waveform distortion is small with a Mask Margin of 43% and an excellent jitter performance of 800 fs rms. Figure 12 shows the results for the Mask Margin optical input power dependency evaluated using the output waveform of this modulator. Here, the optical input power is attenuated by an external optical attenuator for input to the oscilloscope. Normally, as the optical input level becomes smaller, the noise generated inside the oscilloscope becomes relatively larger compared to the DUT signal and the Mask Margin gradually deteriorates. In these test results, the optical input level when the Mask Margin is less than 0% was -13.5 dBm, above the target of -12 dBm.



Figure 11 Observed Optical Waveform (25.78125 Gbit/s, LN Modulator)





#### 4.2 Precision Trigger Performance

Figure 13 shows the observed waveform when inputting an electrical 10-GHz sine-wave signal output from a commercial high-purity synthesizer (-130 dBc/Hz @ 1 MHz Offset) to the MP2110A. At this measurement, the 10-GHz sine-wave signal was split into two for input to the oscilloscope electrical signal input connector and Trigger Clock connector. Since the electrical signal and trigger Clock have the same timing, the observed jitter indicates jitter generated within the oscilloscope. The observed jitter with the precision trigger function off was 300 fs rms, but improved to 230 fs rms when the function was set to on. Using this precision trigger function is believed to suppress Sampling Jitter in the MP2110A. Figure 14 shows the observed jitter when the trigger input frequency is changed using a commercial synthesizer. Based on this result, the achieved average value of 174 fs rms exceeded the target value of 200 fs rms in the trigger frequency range from 2.4 GHz to 15 GHz.



Figure 13 Observed Jitter at 10-GHz Input Frequency (Left: Precision Trigger OFF; Right: ON)



Figure 14 Relationship between Trigger Frequency and Observer Jitter at Precision Trigger ON

## 5 Conclusion

Demand for optical transceivers for 25GbE and 100GbE networks is increasing rapidly due to the explosive growth in data traffic at data centers. To meet test requirements, we developed the all-in-one MP2110A with built-in 4ch BERT and sampling oscilloscope supporting bit rates of 25 Gbit/s. The newly developed 40-GHz sampler module and 40-GHz O/E module for the sampling oscilloscope supports high-accuracy Mask Margin measurements of -13.6 dBm. Additionally, adoption of a new trigger system achieved a trigger jitter performance of 174 fs rms.

By offering flexible solutions for evaluating BER and Eye patterns of future communications systems, we hope to play a key role both in upgrading the development and production efficiency of optical transceivers supporting high-speed, large-capacity communications infrastructure as well as in improved quality evaluation.

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# Authors



Takashi Murakami Product Development Dept.





Yuki Yokoyama Product Development Dept. Service Infrastructure Solutions Division



Takashi Kamizono

High Speed Device Development Dept. Device Development Center



Fumihito Hirabayashi High Speed Device Development Dept. Device Development Center