Development of MU100011A 100G Module for 5G Mobile Fronthaul and Backhaul Measurements

Tomohiro Ito, Atsushi Furuki, Hokuto Saeki, Akinobu Tsuyuki

[Summary] Adoption of the Common Public Radio Interface and Radio over Ethernet technologies is being examined to implement the enhanced Mobile BroadBand 5G requirement at low cost. Improving the clock synchronization accuracy between base stations is a key issue for 5G mobile networks and we have developed the new MU100011A as a 100G module for the MT1000A to meet this market requirement as soon as possible. Moreover, we have added an eCPRI/RoE measurement function and improved the latency and clock synchronization measurement functions.

1 Introduction

As well as featuring evolving enhanced Mobile BroadBand (eMBB) attributes, fifth-generation (5G) mobile communications systems must also support new network requirements, such as Ultra-Reliable and Low Latency Communications (URLLC) and massive Machine Type Communications (mMTC), to offer stable basic services, including 4K video streaming, IoT functions typically represented by sensor business, and self-driving vehicles services[1), 2)].

A switch from the 4G mainstream Common Public Radio Interface (CPRI) technology to the Enhanced Common Public Radio Interface (eCPRI) and Radio over Ethernet (RoE) technologies is now being examined to implement eMBB for the mobile fronthaul (MFH) network segment. eCPRI and RoE are Ethernet interface technologies supporting 10GbE and 25GbE transmission speeds now becoming the market main stream. The resulting increased MFH capacity is expected to lead to faster 100GbE speeds in the mobile backhaul (MBH) network segment. Implementing URLLC to achieve this fast and large capacity for excellent reliability and response times supporting new services, such as self-driving vehicles, requires low network latency of 1 ms or less.

For evaluating fast and lotency mobile network, the tester is required compact and lightweight for on-site use, in addition to high speed, high functionality, and high performance. To support 5G MFH and MBH evaluations using the Network Master Pro MT1000A series, we performed the following.

(1) Developed compact and lightweight MU100011A module for 25GbE and 100GbE evaluations

(2) Added eCPRI and RoE Frame generation and analysis functions

(3) Strengthened latency measurement function and improved clock synchronization accuracy

Section 2 of this article explains the MFH standardization trends; section 3 explains the MU100011A hardware design requirements; section 4 explains the frame generation function; and section 5 explains the function improvements.

2 Trends in 5G Mobile Fronthaul Network Standards

The MFH required Tx band and permissible latency differ according to the division of functions between the Central Unit (CU) node and the Distributed Unit (DU) node. The permissible latency requirements become more severe as the required transmission band approaches the Radio Frequency (RF) side. When the functional split between the CU and DU is lower (RF side) than between the Media Access Control (MAC) and Physical (PHY) layer) (Figure 1 Option 6), the required transmission band exceeds 10 Gbit/s. For example, the band is about 160 Gbit/s when split at Option 8 in the same manner as CPRI in current MFH interfaces[1)].

Configuring the MFH by extending current technology like this massively increases the required transmission band. To reduce the required transmission band, functional separation of the mobile base station remote radio head (RRH) unit and the baseband processing unit (BBU) is being re-examined[1)]. Additionally, the wideband and stable Ethernet-based eCPRI and RoE technologies standardized by CPRI and IEEE1914 are being adopted as new MFH interfaces.

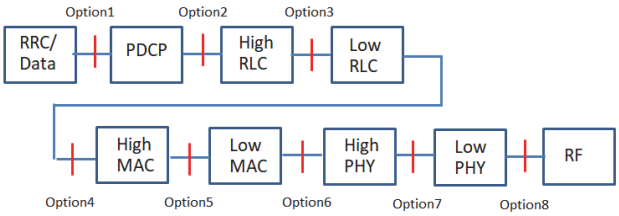
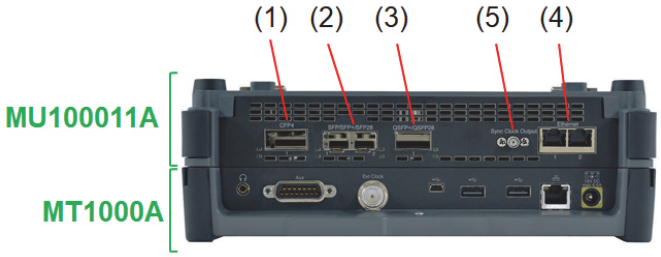


Figure 1 Division of Functions Between CU and DU[3)]

3 MU100011A 100G Multirate Module

3.1 MU100011A Outline

Figure 2 shows the external appearance of the MT1000A with installed MU100011A. The MU100011A is not only compact and lightweight but also supports multiple interfaces up to 100 Gbit/s. It has an electrical interface for various transceivers meeting the CFP4, QSFP28, and SFP28 standards as well as an RJ45 interface, and support Ethernet including 100G, 40G, 25G, 10G, 1G, 1000M, 100M, and 10M, Optical Transport Networks (OTN), Fibre Channel, and transport networks, such as CPRI. In addition to the measurement interfaces, there is also a Sync Clock Output connector to connect a sampling oscilloscope trigger signal for monitoring optical waveforms. The optical waveforms output from optical transceivers connected to each interface can be monitored using this setup.



(1) CFP4, (2) SFP28, (3) QSFP28, (4) RJ45, (5) Sync Clock Output

Figure 2 External Top View of MT1000A with Installed MU100011A Module

3.2 25 Gbit/s Electrical Interface Design

The electrical interfaces for CFP4, QSFP28, and SFP28 have a transmission speed of 25 Gbit/s for each lane. Figure 3 shows the block diagram of the MU100011A 25 Gbit/s electrical interface circuit. The electrical and mechanical specifications for this interface are both in compliance with the Multi Source Agreement (MSA) and Small Form Factor (SFF) standards, and CEI-28G-VSR of the Optical Internetworking Forum (OIF).

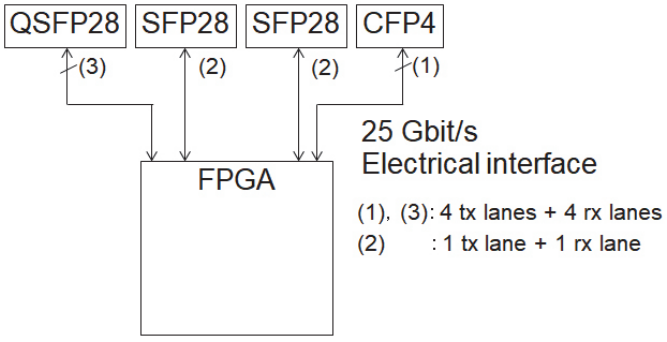


Figure 3 25 Gbit/s Electrical I/F Circuit Block Diagram

3.3 Parts Layout and Thermal Radiation/Air Cooling

Achieving a compact size imposes limits on the internal parts density. A 25-Gbit/s high-speed electrical signal using even high-speed PC board materials suffers degraded waveforms if the pattern wiring has redundant sections, but reducing the parts layout degrees of freedom causes issues with assuring the quality of high-speed electrical signals. To minimize waveform degradation, the PC board was designed taking the following precautions using 3D electromagnetic field analysis tools.

- Use short wiring patterns
- Minimize unnecessary internal layers
- Eliminate unnecessary through holes and through-hole lands

Figure 4 shows the wiring pattern from the FPGA to the CFP4 connector and Figure 5 shows the S-parameter 3D analysis results for the wiring part. An insertion loss of 3 dB max. and a reflection loss of 18 dB min. was obtained at a 13-GHz.

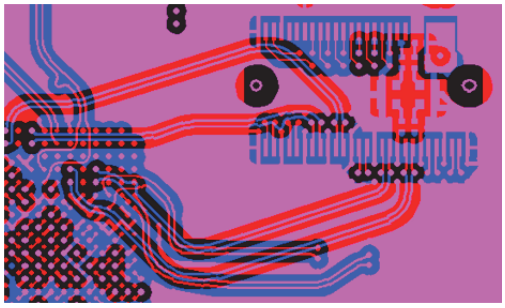


Figure 4 PC Board Wiring Pattern to CFP4 Connector

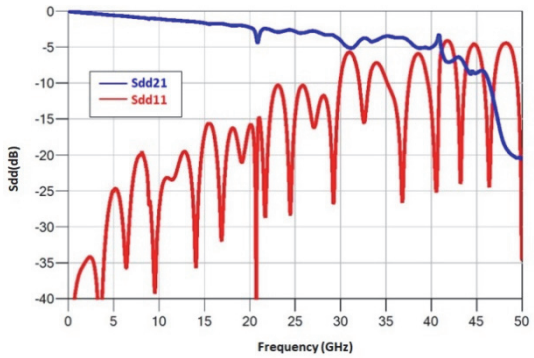


Figure 5 S-Parameter 3D Analysis Results (Differential Signal)

There are thermal and cooling issues with optical modules, such as CFP4 and QSFP28, as well as for FPGAs. To keep the design compact and lightweight we adopted air cooling using large fans and copper sheets based on the following thermal and cooling design concepts.

- Case with airflow baffles
- Small lightweight heatsink for heat dissipation
- Cooling air inlet and outlet locations based on portable design
- Use of small fans pushing large air volumes

Figure 6 shows the thermal simulation model analysis results, indicating that the FPGA and optical module temperatures were held within the specified range even when running the MU100011A at the upper limit of its operating range.

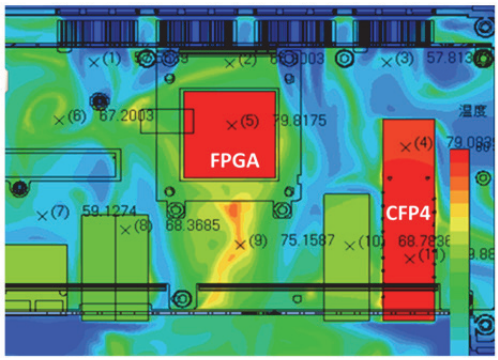


Figure 6 Example of Thermal Simulation Results

4 eCPRI/RoE Measurement Function

4.1 eCPRI/RoE Frame Structure

Figure 7 shows the eCPRI/RoE Frame structure[4), 5)] composed of Ethernet header, eCPRI/RoE header, and payload. The eCPRI/RoE header is itself composed of a common header and individual header. The payload includes IQ (In-phase and Quadrature) data, etc.

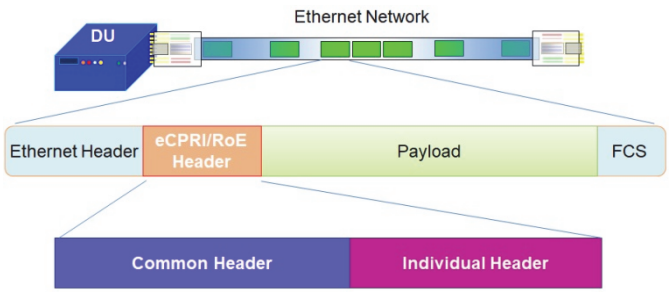


Figure 7 eCPRI/RoE Frame Structure

4.2 eCPRI/RoE Frame Tx

Testing networks and devices supporting eCPRI/RoE requires a measuring instrument that can both generate and test frames. The MT1000A has both of these functions. Using eCPRI, the structure of the individual header is switched based on the Message Type specified at the common header. In contrast, using RoE, the structure of the individual header is switched based on the Sub Type. Table 1 lists the supported Message Type and Table 2 lists the supported Sub Type.

Table 1 List of Message Types

Message Type
IQ Data
Bit Sequence
Real-Time Control Data
Generic Data Transfer
Remote Memory Access
One-way Delay Measurement
Remote Reset
Event Indication

Table 2 List of Sub Types

Sub Type
RoE Control sub type
RoE Structure-agnostic data sub type
RoE Structure-aware CPRI data sub type
RoE Slow C&M CPRI sub type
RoE Native time domain data sub type
RoE Native frequency domain data sub type
RoE Native PARCH data sub type
RoE Control sub type

4.3 Screen Setting

Figure 8 shows the eCPRI setting screens. The common header, individual header and payload settings are dis-

played on separate tabs. The screen on the left side of Figure 8 indicates the selected common header status for selecting the Message Type and Sub Type for the sent frame. The screens on the right side of Figure 8 indicate the selected individual header tab status and the screens are switched automatically for settings corresponding to Message Type. The Pseudo Random Bit Sequence (PRBS) pattern for inserting into the payload is set at the Payload tab.

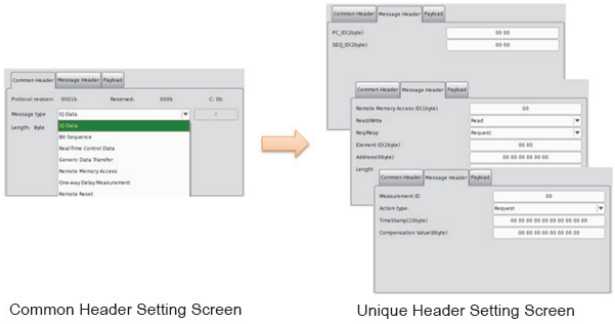


Figure 8 eCPRI Tx Frame Setting Screen

Figure 9 shows the RoE setting screen. Since the RoE standards are now being drawn-up, a frame sending function that can respond flexibly to changes in the standard is required. As a result, the MT1000A has a function for defining any data configuration at any Message Header and Sub Header.

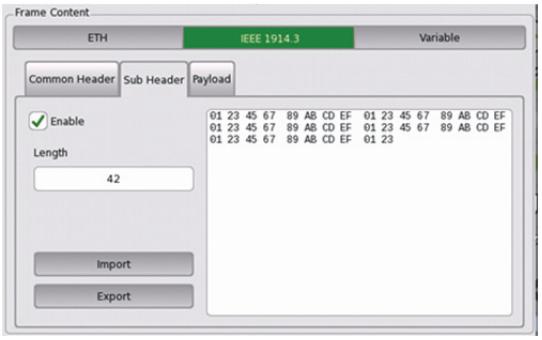


Figure 9 RoE Tx Frame Setting Screen

5 Improving Latency Measurement and Clock Sync Measurement Functions

5.1 Latency Measurement

Mobile 5G networks require an End-to-End latency of 1 ms or less. This requirement includes the wireless network segment and the one-way latency of the wired section must be about 100 µs. Consequently, evaluating these networks necessitates measuring instruments with even higher latency measurement accuracy.

This developed improvement was split into two main items. First, was to improve the latency measurement resolution. In concrete terms, this improved the resolution of the clock data frame for Ethernet measurement from 100 to 5 ns. Second, was to support Far-End measurement at one-way latency measurement. One-way latency measurement requires accurate clock synchronization of two MT1000A units operating as the Tx source and the Rx destination. As shown in Table 3, one-way Near-End measurement using the same cabinet is already supported (Item 3A), but this development strengthens and extends the Near-End function (3B) while also supporting Far-End measurement (3C). The details are explained below.

Table 3 Sync Method for One-Way Latency Measurement and Measurement Target

Sync Method		Measurement Target	MT1000A Support
A	Same cabinet	Near-End	Already supported
B	1PPS-10 MHz	Near-End	Supported by this development
C	GPS	Far-End	Supported by this development

A: One-Way Near-End Latency Measurement with Same Cabinet

Near-End measurement is used when the evaluation target is near the measurement end, such as when evaluating local devices and small-scale networks. At rates of 10GbE or less, the MU100011A can be used by synchronizing two ports. The one-way latency is measured by sending one way from one of the two ports and receiving at the other port. When using the same cabinet, the Tx source and Rx destination have the same time.

B: One-Way Near-End Latency Measurement using 1PPS-10 MHz Sync

Figure 10 shows a one-way latency measurement system using two cabinets. This system is used especially for 25G, 40G, and 100G measurements. The cloud image in the figure indicates the networked Device Under Test (DUT) and the green lines indicate the test packet path; a MU100011A unit is installed in each MT1000A. Additionally, the MT1000A on the left side of the figure also has the MU100090A GPS Disciplined Oscillator installed, from which 10 MHz and 1 pulse per second (PPS) signals are divided and input to each of the two cabinets. When the clock synchronization signal source is set to 1PPS (Ext. 10 MHz Ref.), the clock counter used for measurement is based on the Ext. 10 MHz Ref source and is

reset by 1 PPS signal, synchronizing the clocks in the two cabinets.

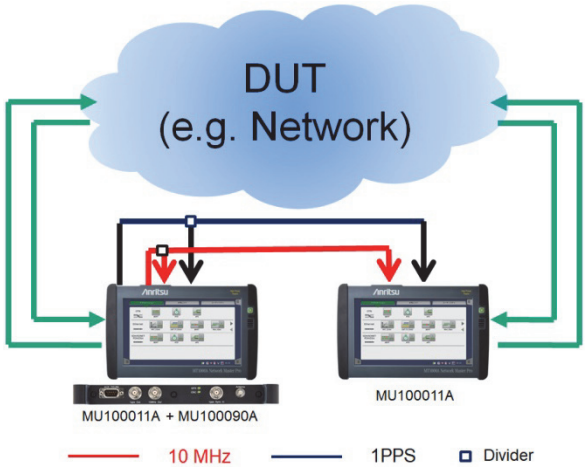


Figure 10 One-Way Latency Measurement System with Two MT1000A Units

C: One-Way Far-End Measurement using GPS Sync

In most real networks, the evaluation target is far from the measurement end and Figure 11 shows the measurement system for this setup in which two MT1000A units each with installed MU100090A are synchronized by the GPS signal. Adding the GPS Ext. 10 MHz Ref selection for the clock sync signal source supports Far-End latency measurement.

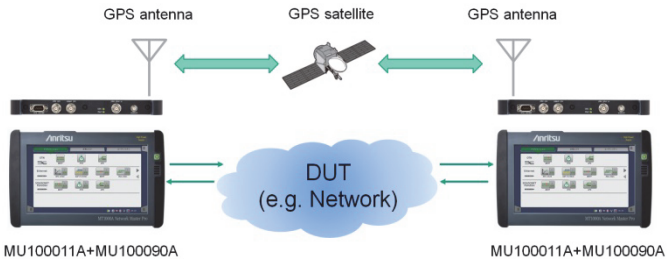


Figure 11 Far-End One-Way Latency Measurement System

5.2 Improving Clock Sync Measurement Function

The MT1000A series has been developed for the Precision Timestamp Protocol (PTP) for clock sync measurement, which has been adopted by LTE-Advanced, particularly TD (Time Division)-LTE[6]. This current development aimed to solve the following issues to meet 5G MFH market requirements.

- Support for PTP measurement at 25GbE
- Improved clock accuracy

Support for 25GbE is achieved using the MU100011A described in Section 3.

Table 4 lists the 5G clock accuracy requirements[7] which are higher the than the prior LTE TDD (Time Division Duplex) requirements.

Table 4 Required Clock Accuracy

Category	Typical Applications	TAE (Typical applications and time alignment error)
A+	MIMO or TX diversity transmissions, at each carrier frequency	65 ns
A	Intra-band contiguous carrier aggregation, with or without MIMO or TX diversity	130 ns
B	Intra-band non-contiguous carrier aggregation, with or without MIMO or TX diversity, and Inter-band carrier aggregation, with or without MIMO or TX diversity	260 ns
C	3GPP LTE TDD	3 µs

Figure 12 shows the measurement flow for the Time transfer Error (Terr) typically used as an index for evaluating time and phase using PTP packets. Terr is calculated as the mean of TE4 which is the Time Error of the PTP uplink Delay_Req packet, and the mean of TE1, which is the Time Error of the PTP downlink Sync packet.

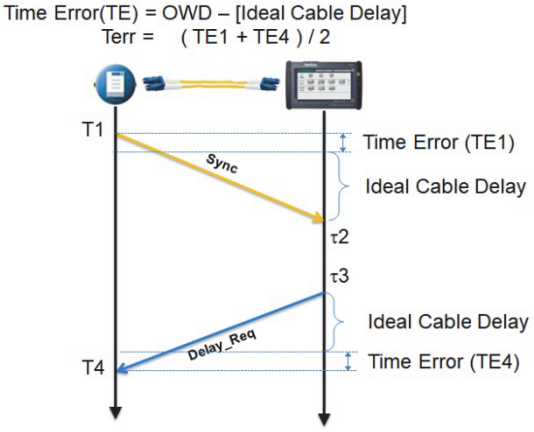


Figure 12 PTP Time Error

To improve the clock accuracy, the MT1000A Rx time τ (Figure 12) measurement method was improved. Figure 13 shows the block diagram before and after the improvement. Before the improvement, the Sync packet Rx time τ1 measured downstream of the buffer suffered from large variation. Implementing the τ1 measurement upstream of the buffer eliminated buffer effects.

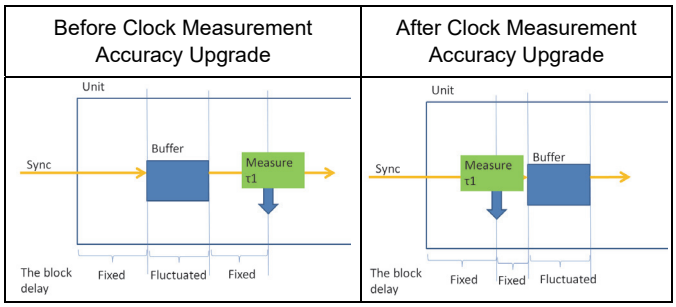
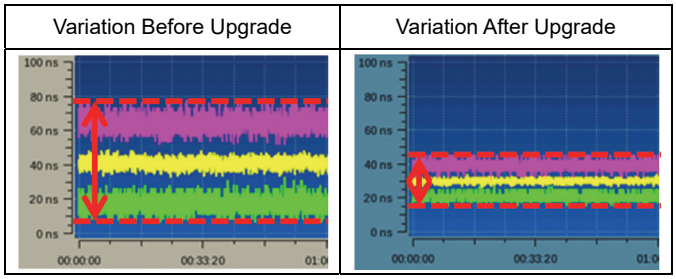


Figure 13 Comparison of Clock Measurement Accuracy Before and After Upgrade

Figure 14 and Table 5 show the upgrade Terr results. Figure 14 compares actual results at 1GbE measured before and after the upgrade using the same PTP Master. The horizontal axis is time (s) and the vertical axis is Terr (ns). The three lines in the graphs are the max. (red), mean (yellow), and min. (green) Terr values over time. Comparing the before and after upgrade results, the difference between the max. and min. values is smaller and the variability is suppressed.



(Red: max; Yellow: mean; Green: min.)

Figure 14 Terr Upgrade Result

Table 5 lists the performance and actual measured results before and after the upgrade. The internal timestamp error performance depends on the accuracy of the 10 MHz and 1 PPS external reference signals. The values in the table are the nominal values for the MU100011A, excluding external reference signal error factors; the results (actual values) are the results in Figure 14. From these results, we can clearly see an improvement of about 41% in the difference between the Terr max. and min. values for the full measurement time, as well as an improvement of about 55% in the difference between the TE1 max. and min. values for the full measurement time.

Table 5 Improved Measurement Accuracy Results

	Before Accuracy Upgrade	After Accuracy Upgrade
Internal Timestamp Error	±100 ns	±35 ns
Result (actual value) Max|Terr|	81 ns	47 ns
Result (actual value) Difference between Terr max. and min. values for full measurement time	68 ns	30 ns
Result (actual value) Difference between TE1 max. and min. values for full measurement time	85 ns	45 ns

6 Conclusion

We developed the compact MU100011A module for the MT1000A to support evaluation of 25 and 100GbE mobile fronthaul and mobile backhaul network segments. We added functions for measuring eCPRI and RoE used by 5G fronthaul and also upgraded the latency and clock sync measurement functions.

With the start of commercial 5G service trials, we hope this new MU100011A will meet future measurement needs and play a key role in improving the quality of 5G network services.

References

1) A.Mikuchi, S.Isobe, H.Takahashi, S.Nagata, “5G Standardization Trends at 3GPP”, NTT DOCOM Technical Journal Vo.19 No.3,pp2-12 (Jan. 2018)
2) 3GPP TS22.261 Version 15.5.0, “Service requirements for next generation new services and markets” (July 2018)
3) The Telecommunication Technology Committee, “A Survey Report on Access Network Issues in Front Hall / Backhaul of Next Generation Mobile Network”, Ver. 1.0 (Mar. 2017) (in Japanease)
4) IEEE1914.3, “IEEE Standard for Radio over Ethernet Encapsulations and Mappings” (Sep. 2018)
5) Common Public Radio Interface, “eCPRI Interface Specification V1.1”
6) Mitsuhiro Usuba, Osamu Sugiyama, Yasuji Ishizuka, Atsushi Furuki: “Development of Network Tester for Precision Synchronous Network Verification”, Anritsu Technical Review No.25 (Sep. 2017)
7) Common Public Radio Interface, “eCPRI Transport Network V1.0”

* Ethernet is a registered trademark of Fuji-Xerox Co., Ltd.

Authors

Tomohiro Ito
Product Development Dept.
Service Infrastructure Solution Division

Atsushi Furuki
Product Development Dept.
Service Infrastructure Solution Division

Hokuto Saeki
Product Development Dept.
Service Infrastructure Solution Division

Akinobu Tsuyuki
Product Development Dept.
Service Infrastructure Solution Division

Publicly available