128G PAM4 BERT Development

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[Summary] Data-center traffic is increasing explosively due to the widespread adoption of cloud computing services. To increase communications speeds between server and network equipment interfaces, the PAM (Pulse Amplitude Modulation) 4 method is replacing the previous NRZ method due to the ability of PAM4 to increase transmission capacity without increasing symbol rates. As a consequence, we developed a PAM4 BERT (Bit Error Rate Tester) to meet the demands of the PAM4 transmission market by supporting PAM4 communications standards at speeds exceeding 100 Gbit/s.

1 Introduction

Due to the recent explosive increase in data traffic at data centers, transmission speeds are being increased for PHY layer devices and modules. As a consequence, standards organizations, such as OIF-CEI (Optical Internetworking Forum Common Electrical Interface) and IEEE802.3, regulating the interfaces between network equipment, are adopting the PAM4 technology to increase transmission capacities beyond the currently used NRZ (Non-Return-to-Zero) method without increasing the symbol rate; these transmissions are being standardized at speeds of 112 Gbit/s (56 Gbaud) by CEI-112G-VSR-PAM4[1)] and 106.25 Gbit/s (53.125 Gbaud) by IEEE802.3bs[2)], etc. In addition, the PCI-Gen6[3)] standard targeted by PCI-SIG for final release in 2021 increasingly requires PAM4 signalling.

A PAM4 signal transmits data using four voltage levels (0, 1, 2, 3) in one time slot. As a result, the data volume per symbol is doubled in comparison to the previous NRZ transmission method using two voltage levels in one time slot. For equal voltage amplitude, the amplitude between each voltage level of the PAM4 signal is one-third that of NRZ signals, demanding high-performance waveform quality at the transmission side and high-sensitivity input performance at the receive side. Moreover, various analysis functions are required to evaluate not only hardware performance but also signal quality.

To meet these needs, we developed the 128G PAM4 BERT (Bit Error Rate Tester) supporting both PAM4 and NRZ signals; it is the first BERT in the industry to achieve error-free measurement of 116-Gbit/s PAM4 signals. The 128G PAM4 BERT is composed of the latest MU196020A PAM4 PPG (hereafter PAM4 PPG: Pulse Pattern Generator) and MU196040B PAM4 ED (hereafter PAM4 ED: Error Detector) measurement modules installed in the MP1900A Signal Quality Analyzer-R series along with the previously released MU181000B 12.5 GHz 4Port Synthesizer (hereafter synthesizer) and the MU181500B Jitter Modulation Source (hereafter Jitter Module) modules, providing an all-in-one test solution.

The PAM4 PPG provides high-quality waveforms with a Signal to Noise and Distortion Ratio (SNDR) standardized by IEEE 802.3cd[4)] of better than 33 dB, as well as an ISI (Inter-Symbol Interference) generation function for DUT (Device Under Test) stress tests in compliance with each standard. Additionally, the PAM4 ED has industry-best high-level sensitivity of better than 50 mV (each Eye height) at 58.2 Gbaud as well as a full range of test functions for error analysis.

This article explains the required points when designing the 128G PAM4 BERT key technologies.

2 PAM4 PPG Outline

2.1 Output Waveform Characteristics

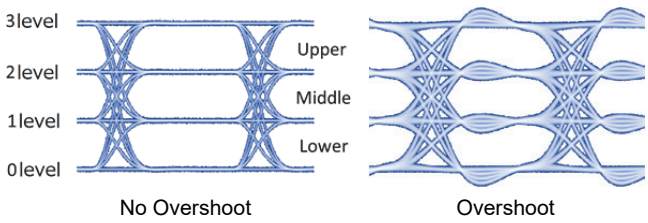


Figure 1 PAM4 Signal Waveform

Figure 1 shows the PAM4 signal waveform. In comparison to NRZ signals, PAM4 signals have faster rise and fall times

as well as low jitter due to the 1/3 lower voltage level for each signal. In addition, the four voltage levels support three Lower, Middle and Upper Eyes. If there is overshoot at level 1 and 2, the Upper and Lower Eye waveforms become closed, but if there is undershoot, the Middle Eye becomes closed, requiring smaller waveform distortion.

To generate high-speed PAM4 signals, we used InP semiconductor technology offering a cutoff frequency of 229 GHz and maximum oscillation frequency of 403 GHz. We developed high-speed ICs operating at up to 128 Gbit/s (64.2 Gbaud) to output PAM4 signals with high-speed rise (Tr) and fall times (Tf), low intrinsic jitter and small waveform distortion. Figure 2 shows a typical PAM4 PPG waveform and Table 1 lists the main performance specifications.

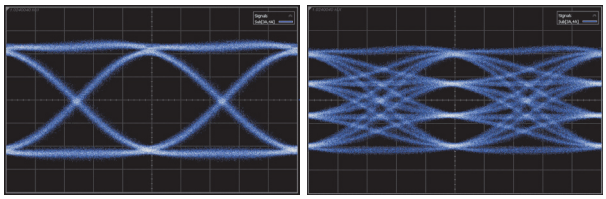


Figure 2 Typical PAM4 PPG Output Waveforms

Table 1 Typical PAM4 PPG Output Waveform Specifications

Items	Specification
Output Amplitude	0.14 to 1.6 Vp-p (differential)
Emphasis	4 Tap, ±20 dB (1 post/2 pre cursor)
Intrinsic Jitter	170 fs (typ. NRZ)
Tr/Tf (20% to 80%)	8.5 ps (typ. NRZ)
SNDR	33 dB (min)
Independently Variable Waveform Eyes	20% to 50%

In addition, since non-linear devices such as EA modulators used in optical transceiver modules can sometimes have distorted balance between the three Eyes of the PAM4 signal output, the levels of the PAM4 signal three Eyes input to the device require flexible adjustment. Consequently, we have incorporated a function for independently changing the Eyes by setting the level for each of the three Eyes as either voltage or ratio. Figure 3 shows a waveform with the Upper Eye set to 50%, Middle Eye set to 30%, and Lower Eye set to 20%.

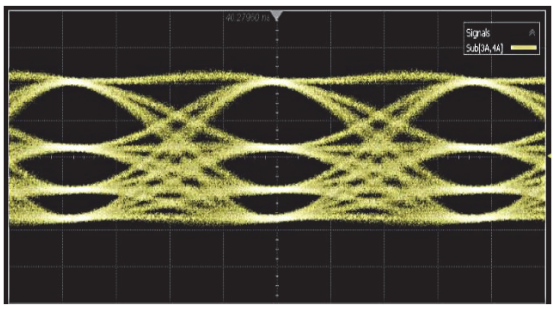


Figure 3 Independently Variable Waveform Eyes

2.2 Built-in 4-Tap Emphasis Function

High-speed data transmission suffers from degraded waveform quality as a result of passage through cables and printed-circuit boards (PC boards). Consequently we have built a 4Tap Emphasis function into the PAM4 PPG to compensate for the Frequency Dependent Loss of transmission lines. This emphasis function is implemented using an FIR (Finite Impulse Response) filter to set the maximum amplitude ±20 dB of other taps relative to the main tap. Figure 4 shows the waveform before and after Emphasis compensation when an FR4 PC board with an 80-mm line is connected to the PAM4 PPG output.

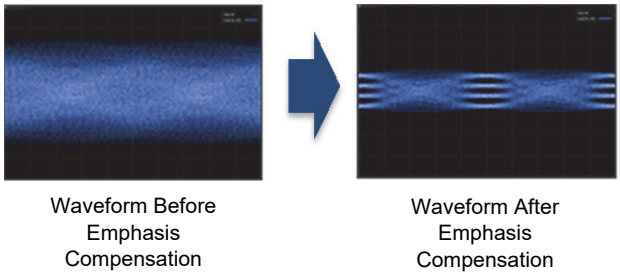


Figure 4 Frequency Dependent Loss Compensated Waveform

2.3 Adjustable ISI Function

The OIF-CEI and IEEE, etc., standards demand generation of a stressed waveform using an ISI board with specific frequency characteristics. As shown in Figure 5, generating a stressed waveform meeting the standard using only an ISI board requires switching attached boards. However as shown in Figure 6, combined use with a PAM4 PPG FIR filter supports stressed waveform generation meeting various standards without switching boards. The FIR emulates the stressed waveform and there are well-known methods for compensating stressed waveforms5); like the Emphasis function, these technologies are implemented using a 4Tap FIR filter.

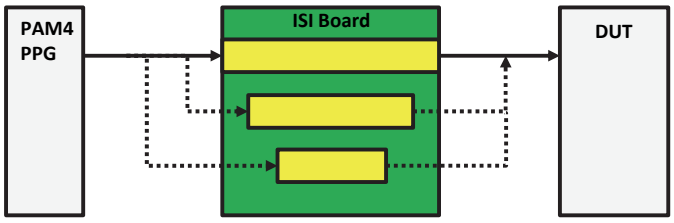


Figure 5 Existing Stress Waveform Generation

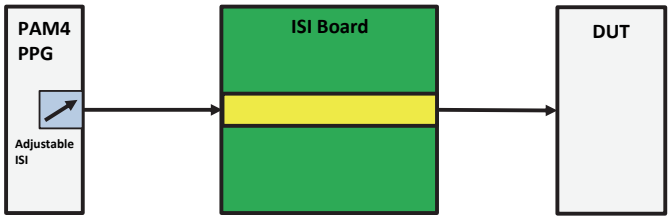


Figure 6 Stress Waveform Generation using PAM4 PPG

One method of emulating frequency characteristics is to perform IFFT (Inverse Fast Fourier Transform) for the required frequency, and this method is included as a method for finding the coefficient for each tap from the impulse response. When there is no limit on the tap coefficient, the frequency characteristics can be fully emulated, but, since in reality there is a limit on the number of taps, the frequency response becomes separated. Consequently, before executing IFFT, compensation is performed so the gain for the Nyquist frequency and half Nyquist frequency are equal to the ideal frequency characteristics. Figure 7 shows the frequency characteristics before and after gain compensation.

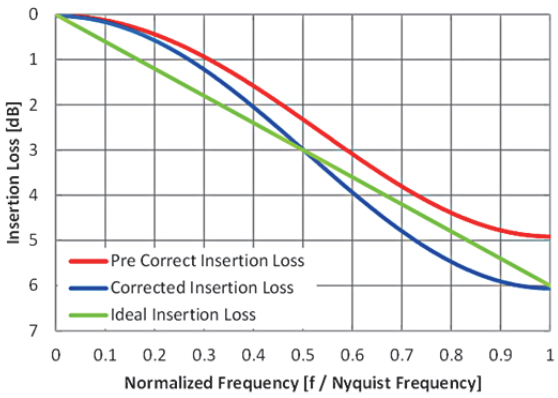


Figure 7 FIR Filter Frequency Gain Compensation

However, since it is sometimes impossible to reproduce the group delay characteristics of the transmission path with only a FIR filter using the Emphasis function, combination with an ISI board can output a waveform broadly matching the ideal frequency and phase characteristics. Figure 8 shows a waveform to which the Adjustable ISI function has been applied.

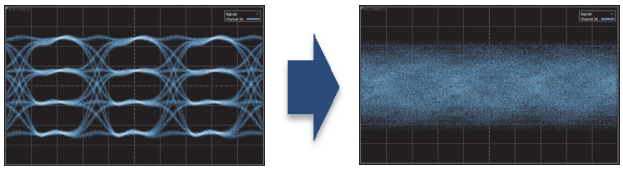


Figure 8 Adjustable ISI Waveform

2.4 PAM4 Pattern Setting

Although the PAM4 PPG can generate patterns defined by the standards, sometimes patterns anticipated by the Rx section of a DUT, such as a SerDes (SERializer/DESerializer), can differ from the standards. Consequently, a function is required for flexibly changing the inverse logic and bit skew between the MSB (Most Significant Bit) and LSB (Least Significant Bit) from the pattern generation methods defined in the standards.

As a result, we visualized a pattern generation method using a GUI meeting the following conditions to facilitate flexible settings.

①Seed pattern data

②Inverse logic setting for both MSB and LSB before and after Gray Coder/Pre Coder stages

③ON/OFF setting for Gray Coder and Pre Coder

④MSB bit skew setting

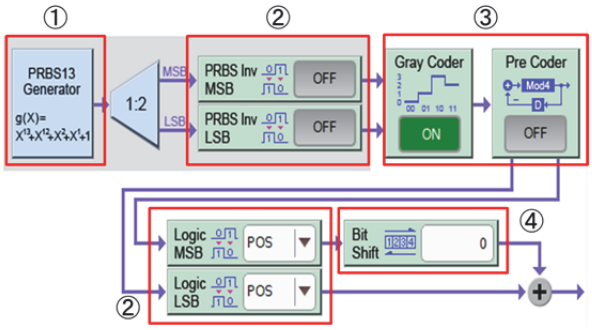


Figure 9 PAM4 Pattern-Setting GUI

2.5 PAM4 Error Addition Function

Testing the PHY layer requires simulated error input to the DUT. There are various types of error simulation, such as adding only MSB or LSB errors to simulate logic errors, and Level-1 transition errors assuming passage through an ISI channel, etc. Since NRZ signals have only two values of 0 and 1, the relevant bit is inverted whichever type of error is added. However, with 4-level PAM4 signals, an arbitrary transitional error cannot be added at simple bit inversion.

Consequently, it is permissible to add an error to either one of the MSB or LSB, or to both the MSB and LSB so that the level transition is one level. Figure 10 shows an example of error addition where the level transition is one level. Errors can be added in this way to cause any symbol transition.

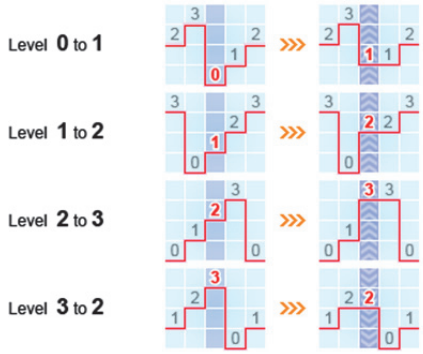


Figure 10 PAM4 Error Addition Image

3 PAM4 ED Outline

3.1 Industry Best High-Level Sensitivity Performance

Since PAM4 signals have a difference between each signal level of 1/3rd that of NRZ signals, a measuring instrument for evaluating signal quality requires high sensitivity input characteristics. Consequently, suppressing harmonic-frequency loss using high-speed InP technology as used in the PAM4 PPG enabled implementation of an error detector (ED) supporting a high baud rate of 64 Gbit/s for NRZ input signals and 116 Gbit/s (58 Gbaud) for PAM4 input signals, enabling world-first error-free measurement of 116-Gbit/s PAM4 signals.

As a consequence, as shown in Figure 8, an input sensitivity of better than 45 mVp-p was achieved with a 64-Gbit/s NRZ signal input, and better than 50 mVp-p with a 58.2-Gbaud PAM4 signal input (height of each of Upper/Middle/Lower Eyes).

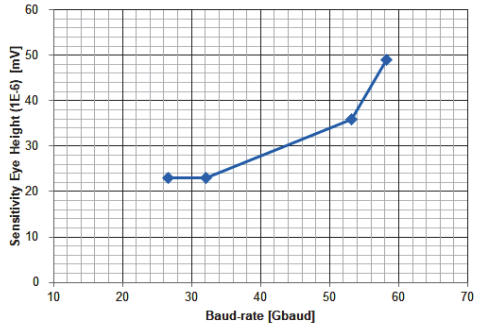
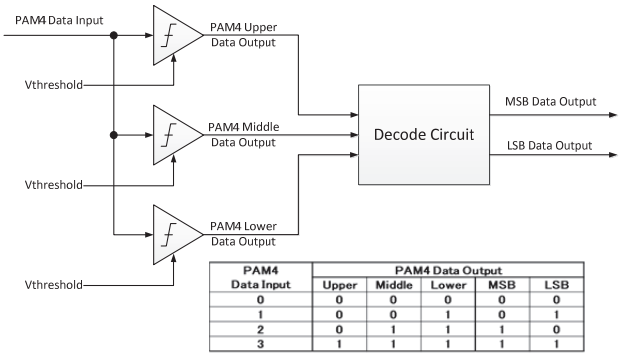


Figure 11 Sensitivity Characteristics at PAM4 Signal Input

3.2 Built-in MMIC for PAM4 Decode Processing

NRZ signals have two values, 0 or 1, so level evaluation uses one threshold. By contrast, PAM4 uses four values (0, 1, 2, and 3), so level evaluation requires three thresholds for the Upper/Middle/Lower Eyes. We developed a PAM4 Decoder MMIC (Monolithic Microwave Integrated Circuit) with three threshold circuits and a built-in logic processing circuit for decode processing of these 2-bit (four values). As shown in the block diagram and truth table for the Decoder MMIC (Figure 12), the MSB is evaluated as the Middle output and the result is output. However, the LSB is evaluated for each of the Upper/Middle/Lower outputs and the result is calculated and output.

Performing error measurement for this Decoder MMIC MSB output supports use of this ED for both NRZ signals and for PAM4.



PAM4 Data Input	PAM4 Data Output				
	Upper	Middle	Lower	MSB	LSB
0	0	0	0	0	0
1	0	0	1	0	1
2	0	1	1	1	0
3	1	1	1	1	1

Figure 12 Decoder MMIC Simple Block Diagram and Truth Table

3.3 Equalizer Function

The PAM4 ED includes two types of equalizer—a Low Frequency Equalizer (LFE), and a Decision Feedback Equalizer (DFE).

By lowering the gain of the low-frequency components, the LFE can effectively compensate for sudden losses up to 1 GHz observed in cables and printed-circuit boards through planned equalization of frequency characteristics. The LFE of the PAM4 ED supports variable gain compensation in the range from 0 to −2.0 dB from low frequencies up to 1 GHz. In addition, the DFE can compensate the signal when an impulse response is observed by feedback of part of those signal components based on the prior 0/1 evaluated data; the loss compensation is effective for harmonic components up to Nyquist frequencies and a variable compensation value can be set.

Analog-type flat frequency characteristics are created

using the LFE while digital-type signal compensation is achieved using the DFE. Compensation using these equalizers is a key function that cannot be omitted for compensating for transmission path Frequency Dependent Loss like the PAM4 PPG Emphasis function. For example, for losses of 4.5 dB at the Nyquist frequency and for 3.0 dB at the half Nyquist frequency, if the 53.125-Gbaud PAM4 SER (Symbol Error Rate) measurement result is about 1E-5, it can be improved to less than 1E-12 at a minimum by setting the optimum LFE and DFE values.

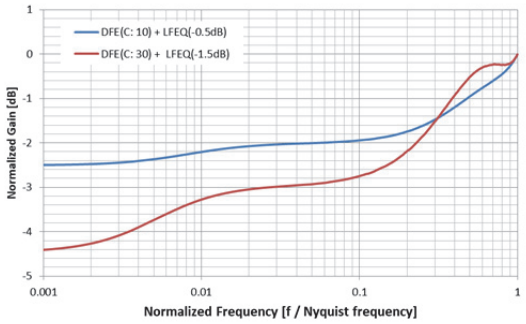


Figure 13 Example of 53.125 Gbaud DFE + LFE Frequency Characteristics

3.4 Clock Recovery Function

Error rate measurement requires a clock synchronized to the data. However since some DUTs, such as SerDes, do not have a synchronous clock, the clock must be extracted from the transmitted data. Consequently, as shown in Figure 14, we developed a clock recovery device for each of the three frequency bands in the PAM4 ED; it supports a wide range of baud rates for each standard specification from 2.4 to 32.1 Gbaud, and from 51.0 to 58.2 Gbaud, and also has low-jitter clock recovery.

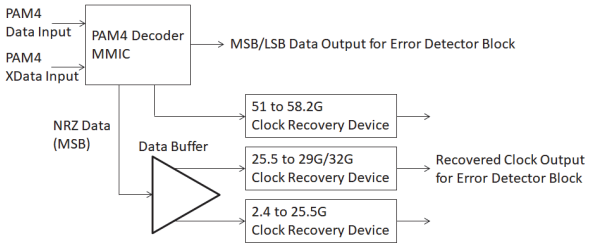


Figure 14 Simplified Clock Recovery Block

3.5 PAM4 SER Measurement Function

The PAM4 ED not only measures the Bit Error Rate (BER) by calculation using the MSB and LSB but also supports PAM SER measurements. As shown in Figure 15, the symbol measurement results are displayed as the Error Count (EC) and Error Rate (ER) for each symbol and bit for at-a-glance confirmation. Moreover, as shown in Figure 16, the detailed results display screen splits the symbols into MSB and LSB to confirm the EC and ER for each. Consequently, the simple transition status for each level can be easily understood by users from this display format, making it easy to grasp error conditions.

Furthermore, we also developed a PAM4 signal Diagnostic Mode for when the PAM4 signal could not be synchronized as PAM4 symbols. Using this function, makes it possible to measure errors for each of the MSB and LSB separately and confirm the MSB and LSB phase shift. Moreover, like the PAM4 PPG, there is a pattern-setting function for setting each of the MSB and LSB logic inversion as well as a Gray Coder and PreCoder On/Off setting for the pre and post Gray Coder/PreCoder stages.

Matching these functions, for DUTs with NRZ signal input and PAM4 signal output functions, such as digital signal processors with built-in optical transceivers, there is also an analysis functions for specifying the cause when pattern inversion or MSB and LSB bit shift occurs.

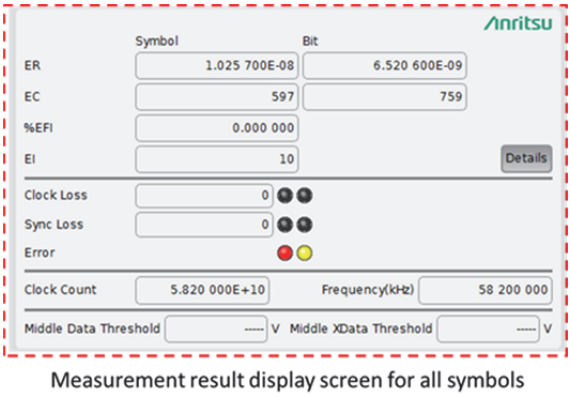


Figure 15 PAM4 SER Measurement Total Results Screen

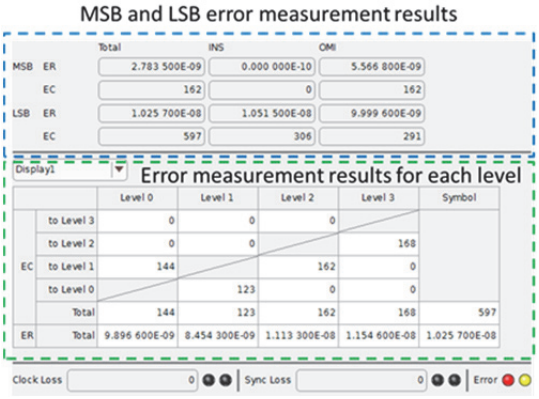


Figure 16 PAM4 SER Measurement Details Results Screen

3.6 PAM4 Symbol Capture Function

The PAM4 ED has a built-in function for loading input test patterns and on-screen display of loaded patterns. Figure 17 shows the capture results display screen.

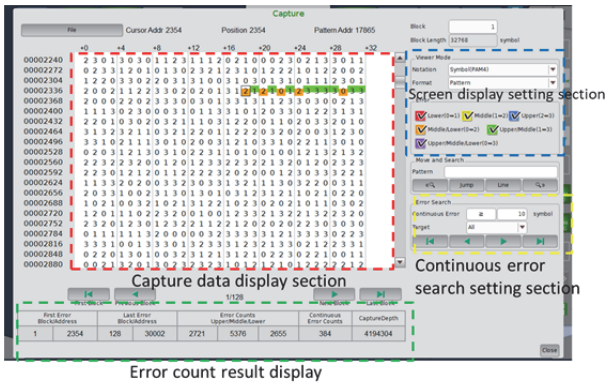


Figure 17 PAM4 Capture Results Display Screen

In the previous method for capturing data, a Sync Mode Capture mode was built into earlier models. In this mode, the input data and known internal reference data patterns are synchronized and errors are evaluated based on the comparison data when the input pattern is loaded. A new Raw Data Capture mode was developed for the PAM4 ED in which the unknown data is loaded in the asynchronous condition and displayed on-screen. Since PAM4 signals are composed of one 2-bit symbol for the MSB and LSB, there are various factors, such as logic inversion, the presence/absence of Graycode and Precode, skew, etc., disturbing establishment of synchronization. By adding the Raw Data Capture mode, the input data are saved as is and the results are displayed on-screen, so users can analyze the data in the asynchronous state.

To improve the usability of the capture data display screen, new error count and consecutive error search functions have been added. Deflections in the DUT error count can be easily understood using the error count function by confirming the numeric value of the error count for each of the four voltage levels. The consecutive error search function can play a role in investigating the causes of burst errors because it is easy to identify consecutive errors exceeding specified bit/symbols. These added functions help improve users' design inspection efficiency.

3.7 Logging Measurement Function

To investigate errors and alarms occurring during long-term measurement, the PAM4 ED supports a Logging function for recording measurement results at specific times.

The Logging function selects data to be recorded, such as ER and EC, and displays results captured in the time specified at the Cycle setting field at the top right of the Logging screen shown in Figure 18 to record chronological changes.

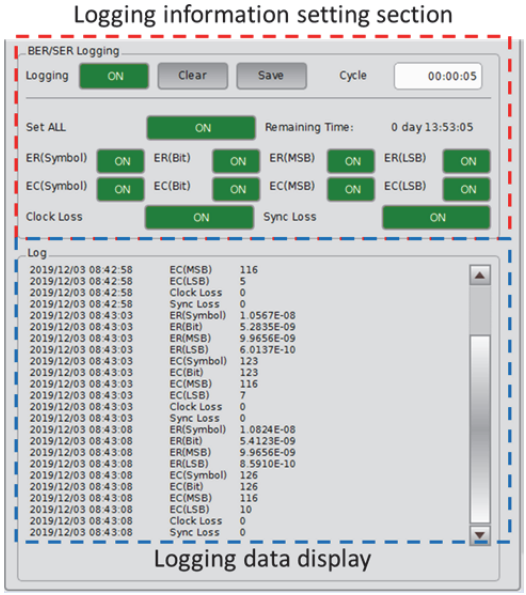


Figure 18 PAM4 ED Logging Results Display Screen

4 Stress Tolerance Measurement using MP1900A

4.1 Measurement Outline

As defined in the CEI-112G-VSR-PAM4 and IEEE802.3bs standards, data signals sent and received between devices and the line card in the communications equipment pass through physical paths such as cable connectors, printed-circuit boards, etc. These physical paths include factors, such as transmission loss, crosstalk from adjacent channels, power-line noise, etc., that degrade signal quality. In particular, high-speed PAM4 signals with small differences between voltage levels suffer major impact from the above-described waveform degradation. Consequently, accurate evaluation of high-speed PAM4 signal transmissions requires generation of stressed signals taking these causes of degraded waveforms into consideration, as well as simulation of the actual transmission environment.

Accordingly, using the 128G PAM4 BERT and generating a high-speed PAM4 stressed signal using ISI and jitter addition offers a receiver test method. Using the features and functions described in section 2, the PAM4 PPG can be used as the stressed signal source required by the standards. Moreover, using the functions and features described in section 3, the PAM4 ED can be used as a reference receiver

for receiving stressed signals required by the standards.

Further, using the synthesizer as the clock source, sinusoidal jitter, random jitter, etc., can be impressed by the Jitter Module for the Jitter Tolerance test for each standard. As a consequence, the all-in-one MP1900A is the ideal test solution for measurements supporting each standard.

4.2 CEI Standard PAM4 Stress Test

The CEI-56G/112G-VSR-PAM4 standard defines the specifications for stressed signals input to modules at each test point for tests between modules. Using the PAM4 PPG as the host and user's DUT as the module, it is important to input the stressed signal to the DUT in accordance with the specifications. As a result, the stressed signal is generated using the measurement system shown in Figure 19, and the DUT Jitter Tolerance test is performed using this stressed signal.

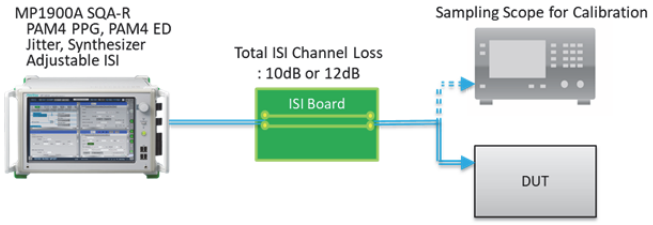


Figure 19 Stress Signal Generation/Jitter Tolerance Measurement System

First, the specification target values are determined as shown in Tables 2 and 3 based on the specifications to generate a stressed signal satisfying these requirements.

Table 2 56G-VSR-PAM4 Typical Target Values

Parameter	Target	Units
End-to-end ISI channel loss (SDD21)	10	dB
Eye Height at 1E-6 probability (EH6)	32	mV
Eye Width at 1E-6 probability (EW6)	7.53	ps
Eye Linearity	0.85	—

Table 3 112G-VSR-PAM4 Typical Target Values

Parameter	Target	Units
End-to-end ISI channel loss (SDD21)	12	dB
Eye Height at 1E-6 probability (EH6)	37	mV
Eye Width at 1E-6 probability (EW6)	3.76	ps
Eye Linearity	0.85	—

The stressed waveform can be generated using the PAM4 PPG Amplitude Setting function, Independently Variable Eye function, Adjustable ISI function, and Emphasis function to achieve a PAM4 stressed waveform with balanced openings for each of the Upper/Middle/Lower Eyes as shown in Figure 20 and Figure 21 satisfying the target values for each baud rate.

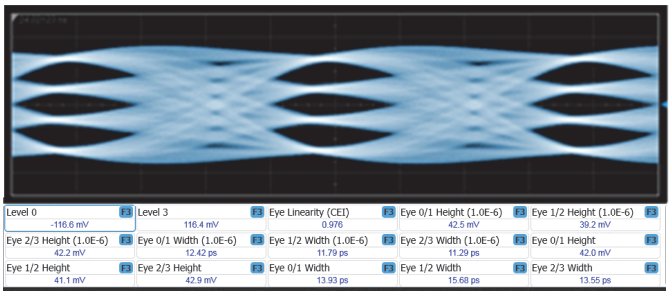


Figure 20 CEI-56G-VSR-PAM4 Stressed Waveform

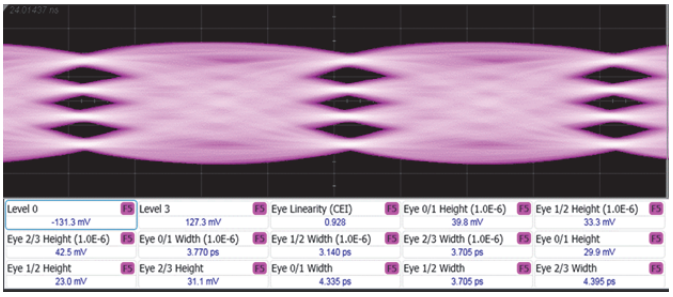


Figure 21 CEI-112G-VSR-PAM4 Stressed Waveform

Next, the stressed waveform is input to the DUT to measure the Jitter Tolerance. Figures 22 and 23 show the results with added sinusoidal jitter while changing the modulation frequency and amount; the DUT satisfies the CEI-defined Jitter Tolerance, confirming use of the MP1900A for receiver tests.

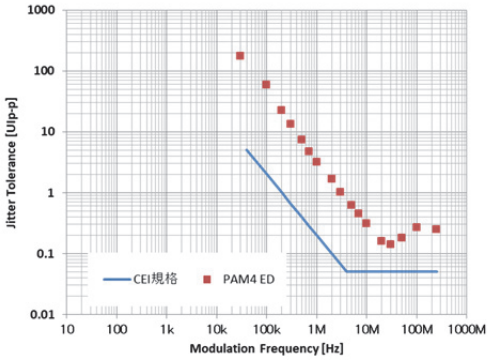


Figure 22 CEI-56G-VSR-PAM4 Jitter Tolerance Test Results

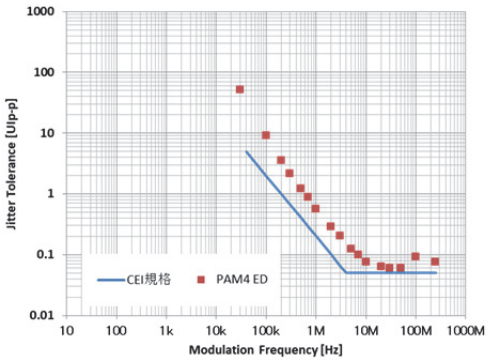


Figure 23 CEI-112G-VSR-PAM4 Jitter Tolerance Test Results

5 Conclusions

We developed the 128G PAM BERT to measure PAM4 signals now becoming the mainstream modulation method for future network interfaces to cope with the explosive growth of data-center traffic. With both high waveform quality and high input sensitivity, the 128G PAM4 BERT has measurement functions supporting standards such as OIF-CEI.

By developing an instrument supporting various future communications standards, we hope to improve both measurement efficiency and evaluation quality as required by PHY layer devices and modules.

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