# 400GbE Multichannel High-Accuracy TDECQ Measurement

Yuki Yokoyama, Takashi Murakami, Keisuke Kishida, Hajime Yoshino

[Summary] Demand for 400GbE optical transceivers is growing rapidly due to the need for high-speed, largecapacity communications re-sulting from the spread of cloud computing services. With the adoption of 4 Pulse Amplitude Modulation (PAM4) for 400GbE, the communications quality of these optical transceivers is evaluated using the Transmitter Dispersion and Eye Closure Quaternary (TDECQ) index. IEEE 802.3bs specifies use of a Clock Recovery Unit (CRU) to measure TDECQ, resulting in development of this CRU to meet the required performance. The evaluation results show that the developed CRU has no dependency on input power and also suppresses the impact on the TDECQ value to ≤0.08 dB relative to measurement without a CRU.

# 1 Introduction

With the explosive increase in data traffic due to the spread of cloud computing services, servers and network equipment in data centers urgently need to increase transmission capacity.<sup>1) to 3)</sup> Consequently, demand for optical transceivers is increasing rapidly as data centers switch to optical interfaces for servers and network equipment. Demand for Quad Small Form-Factor Pluggable Double Density (QSFP-DD) optical transceivers for 400GbE (53.125 Gbaud × 4 lanes) is expected to grow rapidly from 2020. On the other hand, operators are always looking to cut costs when configuring high-speed, large-capacity networks. Development and manufacturing of 400GbE optical transceivers requires evaluation of waveform quality using a sampling oscilloscope. In 2017, Anritsu developed its MP2110A BERTWave<sup>™</sup> as a 25 Gbit/s 4ch Bit Error Rate Tester (BERT) and sampling oscilloscope in one instrument for developing and manufacturing optical transceivers.<sup>4)</sup> It subsequently commercialized built-in options for analysis of 4 Pulse Amplitude Modulation (PAM4) signals in 2018 and a 4ch sampling oscilloscope in 2019, supporting manufacturing demand for a solution offering multiple modules and multichannel simultaneous measurement. However, with a maximum measurable baud rate of 28.2 Gbaud, the Clock Recovery Unit (CRU) in the MP2110A cannot support the 53.125-Gbaud (abbreviated to 53 Gbaud hereafter) signal output for 400GbE optical transceivers. The CRU functions to recover the synchronization clock from the data signal and is indispensable for measuring 400GbE optical transceivers. Consequently, we developed a built-in CRU option for the MP2110A supporting 53 Gbaud. The conventional configuration requires two instruments using a sampling oscilloscope and CRU, but only one instrument is required to measure the Transmitter Dispersion and Eye Closure Quaternary (TDECQ) of a 400GbE optical transceiver using this developed CRU.

This article explains the evaluation method and procedure for 400GbE optical transceivers and demonstrates the required CRU performance. It also presents evaluation results for the newly developed CRU.

# 2 400GbE Optical Transceiver Measurement2.1 Measurement Method

Measurement of 400GbE optical transceivers using a CRU is explained in IEEE 802.3bs.<sup>5)</sup> Consequently, a CRU must measure in accordance with the standard. Conventionally, many manufacturing applications use systems without a CRU by supplying a clock from a Tx source. Figure 1 shows a measurement system for optical transceivers using this conventional method. An 8-lane 26.5625-Gbaud PAM4 signal output from a PAM4 Pulse Pattern Generator (PPG) is input to the optical transceiver where it is multiplexed by a multiplexer (MUX) into a 4-lane 53-Gbaud optical signal for output, which is measured by inputting the optical signal to the sampling oscilloscope that captures the synchronization signal from the PAM4 PPG.



Figure 1 Conventional 400GbE Optical Transceiver Measurement System

However, the 400GbE optical transceiver cannot synchronize the phase of the Tx and Rx sides. As a result, a sampling oscilloscope cannot use the synchronization clock from the Tx-side PAM4 PPG as a trigger signal. Since there is no available trigger signal output and the optical transceiver also cannot output a synchronization clock, the waveform pattern cannot be observed. As a result, manufacturing of 400GbE optical transceivers requires measurement using a CRU out of necessity. In comparison to the previously described measurement system not using a CRU, measurement of 400GbE optical transceivers incurs extra costs for the CRU. Measurement methods using the CRU either have one CRU for each lane or measure by switching between lanes using an optical switch. Ideally, it is best to measure the recovered clock from each lane but four lanes requires provision of four CRUs, which greatly increases the capital investment cost. Although these costs can be reduced by adding only an optical switch, the measurement time becomes longer since only one lane can be measured at a time which greatly increases mass-production manufacturing costs due to the longer tact time for each module. As shown in Figure 2, measuring all lanes simultaneously is an ideal way to cut measurement time.



Figure 2 Comparison of Measurement Time for Single Lane Sequentially and All Lanes Simultaneously

The ideal system in Figure 2 can be achieved if other lanes can be measured using the clock recovered from just one CRU. The phase difference between lanes using a clock recovered from a different lane is extremely small and it becomes less than 0.05 dB for a waveform of about the TDECQ 2.5 dB. The effect on manufacturing yield is small because the value is masked by the measurement reproducibility. As a consequence, we believe using one CRU with a 4ch sampling oscilloscope is the optimum combination for manufacturing 400GbE optical transceivers. Figure 3 shows the ideal system for manufacturing applications; it can be configured as an all-in-one solution that eliminates the need to control multiple instruments and supports high-accuracy TDECQ measurement at low cost. Combination with an optical switch facilitates rigorous measurement of each lane using one CRU.



Figure 3 Ideal System for Manufacturing Application

## 2.2 Evaluation Index



Figure 4 PAM4 Waveform and TDECQ

Figure 4 shows a PAM4 waveform and a TDECQ measurement schematic. 400GbE optical transceivers can PAM4 methods instead of conventional Non Return to Zero (NRZ) methods. PAM increases the transmission capacity using amplitude modulation; PAM4 transmits signals at four voltage levels (0, 1, 2, 3) in contrast to NRZ using two voltage levels (0, 1), so PAM4 has the advantage of sending twice as much data at the same rate as NRZ. Since PAM4 has been formally adopted for 400GbE, the valuation index is also changing. The evaluation index for NRZ is mainly the eye mask margin, whereas PAM4 uses the TDECQ value. The 400GbE optical transceiver performance evaluation is also the same. TDECQ is a measurement of the PAM4 signal Eye opening and is calculated using the following formula (Eq. 1).

$$TDECQ(dB) = 10log_{10} \left( \frac{Outer \ OMA}{6} \times \frac{1}{Q_t R} \right) \cdots (1)$$

where, Qt is the symbol error rate (SER) specified in

IEEE802.3cd<sup>6)</sup> (Qt = 3.414 at  $4.8 \times 10^{-4}$ ), and *R* is the added noise required for SER =  $4.8 \times 10^{-4}$ .

Based on this formula, TDECQ is a measure of the noise and an index expressing how much noise can be added before reaching the SER.

TDECQ measurement requires waveform signal processing using an equalizer. Since a specific position in the pattern must be detected, the oscilloscope must sample consecutively to obtain a complete pattern for one period. Consequently, this is difficult using long-period patterns, such as the conventional PRBS31 (Pseudo Random Binary Sequence) pattern. So TDECQ measurement uses a Short Stress Pattern Random Quaternary (SSPRQ) pattern simulating a high load with the same voltage level continuously for as short a period as necessary. The SSPRQ voltage level distribution is the same as the PRBS31 pattern by cutting the latter pattern, and use of the SSPRQ pattern for TDECQ measurement is specified in IEEE 802.3bs.

The TDECQ measurement result varies greatly depending on the jitter, noise, and waveform. Out of these factors, noise does not affect TDECQ in theory because it is cancelled at calculation of R in Eq. 1. Accordingly, jitter and waveform are the main factors causing errors at TDECQ measurement. Accurate TDECQ measurement requires understanding these elements.

### 3 Required CRU Performance

Accurate measurement of TDECQ is impacted greatly by the performance of the CRU, which requires a recovery clock with small Additive Jitter as well as low dependency on input power. Each of these performance requirements is explained below.

## 3.1 Recovery Clock Additive Jitter

Figure 5 shows the relationship between the Additive Jitter of the recovery clock and TDECQ for the first-developed CRU for a 53-Gbaud SSPRQ waveform. The y-axis is the TDECQ degrade value (dB) relative to the condition with no Additive Jitter. When the Additive Jitter is  $\leq 0.2$  ps rms, there is almost no deterioration in the TDECQ degrade value at  $\leq 0.1$  dB. However, as the Additive Jitter gradually approaches 0.3 ps rms, the TDECQ degrade value starts increasing and becomes 0.5 dB when the Additive Jitter exceeds 0.5 ps rms. This is probably due to the small margin in the phase direction of the 53-Gbaud SSPRQ waveform and because jitter closes the Eye opening. Consequently, for highbaud-rate waveforms, even a small increase in Additive Jitter has an impact on TDECQ. Based on this result, holding the TDECQ degrade value to  $\leq 0.1$  dB requires a CRU recovery clock with a maximum Additive Jitter of 0.2 ps rms.



Figure 5 Relationship between CRU Recovery Clock Additive Jitter and TDECQ

## 3.2 Input Power Dependency

Input power dependency of the CRU is an important factor in determining CRU performance. Optical transceivers can output powerful signals exceeding +1 dBm. Additionally, when measuring TDECQ, the input power to the CRU can be greatly reduced by fiber losses over long-distance transmission. Even using an optical transceiver with an output power of about +1 dBm, the signal loss after transmission through 20 km of fiber is about -8 dB, so the actual power of the input signal to the CRU is about -7 dBm. Based on this, accurate measurement of TDECQ requires stable CRU performance at both large and small input powers. Figure 6 shows an actual measurement example of TDECQ versus input power for the CRU developed first. It is clear that the TDECQ value becomes worse as the input power to the CRU drops. The cause of the degraded value is the decreasing accuracy of the CRU recovery clock with falling power and the increasing Additive Jitter. Figure 7 shows the recovered clock jitter for the first-developed CRU for a 53-Gbaud SSPRQ waveform. There is a clear increase in jitter as the input power falls.



Figure 6 Relationship between CRU Input Power and TDECQ



Figure 7 Relationship between CRU Input Power and Recovery Clock Jitter

### 4 Development of High-Accuracy CRU

We developed a new CRU to solve the problems of recovery clock Additive Jitter and input power dependence outlined in section 3. Figure 8 shows the overall block diagram of the developed CRU block. The optical signal input to the CRU is divided by a first-stage Coupler and the divided optical signal is converted to an electrical signal by the next O/E stage. Subsequently, the signal that has been amplified by the Limiting Amp is input to the CRU unit for clock recovery.



Figure 8 Block Diagram of CRU Block

Figure 9 shows the configuration of the PLL circuit in the detailed block diagram of only the CRU unit. The next sections describe issues and solutions at this CRU development.



Figure 9 Block Diagram of CRU Only

#### 4.1 SSPRQ Measures using DC Coupling

The SSPRQ pattern has low-frequency components due to its unique pattern. For a 53-Gbaud signal, these components are 53.125 Gbaud/65535  $\Rightarrow$  810 kHz. In Figure 8, since the Limiting Amp shown has a negative power supply and the CRU has a positive power supply, they ware designed to be AC-coupled. As a result, the waveform low-frequency components are filtered using a condenser to cut AC-coupled DC components. Consequently, the amplitude offset of the waveform after passage via the condenser changes; at phase detection by the Phase Detector the recovered phase suffers drift from the original timing, causing problems with worse Additive Jitter. As a countermeasure, the CRU was redesigned with a negative power supply, changing to a DC-coupled connection between the Limiting Amp and CRU. When the signal including SSPRQ low-frequency components is input to the Phase Detector, the phase adjustment is optimized to improve the CRU Additive Jitter for the SSPRQ pattern.

# 4.2 Improving Limiting Amp Performance

As described in section 3, we observed a phenomenon for the SSPRQ pattern whereby Additive Jitter increased when the input power to the CRU decreased. The SSPRQ pattern includes components with small amplitude variations, such as the transitions from level 0 to 1, and level 1 to 0. When the input power to the CRU drops, due to the effect of these components, there appears to be a problem with evaluating the level-0 and level-1 values due to intermediate-level voltages because of Limiting Amp limiting restrictions. The Limiting Amp is configured with a differential amplifier circuit but the input offset requires adjustment to operate normally when the input amplitude is very small. Figure 10 shows the impact on the waveform of different limiting. The waveform on the left is with normal limiting and each voltage level can be clearly seen; the waveform on the right has parts that appear to be level 1 but should be level 0 due to the impact of intermediate voltage levels caused by limiting issues. When these types of components remain in the signal, at phase detection by the Phase Detector, the difference at comparison with the reference clock prevents optimum phase detection and worsens the Additive Jitter.



(a) Normal Waveform

(b) Limiting-Problem Waveform

Figure 10 Effect of Limiting Differences on Waveform

As a countermeasure, we used a design applying external voltage to the Limiting Amp to adjust the input offset voltage and improve the limiting performance at low input powers. Figure 11 shows the CRU input power dependency evaluation results before and after the Limiting Amp improvements. The plot before the improvement shows the increased jitter as input power drops, but the plot after improvement shows flat characteristics from -2 to -10 dBm.



Figure 11 Improvement in CRU Input Power Dependency using Improved Limiting Amp Performance

# 5 Performance Verification with High-Accuracy CRU5.1 Impact on TDECQ from using CRU

We tested whether or not the newly developed CRU can suppress degradation of TDECQ by comparison with not using the CRU. The TDECQ without using the CRU is the target value indicating the target without deterioration. Figure 12 shows the measurement setup. The pattern is SSPRQ at 53.125 Gbaud with an input power to the oscilloscope of -2dBm. Since there is no clock without the CRU, as-is measurement is not possible and, consequently, a clock was output from the lane to be non-measured and used as the clock after conversion to an electrical signal at the O/E.



Figure 12 Impact of Evaluation With and Without CRU (Top: w/o CRU; Bottom: w/ CRU)

Figure 13 shows the evaluation results for the impact of using the CRU. It is hard to see any clear difference by eye between the waveforms with and without the CRU. The TDECQ without the CRU is 2.03 dB and is 2.11 with the CRU, indicating a slight impact of using the CRU on the TDECQ.



Figure 13 Waveform With and Without CRU (Top: w/o CRU TDECQ = 2.03 dB; Bottom: w/ CRU TDECQ = 2.11 dB)

# 5.2 Input Power Dependency

Figure 14 shows the measurement set-up for evaluating the CRU sensitivity performance. Measurement was performed using a 53.125-Gbaud signal with SSPRQ pattern and inputting lane 0 to the CRU and measuring the lane-2 signal with the MP2110A. The input power of the lane-2 signal at this time was fixed at -2 dBm, and the input to the CRU was gradually reduced using an optical attenuator to evaluate the change in the TDECQ.



Figure 14 CRU Sensitivity Performance Measurement System

Figure 15 shows the CRU sensitivity performance evaluation results. The TDECQ value ranged from 2.3 to 2.4 dB over an input power range to the CRU of 0 to -11 dBm. Based on this result, it is clear that a drop in input power has no resultant impact on TDECQ.



Figure 15 CRU Sensitivity Performance Measurement Result

## 6 Conclusions

Demand for 400GbE optical transceivers is increasing rapidly as traffic volumes at data centers expand. To support these test requirements, we have developed a CRU for installation in the MP2110A along with the sampling oscilloscope. This developed CRU suppresses any impact on TDECQ when input power drops, achieving flat performance with little input power dependency over a range from 0 to -11 dBm. Additionally, the increase in TDECQ value was held to less than 0.08 dB in comparison to use without the CRU. As a consequence, this new CRU supports high-accuracy TDECQ measurement. Combining this CRU with a 4ch oscilloscope in one instrument supports both 4-lane and 1lane measurements using one CRU.

With this new solution optimized for evaluating future Eye patterns, we hope to increase the development and massproduction efficiency as well as the quality of various optical transceivers supporting high-speed, large-capacity communications infrastructure.

## References

- 1) Ethernet Alliance EthernetRoadmap-2020-Side1-FINAL
- 2) Ethernet Alliance EthernetRoadmap-2020-Side2-FINAL
- 3) Cisco Annual Internet Report (2018–2023)
- Takashi Murakami, Yuki Yokoyama, Takashi Kamizono, Fumihito Hirabayashi: "Development of Sampling Oscilloscope MP2110A", Anritsu Technical Review No.26 (Sep. 2018)
- 5) IEEE Std 802.3bs<sup>TM</sup>/-2017
- 6) IEEE Std 802.3cd<sup>™</sup>-2018

#### Authors



Yuki Yokoyama Product Development Dept. Service Infrastructure Solutions Division Test & Measurement Company



Takashi Murakami Product Development Dept. Service Infrastructure Solutions Division Test & Measurement Company



Keisuke Kishida Product Development Dept. Service Infrastructure Solutions Division Test & Measurement Company



Hajime Yoshino Product Development Dept. Service Infrastructure Solutions Division Test & Measurement Company