

Development of Wideband Linear Amp with New InP HBT

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[Summary]

Faster data transmission requires higher performance devices. Until now, Anritsu has used $f_T/f_{\max}=220/350$ GHz Indium Phosphide (InP) Heterojunction Bipolar Transistor (HBT) designs in its test instruments. This article reports the development of a new high-performance ($f_T/f_{\max}=323/510$ GHz) HBT by optimizing the structure of the IC layers and processing technology. This newly fabricated HBT was used in a high-output, high-speed wideband linear amp with good 120 Gbaud pulse response characteristics. It was possible to amplify input signal of 0.3 V_{pp} up to 2.0 V_{pp}. Future work will focus on designing even faster ICs using the developed HBT.

1 Introduction

Required network transmission capacity is increasing rapidly due to the advancements of the information society as represented by the growth of cloud computing. Device technologies to achieve high transmission speeds exceeding 100 Gbps both between and within data centers are becoming common, and standardization discussions are shifting from 400 to 800 Gbps. Research and development is advancing into implementing high-speed communications exceeding 100 Gbps even in the 6G wireless communications world, and there is also a strong demand for technologies supporting increased data speeds, such as Peripheral Component Interconnect Express (PCIe). Innovative applications, such as Artificial Intelligence (AI) and Machine Learning (ML), are becoming commonplace, increasing the demand for faster transmissions. As a result, test equipment must also support more standards. In particular, devices used in test equipment must meet the latest high-speed transmission communication standards, and always exposed to global competitive environment.

Anritsu Devices has Monolithic Microwave Integrated Circuit (MMIC) technology that uses in-house InP based heterojunction bipolar transistors (HBT) and has been working hard to improve device technologies with the aim of creating a 58 Gbaud Pulse Amplitude Modulation (PAM4) solution and develop measurement instrument supporting the latest PCIe standards.

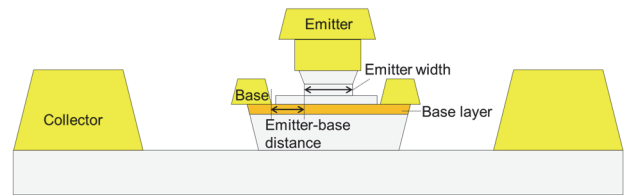
This article explains both the layer structure of transistors forming the heart of the improved performance of second generation (Gen2) InP HBT and the fabrication process technology. In addition, it also explains the MMIC design and

packaging technologies for the implementing bandwidth exceeding 100 GHz in our 120 Gbaud (equivalent to 240 Gbps PAM4) AH15190A Linear Amplifier using Gen2 HBT.

2 High-Performance InP HBT and MMIC

(1) Structure and Performance of High-Speed HBT

(a)



(b)

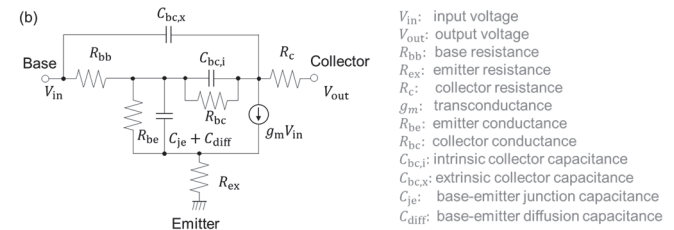


Figure 1 (a) HBT Cross Section (b) HBT Equivalent Circuit

The typical indices of HBT high-frequency performance are the cutoff frequency f_T , and the maximum oscillation frequency $f_{\max}$. In high-frequency amplifier ICs, it is said that assuring amplification performance requires an $f_{\max}$ of two or three times the IC modulation frequency and is a key index for increased speed. Figure 1 (a) and (b) show the HBT structure and equivalent circuit, respectively. The values of f_T and $f_{\max}$ are defined¹⁾ by the following equations (1) and (2), respectively.

$$f_T = \frac{1}{2\pi} \left(\tau_B + \tau_C + \frac{n_c k T}{q I_C} (C_{je} + C_{bc}) + (R_{ex} + R_c) C_{bc} \right)^{-1} \quad (1)$$

$$f_{\max} = \sqrt{\frac{f_T}{8\pi R_{bb} C_{bc,i}}} \quad (2)$$

where, τ_B is the base transit time, τ_C is the collector transit time, C_{je} is the base emitter joint capacitance, n_c is the ideal collector current coefficient, k is the Boltzmann constant, T is temperature, q is the elementary charge, I_C is the collector current, C_{bc} is the base collector capacitance, R_{ex} is the external emitter resistance, R_c is the collector resistance, R_{bb} is the base resistance, and $C_{bc,i}$ is the base collector internal capacitance contributing to $f_{\max}$. In addition, $C_{bc,x}$ (Figure 1 (b)) is the base collector external capacitance not contributing to $f_{\max}$.

Thinning the base and collector layers to shorten the electron transit times τ_B and τ_C is an effective method for increasing f_T . On the other hand, $f_{\max}$ is decreased because thinning the base layer increases the base resistance. The base resistance is expressed as Eq. (3) as the sum of the contact resistance between the metal base and semiconductor, the semiconductor resistance between the base and emitter, and the diffusion resistance immediately under the emitter layer.

$$R_{bb} \cong \frac{\rho_{Bs}}{2 L_E} \left(L_t + W_{Bg} + \frac{W_E}{6} \right) \quad (3)$$

where, ρ_{Bs} is the base sheet resistance, L_E is the emitter length, L_t is the transfer length, W_{Bg} is the distance between the emitter and base, and W_E is the emitter width. Effective methods for reducing the base resistance are increasing the doping density of the base layer to lower the base sheet resistance (ρ_{Bs}) and shortening the distance between the base and emitter (W_{Bg}).

Since the emitter current time (item 3 in Eq. (1)) becomes smaller as the collector current increases, f_T increases. However, when many electrons are injected, the potential gradient felt by the electrons traveling through the collector layer decreases due to the Kirk effect, which makes it difficult for the current to flow, causing f_T to decrease. Therefore, f_T has a peak at a certain collector current.

Since reducing the emitter thickness reduces the internal capacitance of the base collector as well as the contact capacitance with the base emitter, it is effective in increasing f_T . However, only reducing the emitter thickness lengthens the distance between the emitter and base, which increases the base resistance. As shown in Eq. (2), increasing the base resistance reduces $f_{\max}$. Increasing $f_{\max}$ not only requires

increasing f_T but also requires decreasing the base resistance and the base collector internal capacitance.

(2) MMIC Technology and Development Aims

Since 2003, Anritsu has developed MMIC gallium arsenide (GaAs) and InP HBT to use in its test equipment^{2), 3)}. The three-layer wiring process enables high integration. Additionally, ground (GND) is strengthened, and high-frequency IC operation is stabilized by forming via through holes. So far, we have been making prototypes of DA converters using first generation (Gen1) InP HBT devices, but limitations in the operating speed have become apparent with just making integration higher. Improvement in transistor performance is becoming essential not only in digital circuits but also in analog circuits such as linear amplifiers. For this reason, we started developing high-performance HBT elements that would be useful for both digital and analog applications. IC operating speed is limited to about 100 Gbps when using Gen1 HBT (Figure. 2). 6G communications require a minimum speed of 100 Gbps, so test instruments must operate at speeds higher than 100 Gbps. To implement operating speeds of at least 160 Gbps, well beyond the 100 Gbps limit, we developed a Gen2 HBT process targeting $f_T > 300$ GHz and $f_{\max} > 450$ GHz. The Gen2 HBT targets are summarized below.

- High speed ($f_T > 300$ GHz, $f_{\max} > 450$ GHz) and high durability (> 5 V)
- High-speed operation at practical current density ($< \text{several mA/cm}^2$)
- Practical long-term reliability ($\geq \text{several decades}$)

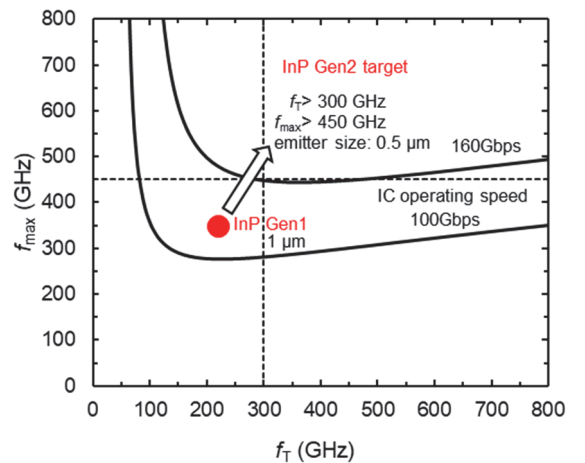


Figure 2 Relationship Between IC Operation Speed and $f_T/f_{\max}$

3 Layer Structural Design and Fabrication Process

To improve f_T , we aimed to shorten the electron transit

times (τ_B and τ_C) by optimizing the structure of the base and collector layers. We designed the collector structure to suppress the potential modulation of the band structure as the current density doubles when the decrease in f_T due to the Kirk effect occurs. To reduce base resistance, the p^+ -InGaAs base-layer doping density was increased from $4 \times 10^{19} \text{ cm}^{-3}$ to $6 \times 10^{19} \text{ cm}^{-3}$ and the thickness was reduced from 50 nm to 30 nm. From the viewpoint of changes in electron mobility⁴⁾, we expected a 28% decrease in the base sheet resistance. Additionally, we planned to reduce base resistance between the base and emitter by minimizing the emitter-to-base separation distance (minimizing W_{Bg}).

We used the emitter-mesa-formation dry-etching process for processing emitter tungsten silicide (WSi) electrodes, and the wet etching process for the semiconductor layer. Minimizing the emitter-to-base separation distance was important to improve performance, so it was necessary to form a narrow mesa structure for the emitter etching process. We formed $\sim 0.5 \mu\text{m}$ width emitter. On the other hand, large side etching (undercut) can lead to an increase in the emitter-to-base separation distance. We reduced the undercut amount and optimized the etching conditions. For dry etching, we adopted Inductively Coupled Plasma (ICP)-Reactive Ion Etching (RIE) offering new high anisotropy. For the wet etching process, we optimized the etching time to form a $\sim 0.5 \mu\text{m}$ wide emitter. From the Scanning Electron Microscope (SEM) image (Figure 3) of the fabricated Gen2 HBT, we can clearly see a transistor with our target emitter width of $\sim 0.5 \mu\text{m}$ and the emitter-to-base separation distance of $0.25 \mu\text{m}$.

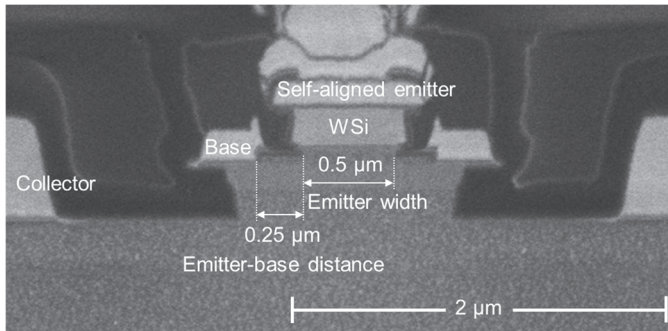


Figure 3 Gen2 HBT Cross-Section SEM

Assuring reliability requires controlling recombination current at the surface of the high-density base layer. To assure long-term reliability for the Gen2 HBT, we used the common guard ring structure (ledge layer). To prevent exposure of the base layer surface, we used n-InP emitter layer

with a depleted doping density of $3 \times 10^{17} \text{ cm}^{-3}$ on the upper part of the base-layer as the ledge layer.

4 HBT Features

The direct current (DC) and frequency characteristics of the prototype Gen2 HBT element with an emitter size of $0.5 \times 5 \mu\text{m}^2$ were measured and the results were used to extract the equivalent circuit parameters for circuit design. Figure 4 shows the measured static characteristics. The DC current amplification factor averaged about 57 in the base current (I_b) range of 50 to 350 μA . Although an HBT current amplification factor of about 30 has been reported⁵⁾, it is suitable for high-output amplifier applications since this fabricated IC has a relatively high current amplification factor. Additionally, it also has a high collector-to-emitter withstand voltage satisfying the minimum target value of 6 V.

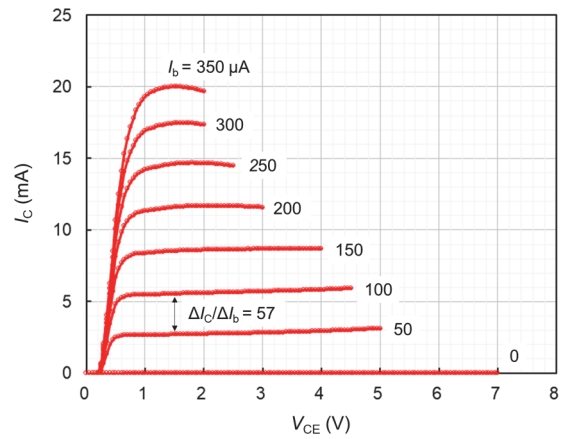


Figure 4 Static Characteristics

The S-parameter was measured using Anritsu's MS4647B Vector Star to evaluate high-frequency characteristics. The S-parameter measured at each bias was used to derive H_{21} and the Unilateral power Gain (UG). Figure 5 shows the H_{21} and UG frequency dependency at the f_T peak bias (1.4 V collector voltage, and 10 mA collector current). The f_T/f_{max} values of 323/510 GHz were extracted by the least-squares method. These values satisfy the target f_T/f_{max} values of $>300/450$ GHz. In addition, high-accuracy measurement is performed using the iterative de-embedding method⁶⁾.

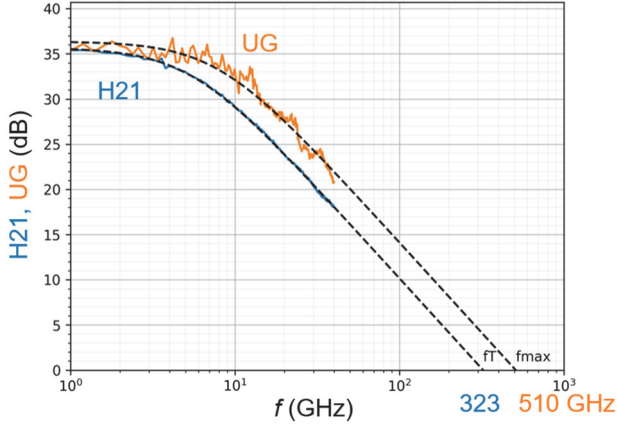
Figure 5 H₂₁ and UG Frequency Response at 1.4 V, 10 mA

Figure 6 shows measured f_T and f_{max} collector current dependency (○ plot) at a collector voltage of 1.4 V. The f_T value peaks (323 MHz) at a collector current of 10 mA. The current density at an emitter size of $0.5 \times 5 \mu\text{m}^2$ is 400 kA/cm², which satisfies the target value of less than several mA/cm². The capacitance and resistance were derived⁷⁾ from $-\text{imag}(Y_{12})/2\pi f$ and from $\text{real}(Z_{11}-Z_{12})$ for the base-to-collector capacitance C_{bc} (green) and base impedance Z_b (brown), respectively. In the created model (solid line), parameters were adjusted so that the base-collector capacitance C_{bc} (brown) and base impedance Z_b (green) were close to the measured values, making it a model suitable for high-frequency circuit design. The base resistance R_{bb} in the Gen2 HBT model using the extracted parameters was 15Ω , which was about 35% less than that in the Gen1 HBT model. From Eq. (3), the base resistance is found as a product of the base sheet resistance and size effect. As previously described, base sheet resistance changes according to the layer structure and is 28% lower in Gen2 HBT than in Gen1 HBT. To examine the size effect, we substituted $L_t=0.2 \mu\text{m}$, with $W_{Bg}=0.35 \mu\text{m}$ and $W_E=1 \mu\text{m}$ into Eq. (3) for Gen1 HBT, and $L_t=0.2 \mu\text{m}$, with $W_{Bg}=0.25 \mu\text{m}$ and $W_E=0.5 \mu\text{m}$ for Gen2 HBT, and found a 11% drop in base resistance. Therefore, we expect a total drop in base resistance of 36%. This is close to the approximate 35% resistance drop obtained by the model. Based on the above, we think that shortening the emitter-to-base distance and increasing the base-layer doping density explains the lower base resistance.

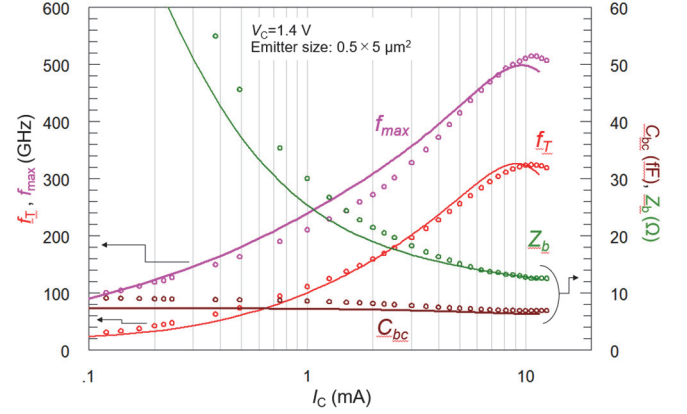
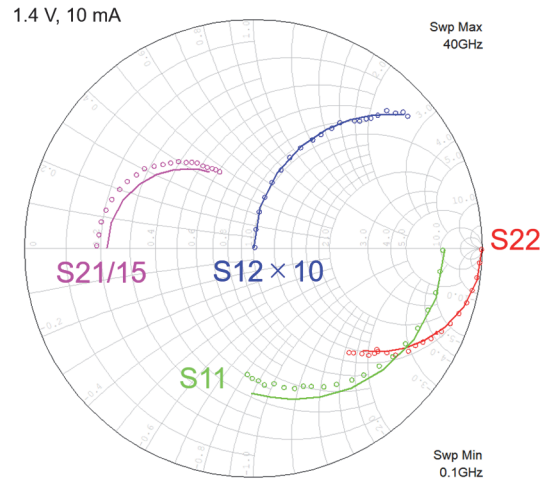
Figure 6 f_T , f_{max} , C_{bc} , Z_b Collector Current Dependency Test Results (Plot) and Model (Solid Line)

Figure 7 shows the measured S-parameters (plots) at a collector voltage of 1.4 V and collector current of 10 mA. For modeling, we adjusted the high-frequency characteristics parameters based on parameters obtained from the DC characteristics to obtain a model (solid line) closely approximating the actual measurements (plot).

With respect to long-term reliability, using a ledge structure confirmed a life of several decades (≈ 70 years) more than the design target. Based on the above, we have developed a Gen2 HBT meeting our targets.

Figure 7 S-parameter Test Results (○ Plot) and Model (Solid Line) S_{12} plotted at 10 times and S_{21} plotted at 1/15 times

5 Wideband Linear Amp Design

(1) Linear Amp Development Target

With the recent growth of cloud and mobile applications, IP network traffic continues to grow, and IEEE is examining introduction of a new Ethernet 800GbE/1.6TbE standard to support this growth. As a result, PAM4 signaling at speeds above 100 Gbaud will become mainstream. A 2.0 Vpp (single-

end) 112 Gbaud PAM4 signal is required by the small Transmitter Optical Sub-Assembly (TOSA) with a 200 Gbps per lane Electro-absorption Modulator integrated Laser diode (EML) using Intensity Modulation/Direct Detection (IM/DD) for 800GbE/1.6TbE signaling; evaluation of the Coherent Optical Sub-Assembly (COSA) optical module for digital coherent communications longer than 80 km using the 800ZR requires a 2.0 Vpp (single-end) 118 Gbaud or faster PAM4 signal. To meet these needs, we developed a wideband linear amplifier using the developed Gen2 HBT supporting 120 Gbaud PAM4 signaling.

(2) Linear Amp Design

In designing the 120 Gbaud wideband linear amplifier, as well as targeting a wideband of at least 100 Gbaud we also targeted (Table 1) output of a 2.0 Vpp high-amplitude signal.

Table 1 Linear Amplifier Target Specifications

	Target Specification
Max. Operating Baud Rate	120 Gbaud typ.
Output Amplitude	2.0 Vpp typ.
Min. Signal Gain	16 dB typ.
-3 dB band	>100 GHz

We used the Gen2 HBT development process. To support pulse responses to the high 120 Gbaud rate, the IC design used a distributed amplifier circuit for wideband flat gain. Moreover, when improving the accuracy of simulation beyond 100 GHz, it helps minimize degraded characteristics due to packaging.

Figure 8 shows the small signal evaluation results for the linear amplifier standalone IC measured using Anritsu's ME7838D VectorStar. The small-signal gain was 17 dB, and the -3 dB gain bandwidth was 113 GHz.

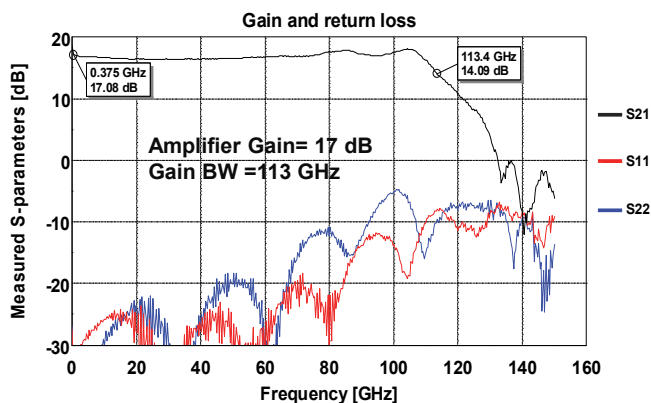


Figure 8 Linear Amp IC Minimum Signal Characteristics Evaluation Results

We then designed the packaged linear amp IC module (Figure 9).

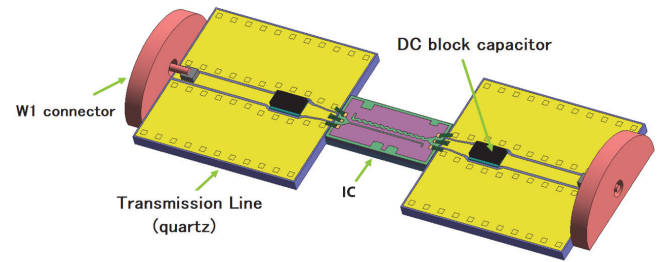


Figure 9 Designed Linear Amp Module Package

The linear amp module I/O uses W-connectors. Quartz board with capacitor in the transmission line filter DC components. Wiring connects the linear amp IC and quartz boards. The results for the first prototype showed module implementation narrowed the -3 dB bandwidth to 60 GHz. Subsequently, we simulated the module transmission characteristics. Based on the simulation results, we made the following improvements; 1) strengthened the GND of the transmission line; 2) used a common GND between separated connector and the transmission line; and 3) improved impedance mismatch.

Figure 10 shows the minimum signal characteristics of the linear amp module measured using the ME7838D. Flat, good pass characteristics of better than 15 dB (16 dB typ.) above 100 GHz were obtained even with the packaged module. Moreover, with a -3 dB bandwidth covering 200 kHz to 105 GHz (typ.) the linear amp module supports the 100 GHz band. These values satisfy the minimum signal gain and band specifications (Table 1).

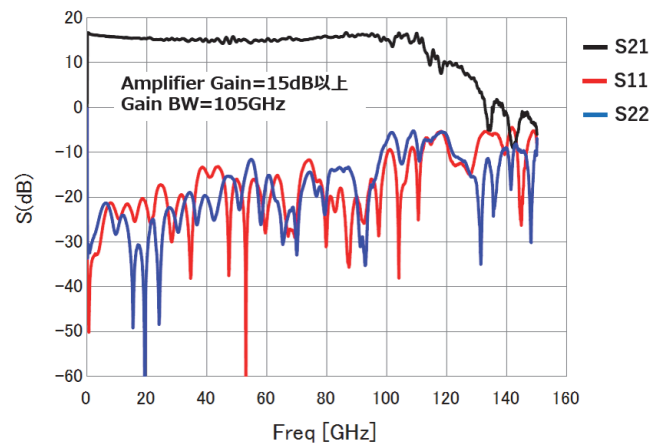


Figure 10 Linear Amp Module Minimum Signal Characteristics Evaluation Results

(3) Linear Amp Product Performance

Figure 11 shows the external appearance of the AH15199A 120 Gbaud Wideband Linear Amp.



Figure 11 External View of AH15199A

Figure 12 shows the AH15199A 120 Gbaud pulse response characteristics (single-end). Compared to the PAM4 input waveform (left), the AH15199A output waveform Eye is open, indicating linear amplification of the input waveform. Consequently, the maximum operating baud rate satisfies the target specification (120 Gbaud typ.). Moreover, the output is amplified to 2.0 Vpp compared to the 0.3 Vpp single-end input amplitude and the voltage gain is 16 dB. As a result, the output amplitude satisfies the target specification (2.0 Vpp typ.).

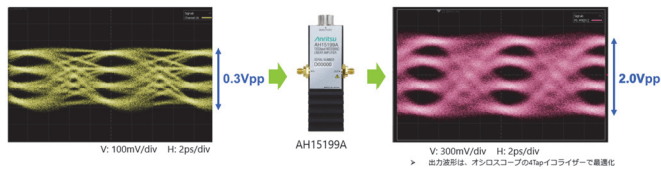


Figure 12 AH15199A 120 Gbaud Pulse Response Properties (Single-End)

As an additional application, combining two AH15199A amps supports amplification of differential output waveforms. However, common mode noise cannot be filtered because this is not fully differential. Figure 13 shows the AH15199A 120 Gbaud pulse response characteristics (differential equivalency) where the input 120 Gbaud 0.6 Vpp input amplitude can be amplified to an output amplitude of 4.0 Vpp.

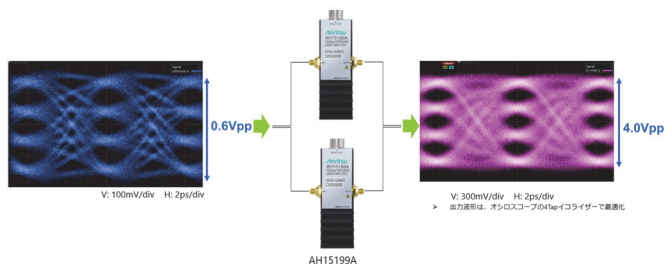


Figure13 AH15199A 120 Gbaud Pulse Response Characteristics (Differential Equivalency)

6 Conclusions

We developed a high-performance ($f_T/f_{max}=323/510$ GHz) InP HBT by optimizing the structure of the transistor layer and processing technology. We designed a wideband linear amp with good 120 Gbaud pulse response characteristics using the fabricated Gen2 HBT. It was possible to amplify input signal of 0.3 Vpp up to 2.0 Vpp.

Future work will focus on designing even faster ICs using the developed HBT.

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