

Implementing FEC Rx Test using FEC Symbol Capture Function

Signal Quality Analyzer-R MP1900A

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1. Introduction

IP data traffic is increasing continuously due to the recent rollout of 5G mobile communications and spread of IoT. Data centers supporting large-volume data communications are not only progressing with the introduction of 400GbE communications technology, but are also examining the introduction of 800GbE and 1.6TbE technologies to support future large-capacity transmissions. The 200GbE and 400GbE speeds standardized in 2017 adopted the use of the PAM4 format to increase transmission capacities. Although the PAM4 format using 4 values doubles the transmission capacity of the earlier NRZ format using two values, the signal-to-noise ratio (SNR) is degraded by about 10 dB. At 200GbE and 400GbE PHY layer transmission, due to the upper limit on the transmission speed and the degraded SNR, the use of PAM4 is premised on the adoption of Forward Error Correction (FEC) technology, without which it would be difficult to achieve the error-free transmissions that characterize the NRZ format. This application note explains the Signal Quality Analyzer-R (SQA-R) MP1900A FEC Solution and describes a concrete example of the FEC Rx test using the PAM4 ED MU196040B FEC Symbol Capture function.

2. FEC Outline and FEC Solution Using MP1900A

This section first explains the outline of FEC, and then explains the FEC Symbol Capture function of the PAM4 ED used by the MP1900A series as well as the FEC Symbol and Codeword definitions.

2.1 IEEE 802.3 FEC Outline

The IEEE 802.3 standard defines various types of FEC. The Reed-Solomon code expressed as RS (n, k) is one typical method. As shown in Table 2.1-1 and Figure 2.1-1, NRZ-format Physical layer transmission uses RS (528, 514), whereas PAM4 transmission uses RS (544, 514). The constants n and k are listed in Table 2-1, which summarizes each definition related to these constants and the FEC Symbol.

Table 2.1-1 RS-FEC Types

RS-FEC	Constant	NRZ RS-FEC RS (528, 514)	PAM4 RS-FEC RS (544, 514)
Total FEC Symbol Count/Codeword	n	528	544
Message FEC Symbol Count	k	514	514
Parity Symbol Count	n-k	14	30
Bit Count (/1-FEC Symbol)	–	10	10
Correctable FEC Symbol Count	–	7	15

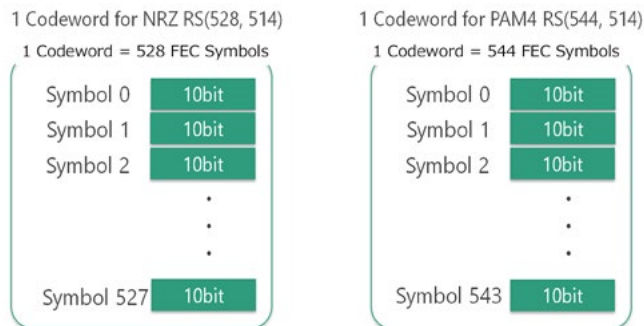


Figure 2.1-1 NRZ/PAM4 RS-FEC

Using RS-FEC specified in IEEE 802.3, the signal itself is split into units called the Codeword; each Codeword is split into 10-bit units called the FEC Symbol.

The NRZ-format RS (528, 514) includes 528 FEC Symbols in one Codeword; 514 of these FEC Symbols are data, while the difference of 14 between 528 and 514 are parity symbols for error detection and correction. Similarly, the PAM4-format RS (544, 514) includes 544 FEC Symbols in one Codeword; 514 of these FEC Symbols are data, while the difference of 30 between 544 and 514 are parity symbols for error detection and correction.

When measuring errors in transmissions using FEC, no consideration is given to the actual number of error bits in one 10-bit FEC Symbol; a FEC Symbol error is detected whether there is one error bit or 10 error bits.

With NRZ-format RS (528, 514), up to seven FEC Symbols containing errors in one Codeword can be corrected and this Codeword is included in the post FEC error-free data. Eight or more FEC symbols containing errors in one Codeword cannot be corrected and are handled as an “Uncorrectable Codeword”.

With PAM4-format RS (544, 514), up to 15 FEC Symbols containing errors in one Codeword can be corrected, but 16 or more errors are handled as an Uncorrectable Codeword.

2.2 Physical Layer Evaluation Using FEC

In the IEEE 802.3 Ethernet Open System Interconnection (OSI), Tx data is sent from the MAC (Medium Access Control) layer side via the PCS (Physical Coding Sublayer) layer to the PMD (Physical Medium Dependent). Conversely, data received at the PMD is passed to the MAC side via the PCS. FEC is one of the function blocks within the PCS.

At sending, data received from the MAC layer is first encoded at 256B/257B after 64B/66B by the Transcoding Block in the PCS. Then, Scrambling is performed at PRBS58, etc., to fix the balance of the signal 0/1 bits. Next, to pass the Tx data via multiple lanes, an Alignment Marker is added at fixed intervals to align bit skew between lanes at receiving. Then, FEC computation is performed, followed finally by Interleaving to multiple lanes in accordance with the PMA lane number. At receiving, conversely, after using the Alignment Markers to correct for skew between lanes, the multilane data is assembled logically into one data stream again. Then, FEC decoding and unscrambling are performed, and the decoded data is passed to the MAC layer.

• 200GBASE-R/400GBASE-R model

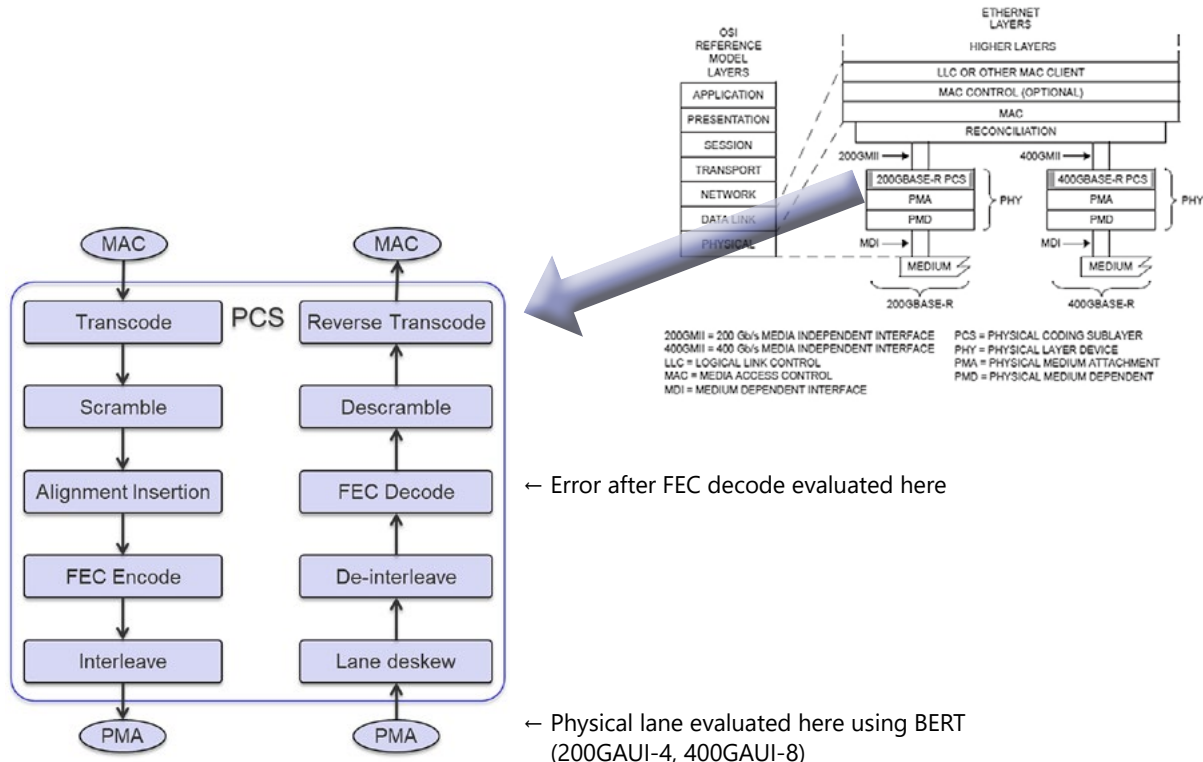


Figure 2.2-1 Ethernet Function Block Diagram

Evaluation of 200GAUI-4/400GAUI-8 defined by the 200GbE/400GbE standards (IEEE 802.3 Annex 120E) using a Bit Error Rate Tester (BERT), requires stressed input tests, such as input sensitivity, jitter tolerance, etc. The 200GAUI-4/400GAUI-8 PHY layer transmission methods using the PAM4 protocol have the above-described error-free transmission issues and define an error rate of $<E-5$. Errors at these Physical layer transmissions are corrected by the PCS FEC Decode function to implement 200G/400G transmissions. However, in real circumstances, even when the stressed input test result using a BERT is $<E-5$ for each of the 200GAUI-4/400GAUI-8 lanes, sometimes error correction by FEC Decode is impossible when errors occur as a concentrated burst within a Codeword, as explained in section 2.1.

As a result, the stress test for 200GAUI-4/400GAUI-8 requires evaluation of errors as shown in Figure 2.2-1.

- Input an FEC Encoded stressed signal for multiple lanes to the DUT and evaluate corrected errors after the output of the DUT multiple lanes has been FEC Decoded.
- Using a BERT, evaluate whether the error rate for each Physical Lane is $<10^{-5}$ as defined by the standard.

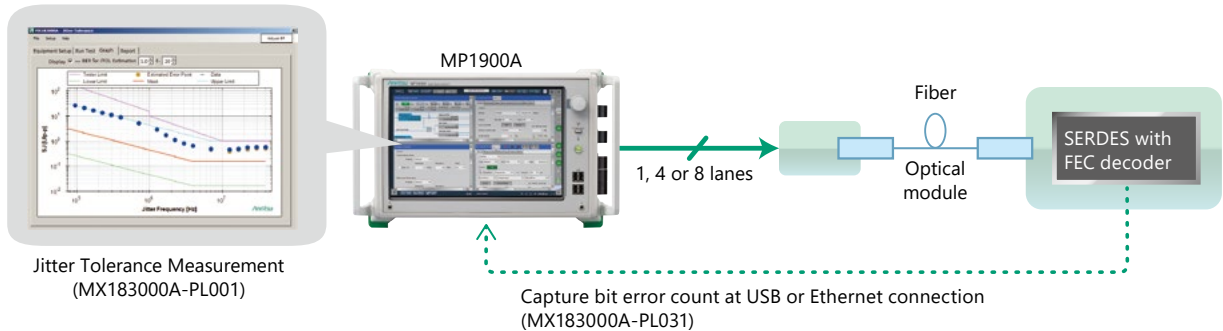
2.3 Outline of FEC Test Solution Using Anritsu MP1900A PAM4 BERT

2.3.1 BER Evaluation of Post-Error Correction Using Multilane Stressed Signal Source and DUT FEC Decode

To evaluate 200GbE/400GbE post-FEC Decode errors, jitter must be impressed with all synchronized 4ch and 8ch signal sources as shown in Figure 2.3-1 for input to the DUT. Using the MP1900A, Random Jitter (RJ), Bounded Uncorrelated Jitter (BUJ), and Sinusoidal Jitter (SJ) are impressed on the RS-FEC pattern of the synchronized multichannel Pulse Pattern Generator (PPG) output to implement the DUT jitter tolerance test. However, since the PAM4 Error Detector (ED) has no RS-FEC Decode function, as shown in Figure 2.3-1, a measurement system is formed for reading the DUT post-FEC Decoder FEC symbol error.

The MP1900A supports stress input tests because it can both read the DUT BER counter value using the DUT Error Counts Import MX183000A-PL031 application as well as perform jitter tolerance tests using the Jitter Tolerance Test application MX183000A-PL001.

Evaluating Optical FEC Signal Transmission



Evaluating Electrical FEC Signal Transmission

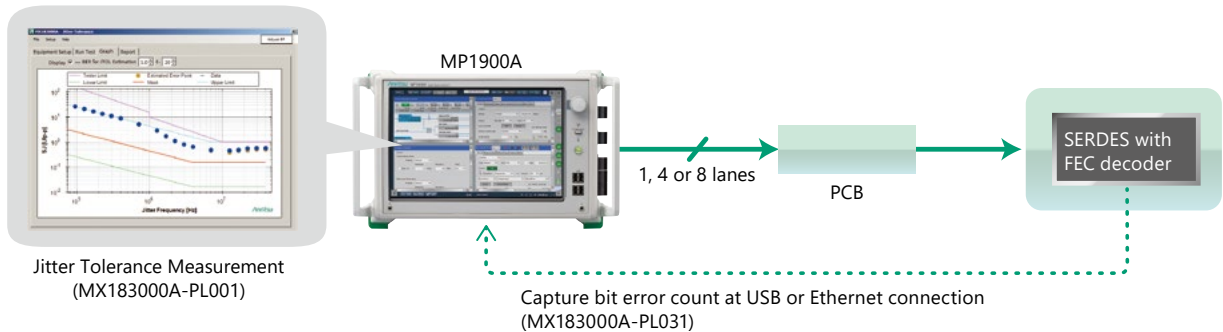
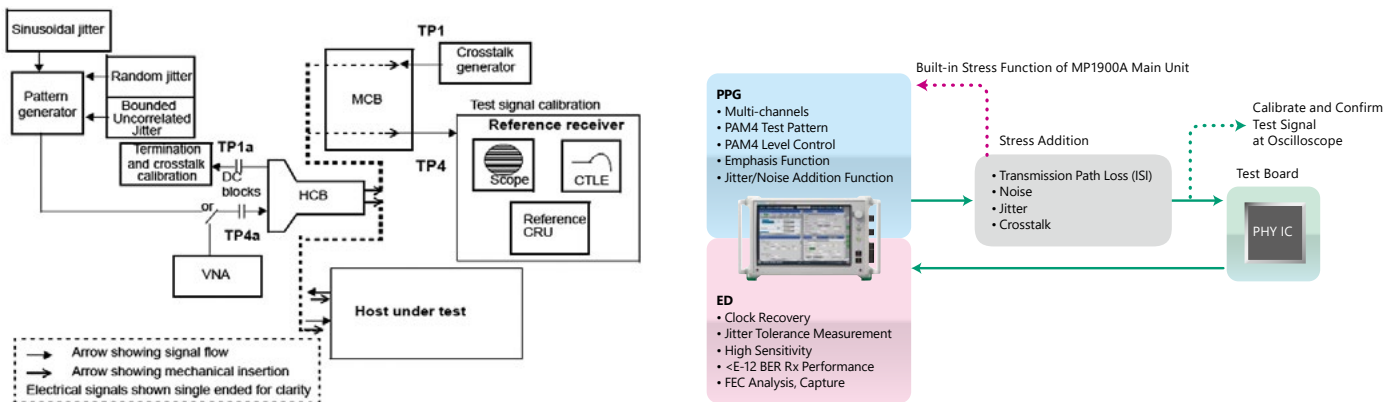


Figure 2.3-1 RS-FEC JTOL Test Block

2.3.2. Evaluating Each Physical Lane Using BERT

The jitter tolerance test is defined for the stress input test specification of the 200GAUI-4/400GAUI-8 interfaces. For example, the Host Stressed Input Test specification defines the jitter tolerance test system (Figure 2.3-2) for impressing SJ, RJ, and BUJ. Using the MP1900A combining the PAM4 PPG and jitter generation source supports the generation of the defined stress signal for input to the DUT and measurement of the output BER.



(200GAUI-4/400GAUI-8 Host Stressed Input Test)

(Outline of Stress Test using MP1900A PAM4 BERT)

Figure 2.3-2 Stressed Input Test for Each Physical Lane

2.3.3. Evaluating Each Physical Lane Using BERT and FEC Symbol Capture Function

The previous section explained the pre-FEC Decode stressed input test using a BERT, but additionally, burst errors that cannot be corrected can be detected and error causes analyzed from captured data for each Physical Lane defined by 200GAUI-4/400GAUI-8, etc., using the FEC Decode ED FEC Symbol Capture function. The details of this function are described in section 2.4.

2.4 FEC Symbol Capture Function for Measuring Physical Lanes

Figure 2.4-1 shows the FEC Symbol Capture settings screen. The MU196040B PAM4 ED considers the input data to follow the RS-FEC pattern and divides FEC Symbols and Codeword at random. When it detects FEC Symbol errors in these Codewords exceeding the set FEC Symbol Error Threshold, it captures both the pattern and error data. Since any FEC Symbol Error Threshold condition can be set as a trigger, in addition to Uncorrectable Codewords, data can be captured and analyzed by inserting FEC Symbol errors corresponding to the measured target FEC symbol criterion.

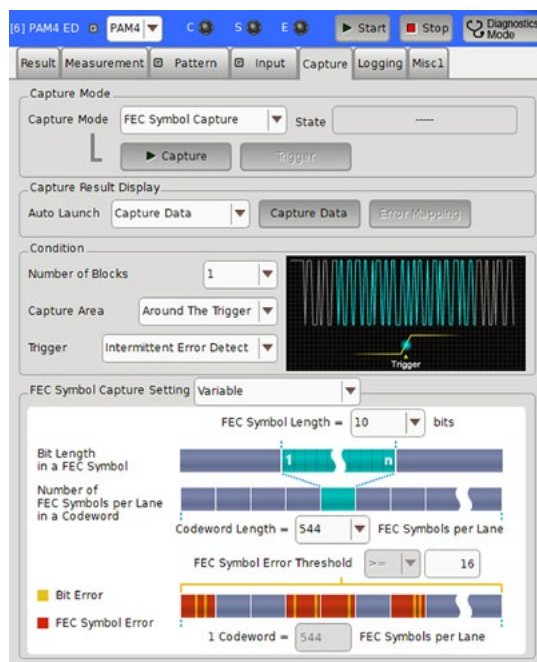


Figure 2.4-1 FEC Symbol Capture Settings Screen

The FEC Symbol Capture function has two trigger conditions: Intermittent Error Detect, and Consecutive Error Detect. Table 2.4-1 lists the trigger conditions for each and the recommended usage.

Table 2.4-1 FEC Symbol Capture Trigger Conditions

Trigger Condition Setting	Function Outline	Usage
Intermittent Error Detect	Depending on Codeword separators, starts capture based on set FEC Symbol error count	To evaluate whether FEC is possible
Consecutive Error Detect	Irrespective of Codeword separators, starts capture of consecutive FEC Symbol errors based on set count	To capture consecutive FEC Symbol errors and evaluate devices generating logical consecutive FEC Symbol errors, such as DFE, CDR, etc.

Intermittent Error Detect divides the received data at random into Codewords and starts capture when the FEC Symbol error count in a Codeword exceeds the set FEC Symbol Error Threshold. The captured results can be used to verify how bit errors and FEC Symbol errors are distributed.

On the other hand, since Intermittent Error Detect divides the data randomly into Codewords, when consecutive FEC Symbol errors occur, sometimes a FEC Symbol error may occur across adjacent Codewords. In this case, the consecutive FEC Symbol error may be divided and counted on the basis of the Codeword separator. Consequently, the Consecutive Error Detect setting is used when wanting to surely capture consecutive FEC Symbol errors. Consecutive Error Detect does not create Codeword separators from the received data and starts capture when the consecutive FEC Symbol error count exceeds the set FEC Symbol Error Threshold.

The FEC Symbol Capture Results screen (Figure 2.4-2) can be used to confirm the detected bit error and FEC Symbol error counts.



Figure 2.4-2 FEC Symbol Capture Results Screen

Since the separators are established for each FEC Symbol, the FEC Symbols with errors and their bit distribution can be confirmed easily. In addition, because the trigger signal can be output externally from the AUX Out connector of the PAM4 ED MU196040B at the instant capture starts, combined use with a real-time oscilloscope, etc., facilitates simultaneous waveform analysis.

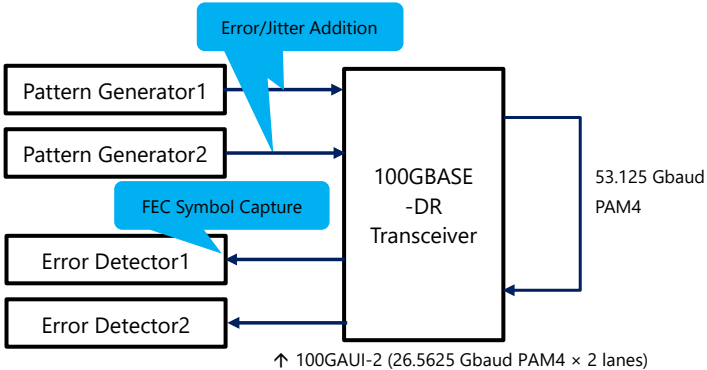
3. 100GAUI-2 FEC-aware Rx Test Solution

This section explains the use of the MP1900A series PAM4 ED FEC Symbol Capture function as well as examples of 100GBASE-DR optical transceiver measurements. It presents the measured results when a logic error is input to the optical transceiver Rx and when jitter stress is in input.

3.1 Measurement System Configuration

Figure 3.1-1 shows the 100GBASE-DR optical transceiver 100GAUI-2 electrical interface measurement system.

• Measurement System Outline



• Setup

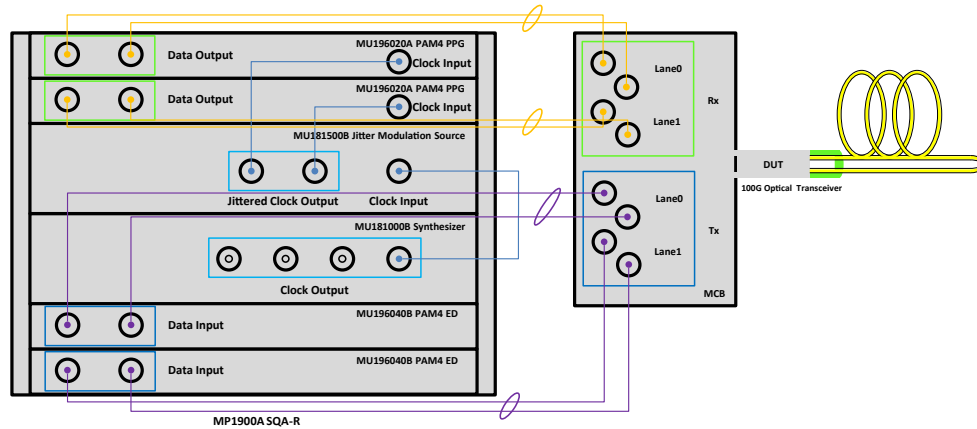


Figure 3.1-1 100GBASE 2Lane FEC Rx Test Measurement System

Table 3.1-1 Required Test Equipment

Model	Name	Qty.	Remarks
MP1900A	Signal Quality Analyzer-R	1	
MU181000B	12.5 GHz 4 port Synthesizer	1	
MU181500B	Jitter Modulation Source	1	
MU196020A	PAM4 PPG	2	Option 001, 011, 030, 042, 050
MU196040B	PAM4 ED	2	Option 001, 011, 021, 041
J1789A	40-cm coaxial cable	8	V connector
34VFK50A	Adapter	8	V (f)-K (m) adapter
–	Optical Transceiver (DUT)	1	
–	Module compliance board	1	
–	Power supply (+3.3 V)	1	

3.2 100GAUI-2 FEC-aware Rx Test

In the above measurement, after measuring FEC Symbol errors without impressing errors or jitter, jitter is added when an error is added to the PAM4 PPG output signal, and the characteristics of dependent FEC Symbol errors are evaluated.

Initial Settings

The following settings are made before starting measurement.

1. Power on the MP1900A, choose Expert BERT from the listed Applications, and start the control software.
2. Synchronize the PAM4 PPG1 and PPG2 outputs as follows (Figure 3.2-1).
 - Select Combination Setting from the Menu function.
 - At the Combination Setting screen, set the Sync ON/OFF and Sync Type settings each to Channel Synchronization.
 - Perform Multi Channel Calibration according to the screen guide.
3. Set Baud-rate at the Settings screen to link the equipment operation (Figure 3.2-2).
 - Select PAM4 PPG1 at the module selection buttons on the right side of the screen and change Clock Source to External once at the Misc2 tab setting.
 - Select Jitter at the module selection buttons on the right side of the screen and change Clock Source from External to MU181000B at the Jitter Modulation Source setting screen.
 - Change Clock Source from MU181000B to External at the PAM4 PPG1 Misc2 tab setting.
4. Perform each of the settings listed in Table 3.2-1 at the PAM4 PPG and PAM4 ED setting screens. (Refer to Figures 3.2-3 and 3.2-4, respectively, for the Pattern and Output/Input settings.)

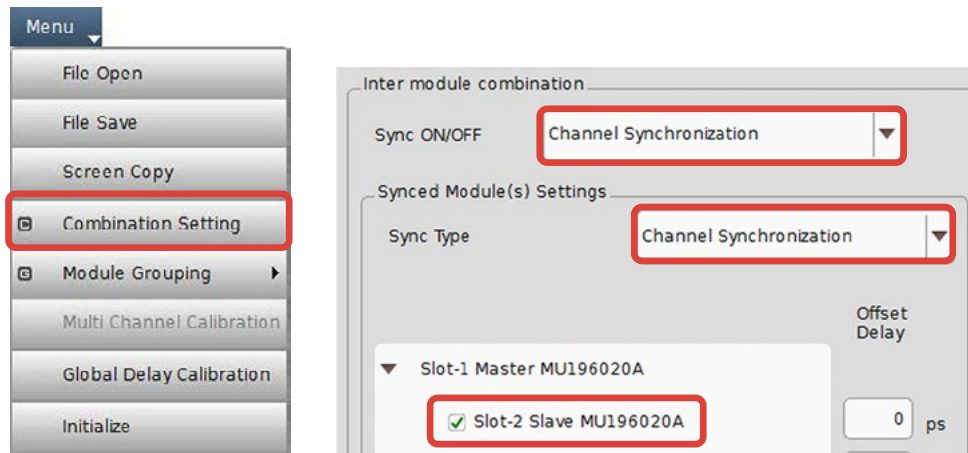
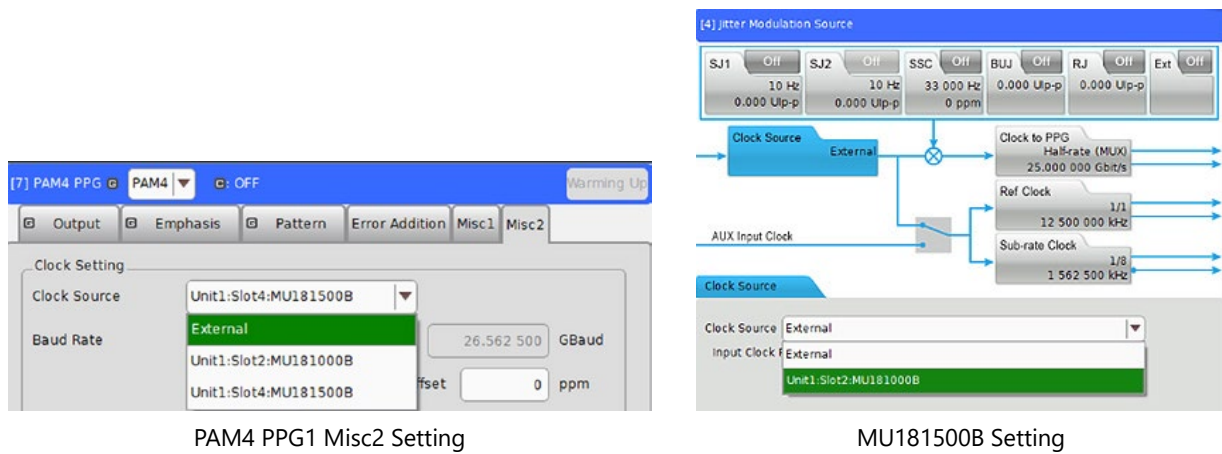


Figure 3.2-1 Synchronization Settings between PPG1 and PPG2



PAM4 PPG1 Misc2 Setting

MU181500B Setting

Figure 3.2-2 Clock Source Settings

Table 3.2-1 List of Initial 100GBase 2Lane FEC Rx Settings

Module	Tab	Function	Setting
PPG1	Output	Baud Rate	26.5625 Gbaud
PPG1/PPG2	Output	Total Amplitude	450 mV (900 mV Differential) Even setting for 3 eyes
		Jitter Input	ON
		Cable for Data Output	J1789A 0.4-m Cable
		Emphasis	Manual Setting
	Pattern	Test Pattern	PRBS31Q
ED1	Pattern	Test Pattern	PRBS31Q
	Input	Input Condition	Differential 50Ohm
		Equalizer	Low Frequency Equalizer: OFF Decision Feedback Equalizer: OFF
		Clock, Selection	Recovered Clock
		Clock, Baud Rate	26.5625 Gbaud
		Clock, LBW	Jitter Tolerance
		Clock, Jitter Input	ON

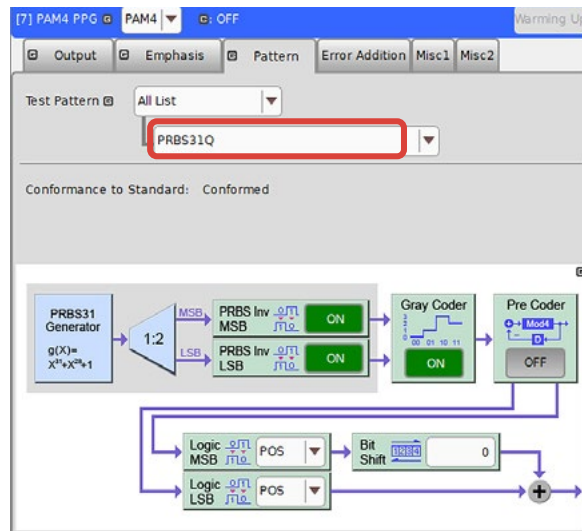


Figure 3.2-3 Pattern Settings

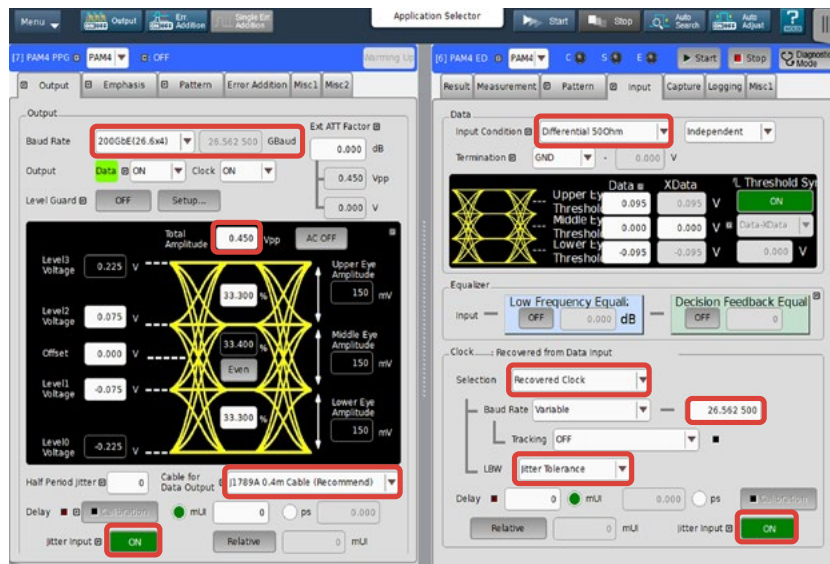


Figure 3.2-4 PPG1 Output Tab and ED1 Input Tab Settings

BER Loopback Measurement Procedure

1. Power on the +3.3 V power supply connected to the optical transceiver, which enters the loopback state at this instant.
2. Set the MP1900A output to ON (Figure 3.2-5).
3. Execute Auto Search Fine (PAM4) with Equalizer ON, and optimize the input threshold and delay settings (Figure 3.2-5).

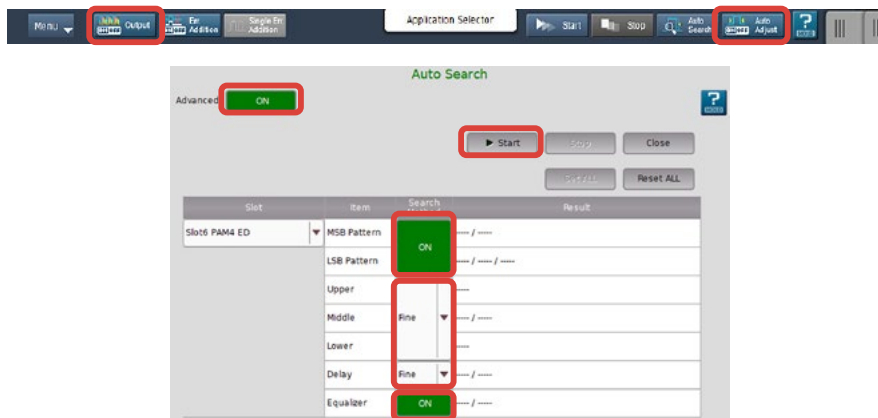


Figure 3.2-5 Output ON and Auto Search Settings

Measurement Procedure using PAM4 ED FEC Symbol Capture Function

1. Set the Capture Mode to FEC Symbol Capture at the Capture tab of the PAM4 ED settings screen (Figure 3.2-6).
2. Set according to Table 3.2-2.

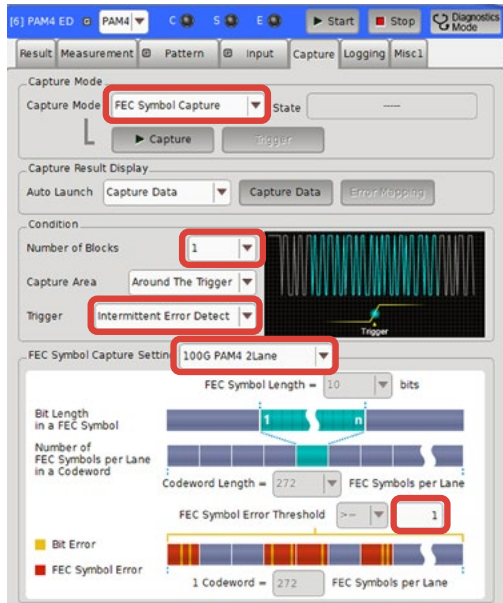


Table 3.2-2 FEC Symbol Capture Function Initial Settings

Function	Setting
Number of blocks	1
Trigger	Intermittent Error Detect
FEC Symbol Capture Setting Selection	100G PAM4 2Lane FEC Symbol Length*: 10-bits Codeword Length*: 272
FEC Symbol Error Threshold	1

*: Refer to Appendix for settings

Figure 3.2-6 FEC Symbol Capture Function Initial Settings

3. Click the Capture button. When FEC symbol errors exceeding the set FEC Symbol Error Threshold are detected, the PAM4 ED starts capture and the status can be confirmed from the State display. The Results screen is displayed when capture is completed (Figure 3.2-7).
4. When Capture Trigger is applied and capture is completed, the results screen is closed and the FEC Symbol Error Threshold value is incremented by one; clicking the Capture button restarts measurement.
5. Repeat the above procedure in step 4 until no Capture Trigger is applied. (Reference: The Capture Trigger wait time at this time is 30 seconds.)
6. Record the maximum FEC Symbol Error Threshold (hereafter Max FEC Symbol Error) when Capture Trigger is applied.

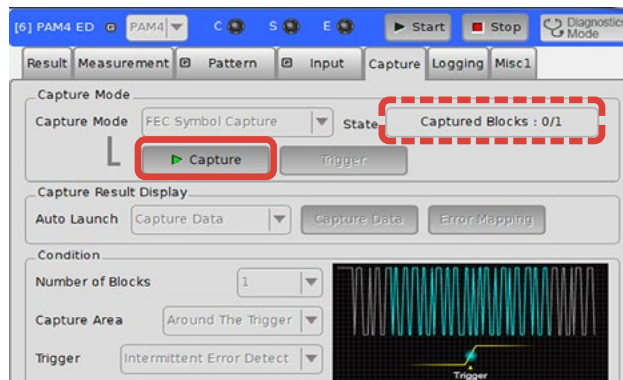


Figure 3.2-7 FEC Symbol Capture Start Button and State Display

The PAM4 Symbol Error Rate and the Max FEC Symbol Error obtained using the above-described procedure are listed in Table 3.2-3. At the baseline condition without jitter and error addition, the presence of a maximum of four FEC symbol errors in one Codeword is confirmed, but since this is smaller than the 15 correctable FEC symbol errors defined by the IEEE 802.3 standard (Table 2.1-1), the baseline condition is described as having a fully correctable Codeword.

Table 3.2-3 Baseline Condition FEC Symbol Capture Results

Test Item	Result
PAM4 Symbol Error Rate	1.066E-7
Max FEC Symbol Error	4

3.3 FEC-aware Rx Test Using PAM4 PPG Error Addition Function

Continuing measurement of the baseline condition described in section 3.2, this section explains FEC Rx measurement when local errors are added using the PAM4 PPG Error Addition function. Figure 3.3-1 shows the PPG Error Addition settings screen.

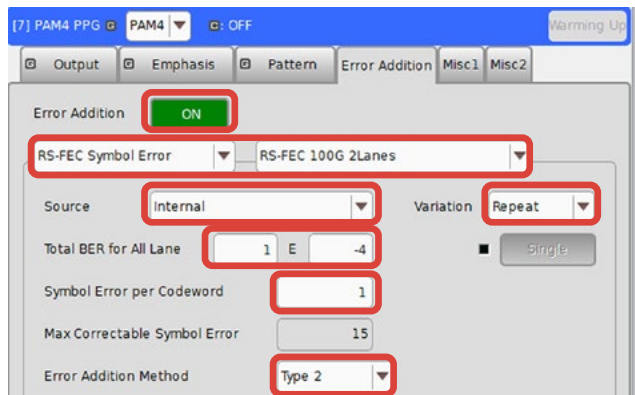


Figure 3.3-1 PAM4 PPG Error Addition Function Settings Screen

The Max FEC Symbol Error value is measured using the PAM4 ED FEC Symbol Capture function in the same manner as described in section 3.2 for the Symbol Error per Codeword value added using the PAM4 PPG Error Addition function.

Measurement Procedure

- 1. Make the initial settings shown in Table 3.3-1 at the PAM4 PPG Error Addition tab (Figure 3.3-1).

Table 3.3-1 PAM4 PPG Error Addition Initial Settings

Function	Setting
Error Addition	ON RS-FEC Symbol Error RS-FEC 100G 2Lane
Source	Internal
Variation	Repeat
Total BER for All Lane	1E-4
Symbol Error per Codeword	1
Error Addition Method	Type2

- 2. Measure the Max FEC Symbol Error value according to the measurement procedure using the FEC Symbol Capture function described in section 3.2.
- 3. Increase the PAM4 Symbol Error per Codeword values at the PAM4 PPG and measure the Max FEC Symbol Error values in the same way using the FEC Symbol Capture function.

Figure 3.2-2 shows the measured Max FEC Symbol Error results for the PPG data output added Symbol Error per Codeword.

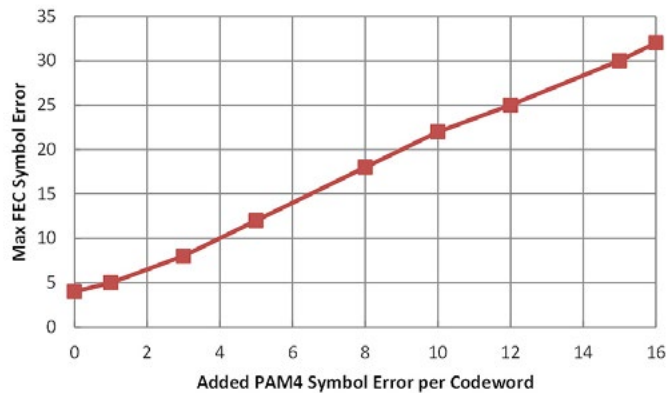


Figure 3.3-2 Max FEC Symbol Error Values vs PAM4 Symbol Error Inserted Values

The figure confirms that the Max FEC Symbol Error value increases as the number of PAM4 Symbol Errors inserted in one Codeword increases. However, PAM4 PPG errors can be inserted by selecting either FEC Symbol or PAM4 Symbol using the Error Addition Method setting. FEC Symbol Errors are inserted by setting the Error Addition Method to either MSB Only or LSB Only. The other settings are used for inserting PAM4 Symbol Errors. At PAM4 Symbol Error insertion, the range between the inserted error value (x) and the expected FEC Symbol Error value per one Codeword (y) is $x \leq y \leq 2x$.

Since Max FEC Symbol Error 4 has already been observed as the baseline condition, the range of the FEC Symbol Error values observed using the Error Addition function is $x \leq y \leq 2x + 4$. Using the PPG Error Addition function in this manner supports Codeword simulation for various logic error conditions. These errors can also be captured and analyzed using the FEC Symbol Capture function.

3.4 FEC-aware Rx Jitter Tolerance Test

To evaluate the characteristics of devices supporting 200GAUI-4/400GAUI-8, etc., it is essential to perform evaluation by combining various types of jitter, including not only SJ but also RJ and BUJ. In this case, the MU181500B Jitter Modulation Source (Jitter Module hereafter) is used to perform FEC Rx Jitter Tolerance tests while adding SJ, RJ, and BUJ, respectively. Figure 3.4-1 shows the settings screens for each type of jitter.

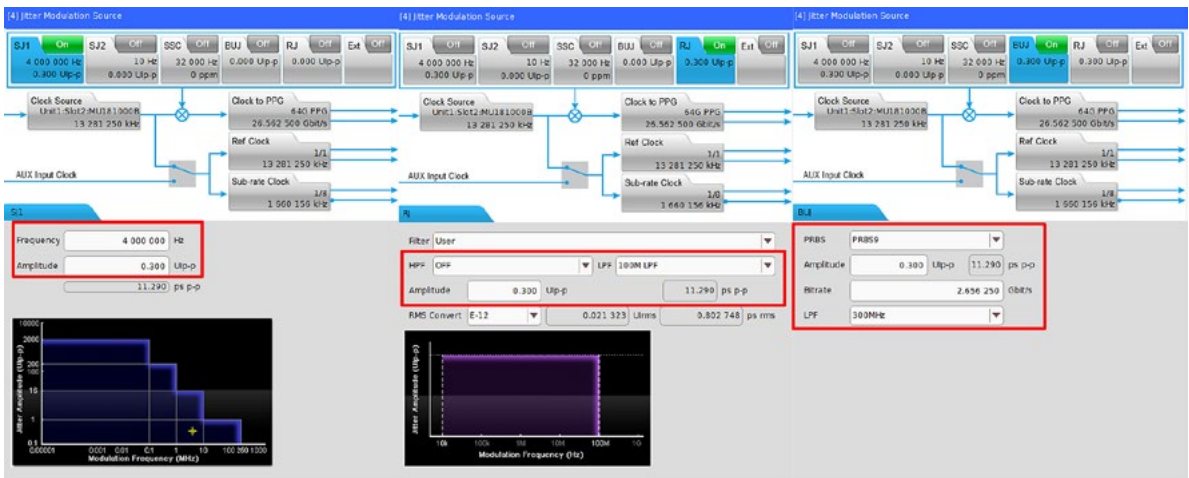


Figure 3.4-1 Jitter Settings Screen List (left: SJ, center: RJ, right: BUJ)

- The PAM4 Symbol Error Rate and Max FEC Symbol Error value are measured by changing the amount of each jitter as follows:
1. Make the settings shown in Table 3.4-1 at the Jitter Module.
 2. Monitor the PAM4 Symbol Error Rate and Max FEC Symbol Error value by following the baseline condition measurement procedure described in section 3.2.
 3. Increase the Amplitude for each of SJ, RJ, and BUJ, and monitor the PAM4 Symbol Error Rate and Max FEC Symbol Error value using the FEC Symbol Capture function as described in section 3.2.

Table 3.4-1 100GBase 2Lane FEC Rx Jitter Test Settings

Jitter Type	Item	Setting
SJ1	Frequency	4 MHz
	Amplitude	Variable
RJ	HPF	OFF
	LPF	100 MHz
	Amplitude	Variable
BUJ	PRBS	PRBS9
	Amplitude	Variable
	Bitrate	2.65625 Gbit/s
	LPF	300 MHz

Figures 3.4-2 and 3.4-3 show the results captured using the above-described procedure.

As shown in Figure 3.4-2, the PAM4 Symbol Error Rate was about $1\text{E-}7$ when impressing any of the SJ, RJ, or BUJ jitter stresses up to a Jitter Amplitude of 0.35 UI. However, as shown in Figure 3.4-3, when the SJ stress exceeded 0.3 UI, the Max FEC Symbol Error value increased, reaching 16 at an SJ of 0.36 UI.

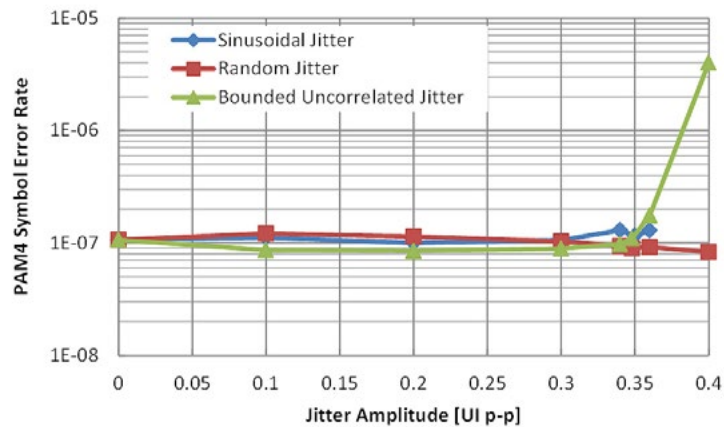


Figure 3.4-2 Jitter vs PAM4 Symbol Error Rate

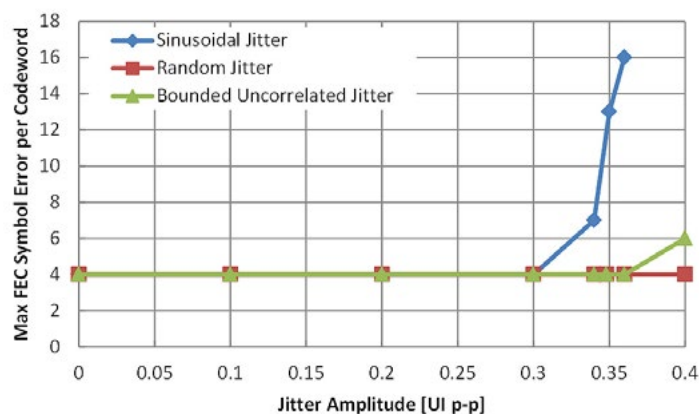


Figure 3.4-3 Jitter vs Max FEC Symbol Error Value

Since SJ is a factor in periodic burst errors, errors are grouped in the same Codeword even at the same PAM4 Symbol Error Rate. As a result, the Max FEC Symbol Error count is thought to increase only when SJ is impressed. However, BUJ and RJ increase the Max FEC Symbol Error count relative to the PAM4 Symbol Error Rate because PAM4 Symbol Errors are inserted randomly. The Max FEC Symbol Error count result is very different even if the PAM4 Symbol Error Rate is at the same level due to the concentration of errors in a specific Codeword as a result of the error distribution. Based on this result, when measuring FEC Rx tolerance by impressing jitter, it is important to confirm the PAM4 Symbol Error Rate and the Max FEC Symbol Error count and not just the BER.

3.5 Summary of FEC-aware Rx Test

This measurement performs the stress input test for each lane defined by 100GAUI-2 (IEEE 802.3 Annex 135G) using the FEC Symbol Capture function. Using this measurement supports the detection and analysis of burst errors that cannot be corrected by FEC Decode, as well as BER results for each lane.

However, unlike measuring using FEC Decode by impressing jitter on multiple lanes, due to the difference of the evaluation point described in sections 2.2 and 2.3, there is no match with error correction results for multiple lanes. Moreover, since the result for one lane may not be the same for other lanes, the use of this measurement solution is recommended for measuring each lane or worst-case lanes, as well as for error analysis.

4. Summary

FEC receive measurements like those in section 3 require consideration of the FEC Symbol error count in one specific section called a Codeword, which did not require consideration in previous BER/SER measurements. Consequently, this Application Note introduces the MP1900A FEC Rx measurement solution and an example of an RS-FEC Rx test measurement using the MP1900A.

Anritsu offers timely solutions to help business development by working in partnership with its customers to understand business trends.

References

IEEE Std 802.3™-2022

Appendix: Handling FEC Symbols at FEC Lane and Physical Lane

As described in section 2.1, two types of RS-FEC are specified by IEEE: RS (528, 514), and RS (544, 514). Although the FEC Codeword size is different, the length of the FEC symbols configuring the Codeword is 10 bits for both these RS-FEC types.

Figure a-1 shows the bit ordering and FEC Symbol transmits bits for 100G 1 Lane. Although there are 10 continuous bits in one FEC Symbol at Symbol Distribution in each FEC Lane after Codeword, since Bit MUX is performed subsequently for each FEC Lane, there are not 10 continuous bits in one FEC Symbol in Physical Lane. As a result, the MP1900A for physical layer measurement defines the FEC Symbol and Codeword uniquely.

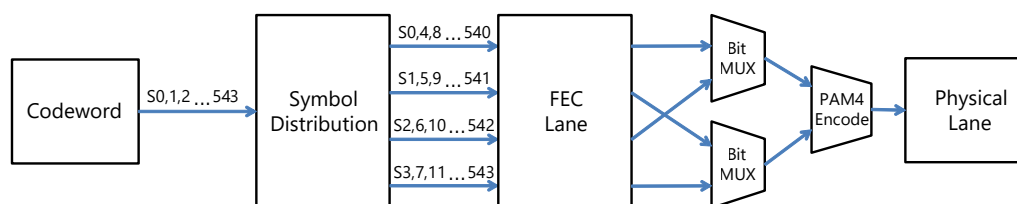


Figure a-1 100G 1 Lane RS (544,514) Transmit Bit/FEC Symbol Ordering

Figure a-2 shows a concrete example of bit transmission for the 100G 1 Lane specification as well as the 100GBase PMA multiplexing. The blue lines in Figure a-2 indicate the FEC Symbol breaks at every 20 bits for reference. S0 is FEC Symbol0, S1 is FEC Symbol 1, and the later values indicate the bit number at each respective FEC Symbol. Although 1 Lane is the only Physical Lane in the 100G 1 Lane specification, the FEC Lane is divided into 4 lanes. As shown in Figure a-1, due to the PAM4 Encode processing after Bit MUXing of either two FEC Lanes, the Physical Lane becomes a 1 Lane PAM4 signal. The effect of this Bit MUXing is to generate 10 continuous bits in one FEC Symbol in the FEC Lane but not in the Physical Lane.

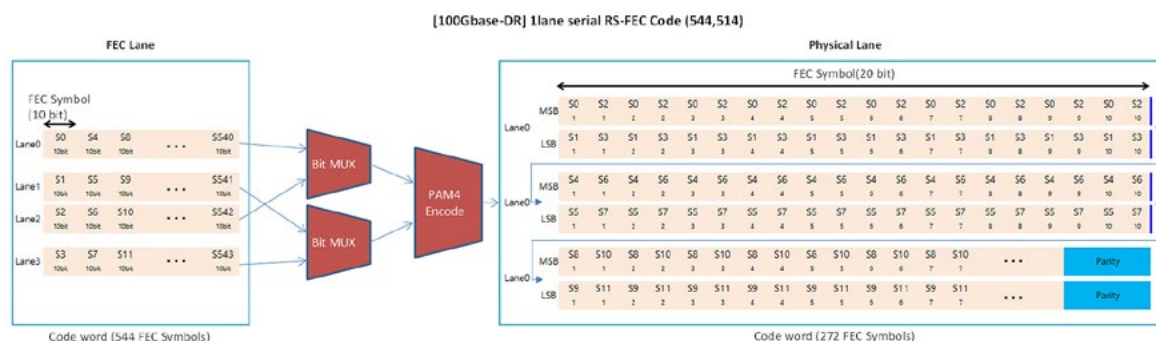


Figure a-2 100G 1 lane RS (544,514) Codeword Structure

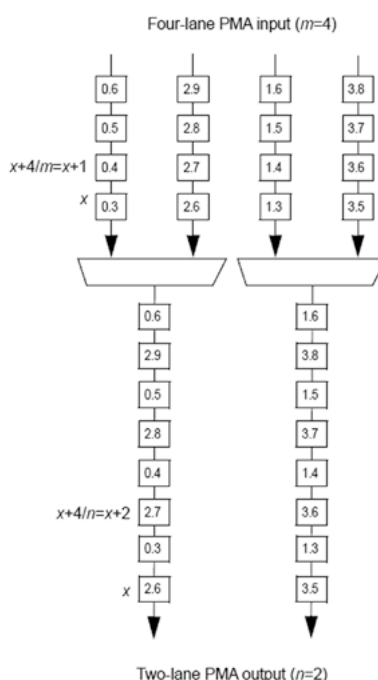


Figure a-3 4:2 100GBase PMA Bit MUX

Figure a-4 shows the error distribution when the FEC Symbol length is 10 bits and 20 bits as defined in the 100Gbase 1 Lane specification. Although bit errors are inserted at the same position in both cases, it is clear there are four FEC Symbol Errors when the FEC Symbol Length is 20 bits, and eight when it is 10 bits. When confirming bit errors, bit errors are inserted at FEC symbol numbers 2, 7, 8 and 9, and actually four FEC symbol errors are inserted in both cases. In this way, bits with the same FEC Symbol appear at the adjacent FEC Symbol when one FEC Symbol = 10 bits like in the FEC Lane. Consequently, when one FEC Symbol is divided into 10 bits, there is a possibility that the measured FEC Symbol Error result will not be the expected value. To prevent this, when using the MP1900A to measure this standard, we recommend setting one FEC Symbol to 20 bits. By doing so, measurement can be performed without changing the Uncorrectable threshold. Although the length of one FEC Symbol changes at this time, one Codeword is 272 FEC Symbols and not 544 FEC Symbols because the Codeword bit length does not change.

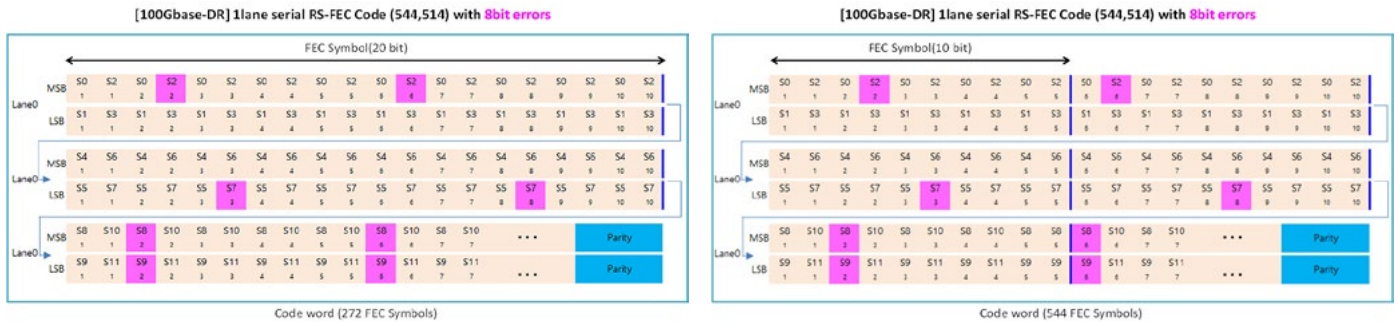


Figure a-4 100G 1 lane RS (544,514) Example – Same BER, Different FEC Symbol Length

Figure a-5 shows an example of multiple lanes. Since PAM4 Encode is performed directly by choosing two FEC Lanes from each FEC Lane, one FEC Symbol at the Physical Lane is 10 continuous bits. As a result, one FEC Symbol is 10 bits in this case. Moreover, although Lane 0 and Lane 1 of the Physical Lane are originally the same Codeword, the Codeword size for each Physical Lane can be defined using the MP1900A. Consequently, one Codeword is 272 FEC Symbols at this time.

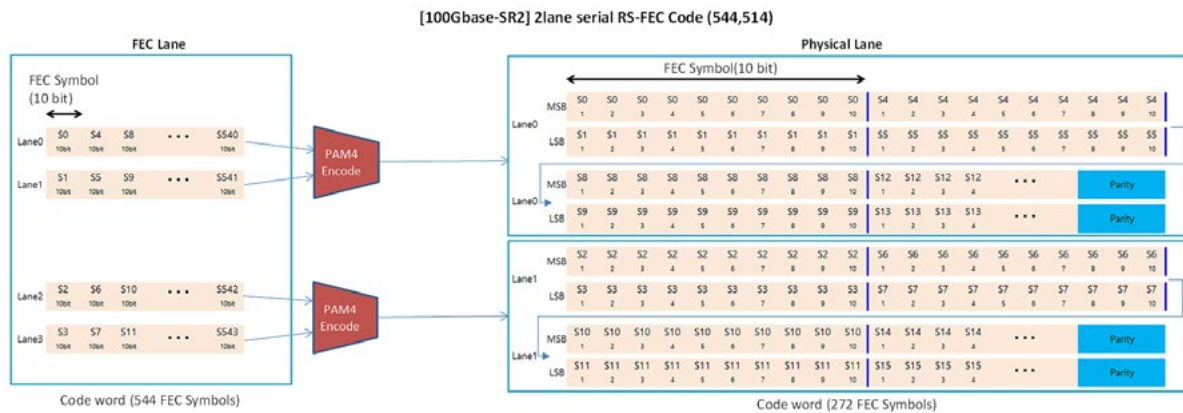


Figure a-5 100G 2 lane RS (544,514) Codeword Structure

When there are multiple Physical Lanes, it is necessary to consider whether there are FEC Symbol Errors when the Codeword timing is the same. Normally, the DUT has some randomness because the jitter tolerance is different between Physical Lanes. Consequently, even when the same jitter and ISI are impressed, the same number of FEC Symbol Errors does not occur when the Codeword timing is the same.

As shown in Figure a-6, normally, the FEC Symbol Error count at a specific Codeword is different for each Physical Lane. As a result, when using the PAM4 ED to measure only one Physical Lane, it is not necessary to divide the Uncorrectable FEC Symbol Error count equally between the number of Physical Lanes. However, this does not mean that there are no FEC Symbol Errors in other Physical Lanes. Consequently, we recommend setting the FEC Symbol Error Threshold after measuring and generally evaluating the BER of all Physical Lanes.

Moreover, unlike the above-described operation, consideration must be given to entering the same number of Max FEC Symbol Errors in all Physical Lanes. However, it is not necessary to divide the number of Uncorrectable FEC Symbol Errors equally between the number of Physical Lanes as in the previous example, because the probability of this type of case occurring FEC symbol errors at all Physical Lanes is so low that it does not need to be considered usually.

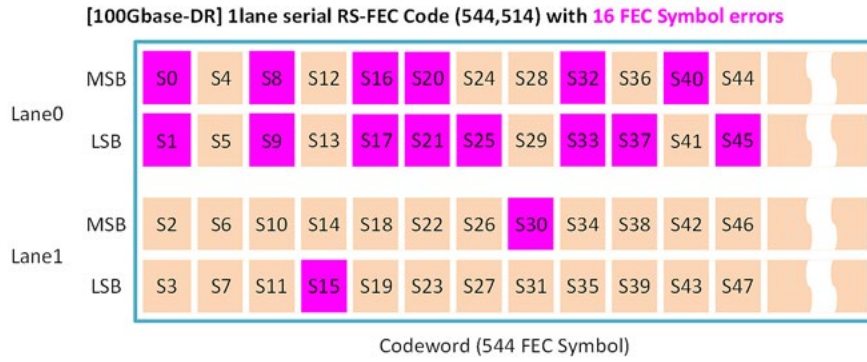


Figure a-6 100G 2 Lane RS (544, 514) with FEC Symbol Errors

Table a-1 lists the MP1900A-defined Codeword and FEC Symbol lengths for each specification and number of Physical Lanes.

Table a-1 MP1900A RS-FEC Setting Variation

FEC	Format	Standard	Baud-rate	Physical Lanes	Codeword Length	FEC Symbol Length
RS (528, 514)	NRZ	25GbE	25.78125 G	1	528 FEC Symbols	10 bits
		100GbE	25.78125 G	4	132 FEC Symbols	10 bits
RS (544, 514)	PAM4	50GbE	26.5625 G	1	544 FEC Symbols	10 bits
		100GbE	26.5625 G	2	272 FEC Symbols	10 bits
			53.125 G	1	272 FEC Symbols	20 bits
		200GbE	26.5625 G	4	272 FEC Symbols	10 bits
		400GbE	26.5625 G	8	136 FEC Symbols	10 bits
			53.125 G	4	136 FEC Symbols	20 bits

Moreover, the MP1900A-defined Codeword and FEC Symbol Lengths can be found using the following equations (1) to (5):

$$\text{Codeword Length (NRZ)} = \frac{5280 \times 5}{2 \times \text{SBR}} \quad (1)$$

$$\text{Codeword Length (PAM4 50G/100G)} = \frac{5440 \times 5}{\text{SBR}} \quad (2)$$

$$\text{Codeword Length (PAM4 200G/400G)} = \frac{5440 \times 5 \times 2}{\text{SBR}} \quad (3)$$

$$\text{FEC Symbol Length (NRZ)} = \frac{2 \times \text{SBR}}{5 \times \text{PLN}} \quad (4)$$

$$\text{FEC Symbol Length (PAM4)} = \frac{\text{SBR}}{5 \times \text{PLN}} \quad (5)$$

where, SBR is the total bit rate defined by the standard (400 for 400GbE), and PLN is the number of Physical Lanes.

In this way, despite the various Codeword and FEC Symbol lengths, since the Codeword and FEC Symbol lengths are recognized automatically by setting the standard and number of Physical Lanes using the MP1900A as shown in Figure a-7, FEC Symbol Capture in particular can be performed without being conscious of the settings in Table a-1. Moreover, there is no necessity to change the Uncorrectable Codeword threshold according to increases/decreases in the Physical Lane number.

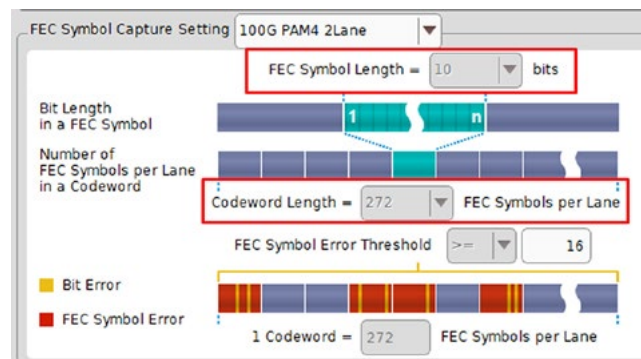


Figure a-7 MU196040B FEC Symbol Capture Setting Display