Application Note

Anritsu Advancing beyond

PCI-Express Generation 4 Rx Test Solution

Signal Quality Analyzer-R MP1900A Series

Contents

1. Introduction

PCI Express (PCIe) Generation (Gen) 1 is a common computer interface with transmission speeds of 2.5 GT/s. Subsequent advances brought Gen 2 at speeds of 5 GT/s and Gen 3 at 8 GT/s; Gen 4 at 16 GT/s is currently being tested by the PCI-SIG Workshop. In addition, internal discussions about Gen 5 at 32 GT/s are starting at PCI-SIG.

As a result of the higher transmission speeds, PCIe Gen 4 at 16 GT/s is being deployed not only in general PC equipment but is also being adopted as an internal interface for various equipment, such as transmission devices, servers, storage, etc., in data centers. Data-center equipment is using 100G/200G/400GbE as external interfaces and PCIe Gen 4 is being adopted as an interface for internal data transmissions.

The Signal Quality Analyzer-R (SQA-R) MP1900A naturally supports NRZ signaling used by this equipment, but it also offers all-in-one support for PAM4 signaling used by 200G/400G external interfaces and for PCIe internal interfaces. Moreover, since it also supports 32 GT/s speeds required by the Gen 5 standard, it is the ideal measurement solution meeting both current and future testing requirements and helping cut capital equipment costs.

This Application Note explains how to use the MP1900A with focus on PCIe Gen 4 Rx Stress tests, which are the current focus of PCIe Workshop, and troubleshooting methods.

2. Equipment Setup

The block diagram and setup required by the PCIe Rx Test is shown in the following figure.

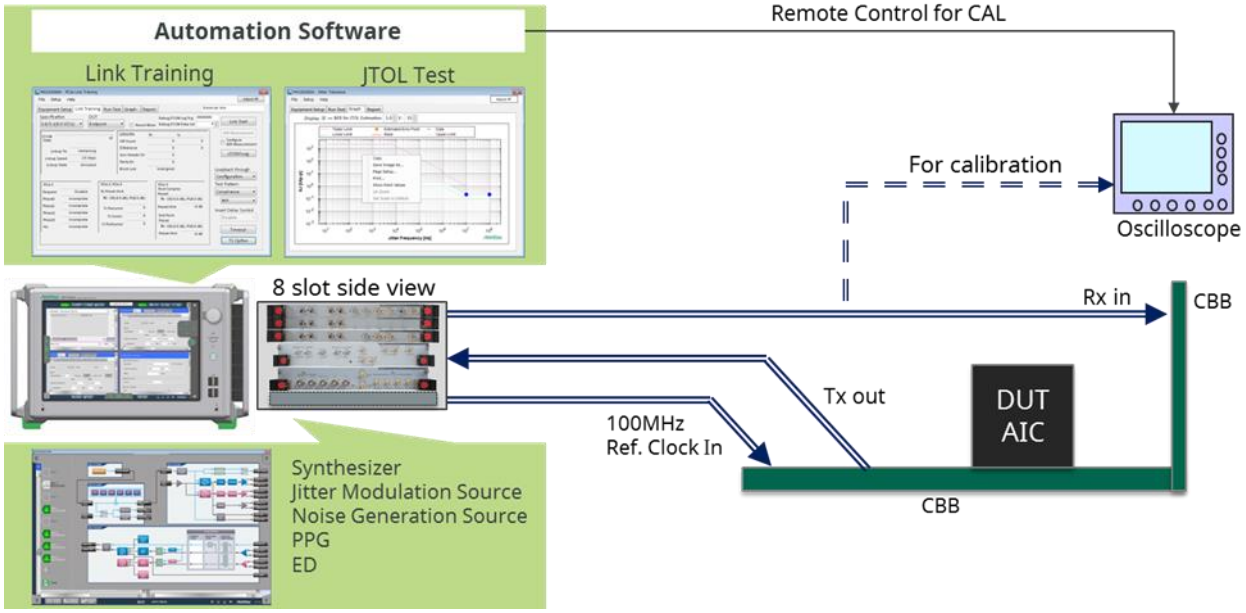

Fig. 2.1 Block Diagram

The real-time oscilloscope in the above figure is used to calibrate the waveform output from the MP1900A. The PCIe certification test validates equipment from each measuring instrument vendor to ensure the same waveform is generated by the calibration procedure.

Table 2.1 PCIe Test Configuration

Model Number	Model Name	Options	Qty	Note
MP1900A	Signal Quality Analyzer-R	-	1	Main unit
MU181000B	12.5GHz 4port Synthesizer	002	1	Synthesizer
MU181500B	Jitter Modulation Source	-	1	Jitter source
MU195020A	21G/32G bit/s SI PPG	001*1, 010, 011	1	SI PPG
MU195040A	21G/32G bit/s SI ED	001*1, 010, 011, 022	1	SI ED
MU195050A	Noise Generator	-	1	Noise source
MX183000A	High-Speed Serial Data Test Software	001, 021	1	Link Training, Jitter Tolerance Software

Note *1: Required for Gen 5 tests

3. Connections

PCIe devices are categorized into two types: System (or Root complex) such as the CPU and motherboard acting as the Primary device, and Add-in Cards (AIC) acting as the Secondary device connected to the Primary. Care is required because the waveform calibration for the compliance test and the cable connections are different for System and AIC devices.
The following diagrams (Figs. 3.1 to 3.4) show the connections for calibration and the RX Stress Test of System and AIC devices. In these diagrams, CLB and CBB mean Compliance Load Board and Compliance Base Board, respectively, both of which can be purchased from PCI-SIG.

Fig. 3.1 System Configuration

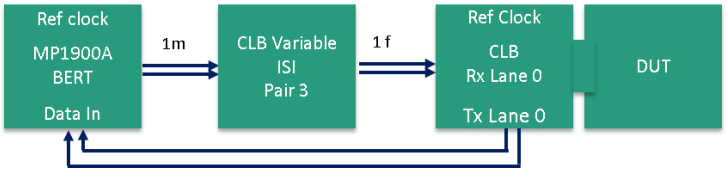

Fig. 3.2 System Stressed Rx Test

Fig. 3.3 AIC Configuration

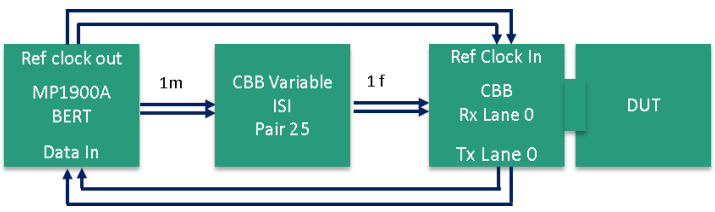

Fig. 3.4 AIC Stressed Rx Test

The MP1900A connections in the above diagrams are as follows.

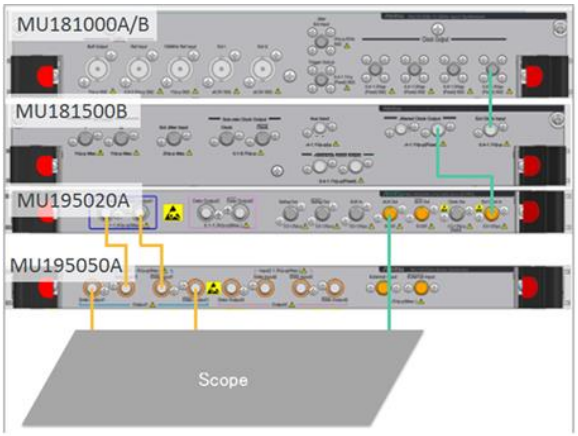

Fig. 3.5 MP1900A Configuration Connection

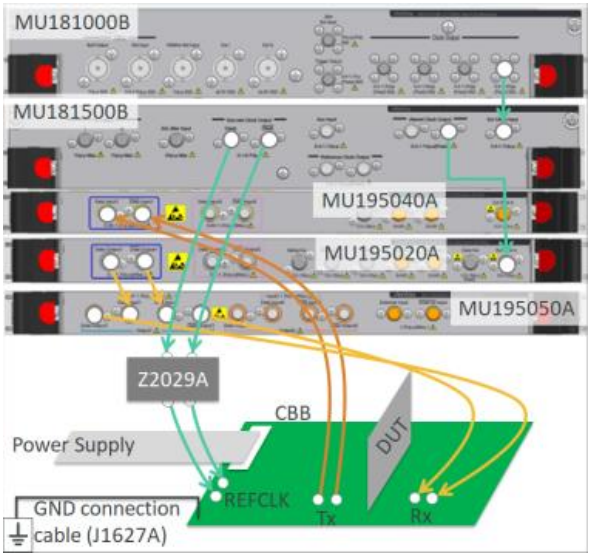

Fig. 3.6 MP1900A Rx Test Connection

4. Calibration

This section describes the waveform calibration method for the PCIe Gen 4 Rx Stress Test using concrete Anritsu measurement solutions.

4.1 Channel Loss

Calibration first confirms that the loss is from 27 to 30 dB at 8 GHz when the CBB and CLB and ISI board, and cables are connected. Figures 4.1 and 4.2 show the loss budget between the boards for the System and AIC devices.

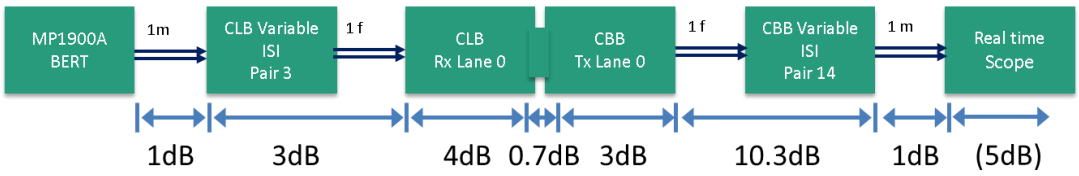

Fig. 4.1 System Loss Budget

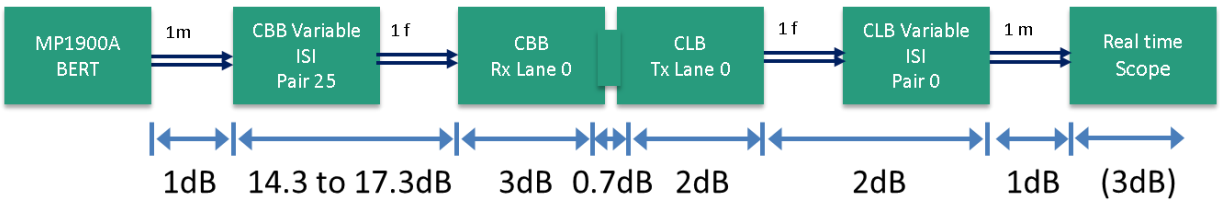

Fig. 4.2 AIC Loss Budget

Referring to the above-described loss budgets, the total loss is measured by the 4-port differential VNA and the best loss pair is selected from among the ISI boards.

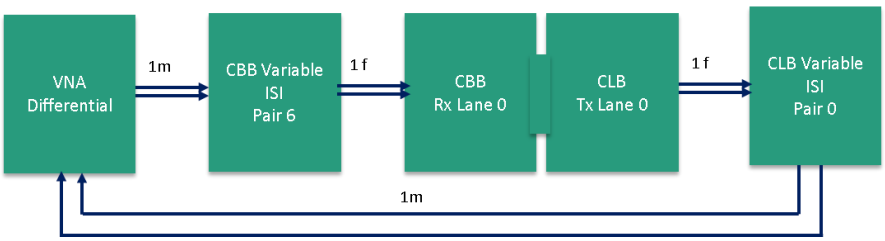

Fig. 4.3 Loss Measurement by VNA

4.2 Amplitude

Next, the Amplitude, Preset, SJ, RJ, and DM values at the BERT side are calibrated. Unless specifically mentioned, the real-time scope requires a bandwidth of 25 GHz or better and a sampling rate of 80 Gsamples/s or better.

The Amplitude calibration uses patterns of 64 bits of contiguous 0s and 64 bits of contiguous 1s followed by 128 bits of repeated 0s and 1s (010101…). With Emphasis set to OFF, the amplitude is adjusted so the differential between the 0101... repetition is 800 mVp-p. The real-time oscilloscope at this time is set to Average of 16 points and Horizontal Scale of 100 ns/div.

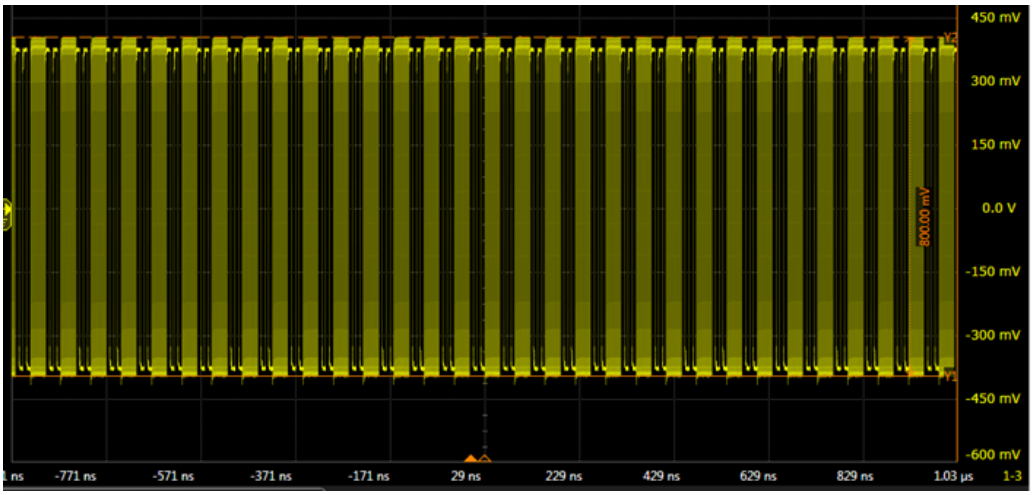

Fig. 4.4 Amplitude Calibration

- Calibrate Amplitude to 800 mV at Preset 4 (Emphasis OFF).
- Change to Preset 5 (or Preset 6) and calibrate Pre-shoot.
- Calibrate Amplitude so Vd becomes 800 mV. (Refer to Fig4.5 for Vd)

4.3 Preset

With Emphasis set to ON, the De-emphasis Pre-shoot values are adjusted using the standards and calculation methods in Table 4.1 and Fig. 4.5.

Table 4.1 Tx Preset Ratios and Corresponding Coefficient Values

Preset #	Preshoot (dB)	De-emphasis (dB)	c-1	c+1	Va/Vd	Vb/Vd	Vc/Vd
P4	0.0	0.0	0.000	0.000	1.000	1.000	1.000
P1	0.0	-3.5 ± 1 dB	0.000	-0.167	1.000	0.668	0.668
P0	0.0	-6.0 ± 1.5 dB	0.000	-0.250	1.000	0.500	0.500
P9	3.5 ± 1 dB	0.0	-0.166	0.000	0.668	0.668	1.000
P8	3.5 ± 1 dB	-3.5 ± 1 dB	-0.125	-0.125	0.750	0.500	0.750
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB	-0.100	-0.200	0.800	0.400	0.600
P5	1.9 ± 1 dB	0.0	-0.100	0.000	0.800	0.800	1.000
P6	2.5 ± 1 dB	0.0	-0.125	0.000	0.750	0.750	1.000
P3	0.0	-2.5 ± 1 dB	0.000	-0.125	1.000	0.750	0.750
P2	0.0	-4.4 ± 1.5 dB	0.000	-0.200	1.000	0.600	0.600
P10	0.0	Note 2.	0.000	Note 2.	1.000	Note 2.	Note 2.

Notes:

1. Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.
2. P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

Fig. 4.5 De-emphasis and Preshoot

When measuring the De-emphasis and Preshoot, the real-time oscilloscope is set to Average of 16 points and Horizontal Scale of 1 ns/div.

4.4 SJ (Sinusoidal Jitter)

SJ calibration uses the Compliance Pattern at the PPG and inputs the data captured by the real-time oscilloscope to SigTest. Adjustment is performed so that the value calculated by SigTest becomes 100 MHz 0.1 UIp-p (6.25 ps p-p). When capturing data at the real-time oscilloscope, the Horizontal Scale is set to 10 µs/div and Averaging is set to OFF.

The procedure for achieving the target first uses the real-time oscilloscope to capture the waveform with SJ set to 0 mUI and then the mean value of five TJ settings is calculated by SigTest. The SJ is set to 100 mUI and the mean of five settings is calculated by SigTest in the same way and SJ is adjusted so the difference becomes 6.25 ps p-p.

4.5 RJ (Random Jitter)

To eliminate the effect of Pattern Dependent Jitter generated by the PPG, RJ calibration uses a 0101… Clock pattern. RJ calibration targets a value of 0.228 UIp-p (1 ps rms) using a 10 MHz HPF; the data captured by the real-time oscilloscope is input to SigTest for adjustment. Data capture and SigTest calculation are performed five times and calibration is completed when the mean value becomes 0.228 UIp-p (1 ps rms).
When using the real-time oscilloscope to capture data for input to SigTest, the Horizontal Scale is set to 10 µs/div and Averaging is set to Off.

4.6 DMI (Differential Mode Interference)

DM calibration sets the PPG output to OFF and adjusts DM using the real-time oscilloscope so that it becomes 14 mVp-p at 2.1 GHz. Set the real-time oscilloscope bandwidth to 8 GHz only when measuring DM.

4.7 EH/EW (Eye Height/Eye Width)

Finally, calibration is completed by adjusting EH/EW. The Compliance Pattern is set at the PPG and all the previously adjusted SJ, RJ, DM, and Preset (Emphasis) are set to ON. There are Preset values of 0 to 10, any one of which must be set to meet the EH/EW standard. PCIe Workshop #102 recommends using either Preset 5 or Preset 6. This waveform is captured for input to SigTest with the real-time oscilloscope Averaging set to OFF, Horizontal Scale set to 10 µs/div, and the bandwidth set to 25 GHz. The SJ and DM are adjusted while observing the SigTest results to achieve the target EH (13.5 to 16.5 mV)/EW (18.25 to 19.25 ps). The final result is the mean of five measurements with SigTest.

5. Link Training

After completing calibration, the measurement system is connected as shown in Figs. 3.2 and 3.4 and the Rx Stress Test is started.
PCIe devices have a state machine called the Link Training State Status Machine (LTSSM).

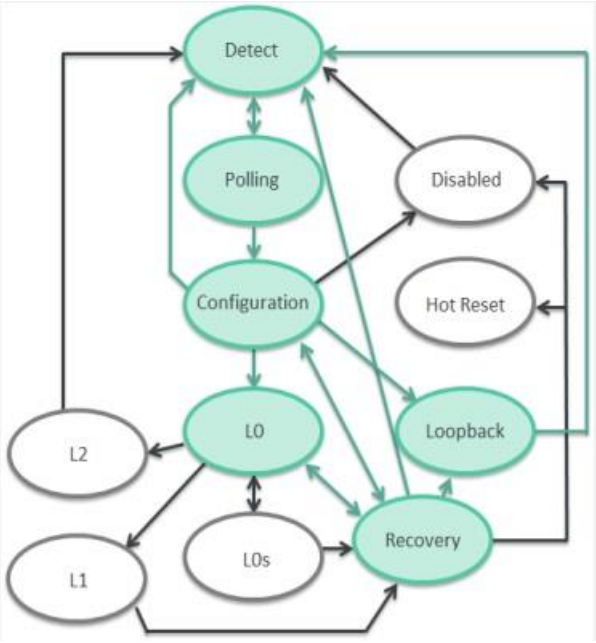

Fig. 5.1 LTSSM

At the Rx Stress test, the device state must transition from the initial Detect state to the Loopback state. There are two methods for transitioning to the Loopback state: from Detect→Polling→Configuration to Loopback, and from Detect→Polling→Configuration via L0→Recovery to Loopback.
In the former method, after establishing a Gen 1 (2.5 GT/s) link between the DUT and measuring instrument, the state immediately transitions to a 16 GT/s link. The Preset value at this time uses previously determined fixed values for the DUT and measuring instrument. Conversely, in the latter method, the link transitions to Gen 4 at 16 GT/s after establishing the initial link at Gen 1 at 2.5 GT/s and then transitioning via Gen 3 at 8 GT/s. Moreover, at this time, the optimum Loopback condition can be established by specifying the best Preset value for the DUT for compatibility between the DUT and measuring instrument. Link Training at the Recovery route method is called the LEQ Test (Link Equalization Test).
Testing at the Gen 4 Workshop found that establishing the Loopback state using Link Training is costly in terms of time. As a result, the rest of this section introduces various methods for resolving problems faced by Link Training.
Anritsu provides a PCIe Link Training MX183000A-PL021 software package for use with the MP1900A at PCIe testing. This software can be used to easily debug the DUT transition to the Loopback state as well as for debugging at BER measurement and Link Training.
As shown in Fig. 5.2, the MX183000A software is started from the MP1900A boot screen, PCIe Link Training is selected, and the [Start] button is pressed to display the Module selection screen shown in the figure on the right for searching for the module installed in the MP1900A main unit at Search Start. Pressing the [Connect] button when the module is found starts the software.

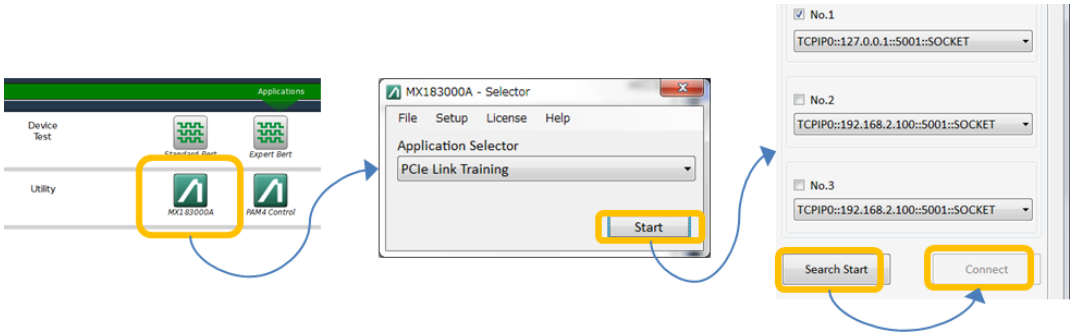

Fig. 5.2 Running MX183000A PL-021

Link Training is started by clicking the [Link Training] tab after the MX183000A software starts and then pressing the [Reset] button on the CBB to reset the DUT and then clicking the [Link Start] button on the MX183000A.

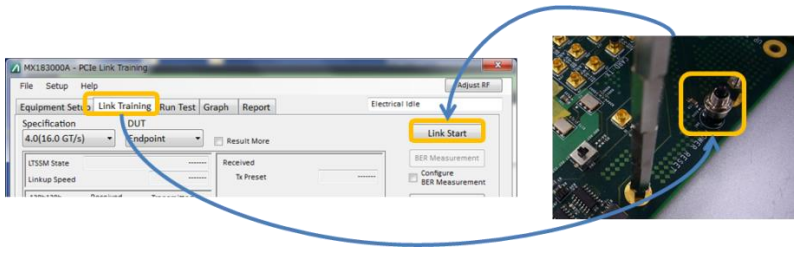

Fig. 5.3 Start Link Training

Some countermeasures are described below if the Loopback status is not entered or if BER measurement is impossible because Sync Loss occurs after transitioning to the Loopback state, or if an error occurs.

5.1 Not Entering Loopback State

Clicking the [Link Start] button on the [Link Training] tab of the MX183000A software displays the current Link status called the LTSSM State shown in the yellow boxes in the following figures. When Loopback.Active. Lead is displayed as shown on the left side of Fig. 5.4, it means the link has been established successfully and the Loopback state has been entered. When link establishment is unsuccessful, Detect.Quiet is displayed as shown on the right side of the figure instead of Loopback.Active. Lead.

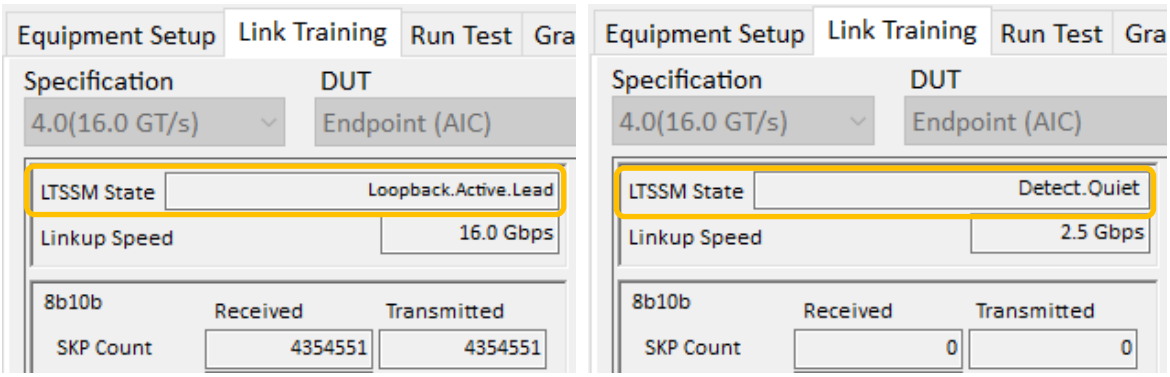

Fig. 5.4 LTSSM State Indication

When the link is not established successfully, it can be confirmed by clicking the [LTSSM Log] button on the same [Link Training] tab.

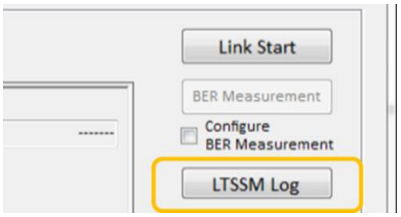

Fig. 5.5 LTSSM Log Button

Figure 5.6 shows successful and failed LTSSM Log examples.

Time[ns]	Delta Time[ns]	State	Speed[GT/s]
8386394516	2860	RECOVERY_RCVR_CFG_TS2	8
8386397376	628	RECOVERY_IDLE	8
8386398004	12	L0	8
8386398016	3412	RECOVERY_RCVR_LOCK	8
8386401428	7367432	RECOVERY_RCVR_CFG_EQTS2	8
8393768860	100016	RECOVERY_SPEED	8
8393868876	32	RECOVERY_SPEED	16
8393868908	4	RECOVERY_RCVR_LOCK	16
8393868912	2011620	RECOVERY_EQUALIZATION_PHASE0	16
8395880532	8	RECOVERY_EQUALIZATION_PHASE0	16
8395880540	1656	RECOVERY_EQUALIZATION_PHASE1	16
8395882196	272	RECOVERY_EQUALIZATION_PHASE2	16
8395882468	1999728	RECOVERY_EQUALIZATION_PHASE2	16
8397882196	1660	RECOVERY_EQUALIZATION_PHASE2	16
8397883856	2000000	RECOVERY_EQUALIZATION_PHASE2	16
8399883856	1684	RECOVERY_EQUALIZATION_PHASE3	16
8399885540	4	RECOVERY_EQUALIZATION_PHASE3	16
8399885544	860396	RECOVERY_EQUALIZATION_PHASE3	16
8400745940	4	RECOVERY_EQUALIZATION_PHASE3	16
8400745944	1507648	RECOVERY_EQUALIZATION_PHASE3	16
8402253592	64	RECOVERY_RCVR_LOCK	16
8402253656	1760	RECOVERY_RCVR_CFG_TS2	16
8402255416	2304	LOOPBACK_ENTRY_LEAD_TS1	16
8402257720	0	LOOPBACK_ACTIVE_LEAD	16

Time[ns]	Delta Time[ns]	State	Speed[GT/s]
435449548		8 DETECT_ACTIVE	2.5
435449556	1245344	POLLING_ACTIVE_TS1	2.5
447902980	4800000	POLLING_CONFIGURATION	2.5
495902980		8 INITIAL	2.5
495902988	1200000	DETECT_QUIET	2.5
507902988		8 DETECT_ACTIVE	2.5
507902996	1244972	POLLING_ACTIVE_TS1	2.5
520352788	4800000	POLLING_CONFIGURATION	2.5
568352788		8 INITIAL	2.5
568352796	1200000	DETECT_QUIET	2.5
580352796		8 DETECT_ACTIVE	2.5
580352804	1246520	POLLING_ACTIVE_TS1	2.5
592818064	4800000	POLLING_CONFIGURATION	2.5
640818064		8 INITIAL	2.5
640818072	1200000	DETECT_QUIET	2.5
652818072		8 DETECT_ACTIVE	2.5
652818080	1245134	POLLING_ACTIVE_TS1	2.5
665269464	4800000	POLLING_CONFIGURATION	2.5
713269464		8 INITIAL	2.5
713269472	1200000	DETECT_QUIET	2.5
725269472		8 DETECT_ACTIVE	2.5
725269480	1244936	POLLING_ACTIVE_TS1	2.5
737718796	4800000	POLLING_CONFIGURATION	2.5
785718796		8 INITIAL	2.5
785718804	1200000	DETECT_QUIET	2.5
797718804		8 DETECT_ACTIVE	2.5
797718812	1246464	POLLING_ACTIVE_TS1	2.5
810183436	4800000	POLLING_CONFIGURATION	2.5

Fig. 5.6 LTSSM Log Examples

When the link is established successfully, LOOPBACK_ACTIVE_LEAD is displayed at the last line of the Status column as shown on the left. When the link is not established successfully, DETECT and the POLLING State are displayed repeatedly as shown on the right. At link failure, there may be other conditions. The following explains some troubleshooting for resolving typical failures to enter the Loopback state.

5.1.1 Repeating at 2.5 GT/s

First, this occurs when DETECT and POLLING occur repeatedly while the link speed remains at 2.5 GT/s. In this case, check the measurement system connections, taking particular care that there is no mistake in the positive and negative polarities and Trace Pair numbering; also confirm that the power supply voltage to the DUT is sufficient. Moreover, since there is a possibility that the DUT internal LTSSM is in an abnormal condition, toggle the power supply off and on and press the [Reset] button on the CBB.

70685952	2000464	INITIAL	8
70685968	16	DETECT_QUITE	8
79337088	8651120	DETECT_QUITE	2.5
82685968	3348880	DETECT_ACTIVE	2.5
82685984	16	POLLING_ACTIVE_TS1	2.5
106685984	24000000	INITIAL	2.5
106686000	16	DETECT_QUITE	2.5
118686000	12000000	DETECT_ACTIVE	2.5
118686016	16	POLLING_ACTIVE_TS1	2.5
142686016	24000000	INITIAL	2.5
142686032	16	DETECT_QUITE	2.5
154686032	12000000	DETECT_ACTIVE	2.5
154686048	16	POLLING_ACTIVE_TS1	2.5
178686048	24000000	INITIAL	2.5
178686064	16	DETECT_QUITE	2.5
190686064	12000000	DETECT_ACTIVE	2.5
190686080	16	POLLING_ACTIVE_TS1	2.5
214686080	24000000	INITIAL	2.5
214686096	16	DETECT_QUITE	2.5
226686096	12000000	DETECT_ACTIVE	2.5
226686112	16	POLLING_ACTIVE_TS1	2.5
250686112	24000000	INITIAL	2.5

Fig. 5.7 Repeating at 2.5 GT/s

5.1.2 Timeout After Changing Link Speed

Sometimes, after the link speed transitions from 2.5 GT/s to either 8 GT/s or 16 GT/s, the speed returns repeatedly to 2.5 GT/s in the RECOVERY_EQUALIZATION_PHASE1 State.

0	13,592	INITIAL	16
13,592	12,000,000	DETECT_QUITE	16
766,776	16	DETECT_ACTIVE	2.5
766,792	8,650,760	POLLING_ACTIVE_TS1	2.5
8,664,352	3,349,240	DETECT_QUITE	2.5
12,013,592	16	DETECT_ACTIVE	2.5
12,013,608	24,000,000	POLLING_ACTIVE_TS1	2.5
24,766,792	16	INITIAL	2.5
24,766,808	24,000,000	DETECT_QUITE	2.5
36,013,608	16	INITIAL	2.5
36,013,624	12,000,000	DETECT_QUITE	2.5
36,766,808	16	DETECT_ACTIVE	2.5
36,766,824	66,000	POLLING_ACTIVE_TS1	2.5
36,832,824	1,352	POLLING_CONFIGURATION	2.5
36,834,176	3,368	CONFIGURATION_LINKWIDTH_START	2.5
36,837,544	128	CONFIGURATION_LINKWIDTH_ACCEPT	2.5
36,837,672	3,408	CONFIGURATIONS_LANE_WAIT	2.5
36,841,080	128	CONFIGURATIONS_LANE_ACCEPT	2.5
36,841,208	4,256	CONFIGURATION_COMPLETE	2.5
36,845,464	4,672	CONFIGURATION_IDLE	2.5
36,850,136	24	L0	2.5
36,850,160	4,008	RECOVERY_RCVR_LOCK	2.5
36,854,168	2,392	RECOVERY_RCVR_CFG_EQTS2	2.5
36,856,560	8,534,400	RECOVERY_SPEED	2.5
45,390,960	465,600	RECOVERY_SPEED	8
45,856,560	8	RECOVERY_RCVR_LOCK	8
45,856,568	12,000,000	RECOVERY_EQUALIZATION_PHASE1	8
48,013,624	16	DETECT_ACTIVE	2.5

Fig. 5.8 Timeout after Changing Link Speed

After the link speed has changed at RECOVERY_EQUALIZATION_PHASE1, negotiation is executed between the DUT and measuring instrument at the selected best Preset value. If this negotiation fails, the link returns to the initial state. Consequently, the test methods are to either check whether the link is successful after disconnecting the ISI Channel from the measurement system, or to change by changing the Preset value. For Gen 4, we recommend using Preset 5, 6, 8, or 9 as the best values.

5.1.3 Timeout at CONFIGURATION_COMPLETE

If a timeout occurs in the Configuration Complete state, the Data Rate Identifier negotiation has probably failed. Check the contents of the Data Rate Identifier generated by the DUT.

3,348,848	DETECT_QUITE	2.5
16	DETECT_ACTIVE	2.5
66,000	POLLING_ACTIVE_TS1	2.5
1,352	POLLING_CONFIGURATION	2.5
3,584	CONFIGURATION_LINKWIDTH_START	2.5
128	CONFIGURATION_LINKWIDTH_ACCEPT	2.5
3,648	CONFIGURATIONS_LANE_WAIT	2.5
128	CONFIGURATIONS_LANE_ACCEPT	2.5
2,000,000	CONFIGURATION_COMPLETE	2.5
16	INITIAL	2.5
16	DETECT_QUITE	2.5

Fig. 5.9 Timeout at CONFIGURATION_COMPLETE

5.1.4 Timeout at LOOPBACK_ENTRY_LEAD_TS1

LOOPBACK_ENTRY_LEAD_TS1 is the state in which the transition to the next link speed is confirmed after the final negotiation. In this case, there is a possibility that the measuring instrument has not been able to receive the Training Sequence (TS) normally.

8399883856	1684	RECOVERY_EQUALIZATION_PHASE3	16
8399885540	4	RECOVERY_EQUALIZATION_PHASE3	16
8399885544	860396	RECOVERY_EQUALIZATION_PHASE3	16
8400745940	4	RECOVERY_EQUALIZATION_PHASE3	16
8400745944	1507648	RECOVERY_EQUALIZATION_PHASE3	16
8402253592	64	RECOVERY_RCVR_LOCK	16
8402253656	1760	RECOVERY_RCVR_CFG_TS2	16
8402255416	2304	LOOPBACK_ENTRY_LEAD_TS1	16
8402257720	2000000	LOOPBACK_EXIT_LEAD	16
8404257720	16	INITIAL	16
8404257736	16	DETECT QUITE	2.5

Fig. 5.10 Timeout at LOOPBACK_ENTRY_LEAD

Consequently, there is a method of specifying the Preset value issued by the DUT from the measuring instrument. Pressing [Option] at the [Link Training] tab to open the Option screen and changing TS1 to EQTS1 at the Loopback Entry item at the [State Machine] tab specifies the TS Preset issued by the DUT from the measuring-instrument side. The TS Preset value executes the Preset items (DE, PS [dB]) for the [Link EQ] tab in the same Option window. There are Upstream and Downstream Preset settings, but when the DUT is System, setting changes to the Downstream side; when the DUT is AIC, setting changes to the Upstream side.

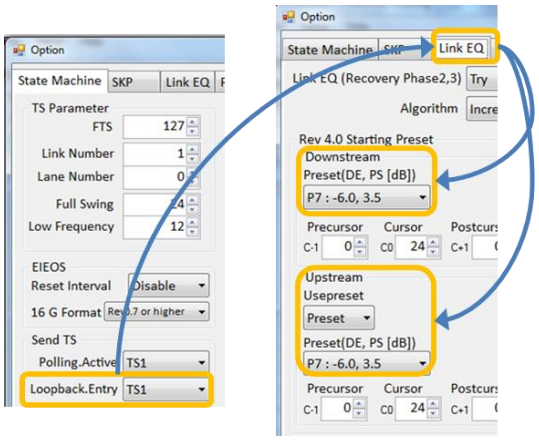

Fig. 5.11 Loopback Entry Preset Setting

At a timeout at LOOPBACK_ENTRY_LEAD_TS1, if the status does not transition to the Loopback state even after changing the Preset, the MX183000A has a debug function for forcing a transition to Loopback_Active. Selecting Loopback_Active from the [Timeout to] item at the [State Machine] tab in the Option screen forces a transition to the Loopback state when a timeout occurs at Loopback Entry. This makes it possible to progress to BER, Jitter Tolerance, and other tests.

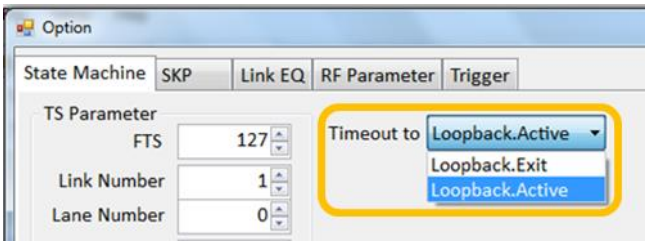

Fig. 5.12 Loopback Active Debugging Function

5.1.5 Trigger Function

When the transition to the Loopback state does not occur even when changing parameters during Link Training, sometimes it is a good idea to check the transition timing for each state. At state transitions, the responding side must return the response within a fixed time. If there is no response from the opposite partner within the fixed time, the side waiting for the response recognizes a timeout and restarts negotiation. Depending on the device, a timeout evaluation may be issued earlier than specified without the device waiting for the specified fixed time. For example, when transitioning to some condition, irrespective of whether the specified waiting time for the response from the opposite partner is 24 ms, some devices may issue a timeout evaluation even when there is no response after waiting about 2 ms shorter than this. These devices can be thought of as establishing a link 2 ms earlier than the response from the partner. However, the opposite partner does not link normally even if replying within the 24 ms because the 2 ms longer response is evaluated as a timeout. When devices that cannot clarify these states appear, there is a possibility of "poor compatibility" connections occurring between target devices.

The MX183000A has a function for issuing triggers after a fixed time in each state to help confirm these types of timings. LTSSM is selected at the [Trigger] item in the [Trigger] tab of the Option screen. Selecting the state and link speed to be monitored generates a trigger at this timing from the AUX Output of the MU195020A SI-PPG.

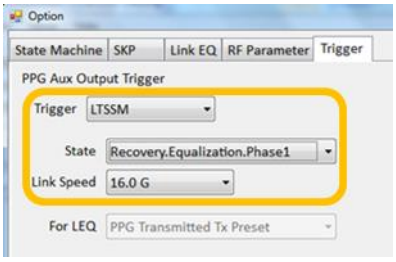

Fig. 5.13 LTSSM Trigger

The connections when measuring timings using LTSSM Trigger are shown below. This measurement system and triggering can be used to analyze the details of the transition timings in each DUT state.

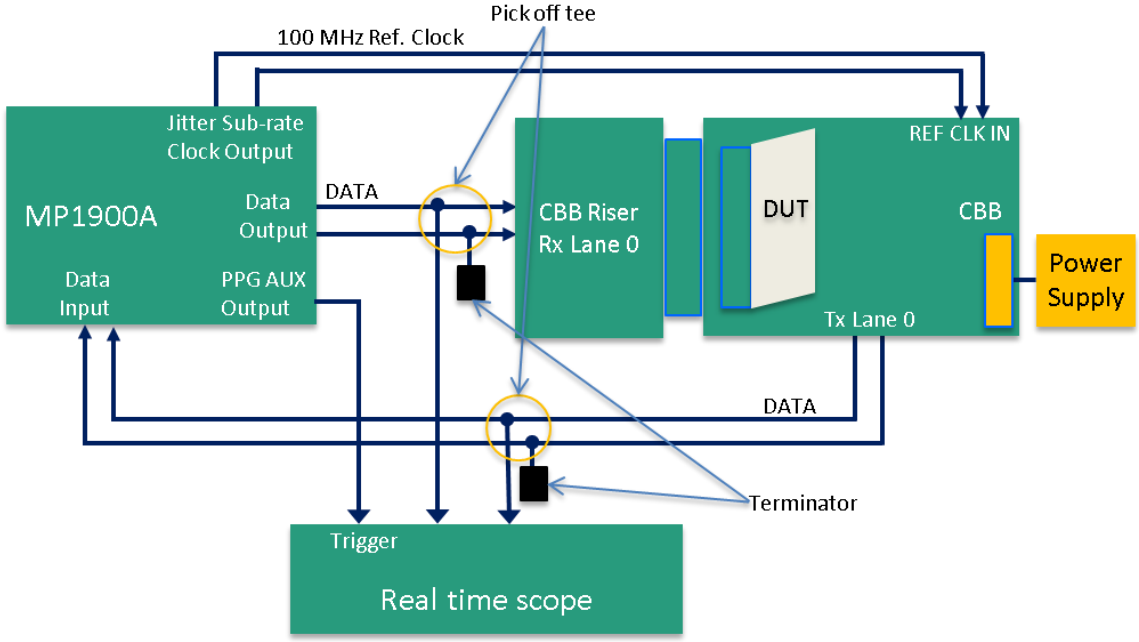

Fig. 5.14 LTSSM Timing Measurement Connection

5.1.6 Others

The Gen 4 base specification is changing the EIEOS handling between Revision 0.5 and Revision 0.7. Clicking the [Option] button in the [Link Training MX183000A] tab enables confirmation that the EIEOS revision setting matches the DUT revision setting. Operation will not be normal if these do not match.
However, if linking is unsuccessful at the Recovery route, it is also possible to confirm the configuration using Configuration route instead of Recovery route. BER and Jitter Tolerance measurements are also supported even when transitioning to the Loopback state using the Configuration route.

5.2 Loopback State with Sync Loss

This section describes methods for resolving problems when BER measurements are impossible at Sync Loss when pattern synchronization is not established even at transition to the Loopback state. Clicking the [BER Measurement] button in the [Link Training] tab displays the BER Measurement screen. If the Sync Loss LED at the bottom-left of this screen is flashing red, Sync Loss has occurred.
If there is no Sync Loss or errors, Go/No Go testing can be executed at the next stage. Clicking the [BER Measurement] button opens the Measurement screen shown below. The DUT passes the PCIe Gen 4 Rx Stress Test requirements when there is one or fewer errors during a 63-second period.

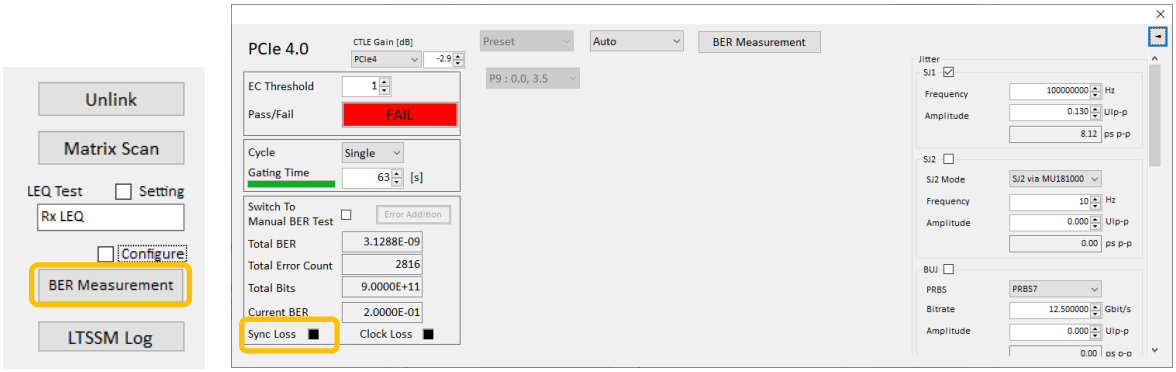

Fig. 5.15 Sync Loss Indication

5.2.1 Tx/Rx Sync Loss Parameter Setting

Internal parameters are changed by clicking [Option] at the bottom-right of the [Link Training] tab.

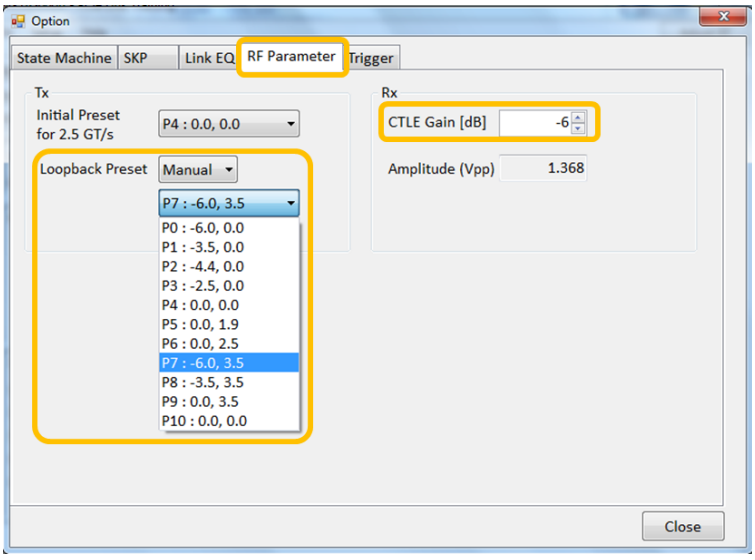

Fig. 5.16 Sync Loss Parameters

There are two parameters in the [RF Parameter] tab: CTLE Gain, and Loopback Preset. Set CTLE Gain to 0 dB when the trace from the DUT to the ED produces an open Eye for a short input signal. CTLE is a function for

re-opening a closed Eye caused by an input signal suffering from channel loss, but sometimes BER measurement may still be impossible if the signal is excessively filtered or the loss of the signal itself is excessively large. The MP1900A ED can set the CTLE Gain parameter from 0 to –12 dB to open the Eye and make it easier to measure.
Loopback Preset is a function for changing the Preset of signals generated from the MP1900A after the transition to the Loopback state.
Changing Loopback Preset in the [RF Parameter] tab to Manual makes it possible to change the Preset value. Changing this parameter allows the DUT to receive the MP1900A signal normally after passage through the channel to confirm whether the Loopback state can be entered normally or not. Since the Preset item in the [Link Training] tab at the top-right of the BER Measurement screen can be changed in the same manner, the Sync Loss status can be confirmed while changing the Preset value.

5.2.2 Sync Loss Parameters for Separate Clocking

When the DUT and measuring instrument are each using independent reference clocks, there are small differences in the operating frequencies at the DUT and measuring instrument. PCIe devices can usually accommodate these small operating frequency differences using the internal FIFO and SKP ordered set functions. Since the operating frequencies are identical between devices when using Common Clock, there is no impact on operation even when changing parameters explained in this section.

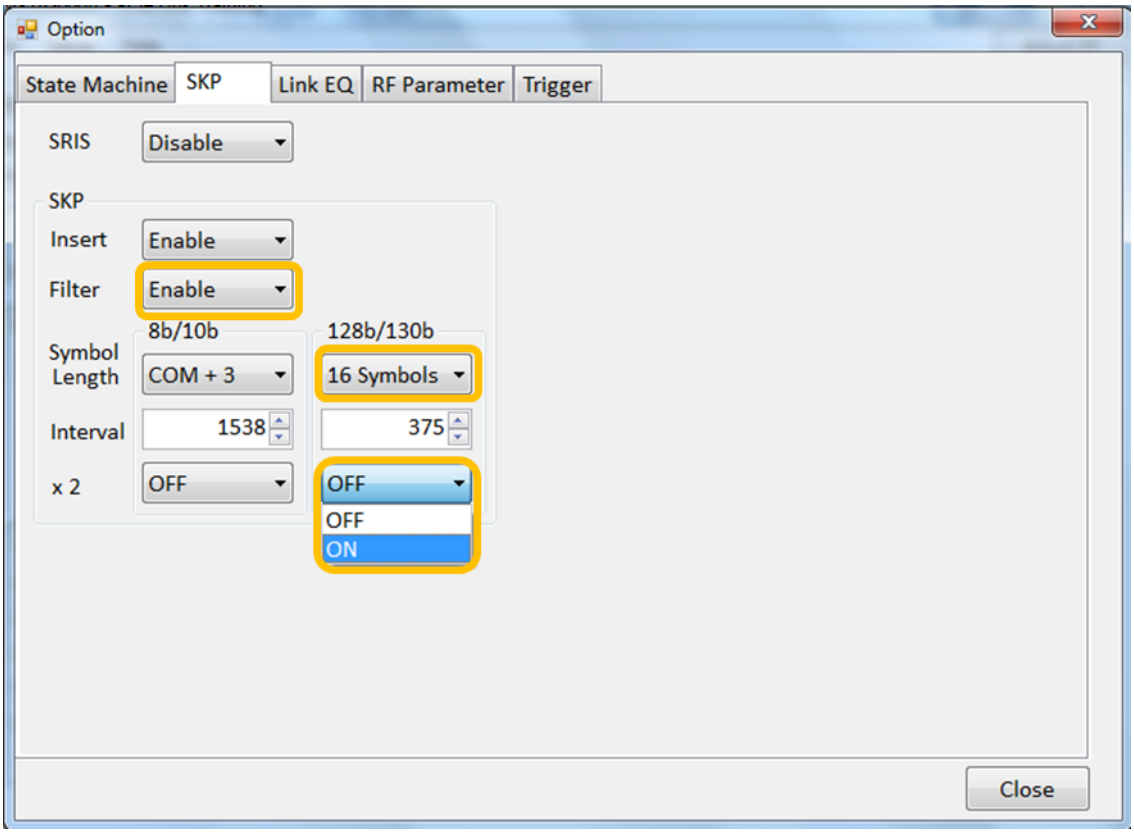

Fig 5.17 Sync Loss Parameters for Separate Clocking

Enabling SKP Filter at the [SKP] tab in the Option screen removes the SKP ordered set from the BER count target. Since the SKP ordered set function accommodates differences in the operating frequency, setting Filter to Enable excludes it as a BER measurement target, because it has no meaning for the communication itself. SKP ordered set is included in the data handled between devices and increasing this SKP can be used to make adjustments ensuring that the FIFO never becomes full or empty. Sync Loss can be caused by differences in device operating frequencies that the SKP and FIFO in devices are unable to accommodate. When the standard

SKP is unable to handle differences in operating frequency, the MX183000A can generate SKP twice consecutively to increase the SKP Symbol length. Generating many SKPs can reduce data stored in the FIFO to accommodate the difference in operating frequency and suppress Sync Loss occurrence.

5.3 Loopback State with Errors

This last section describes countermeasures when errors occur in the Loopback state preventing BER measurement.
Re-adjusting CTLE Gain and the Loopback Preset value as described in section 5.2.1 can prevent error occurrence. If errors still occur, set the SJ, RJ, and DM stress tests to off one-by-one or reduce the values as necessary until the error-free point is found. If the errors disappear in the stress-free state or when the values are smaller than the specification, it may be necessary to increase the device stress tolerance.

6. Summary

This Application Note describes the PCIe Gen 4 Rx Stress Test and troubleshooting methods, which are the focus of the current PCIe Workshop, using the MP1900A. The PCIe Gen 4 and PCIe Workshop test methods are yet to be fully established and Anritsu is continuing with work to understand trends at future Workshops and help provide customers and the business world with timely measurement solutions.

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