

-Anritsu Automotive Solution-PCIe® Receiver Test by MP1900A series

Signal Quality Analyzer-R MP1900A Series



Automotive market trend

Automated Driving

ADAS / Collision avoidance → Full autonomous driving / Upgrades via OTA Infotainment

Features for Luxury car \rightarrow General options for poplar cars and more features



- Real time processing / reliable system
- High quality / stress free experience
- Harsh environment tolerance such as high/low temperature, vibration etc....

➔ Automotive :

Data Center class computing power and Home theater complexity

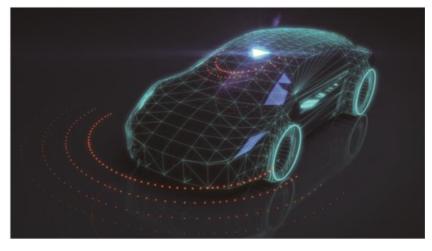
What is required for automotive

Data Center class computing power and Home theater complexity More reliability

Fault tolerance with enough margin **More bandwidth**



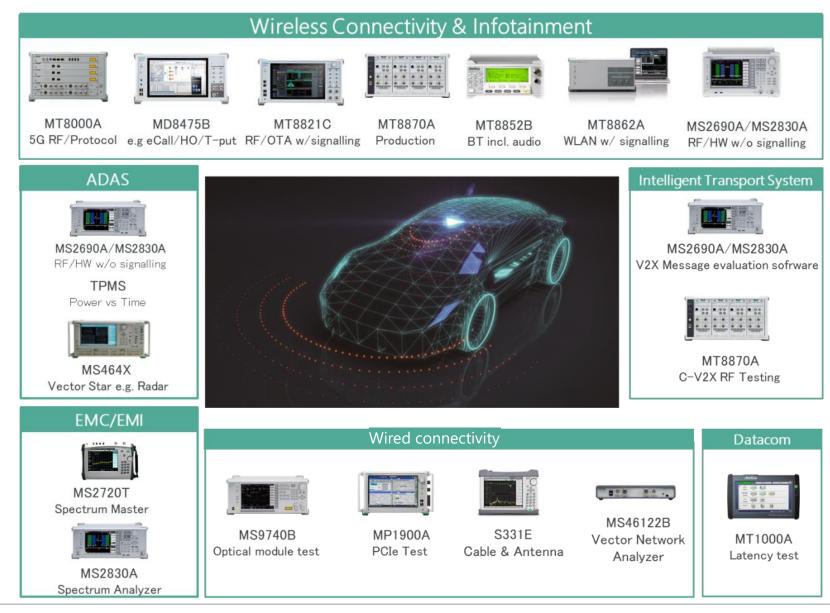
Higher bandwidth architecture



PCI Express features

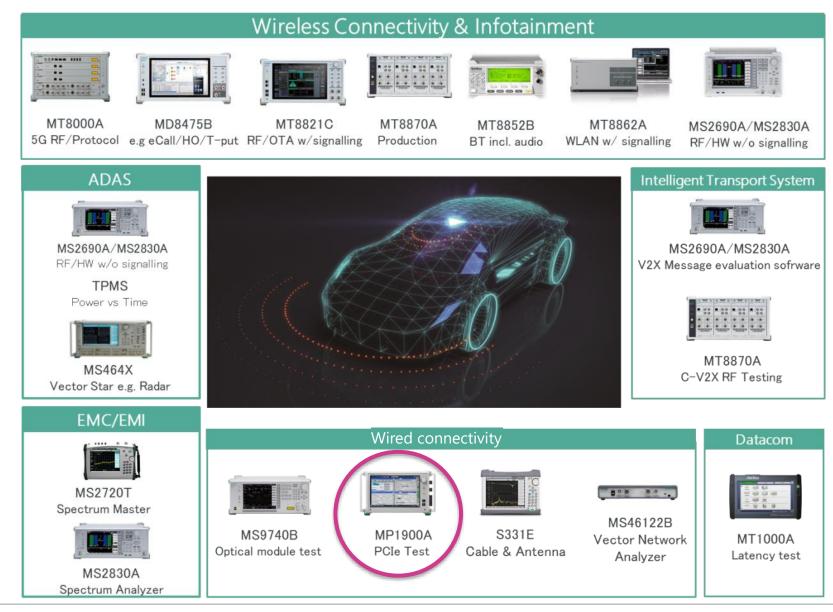
- Fault tolerance by multiple error correction system architecture
- Secured interoperability among vendors
- High bandwidth by generations (Gen3 to Gen5) and bus width (16 lanes)

Anritsu automotive solutions



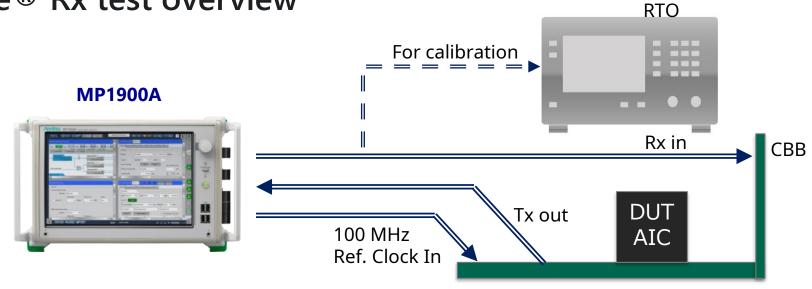
Annitsu envision : ensure

Anritsu automotive solutions



Anritsu envision : ensure

PCle[®] Rx test overview



CBB

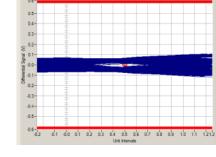
Model	Name	Option	Qty	Remark
MP1900A	Signal Quality Analyzer-R	-	1	
MU181000B	12.5GHz 4port Synthesizer	002	1	
MU181500B	Jitter Modulation Source	-	1	
MU195020A	21G/32G bit/s SI PPG	010, 011	1	Add Opt-001 for expansion to
MU195040A	21G/32G bit/s SI ED	010, 011, 022	1	Gen5 (32 GT/s)
MU195050A	Noise Generator	-	1	
MX183000A-PL001	Jitter Tolerance Test	-	1	Optional
MX183000A-PL021	PCIe Link Training	-	1	Mandatory

PCIe® Rx test overview - test procedure -

Steps of Receiver Testing

Step1: Calibration

- Channel Loss by VNA
- Eye Amplitude, Preset, SJ and RJ by BERT and RTO
- DM-I and Eye Height/Eye Width by BERT and RTO



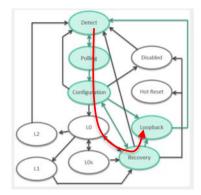
	Min	Мах
EH	13.5 mV	16.5 mV
EW	18.25 ps	19.25 ps

Step2: Link Training

- Make DUT looped-back-mode by BERT

 ->DUT is necessary success through Recovery State.
- Troubleshooting

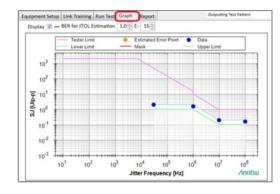
Equipment Setup	Link 1	Training	Run	Test	Grap
Specification	1	DUT			
4.0(16.0 GT/s)	Ψ	Endp	oint		P
LTSSM State		Loopba	ck.Active	.Mast	er
Linkup Speed			16	0 Gb	ps
86106	Received	1	Transmit	tted	- L
SKP Count		*******			- (
Symbol Err					



Step3: Measurement

- Checking BER <1E-12 with Stressed EYE (Mandatory)
- Jitter Tolerance Testing (Optional)



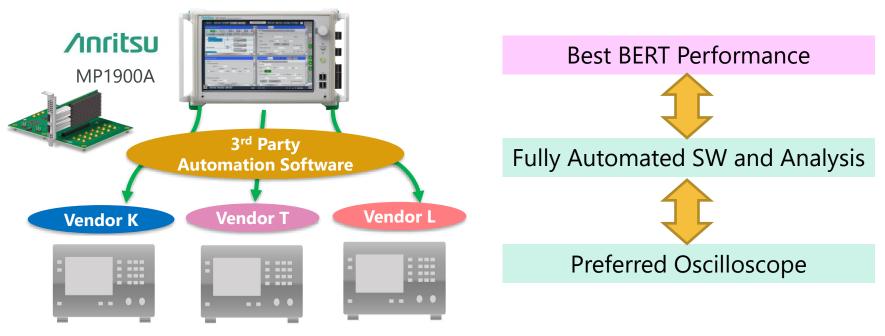


PCIe® Tx LEQ/Rx compliance test

- Combination of best-performance BERT MP1900A and preferred oscilloscope -

Shorter test times and reduced investment cost

- Supports Combination with Lecroy/Tektronix/Keysight Real-Time Oscilloscopes
- > Automated Rx CEM and Base Tests: Calibration, Link EQ and Automated Tx Test
- Protocol Aware: Link Training/Equalization and LTSSM Analysis
- ➢ High Expandability 32G Multichannel BERT for PCIe[®]1 to 5 and 6!



Customers' Real-Time Oscilloscope

PCIe® solution for automated driving / Infotainment

To secure more reliability and more bandwidth

- AAA) Seamless support for entire debugging phase
- BBB) Easy and deeper debugging method
- CCC) Certified by industry
- DDD) Evolving technology support

AAA) Seamless support for entire debugging phase

	Troubleshooting Example	Protocol Analyzer	SCOPE	BERT
1	Rx Test troubleshooting analysis		-	$\sqrt{\sqrt{1}}$
2	2.5 GT/s Link failure	-	\checkmark	$\sqrt{}$
3	Speed change failure	\checkmark	\checkmark	$\sqrt{\sqrt{1}}$
4	Loopback failure	-	\checkmark	$\sqrt{}$
5	Never Becomes Error-Free	-	\checkmark	$\sqrt{}$
6	Debug Example using Scope at Tx Link EQ Test	-	$\sqrt{\sqrt{1}}$	
7	PCI Express – Incorrect Tx EQ Cursor Value	$\sqrt{}$	-	\checkmark
8	Debug Example using Scope – Signal Integrity Problems	-	$\sqrt{}$	-
9	PCI Express – Analysis Focusing on Flow Control	$\sqrt{}$	-	-
		Lecroy	L/T/K	Anritsu

 $\sqrt{\sqrt{2}}$: Main instrument for troubleshooting

- $\sqrt{1}$: Measuring instrument for analysis from different viewpoint
- : Difficult to troubleshoot or no appropriate instrument



We can cover all of those troubleshooting with our partners

BBB) Easy and deeper debugging method – ① LTSSM log

e Setup Hel	lp						Operate M	AP1900/
uipment Setu	p Link Trainir	g Run Test G	raph Rep	ort		Electri	ical Idle	
pecification 4.0(16.0 GT/s)	⊂ DUT	point (AIC)	~	More res	ults		Link Sta	rt
LTSSM State	Received	Transmitted	PPG Fin PPG Fin	al Preset al Cursor Pre-Cursor	[]	 Post-Cursor		Setting
Current RD Err Symbol Lock			Link, Lane		ency		LTSSM Loopback Meth	
128b130b	Received	Transmitted	Recovery.E				Configuration	¥
SKP Count			Phase0	PCIe 3	PCIe 4	PCIe 5	Test Pattern	
TS1/TS2 Symbol1	4-15 DC Balance		(Root)				Compliance	~
			Phase1	******	******		Compliance	Ť
Sync Header Err			Phase2		******	******	MCP	×
TS1 OS Parity Err			Phase3	*******	******	*******		
Block Lock							Timeou	it
EIEOS Counter							Option	

- The MP1900A Training Log Viewer shows the actual Training State transition logs.
- The state transition path (route) and transition times can be analyzed in detail.

# [na]	A Time [na]	State	3peed(GT/s)	Detect Preset	Breef Count	Use Preset	Preset	Pre-cursor	Cureor	Post-curso
	15,568	INTERAL	16.0				-			
360	1,976,208	DETECT_QUIET	16.0			-				-
93,876	10,028,792	DETECT_QUIET	2.5						_	
015,360	16	DETECT_ACTIVE	2.5							
015,884	65,968	POLLING_ACTIVE_TES	2.5							
001,352	5,000	POLLING_CONFIGURATION	2.5							
086,422	8,482	CONFIGURATION_LINEWIDTH_START	2.5							-
089,864	128	CONFIGURATION_LINKWIDTH_ACCEPT	2.5							
089,992	3,456	CONFIGURATIONS_LANE_WAIT	2.5			_				
093,448	128	CONFIGURATIONS_LANE_ACCEPT	2.5							-
093,576	4,226	CONFIGURATION_COMPLETE	2.5							
5897,982	880	CONFIGURATION_IDLE	2.5	anary .	and the second second		0.000			
098,792	24	LO	2.5							
098,816	4,072	RECOVERY_REVR_LOCK	2.5		-		_		-	-
102,988	2,392	RECOVERY_RCVR_CFG_EQTS2	2.5							
108,280	1,866,992	RECOVERY_SPEED	2.5							-
972,272	32	RECOVERY_SPEED	6,0			_				-
\$72,804		RECOVERY_RCVR_LOCK	8.0							
972,312	5,110,640	RECOVERY_EQUALIZATION_PHASE3	6.0		2814					
090,952	6,002,400	RECOVERY_EQUALIZATION_PHASE2	8,0	0	0	0	2	a	24	
093,352	23,009,200	RECOVERY_EQUALIZATION_PHASE2	6.0	0	0	0	7	a	24	
102,552	544	RECOVERY_EQUALIZATION_PHASE3	8.0	0	0	8	· · · · · ·	a	.24	
103,096	1,792	RECOVERY_EQUALIZATION_PHASES	8.0	3	0		7	a	24	3
104,888	2,002,952	RECOVERY_EQUALIZATION_PHASEB	8.0	1	0	2	7	0	24	
107,240	1,997,648	RECOVERY_EQUALIZATION_PHASES	8.0	3	0	1			24	
104,888	2,492	RECOVERY_RCVR_LOCK	8.0							
107,820	824	RECOVERY_RCVR_CFG_T82	8,0	seen.	-		(and the			
107,944	1,928	RECOVERY_IOLE	8.0	anan .	-					
109,872	24	LD	8.0		-1000		-			
109,896	2,496	RECOVERY_ROVR_LOCK	8.0							
112,392	2,480	RECOVERY_RCVR_CFG_EQT52	8.0						_	
114,872	2,792,400	RECOVERY_SPEED	8.0						_	_
907.272	82	RECOVERY SPEED	16.0					-		
907,304		RECOVERY_REVR_LOCK	16.0		-			-	_	
907.312	4,211,792	RECOVERY EQUALIZATION PHASE1	16.0		512	_		_		
119.104	6.002,400	RECOVERY EQUALIZATION PHASE2	16.0	0	0	0	4	0	24	
121,504	28,009,200	RECOVERY EQUALIZATION PHASE2	16.0	0	0			0	24	
						1	7		24	2
130,704	528	RECOVERY_EQUALIZATION_PHASES	16.0	0	0			0		
131,232	1,008	RECOVERY_EQUALIZATION_PHASE3	16.0	1	0	1	7	0	24	¢
132,240	2,000,528	RECOVERY_EQUALIZATION_PHASER	16.0	1	0	1	7	0	24	c
132,768	1,999,472	RECOVERY_EQUALIZATION_PHASES	16.0	1	10	3	7	0	24	C

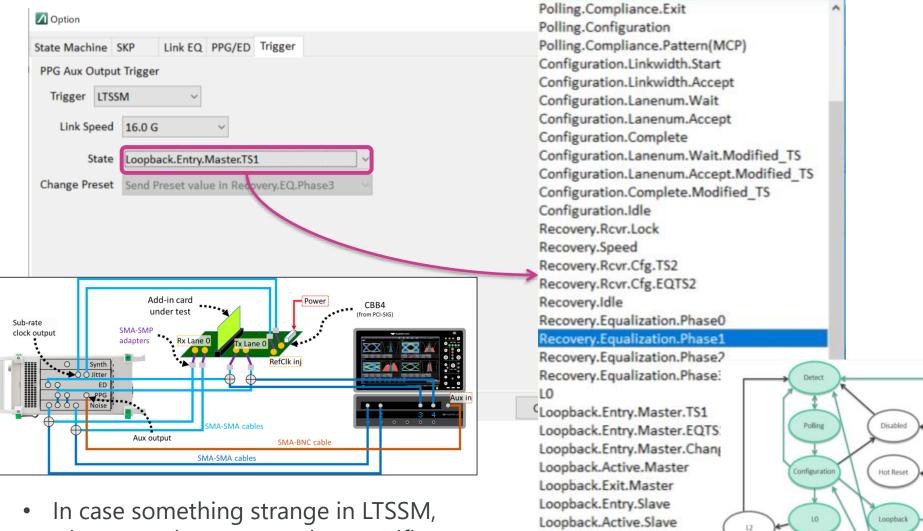
🖳 Training Log Viewer

\$2,10 \$2,11 \$2,11 \$4,90 \$4,90 \$4,90

59,11 65,12 88,11 88,11 98,11 90,11

Time [ns]	∆Time [State	Speed[GT/s]	Detect Pre
٥	٥	INITIAL	16.0	
17280	17280	DETECT_QUITE	16.0	
12017280	12000000	DETECT_ACTIVE	16.0	
12017296	16	POLLING_ACTIVE_TS1	16.0	
36017296	24000000	INITIAL	16.0	
36017312	16	DETECT_QUITE	16.0	
48017312	12000000	DETECT_ACTIVE	16.0	
48017328	16	POLLING_ACTIVE_TS1	16.0	
72017328	24000000	INITIAL	16.0	
72017344	16	DETECT_QUITE	16.0	
84017344	12000000	DETECT_ACTIVE	16.0	
84017360	16	POLLING_ACTIVE_TS1	16.0	
10801 7 360	24000000	INITIAL	16.0	

BBB) Easy and deeper debugging method – 2 LTSSM trigger



trigger can be generated at specific state to see waveform and more.

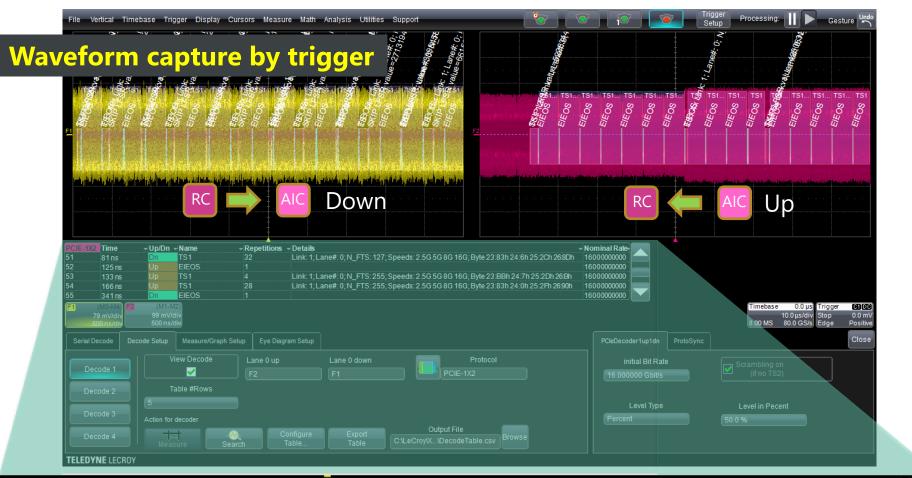
Loopback.Exit.Slave

Recovery

LOs

1.1

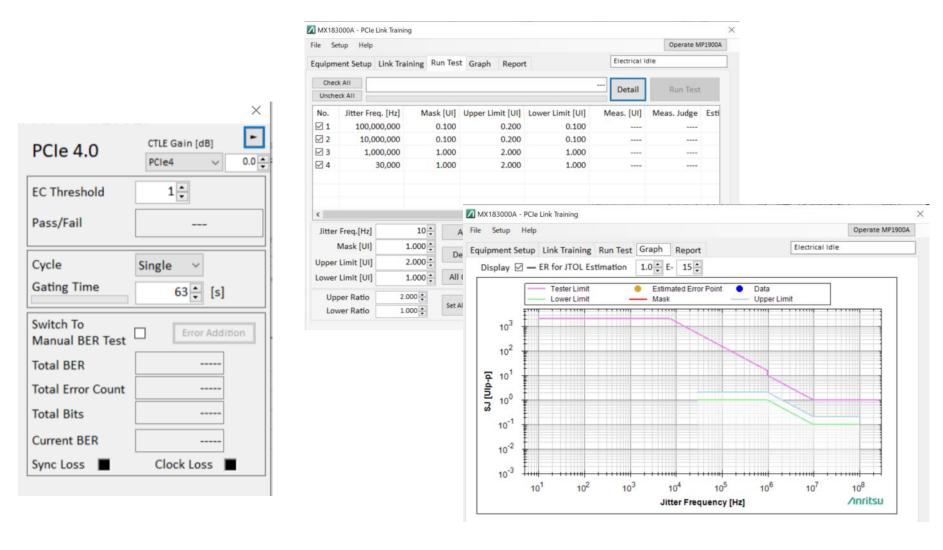
BBB) Easy and deeper debugging method – ③ Protocol decoding



PCIE	E-1X2 Time	- Up/Dn -	Name	- Repetitions	- Details	- Nominal Rate-	
51	81 ns	Dn	TS1	32	Link: 1; Lane#: 0; N_FTS: 127; Speeds: 2.5G 5G 8G 16G; Byte 23:83h 24:6h 25:2Ch 26:8Dh	1600000000	
52	125 ns	Up	EIEOS	1		1600000000	
53	133 ns	Up	TS1	4	Link: 1; Lane#: 0; N_FTS: 255; Speeds: 2.5G 5G 8G 16G; Byte 23:BBh 24:7h 25:2Dh 26:Bh	16000000000	
54	166 ns	Up	TS1	28	Link: 1; Lane#: 0; N_FTS: 255; Speeds: 2.5G 5G 8G 16G; Byte 23:83h 24:0h 25:2Fh 26:90h	16000000000	
55	341 ns	Dn	EIEOS	1		1600000000	

And protocol decoding at captured area

BBB) Easy and deeper debugging method – BER & Margin (1/2)

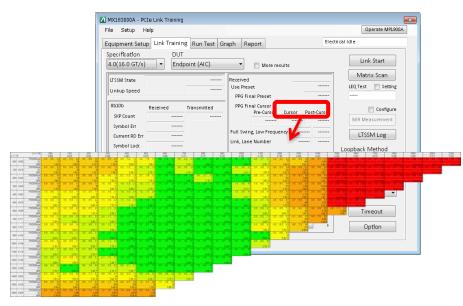


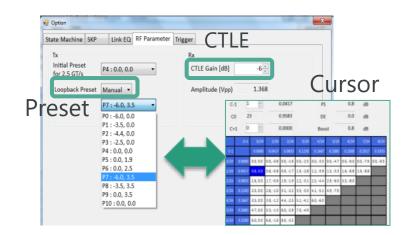
BER measurement

Jitter Tolerance Test

BBB) Easy and deeper debugging method – BER & Margin (2/2)

- Find a optimum Preset/Cursor
- Matrix Scan: Automatically find the optimum Tx EQ value.
- Manual setting Set Loopback Preset to Manual and change the preset from P0 to P10 to determine the optimum preset/Cursor at the DUT.





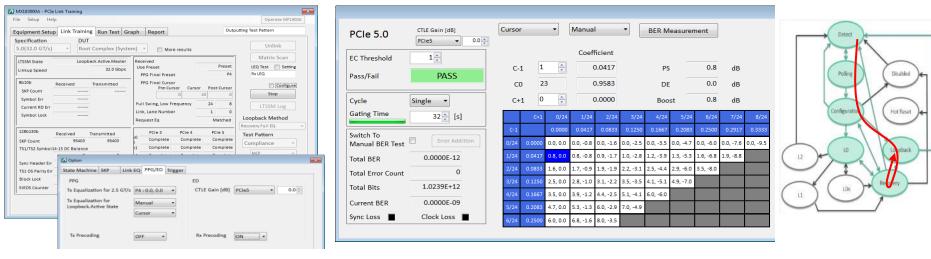
CCC) Certified by industry

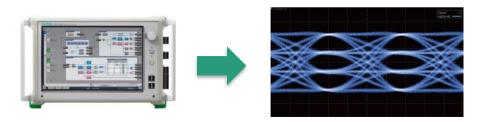
PCI Express	Gen4	Gen5	Gen6
General BERT	Released	Released	Released
Base Spec	Released	Released	In planning
CEM Spec (Link Training)	Released	Released	In planning
Compliance Testing (RX	LEQ)		
w/ Lecroy Scope	Approved as Gold	-	-
w/ Tektronix Scope	Approved as Gold	-	-
w/ Keysight Scope	Approved as Gold	-	-

DDD) Evolving technology support - Gen5 and more

Anritsu already supports newly added below Gen5 functions:

- ✓ Enhanced Link Behavior Control
- ✓ Precoding
- ✓ SKP OS/EIEOS
- ✓ MCP 5.0





And ready for next **Gen6** (32Gbaud PAM4)

Anritsu M	IP1900A Standardization Contributions
PCI SIG	G3 ApprovedG4 ApprovedG5 ReadyMP1900A PCIe-G3 and G4 solution with Lecroy RTO for Rx test was approved by PCI-SIG. Anritsu will aim to get next G5 certification.
SUPERSPEED ***	USB 3.2 Approved USB4 Planning MP1900A USB solution with Lecroy RTO for Rx test was approved by USB-IF.
	 TBT3 Approved MP1900A was approved as a measurement equipment vendor for Thunderbolt 3 compliance test specs.
DisplayPort	DP1.4 FYIDP2.0 PlanningMP1900A will be approved as a Sink test equipment in next DP workshop.
Advancing Technology for Humanity	Standardization activities for IEEE 802.3 25, 50, 100, 200 ,400GbE, and future 800GbE/1.6 TE.
OIFF OPTICAL INTERNETWO FORUM	Anritsu has joined the Physical and Link Layer Working Group. CEI-56G/112G
TRADE ASSOCIATION	FDR/EDR ApprovedHDR FYIMP1900A is approved as a recommended ATD test equipment vendor for Infiniband FDR and EDR.

Anritsu envision : ensure





2021-2 MJM No. MP1900A_PCIE-E-F-2-(1.00)