



PCIe6 Return Path Optimization Manual

Signal Quality Analyzer-R MP1900A

5th Edition

Revision History

Edition	Changes
1 st	Initial release
2 nd	Added explanation on Delay Stabilizer
3 rd	Updated BER Measurement Re-Auto Search GUI
4 th	Updated recommended software version to V10.03.00
5 th	Updated GUI images Added Troubleshooting Flowchart Added minor revisions for smoother optimization procedure

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1 Introduction

When the loss in the return path from the DUT Tx to the MP1900A is large during the receiver test, it is essential to configure this path to minimize errors. This manual describes how to optimize the return path before using the MP1900A PCIe6 application to measure the DUT FBER (First Bit Error Rate).

2 Equipment Configuration

2.1 Outline



The modules installed in the MP1900A slots are listed below in order from the top slot (slot 1).

Slot 1-2	MU181000B
Slot 3-4	MU181500B
Slot 5	MU196060A
Slot 6	MU196040B
Slot 7	MU196020A
Slot 8	MU195050A

2.2 Configuration

The following table lists the configuration and required options at PCIe6 measurement.

PAM4 BERT

Model Number	Name	Qty	Description
MP1900A	SIGNAL QUALITY ANALYZER-R	1	
MU181000B	12.5GHz 4port Synthesizer	1	
MU181000B-002	SSC Extension	1	
MU181500B	Jitter Modulation Source	1	
MU196020A	PAM4 PPG	1	
MU196020A-001	32G baud	1	Can also use Opt-002 and Opt-003
MU196020A-011	4Tap Emphasis	1	
MU196020A-043	FEC Error Insertion for PCIe6	1	Recommended
MU196020A-060	PCIe6 LEQ	1	
MU196040B	PAM4 ED	1	
MU196040B-001	32G baud	1	Can also use Opt-002
MU196040B-011	Equalizer	1	
MU196040B-041	SER Measurement	1	
MU196040B-043	FEC Analysis for PCIe6	1	Recommended
MU195050A	Noise Generator	1	
MU196060A	32G baud NRZ/PAM4 Re-Driver	1	
MU196060A-001	Clock Recovery for SSC	1	
MX183000A-PL001	Jitter Tolerance Test	1	Recommended
MX183000A-PL021	PCIe Link Training	1	
MX183000A-PL025	PCIe 5 Link Training	1	
MX183000A-PL026	PCIe 6 Link Training	1	

• Software version

MX190000A: V10.03.00 or newer

MX183000A: V10.03.00 or newer

<https://www.anritsu.com/en-us/test-measurement/support/downloads?model=MP1900A>

The following table lists the components and accessories used by the PCIe measurement solution.

Components/Accessories

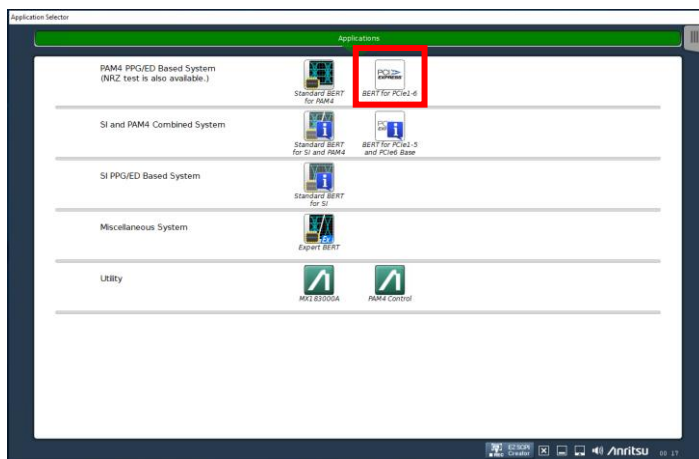
Model Number	Name	Qty	Description
J1815A	MP1900A PCIe Measurement Component Set	1	PCIe5 CEM Test Fixture, assumes use of K-connector I/F
34VKF50A	Precision Adapter (V-M, K-F)	0, 2*	*2 pcs required when using K-cable at MU196060A Data Input 0 pcs when using V-cable
34VFK50A	Precision Adapter (V-F, K-M)	0,2,4*	*2 pcs required when using V-cable at MU195050A Data Output *2 pcs required at Data Input when using MU195040A 0 pcs for any other configuration

3 Method

3.1 Preparation

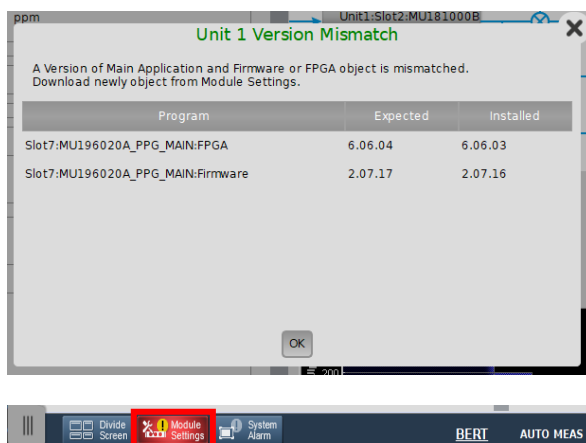
This section explains how to start the application and the preparations before measuring the FBER.

- a. Start the MX190000A software and click [BERT for PCIe6 Application] at the Application Selector screen.

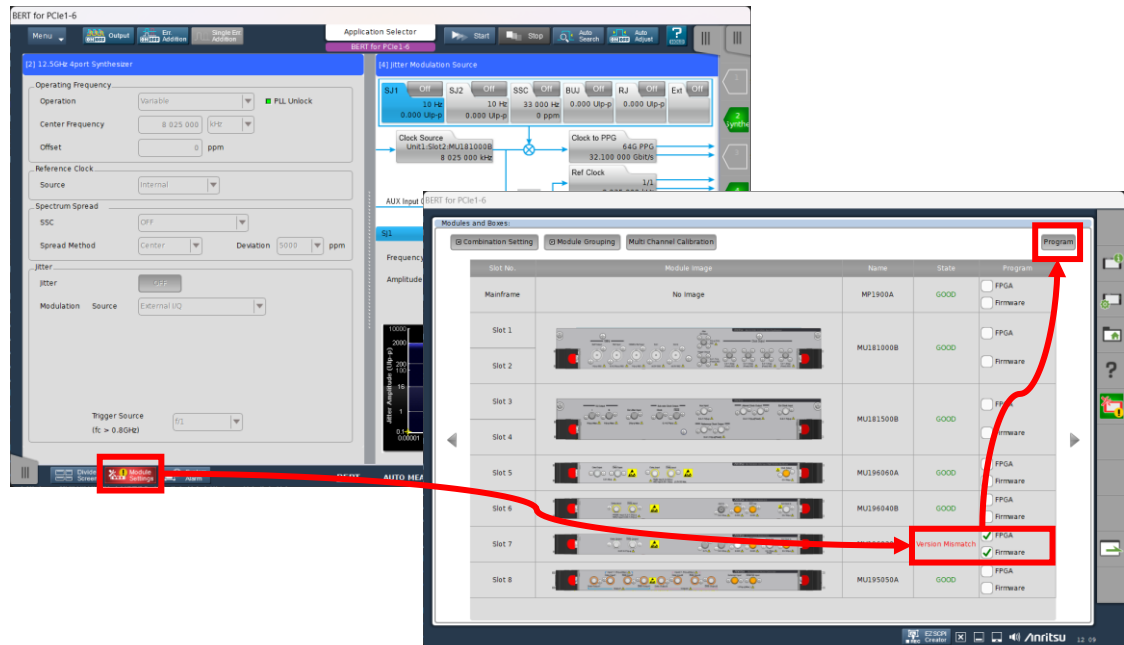


- b. After the application starts, when the installed FPGA and/or firmware versions of the modules do not match the expected versions of the MX190000A installer, a warning like the one below will be displayed. The [Module Settings] button on the bottom of the screen will also be red.

If there is no warning and the [Module Settings] button is not red, proceed to step c.

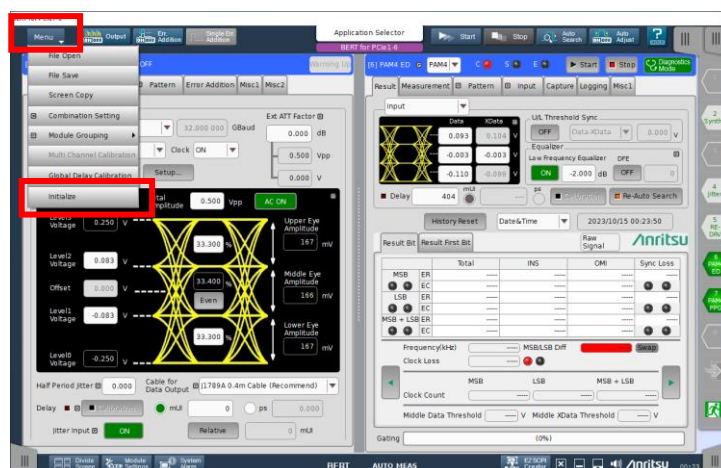


To install the expected FPGA and/or firmware versions, click the [Module Settings] button, confirm the checkboxes for the Version Mismatch, and then click [Program].

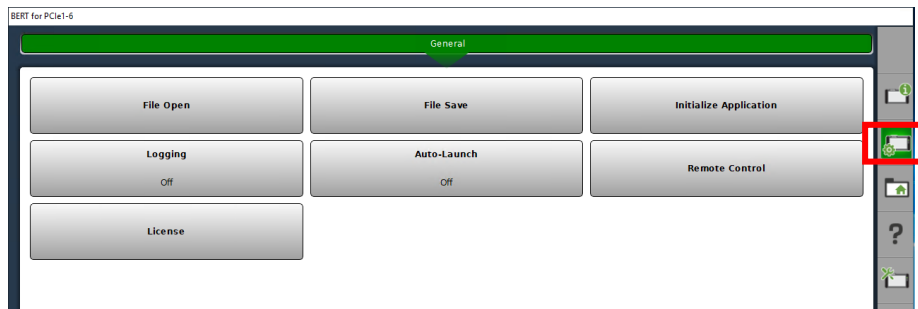


After the version update finishes, confirm that the State of all modules are displayed as [GOOD] and proceed to step c.

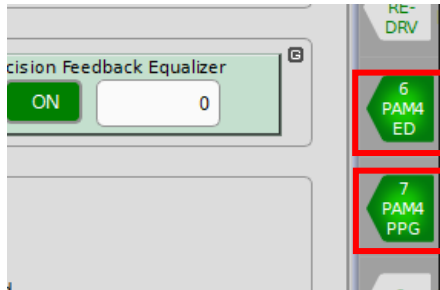
- c. Click [Menu] – [Initialize] – [OK].



- d. After initialization finishes, click the  button at the BERT for PCIe 1-6 screen to display the main screen.

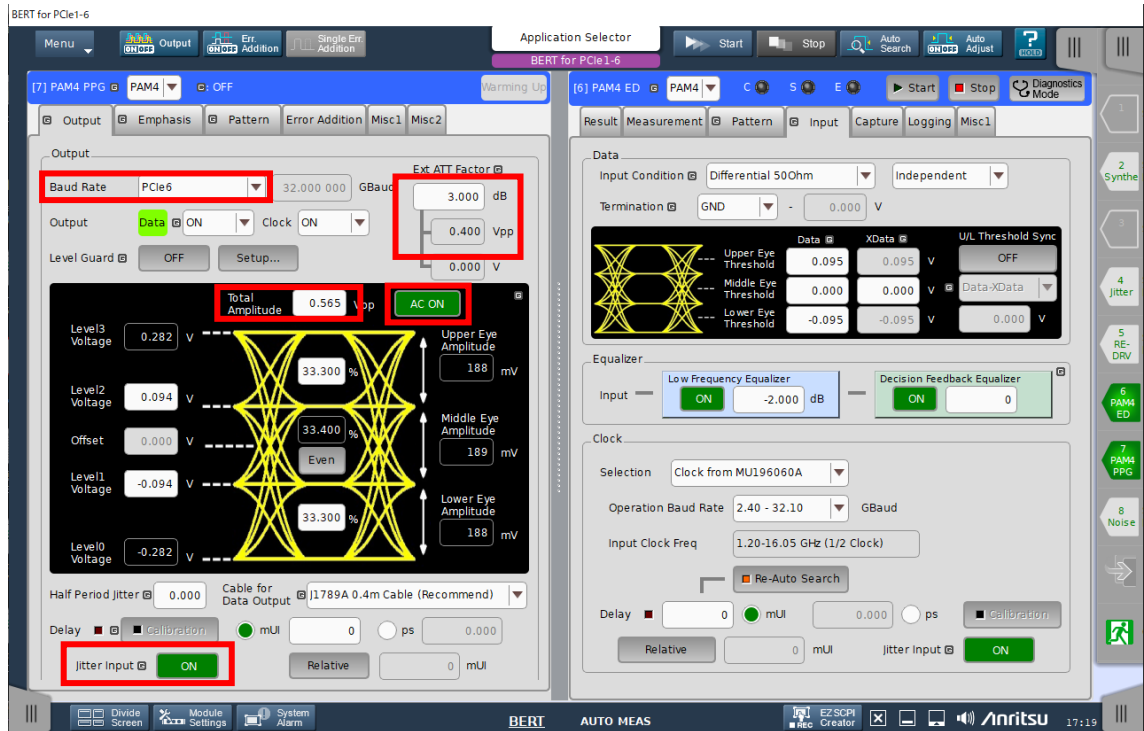


- e. The main screen has two tabs to display the PAM4 PPG and PAM4 ED screens.



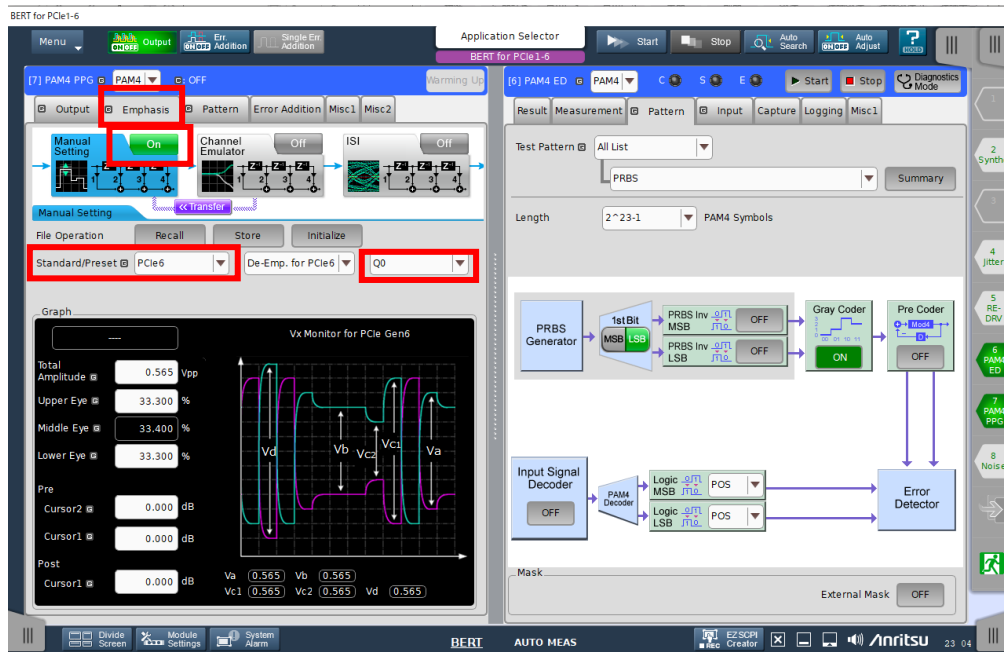
- f. Click the PAM4 PPG tab to display the PAM4 PPG Output tab.
- g. Set Baud Rate to PCIe6.
- h. Set Offset to AC ON.
- i. Set Jitter Input to ON.
- j. Set Ext ATT Factor to 3.0 dB.

- k. Set Total Amplitude to 0.565 Vpp. Since Noise Module reduces the amplitude by about 3 dB compared to the input signal, the output amplitude is about 0.400 Vpp (0.800 Vpp at Differential).

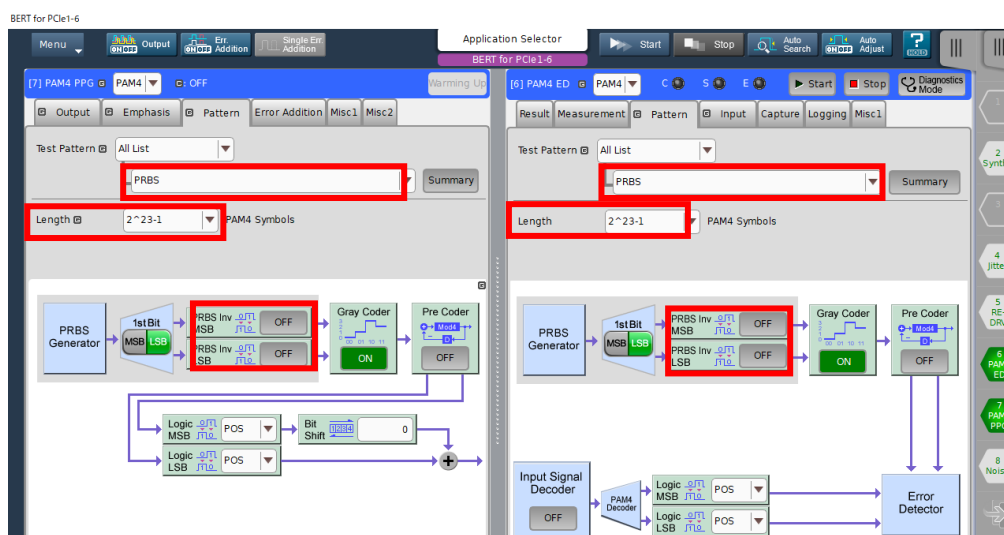


- l. Click the PAM4 PPG Emphasis tab.
- m. Set Manual Setting to ON.

- n. Set Standard/Preset to PCIe6 and Q0.

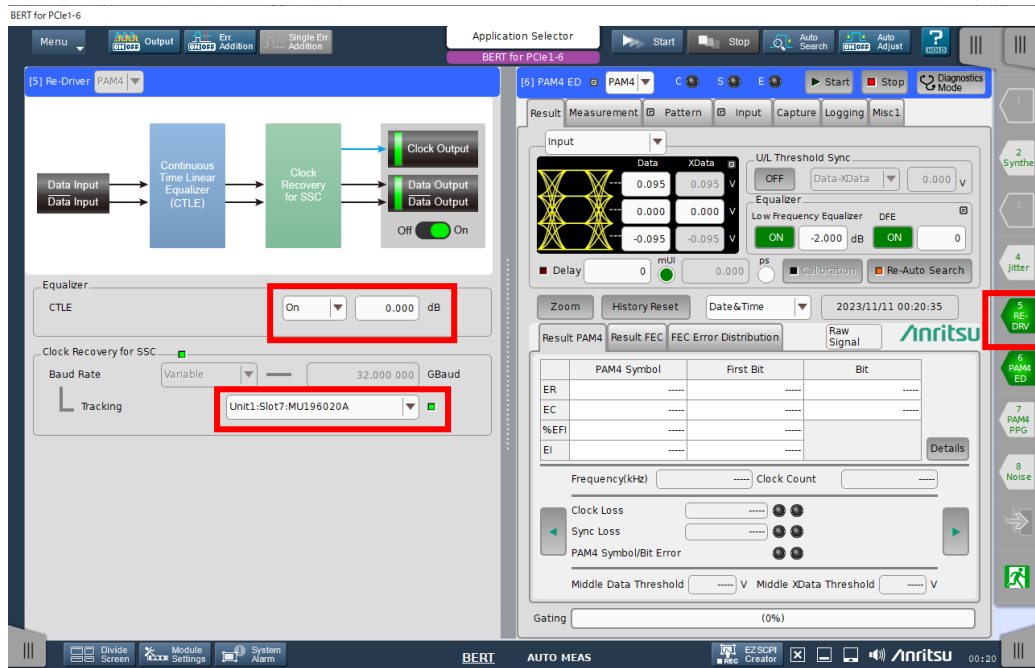


- o. Click both the PAM4 PPG and PAM4 ED Pattern tabs.
p. Set Test Pattern to PRBS and Length to $2^{23}-1$ at both tabs.
q. Set PRBS Inv MSB/LSB to OFF at both tabs.



- r. Click the RE-DIV tab at the right side of the screen and set the Equalizer CTLE to ON.

- s. Select [Unit1, Slot7, MU196020A] at Clock Recovery for SSC Tracking.



- t. Save these settings by clicking [Menu] – [File Save].

This completes the measurement preparations.

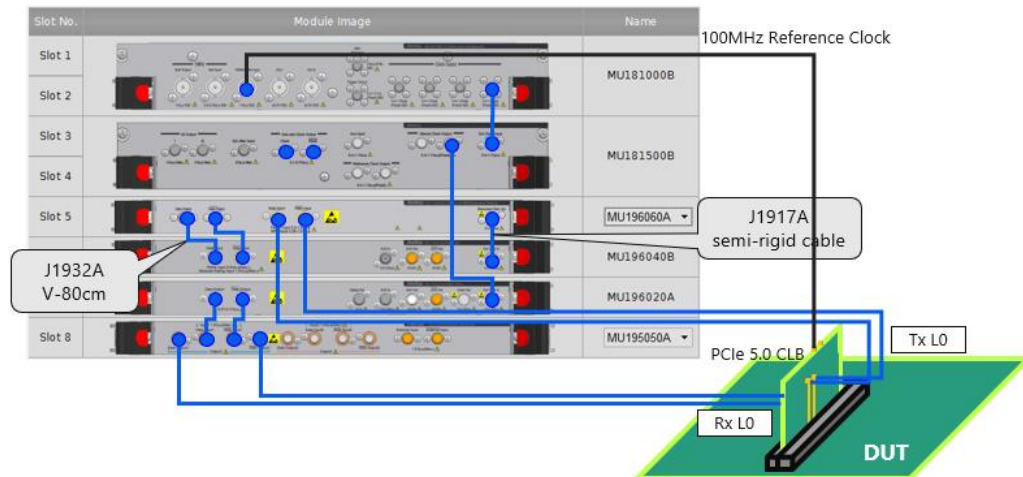
3.2 Optimizing Return Loss (DUT to MP1900A)

This section explains how to optimize the MP1900A receiver setting parameters (Vth, Delay, and CTLE) for the signal input to the MP1900A, as well as the method for minimizing FBER occurring in the return path (MP1900A).

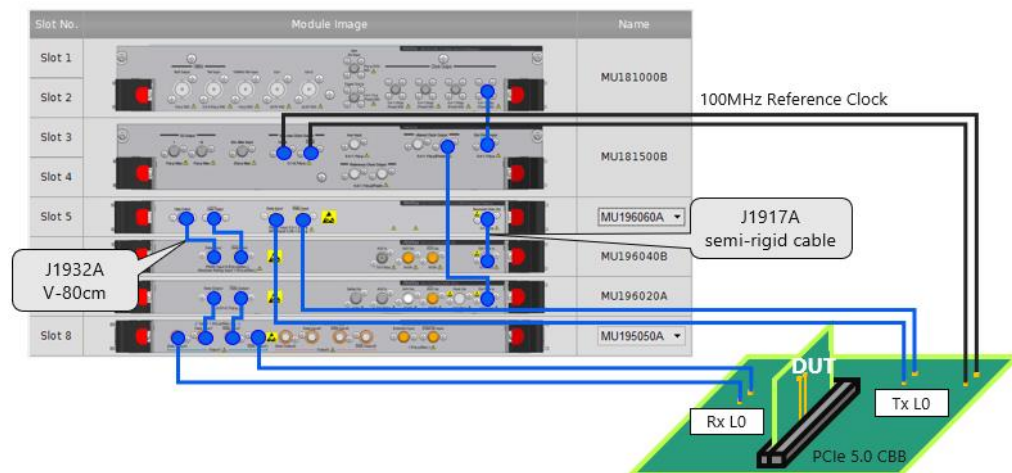
This method does not use the loopback mode for returning the data received by the DUT, but instead generates the PRBS signal at the DUT itself by implementing the Tx function. Even if the DUT has no PRBS signal-generation function, if it has PCIe6 Link Training function, the MX183000A-PL026 function can be used to easily adjust the return path. Go to section 3.3 when wanting to use this function.

- a. Connect the MP1900A and the DUT as shown in the following figure.

This setup shows System as the DUT.

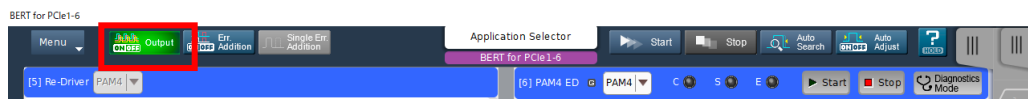


This setup shows AIC (Add-in Card) as the DUT.



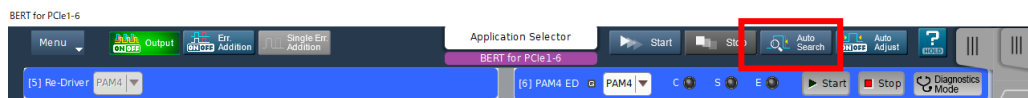
b. Prepare for measurement as described in section 3.1.

c. Set Output to ON after connecting the DUT.



d. Output a 32 GBaud, PAM4, PRBS23, Tx EQ Q0 signal from the DUT.

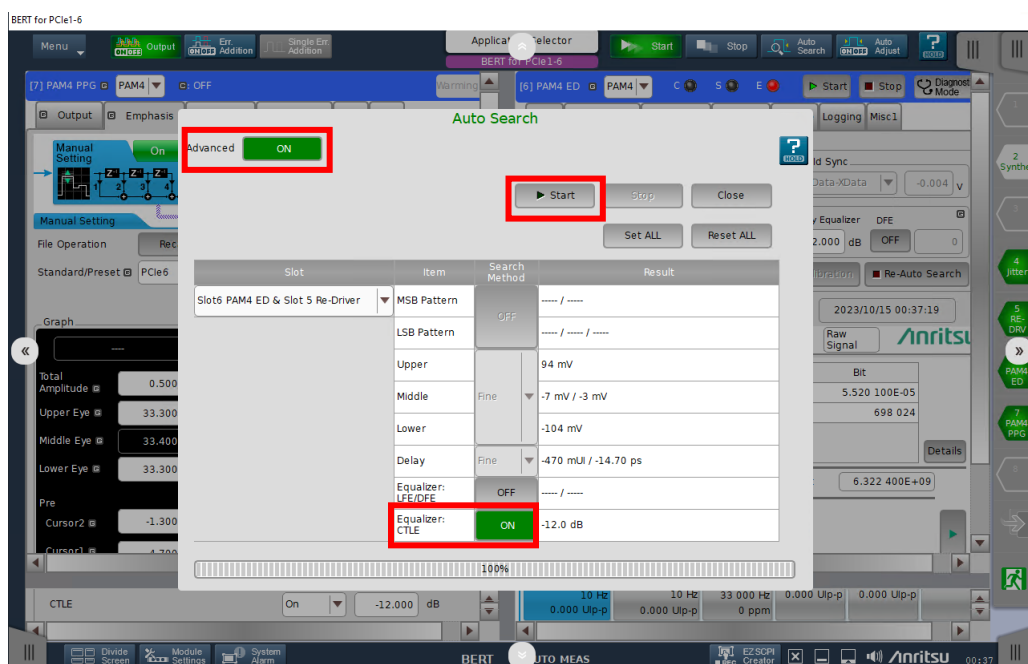
e. To optimize the ED status for the input signal, click the Auto Search icon  at the top of the screen.



f. Set Advanced at the Auto Search screen to ON.

g. Set Equalizer CTLE to ON and Equalizer LFE/DFE to OFF.

h. Click [Start] and wait up to about 2 minutes until Auto Search completes.

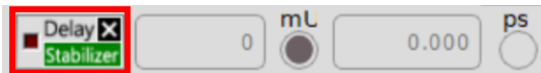


- i. After Auto Search completes, record the Vth (Upper/Middle/Lower), Delay, and CTLE values as shown in the following table.

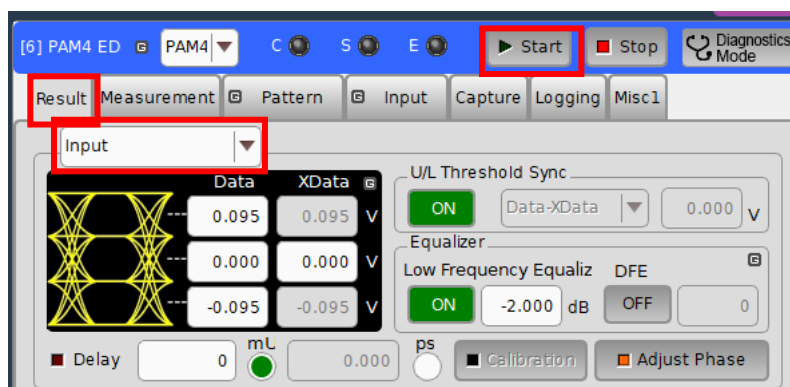
Slot	Item	Search Method	Result
Slot6 PAM4 ED & Slot 5 Re-Driver	MSB Pattern	OFF	---- / ----
	LSB Pattern		---- / ---- / ----
	Upper	Fine	94 mV
	Middle		-7 mV / -3 mV
	Lower		-104 mV
	Delay	Fine	-470 mUI / -14.70 ps
	Equalizer: LFE/DFE	OFF	---- / ----
	Equalizer: CTLE	ON	-12.0 dB

Note:

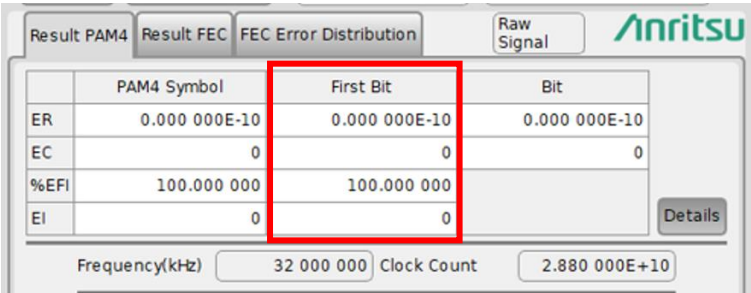
- Here, Sync Loss occurs if the DUT Tx EQ (Preset) either over- or under-compensates Channel Loss, but this is not due to a fault. In this case, go to step n. However, if Sync Loss occurs at every Preset from Q0 to Q9, refer to Section 5 Troubleshooting.
- After Auto Search, the Delay Stabilizer function will be enabled. Delay Stabilizer is a function for adjusting Delay (Phase) in real time to suppress BER fluctuations due to the passage of time and temperature fluctuations. To manually adjust the Delay, click the X button on the Delay Stabilizer logo.



- j. Close the Auto Search screen and click the PAM4 ED Result tab.
- k. Set the parameter pull-down under the Result tab to Input .
- l. Click the [Start] button.



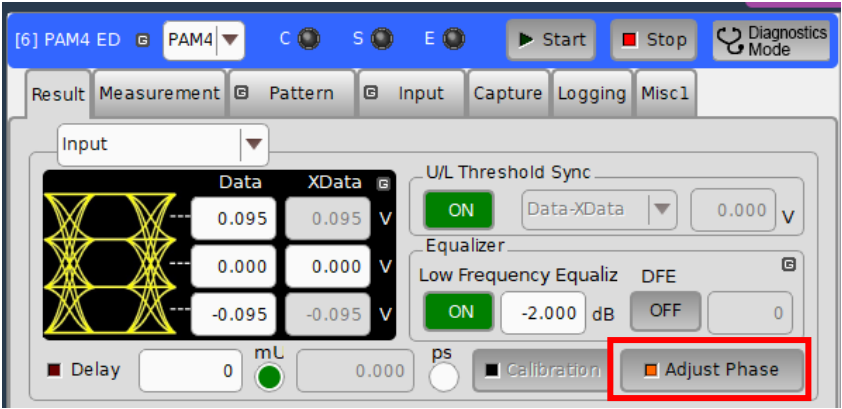
m. The value of the First Bit ER (FBER) is recorded as shown in the following table.



	PAM4 Symbol	First Bit	Bit
ER	0.000 000E-10	0.000 000E-10	0.000 000E-10
EC	0	0	0
%EFI	100.000 000	100.000 000	
EI	0	0	

Frequency(kHz) 32 000 000 Clock Count 2.880 000E+10

Here, the Clock phase (Delay) used by the ED may sometimes change when the Re-Driver locks to the input signal, which is indicated by the Adjust Phase LED being lit on. When this occurs, click the [Adjust Phase] button.



n. Change the DUT Tx EQ value from Q0 set in step d to Q1 to Q9 successively and repeat the procedure up to step m for each change.

The following table lists an example of the measurement results. The DUT Preset producing the minimum FBER is confirmed from these results. In this example, this system measured the best FBER result as 1E-11 for the DUT Q5 Preset.

Example of FBER Measurement Results for Each Preset

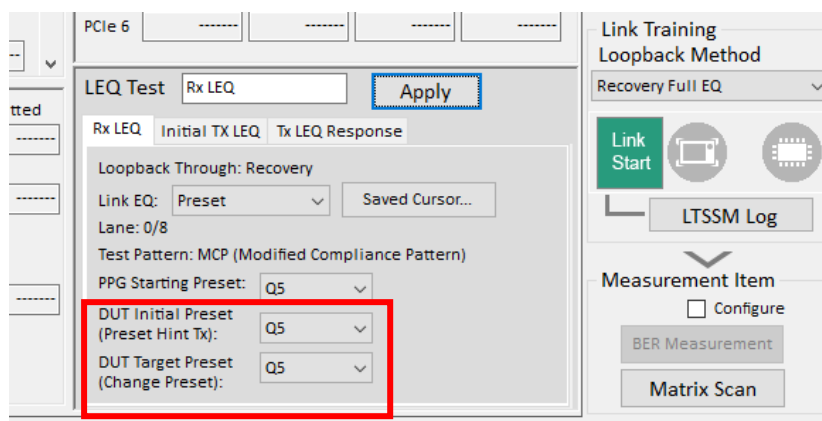
Preset	FBER ^{*1}	Upper Vth [V] ^{*2}	Middle Vth[V] ^{*2}	Lower Vth[V] ^{*2}	Equalizer CTLE [dB] ^{*2}	Delay[mUI] ^{*2}
Q0	xE-5	0.120	-0.008	-0.130	15.0	
Q1	xE-10	0.111	-0.008	-0.125	12.1	
...	...	...	...	...		
Q5	1E-11	0.095	-0.008	-0.108	11.3	
...	...	...	...	...		
Q8	xE-5	0.086	-0.008	-0.100	10.0	
Q9	Sync Loss	-	-	-	-	

*1: Write the values measured in step m. *2: Write the values measured in step i.

When subsequently measuring FBER, set the Preset producing the best FBER listed here as the DUT Tx EQ. Also set the best Upper, Middle and Lower Vth values and CTLE. Click the [Adjust Phase] button as necessary.

[Reference]

Here, when measuring Link Training and FBER using the MX183000A, set the Preset that produces the best FBER at DUT Initial Preset and DUT Target Preset. (Refer to section 4.1 for details.) Either set the best Upper, Middle and Lower Vth values and CTLE at the ED or perform Calibration for PAM4 as described in section 3.3.



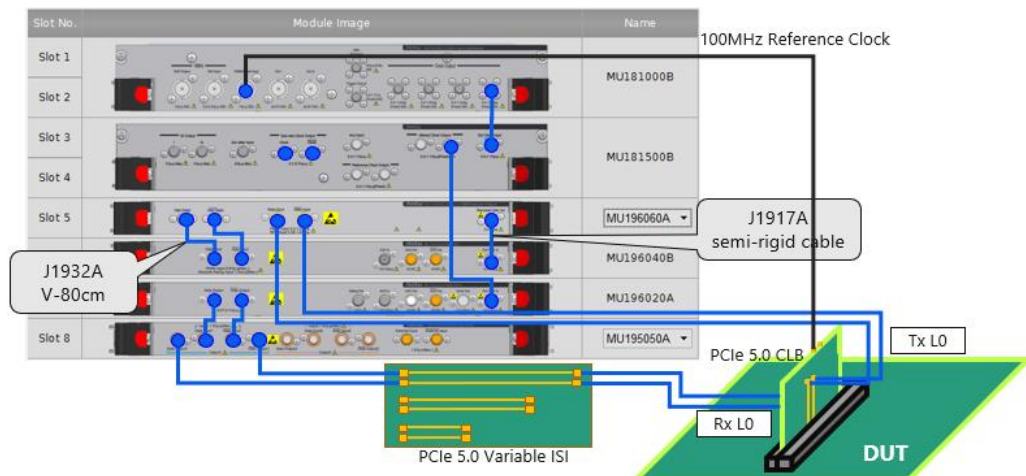
3.3 Adjusting Return Path using MX183000A PCIe Link Training

This section explains how to adjust the return path using the MX183000 PCIe Link Training application. The purpose of this adjustment procedure is to transition the DUT to the Loopback.Active state; instead of using MCP to measure FBER, the return path is adjusted using CP. Consequently, sometimes optimum FBER results may not be obtained, depending on the MCP pattern output after the Loopback.Active state. As a result, when adjusting using only this procedure, optimize the return path by performing Auto Search once after Link Training completes. See section 4.1 for the method.

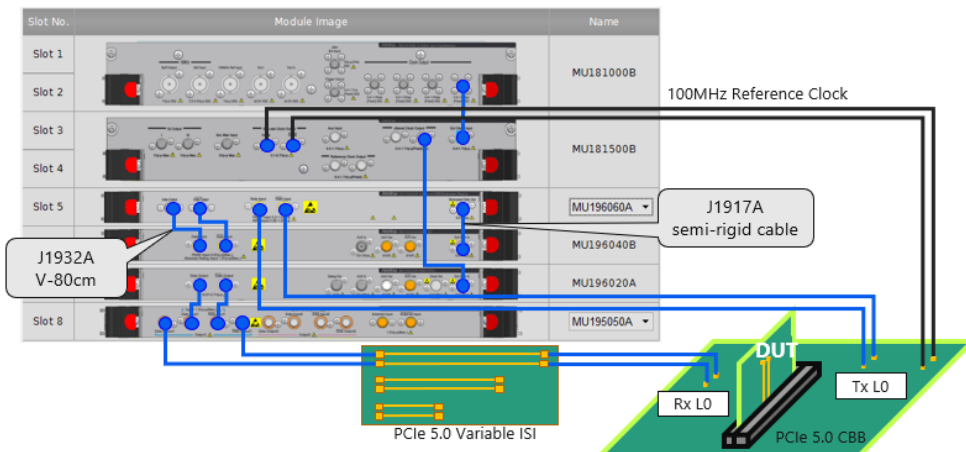
However, ignore this procedure if the return path is optimized as described in section 3.2.

a. Connect as shown in the following figures.

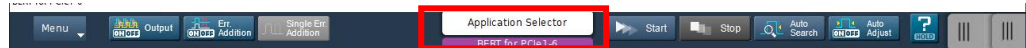
Setup with System as DUT



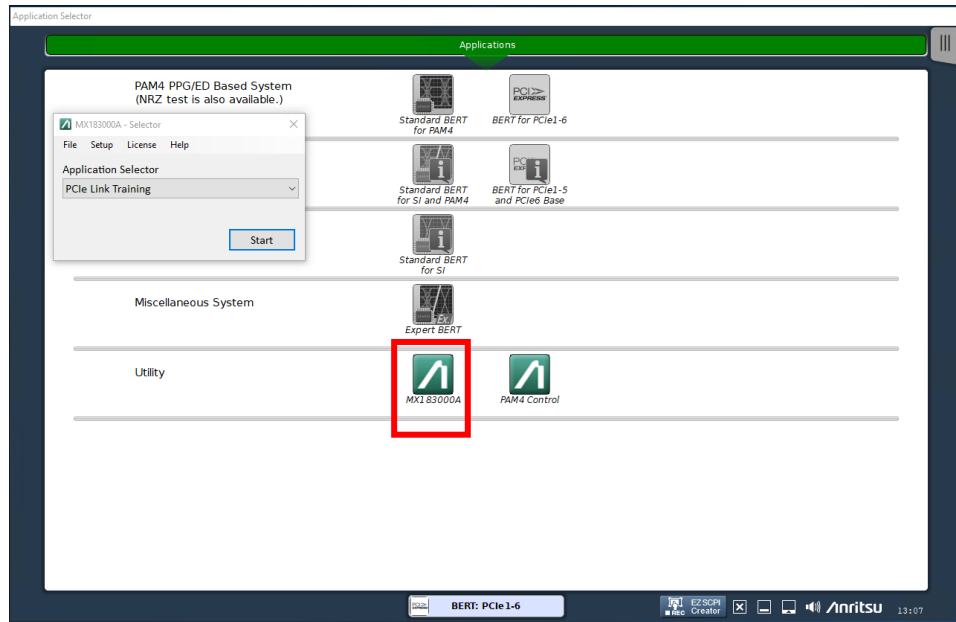
Setup with AIC (Add-in Card) as DUT



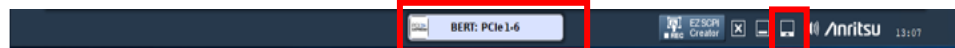
- b. Click Application Selector.



- c. Click MX183000A.

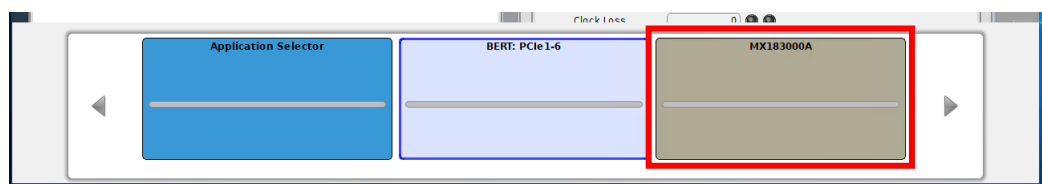


- d. Click BERT: PCIe1-6.

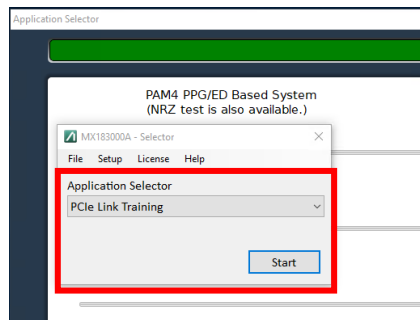


If [PCIe1-6] is not displayed, see preparation as described in section 3.1 step a, and click [BERT for PCIe6 Application].

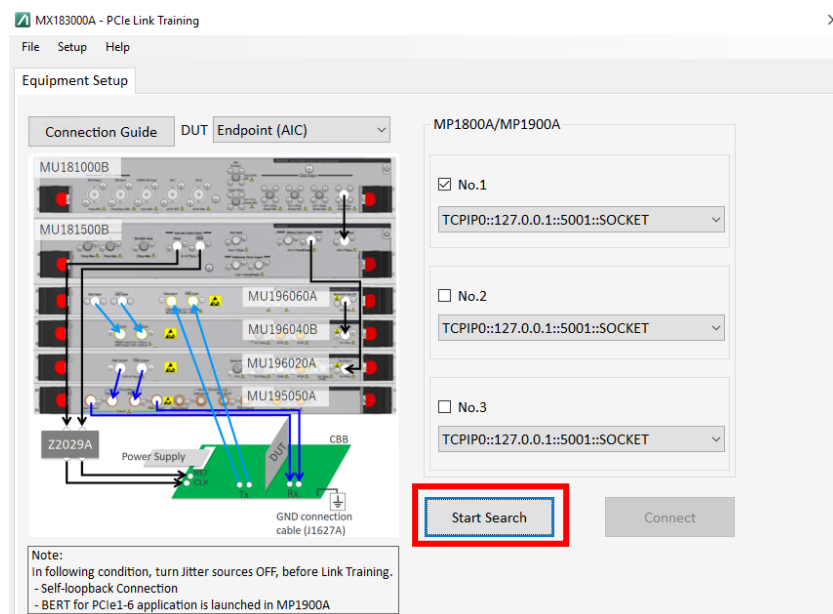
- e. If the MX183000A screen is not displayed, click the  icon at the bottom-right of the screen and click MX183000A.



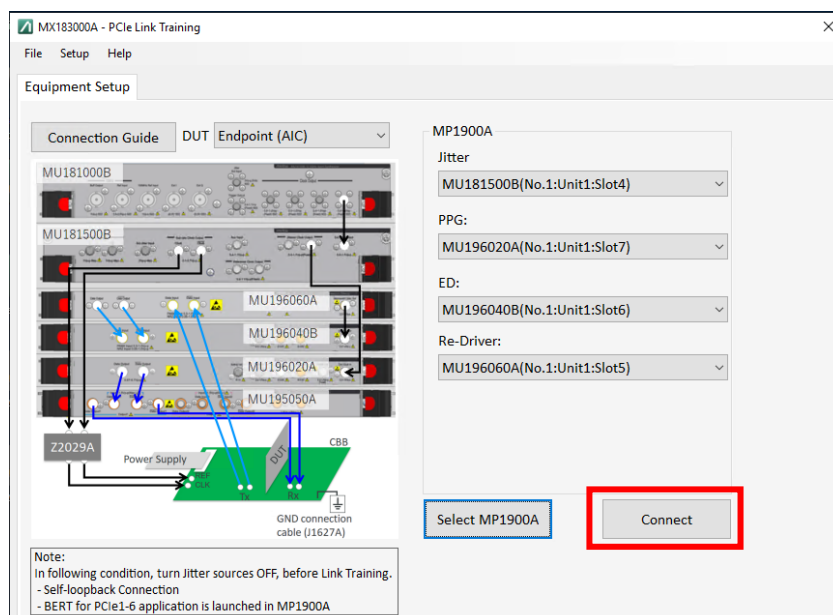
- f. Select PCIe Link Training at MX183000A Selector and click [Start].



- g. Click [Start Search].

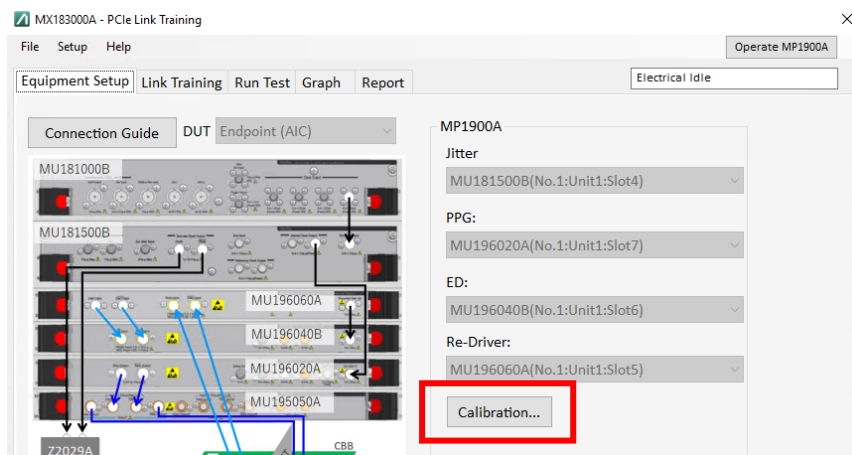


- h. Click [Connect].

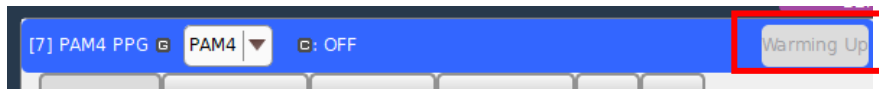


Note:

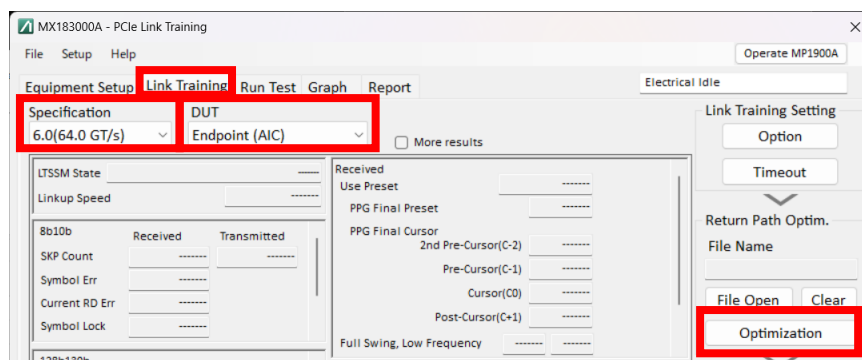
- ✧ When the required Calibration screen is displayed, click [Calibration] to perform calibration according to the screen settings. Calibration takes about 10 minutes to complete.



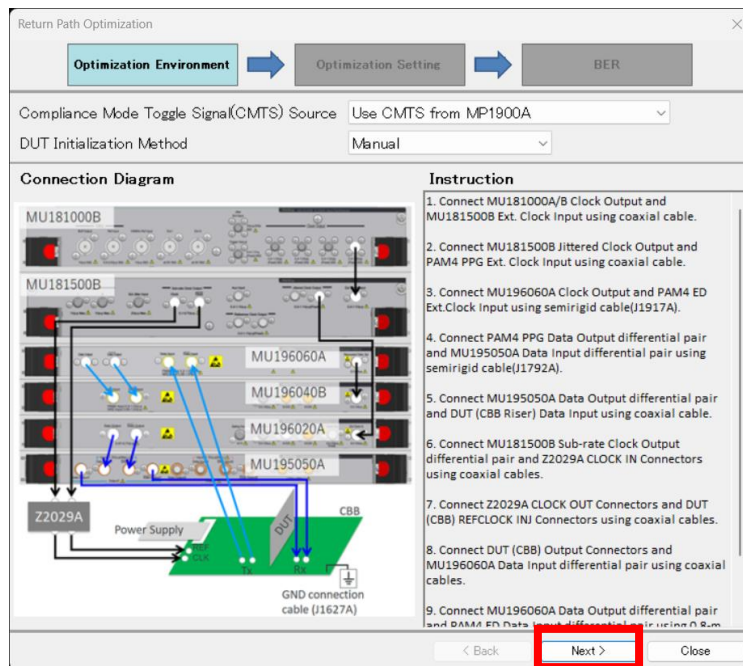
- ✧ After the PAM4 PPG Warming Up LED goes out, click [Connect] at the MX183000A Equipment Setup tab. If the MX183000A displays a warning dialog when [Connect] is clicked explaining that warming-up was not completed, click [Disconnect] at the Equipment Setup tab. Then, click [Connect] once again at the Equipment Setup tab after the PAM4 PPG Warming Up LED goes out. An example of the extinguished Warming Up LED is shown below.



- i. Click the Link Training tab after Connect completes.
- j. Set Specification to 6.0.
- k. Select the DUT (AIC/System) to measure according to the actual DUT type.
- l. Click [Optimization] under the Return Path Optimization settings.

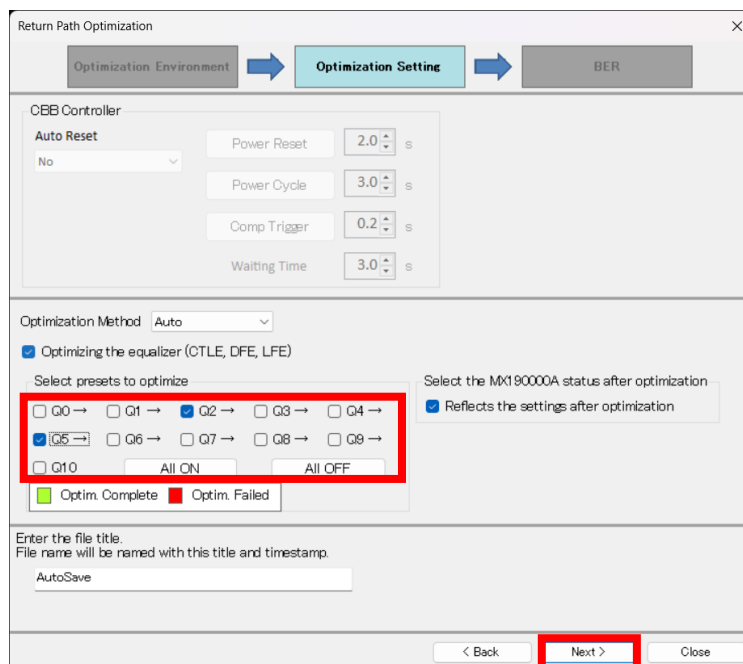


m. Click [Next].

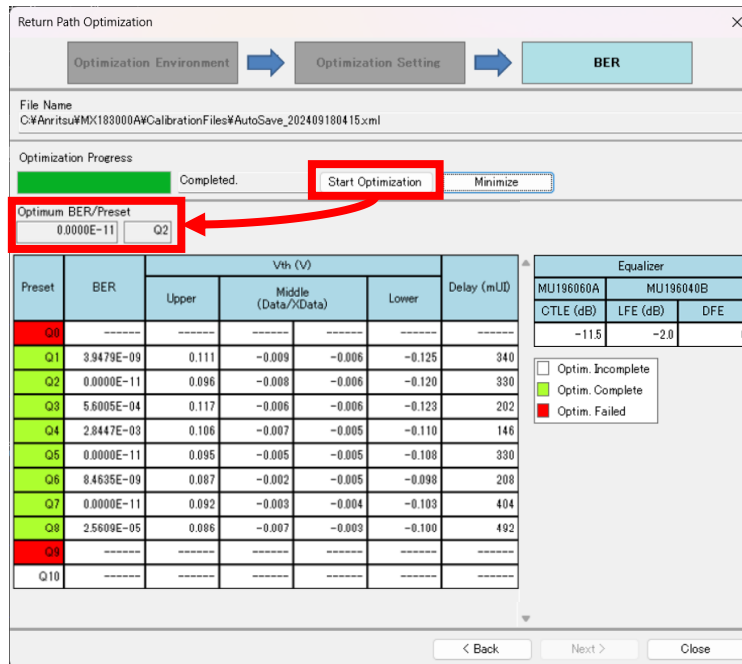


n. Select the Qx number. Calibration takes about 2 minutes for each preset. In principle, we recommend performing calibration for all the Q0 to Q9 presets. To shorten the time, put checkmarks only in Q2 and Q5. If both presets result in in Sync Loss, put checkmarks in Q0 to Q9 excluding Q2 and Q5 and perform optimization.

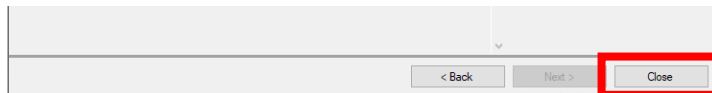
o. Click [Next].



- p. Click [Start Optimization].
- q. After completing optimization, confirm Optimum BER/Preset. The following example confirms an FBER of E-11 was obtained with presets Q2, Q5, and Q7 at a return loss of 14 dB.



- r. Click [Close].



Return path optimization is completed by the above procedure.
To continue with FBER measurement, see section 4.1.

4 Receiver Test Method

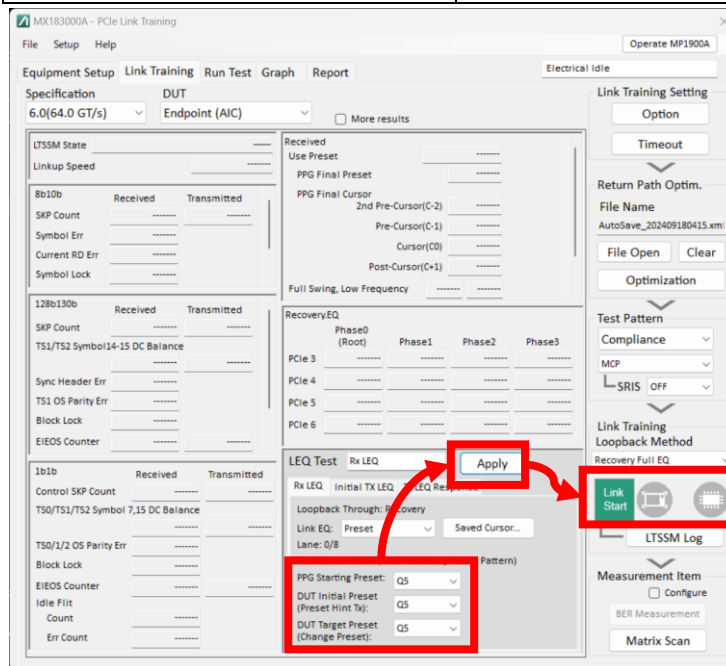
4.1 FBER Measurement

This section explains the FBER measurement procedure using the MX183000A Link Training function.

This procedure can only be used with a DUT that supports the Link Training function.

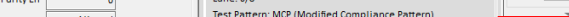
- Perform the procedure described in section 3.3
- Select LEQ Test at the Rx LEQ tab and set each of the following Preset values.

PPG Starting Preset Set Preset when PPG changed to 32 Gbaud PAM4 signal	Set optimum Preset value for DUT. If the optimum Preset is unclear, set Q5. If Link Training is unsuccessful at Q5, set another Preset and retry Link Training.
DUT Initial Preset Preset sent first when DUT enters Recovery.EQ.PhaseX state	Set optimum Preset value found in section 3.2 or 3.3.
DUT Target Preset Preset sent last when DUT enters Recovery.EQ.PhaseX state	Set optimum Preset value found in section 3.2 or 3.3.



- Click [Apply].
- Click [Link Start].
- Wait until the LTSSM State becomes Loopback.Active 64 Gbps.
If the state does not become Loopback.Active:

-
- MX183000A - PCIe Link Training**
- File Setup Help Operate MP1900A
- Equipment Setup **Link Training** Run Test Graph Report
- Specification DUT Outputting Test Pattern
- 6.0(64.0 GT/s) Endpoint A/C [More results]
- LTSSM State** Loopback Active Local
Linkup Speed 64.0 Gbps
- 801b0**
- | | Received | Transmitted |
|----------------|----------|-------------|
| SKP Count | 1876 | 10376 |
| Symbol Err | 281730 | |
| Current RD Err | 2798660 | |
| Symbol Lock | Locked | |
- 128b130b**
- | | Received | Transmitted |
|--------------------------------|-----------|-------------|
| SKP Count | 0 | 0 |
| TS1/TS2 Symbol14-15 DC Balance | 0 | 0 |
| Sync Header Err | 0 | |
| TS1 Q5 Parity Err | 0 | |
| Block Lock | Unaligned | |
| EIEOS Counter | 0 | 0 |
- 1d1b**
- | | Received | Transmitted |
|------------------------------------|----------|-------------|
| Control SKP Count | 192673 | 192673 |
| TS0/TS1/TS2 Symbol 7,13 DC Balance | 0 | -496 |
| TS0/1/2 Q5 Parity Err | 0 | |
| Block Lock | Aligned | |
| EIEOS Counter | 755 | 756 |
| Idle Flit | | |
| Count | 3064492 | |
| Error Count | 1862020 | |
- received Use Preset PPG Final Preset PPG Final Cursor 2nd Pre-Cursor(C-2) Pre-Cursor(C-1) Cursor(C0) Post-Cursor(C-1)
- Full Swing, Low Frequency
- RecoveryEQ Phase0 (Root) Phase1 Phase2 Phase3
- PCie 3 PCie 4 PCie 5
- LEQ Test** Rx LEQ Tx LEQ Response Apply
- Rx LEQ Initial Tx LEQ Tx LEQ Response
- Linkup Through: Recovery Link Eq: Preset Saved Cursor... Lane: 0/8
- Test Pattern: MCP (Modified Compliance Pattern)
- PPG Starting Preset: Q5 DUT Initial Preset (Preset Hint Tx): Q5 DUT Target Preset (Change Preset): Q5
- Link Training Setting**
- Option Timeout
- Return Path Optim.**
- File Name AutoSave_202409180415.xm File Open Clear Optimization
- Test Pattern**
- Compliance MCP SRRIS OFF
- Link Training Loopback Method**
- Recovery Full EQ Unlink Link Loopback CC0 CC1
- LTSSM Log Measurement Item Configure BER Measurement Matrix Scan



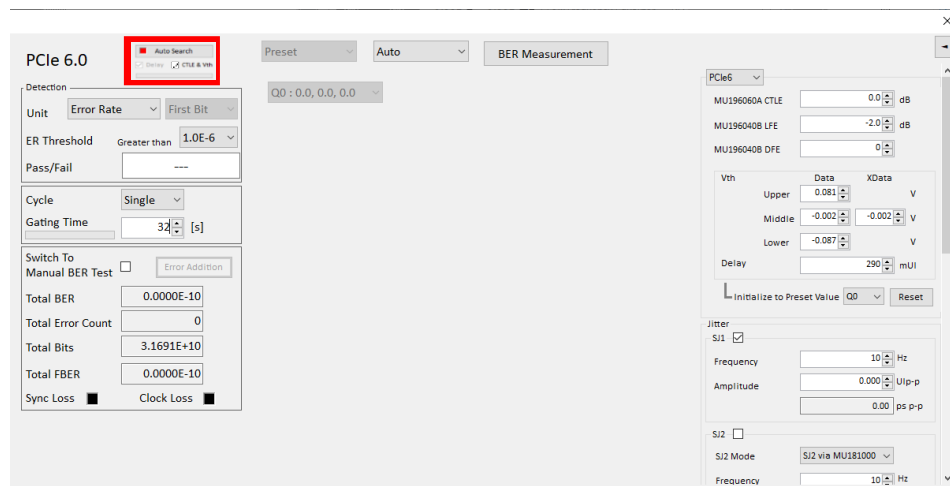
The screenshot shows the 'PPG Configuration' window. On the left, there are several input fields: 'TS0/1/2 OS Parity Err' (0), 'Block Lock' (Aligned), 'E1EOS Counter' (755), 'Idle Flit Count' (3064492), and 'Err Count' (1862020). On the right, there are dropdown menus for 'Lane: 0/8', 'Test Pattern: MCP (Modified Compliance Pattern)', 'PPG Starting Preset: Q5', 'DUT Initial Preset (Preset Hint Tx): Q5', and 'DUT Target Preset (Change Preset): Q5'. A red box highlights the 'Measurement Item' dropdown, which is currently set to 'Configure'. Below it, 'BER Measurement' is also visible. At the bottom right, there is a 'Matrix Scan' button.

PCIe 6.0

☒ Auto Search Preset Auto **Stop**

☒ Delay ☐ CTLE & Vth Q0 : 0.0, 0.0, 0.0

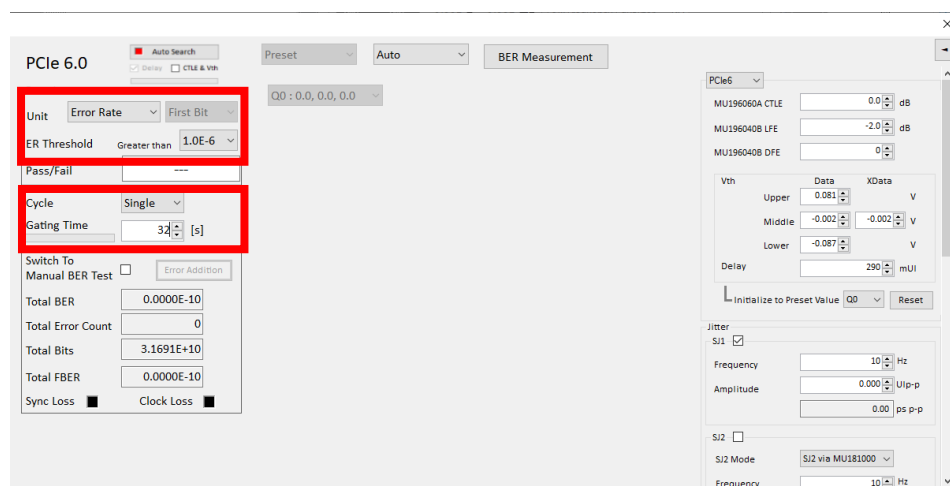
- h. Put a checkmark in CTLE & Vth and click Auto Search.



After Auto Search, the Delay Stabilizer function will be enabled. Delay Stabilizer is a function for adjusting Delay (Phase) in real time to suppress BER fluctuations due to the passage of time and temperature fluctuations. To manually adjust the Delay, close the BER Measurement window and click Operate MP1900A. On the PAM4 ED Result tab->Input, click the X button on the Delay Stabilizer logo.



- i. Set Unit to Error Rate, ER Threshold to 1.0E-6, and Cycle to Single.



- j. Set the Gating Time for the Target BER to measure.

Target BER	Gating Time [s]	Reference Confidence Level (%)
1E-8	1	> 99.9
1E-9	1	> 99.9
1E-10	2	> 99.5
1E-11	12	> 99.5
1E-12	120	> 99.5

- k. Click [BER Measurement].

- l. Wait until measurement completes. The result is PASS when the FBER is less than 1E-6.

PCle 6.0

Auto Search ☐ Delay ☒ CTLE & Vth

Preset Auto BER Measurement

Detection

Unit First Bit

ER Threshold Greater than 1.0E-6

Pass/Fail

Cycle

Gating Time [s]

Switch To Manual BER Test ☐ Error Addition

Total BER

Total Error Count

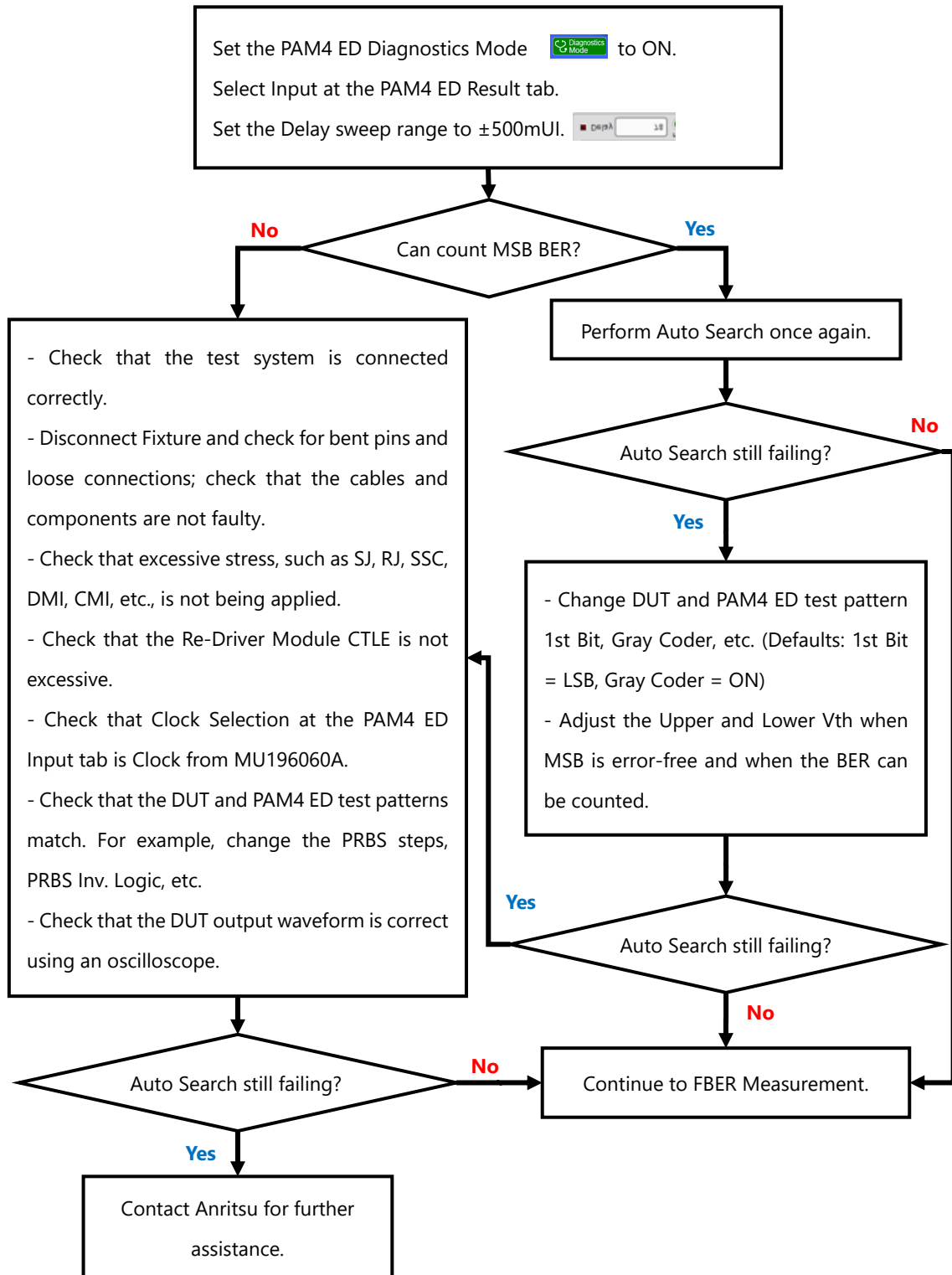
Total Bits

Total FBER

Sync Loss ☒ Clock Loss ☒

5 Troubleshooting

5.1 When Auto Search is Failing

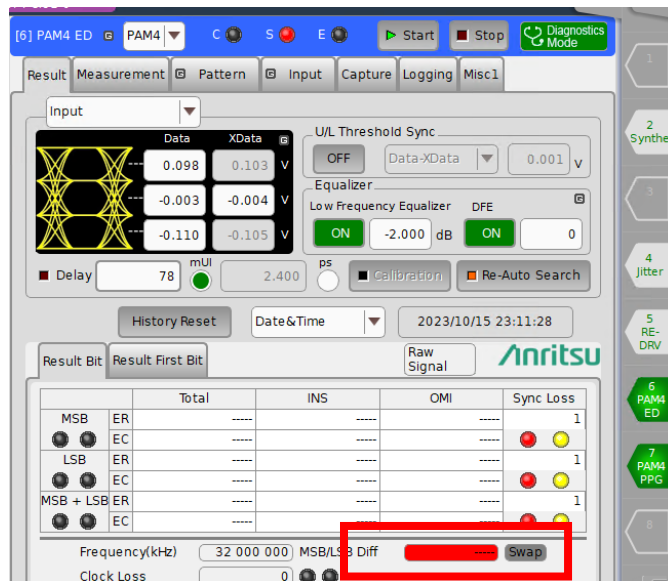


5.2 At Sync Loss only When Diagnostics Mode OFF

If Sync Loss is returned at Diagnostics Mode OFF but the BER can be counted when it is ON, consider the possible occurrence of a MSB/LSB Bit shift which cannot be detected as a PAM4 symbol.

Bit Shift Example

MSB/LSB Diff displays red or yellow at Diagnostics Mode ON



- Set Diagnostics Mode to ON and change the PAM4 ED test pattern to 1st Bit, Gray Coder, etc., and confirm that the MSB/LSB Diff is zero.
- Set the Upper/Lower Vth and confirm that MSB/LSB Diff is zero.



Specifications are subject to change without notice.

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