

Anritsu Advancing beyond

Signal Quality Analyzer-R

PCIe/USB/Thunderbolt/Display Port Test Solutions*

MP1900A

SQA-R



*: Refer to the 32G/64G NRZ/PAM4 Signal Integrity Test Solution Catalog (MP1900A_64G-E-A-1) for the information on MP1900A PAM4 test solution.

Support 400 GbE/800 GbE and PCIe 6/7

Due to the explosive growth of data traffic resulting from the popularity of smartphones and mobile terminals, network interfaces are transitioning to faster 400 GbE/800 GbE standards, and PCI bus interface speeds now exceed 64G. In addition, the equipment and chipsets using these interfaces support multi-channels and multi-protocols.

The MP1900A is a high-performance BERT with excellent expandability for supporting Physical layer evaluations of these high-speed interfaces. The all-in-one design is ideal for early stage R&D evaluations of all interfaces covering next-generation Ethernet networks to bus interconnects.

MP1900A Signal Quality Analyzer-R



Certified for
PCIe, CXL, USB
Thunderbolt,
Display Port

PCIe7
Base Test
Ready

Advanced
Link Debug
For PCIe, CXL

Excellent Expandability

All-in-one support for both high-speed Ethernet and PCI Express interface tests

Supports transmissions up to 512 Gbit/s

- 32 Gbaud bandwidth : 8ch NRZ
- 64 Gbaud bandwidth : 4ch NRZ, PAM4

8 slots for adding extra modules

Backwards compatibility with
MP1800A series modules

Signal Integrity Evaluation

Multi-Tap Emphasis built-in

Variable ISI Function

Multi-band CTLE

CDR Function (supports SSC)

Jitter Addition (SJ/RJ/BUJ/SSC) function

User-defined SSC profile function

Voltage Noise Addition (CM/DM/Gaussian) function

Link Training

Receiver tests are supported by the built-in Protocol Awareness PCIe Link Training, USB Link Training and LTSSM analysis functions.

Supports PCI Express Gen 1/2/3/4/5/6

Supports both USB 3.2 Gen1/2 ×1 and ×2

Supports Link Training troubleshooting using
Sequence Editor

High Waveform Quality and High Sensitivity

Low Intrinsic (Residual) Jitter output

High-sensitivity Data input

Operation bit rates from 2.4 Gbit/s to 32.1, 128 Gbit/s





Wide Application Support

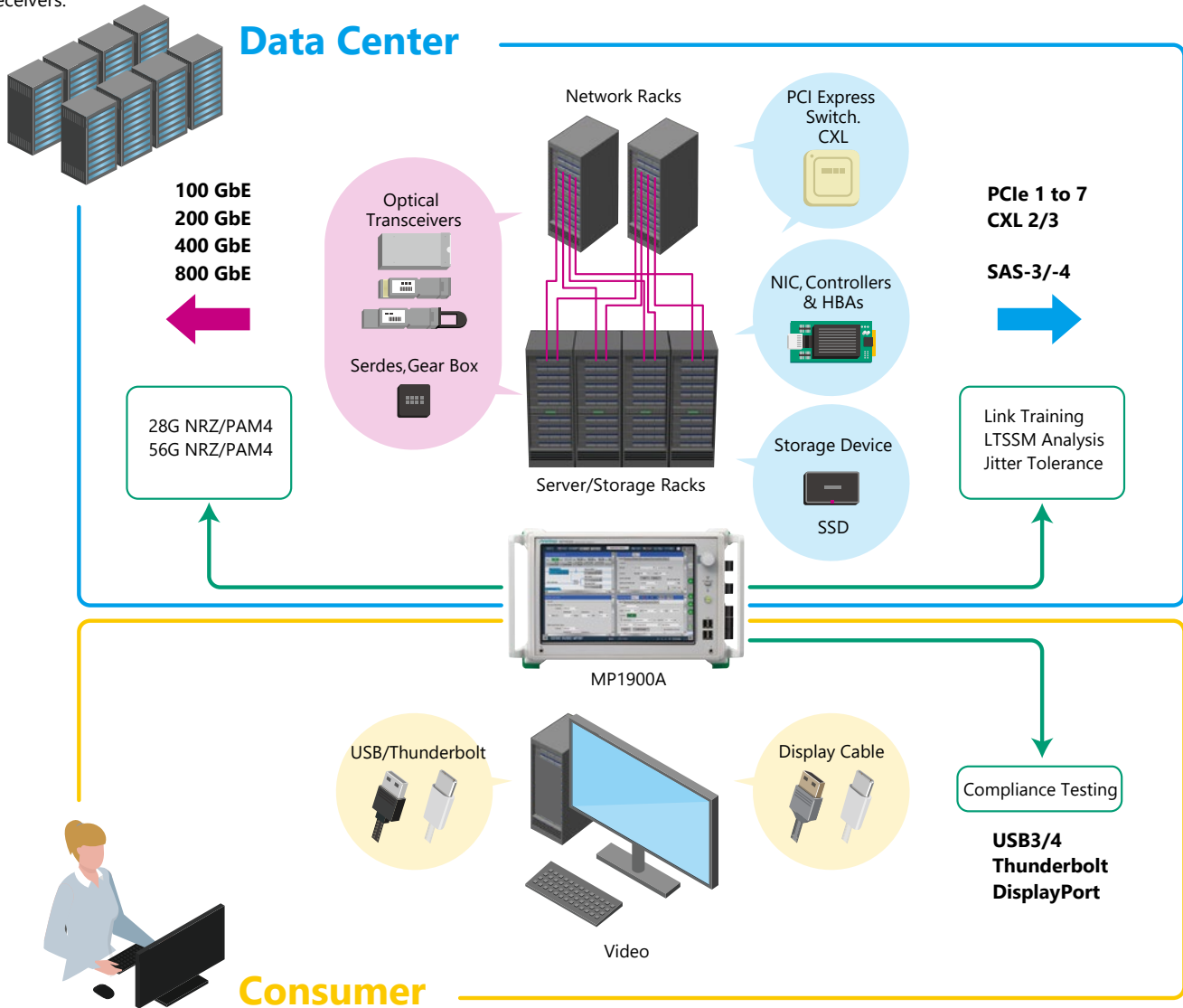
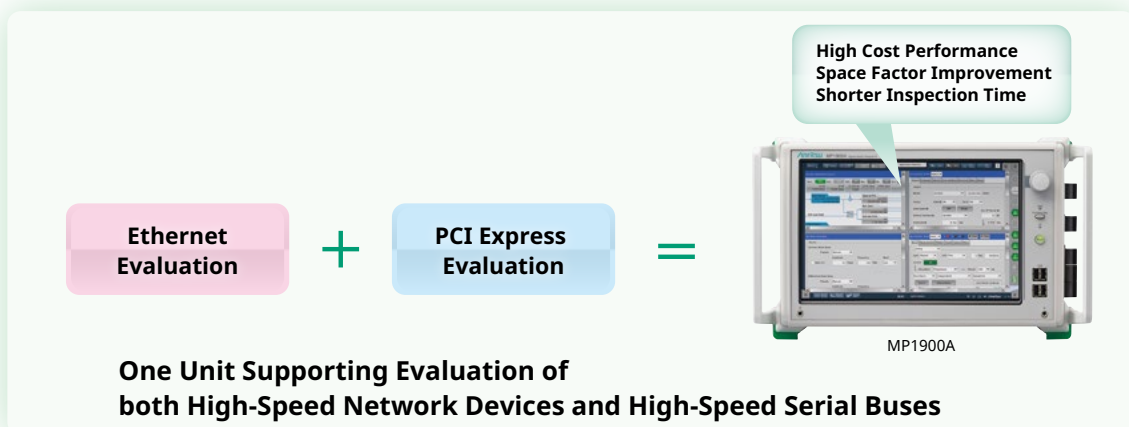
100 GbE/200 GbE/400 GbE/800 GbE, CEI-25G/28G/56G/112G, InfiniBand EDR/HDR, Fibre Channel
 PCIe 1-7, CXL2/3, Thunderbolt 1/2/3/4, USB3.2/4 v1/4 v2, SAS-3/-4, DP1.4/2.0/2.1, DDR5
 Optical module, SERDES, AOC, High-speed Interconnect

Excellent Expandability

All-in-One Support for Evaluating Next-Generation NRZ/PAM4 Network Interfaces and High-Speed Serial Buses

The Signal Quality Analyzer–R MP1900A is a modular Bit Error Rate Tester (BERT) supporting equipment external interfaces, such as next-generation Ethernet, by installing a pulse pattern generator (PPG) for outputting high-quality multi-channel NRZ/PAM4 signals over a wide bandwidth, a high-sensitivity input error detector (ED), Jitter modulation sources for Jitter Tolerance tests, etc.

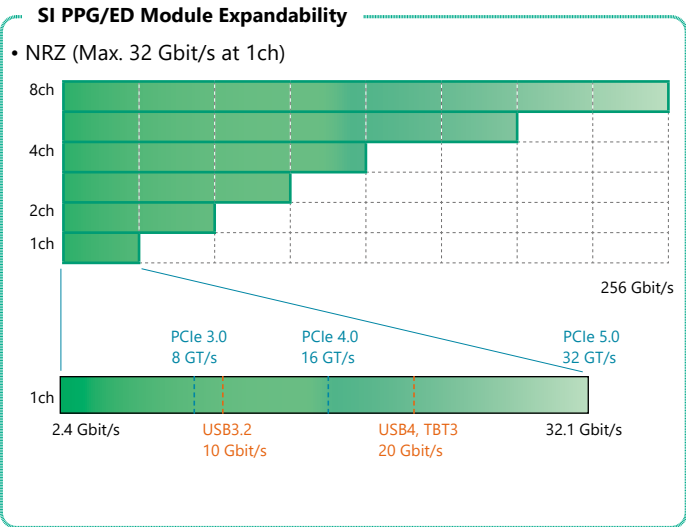
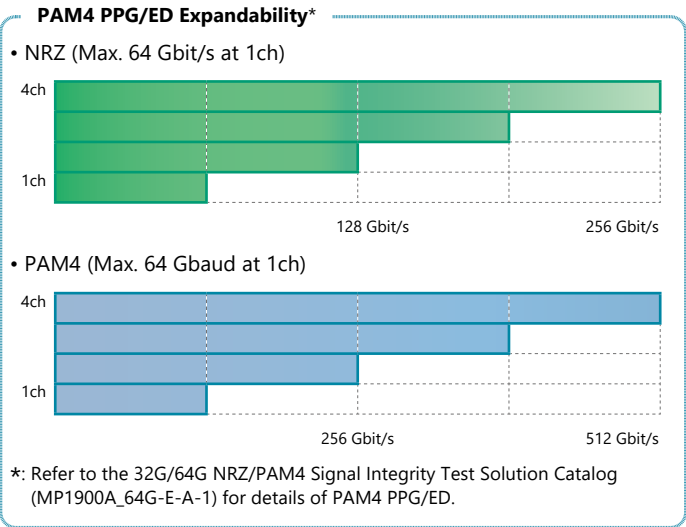
Additionally, optional noise generation and 10Tap Emphasis functions can be installed for Voltage Noise Tolerance tests, etc., and installing the High-Speed Serial Data Test Software software enables efficient design evaluation for increasingly faster PCIe, CXL2/3, USB, Thunderbolt, SAS, DDR5 and DP receivers.



Excellent Expandability

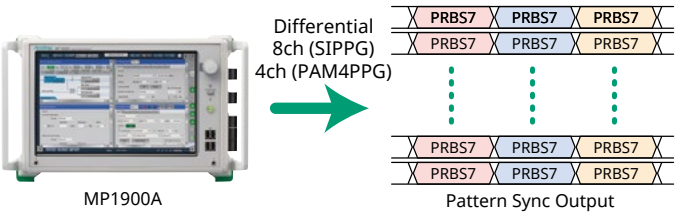
Easy Flexibility for Multi-Channel Measurements at Various Transmission Rates and Formats

400 GbE is the standard for the next generation of large-capacity transmissions but it is still unknown how much further data traffic will grow. To cope with this data traffic growth, in addition to speeding-up NRZ signals and introducing multi-channel signalling, introduction of PAM4-format signals is also progressing. To facilitate this change to multi-channels and the new PAM4 signals, the MP1900A series is an 8-slot modular instrument that can be easily customized by selecting and adding required function modules. This flexible expandability supporting the latest communications methods ensures both efficient R&D investment and the fastest time to market.



In addition to installing PPG, ED, and noise-generation modules in the 8-slot main unit, existing modules for the previous MP1800A series can also be installed. A combined total of up to four PPG and ED modules can be mounted in one MP1900A. The 21G/32G bit/s SI PPG/ED modules support selection of both one and two channels, enabling up to 8-channel measurement for both the PPG and ED. The PAM4 PPG and ED modules are configured with one channel per module, allowing up to four PPG or ED channels to be implemented simultaneously in one main unit. Moreover, the pattern for each channel can be synchronized, providing an ideal solution for evaluating DAC, MUX and DEMUX devices as well as for crosstalk and skew tolerance tests.

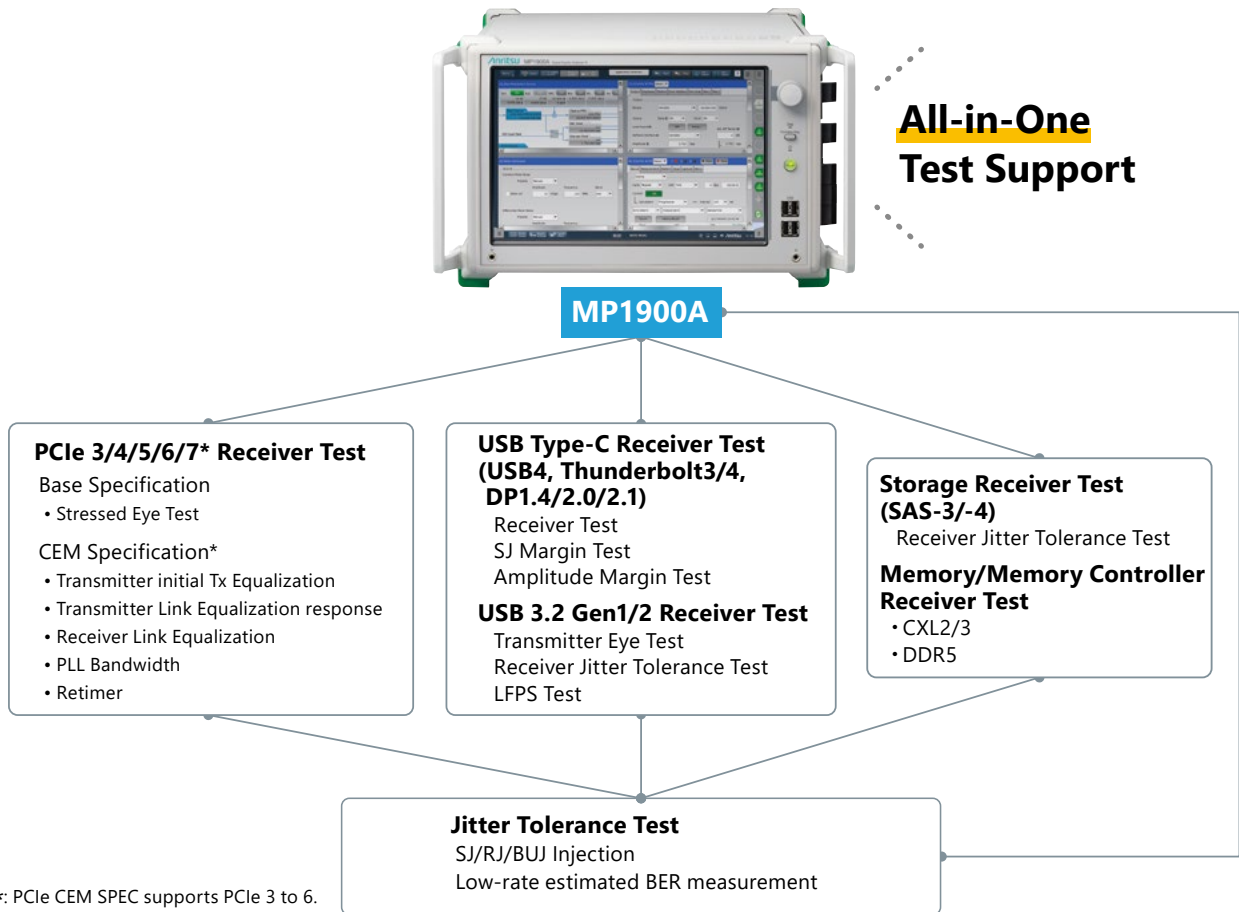
*: Refer to the MP1900A Selection Guide (MP1900A-E-Z-1) for details of the supported multi-channel configurations and module combinations. Consult our business sales representative for use of other module configurations not described in the MP1900A Selection Guide.



Next-Generation High-Speed Digital Interface Receiver Test

The growth of IoT and Cloud computing applications is driving the need for digital equipment with high-speed serial interfaces handling large data volumes. To meet this need, the PCI Express (PCIe) and USB interfaces used by this digital equipment are transitioning to both next-generation PCIe 6 supporting speeds up to 64 GT/s as well as to Type-C USB3.2 Gen2 supporting 10 Gbit/s and USB4 supporting 20 Gbit/s, which is also compatible with Thunderbolt.

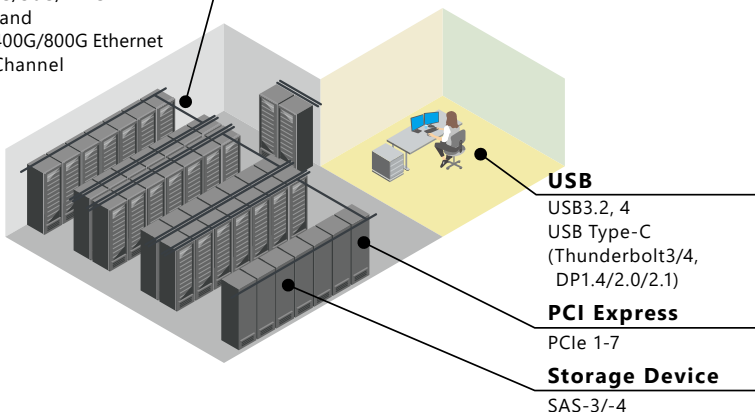
The MP1900A is a wideband BERT with a built-in Gbit/s-class PPG, ED, and Jitter/Noise addition functions as well as application software supporting measurement of next-generation, high-speed digital-interface standards (CEI-28G/56G/112G, InfiniBand, 100G/400G/800G Ethernet, Fibre Channel, Thunderbolt, PCIe, CXL, USB, SAS, DP, DDR) from development through to manufacturing.



Target Applications

General Interfaces

CEI-28G/56G/112G
InfiniBand
100G/400G/800G Ethernet
Fibre Channel



Various Applications

Internal and external interfaces, such as Ethernet, PCIe, SAS, and DDR5, are supported along with USB3.2, 3.4, and Thunderbolt via USB Type-C connectors and cables, and Display Port.

MP1900A supports PCIe 3.0, 4.0, 5.0, 6.0 and 7.0 as well as SAS using the same configuration.

Full Automation Software

Automation software for automating receiver tests of high-speed serial bus interfaces controls the MP1900A (PPG/ED, noise signal source, variable ISI channel) and real-time oscilloscope to automate calibration of signals required for complex operations, Jitter Tolerance tests, and creation of reports. The high-reproducibility, easy measurements greatly reduce the work load of test engineers.

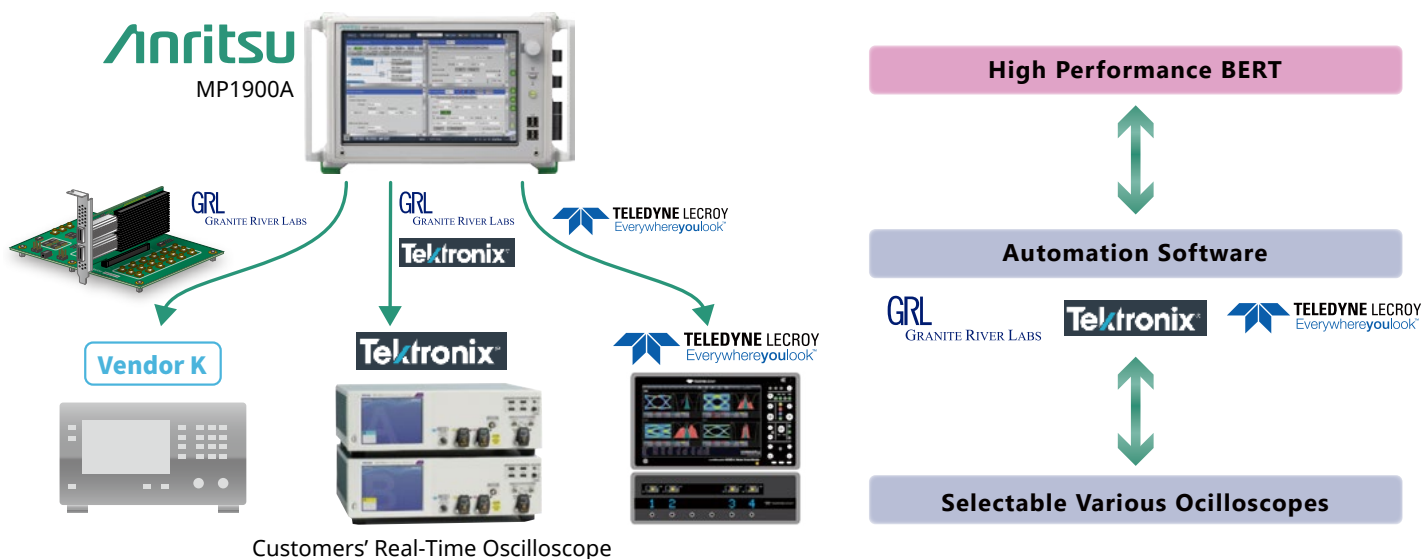
Features

- Controls each measuring instrument to simplify calibration, measurement conditions settings, and test execution
- Calibrates test signal and executes receiver test with high reproducibility
- Automates standards-compliant Jitter and amplitude Pass/Fail evaluations
- Selectable Various Oscilloscope

Selectable Various Oscilloscope

Real-time oscilloscopes from the main makers can be used in combination with the MP1900A to calibrate test signals, helping cut capital investment costs by making efficient use of owned assets.

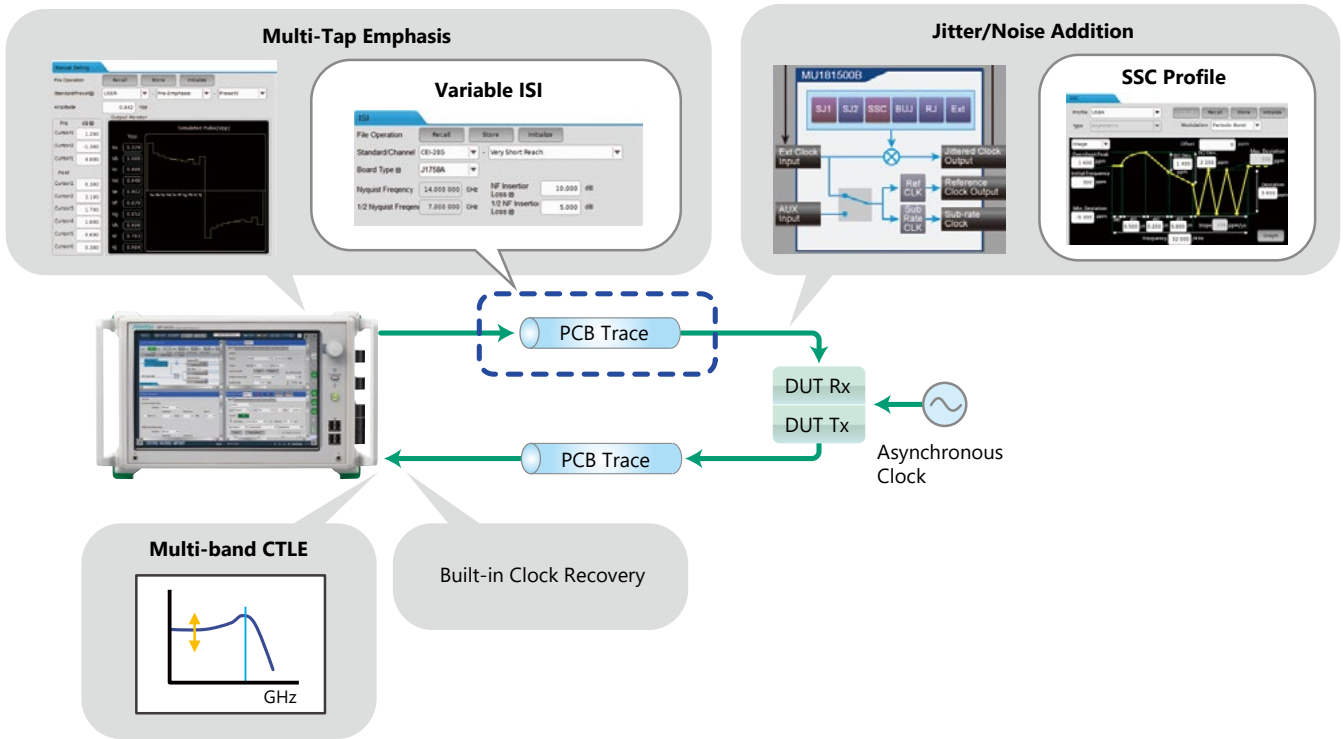
Refer to the Selection Guide (MP1900A-E-Z-1) for the combination of supported real-time oscilloscopes and automation software.



Signal Integrity Evaluation

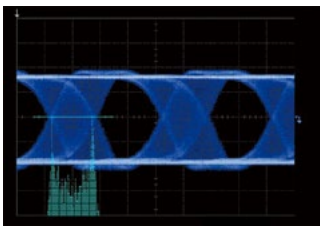
Strengthened Signal Integrity Evaluations in Addition to High performance NRZ/PAM4 BERT and Noise Generator Modules

Emphasis and equalizer functions are built-in to correct transmission path losses and assure signal integrity as signals become faster and as high-speed devices use lower signal levels to help reduce power consumption.

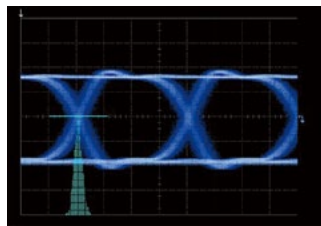


Jitter/Noise Addition

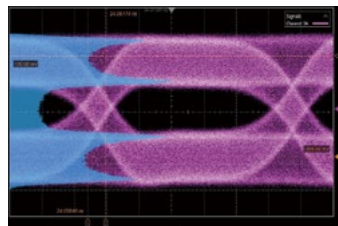
To perform DUT receiver stressed input tolerance tests, the BER is measured under the worst conditions using a stressed signal with added jitter and voltage noise. Using the MP1900A series with the Jitter Modulation Source MU181500B, Jitter Tolerance Test MX183000A-PL001 software, and Noise Generator MU195050A/MU196050B for adding CM/DM/White Noise supports receiver tolerance tests in conformance with the various interface standards. The MP1900A series offers strong support for receiver stressed input tolerance tests by generating high-quality signals before jitter and noise addition as well as for adding high-linearity jitter and noise.



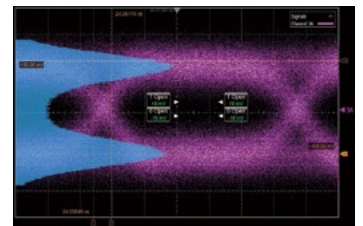
Sinusoidal Jitter (SJ)



Random Jitter (RJ)



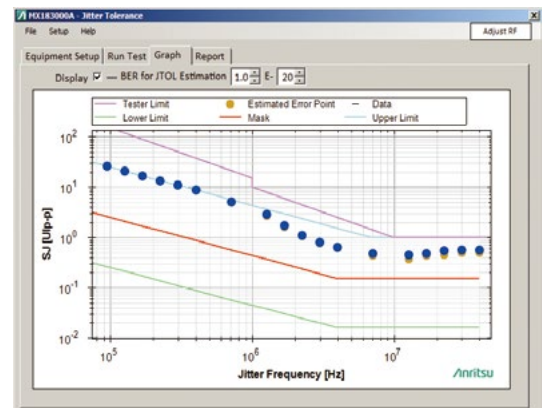
CM/DM Noise



White Noise

Jitter Tolerance Test Function (MX183000A-PL001)

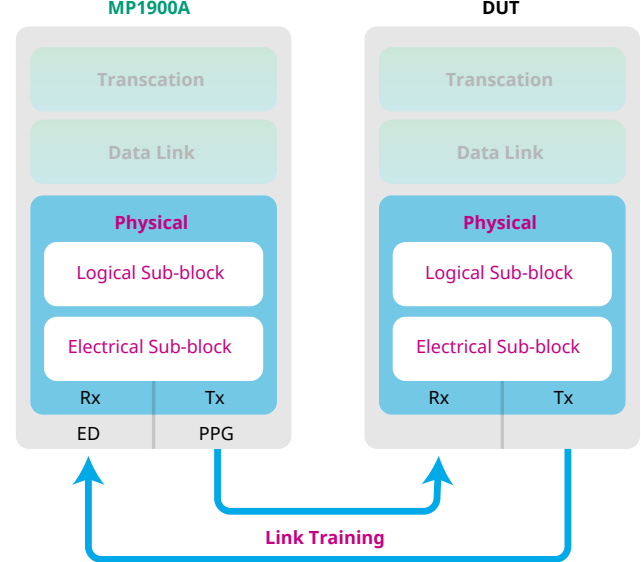
- High-versatility Jitter Tolerance measurements
- PHY Device Jitter Tolerance tests by impressing SJ/RJ/BUJ
- Standards-compliant Mask measurements
- Fast measurement times using low error rate estimation function, such as 1E-12 and 1E-15
- Tolerance measurements versus device characteristics using four Binary, Upward, Downward, Binary + Linear methods



Low Error Rate Estimation BER Measurements

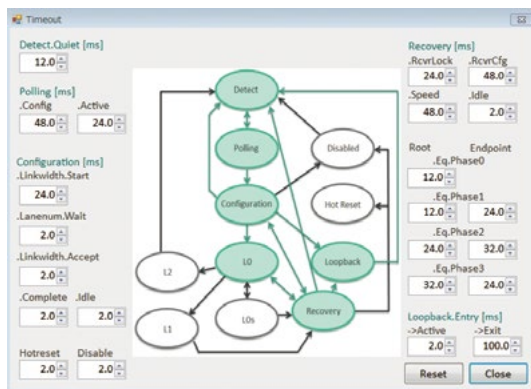
The MP1900A PCI Express/USB functions have Protocol Awareness with a Link Training function required for evaluating the PHY layer as well as an analysis function for detecting each LTSSM state transition to help troubleshoot faults. When more detailed debugging is required, the training sequence generation timing can be adjusted using the Sequence Editor function (MU195020A-x50/x51).

Moreover, combination with the Jitter Tolerance Measurement function (MX183000 A-PL001) supports consistent receiver tests of high-speed serial interfaces.

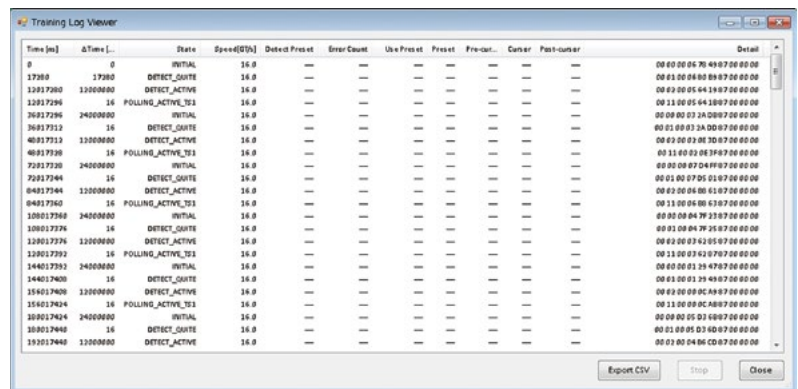


- Tx LEQ: Transmitter Link Equalization response Test
- Rx LEQ: Receiver Link Equalization Test
- Receiver Jitter Tolerance Test

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PCIe Link Training State Transition

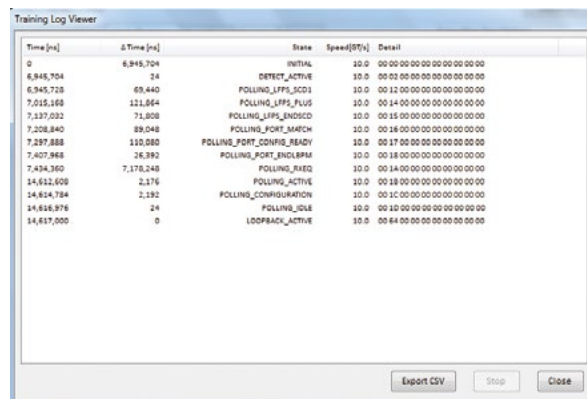


LTSSM Log of each LTSSM State Transition

L73004 Sermons



USB Link Training State Transition



LTSSM Log of each LTSSM State Transition

Sequence Editor (PCIe1 to 6, USB3.2, CXL2/3, Multi-channel)

Sequence Editor (MU195020A-x50/x51, MU196020A-x51/x52/x56, MU196040B-x51)

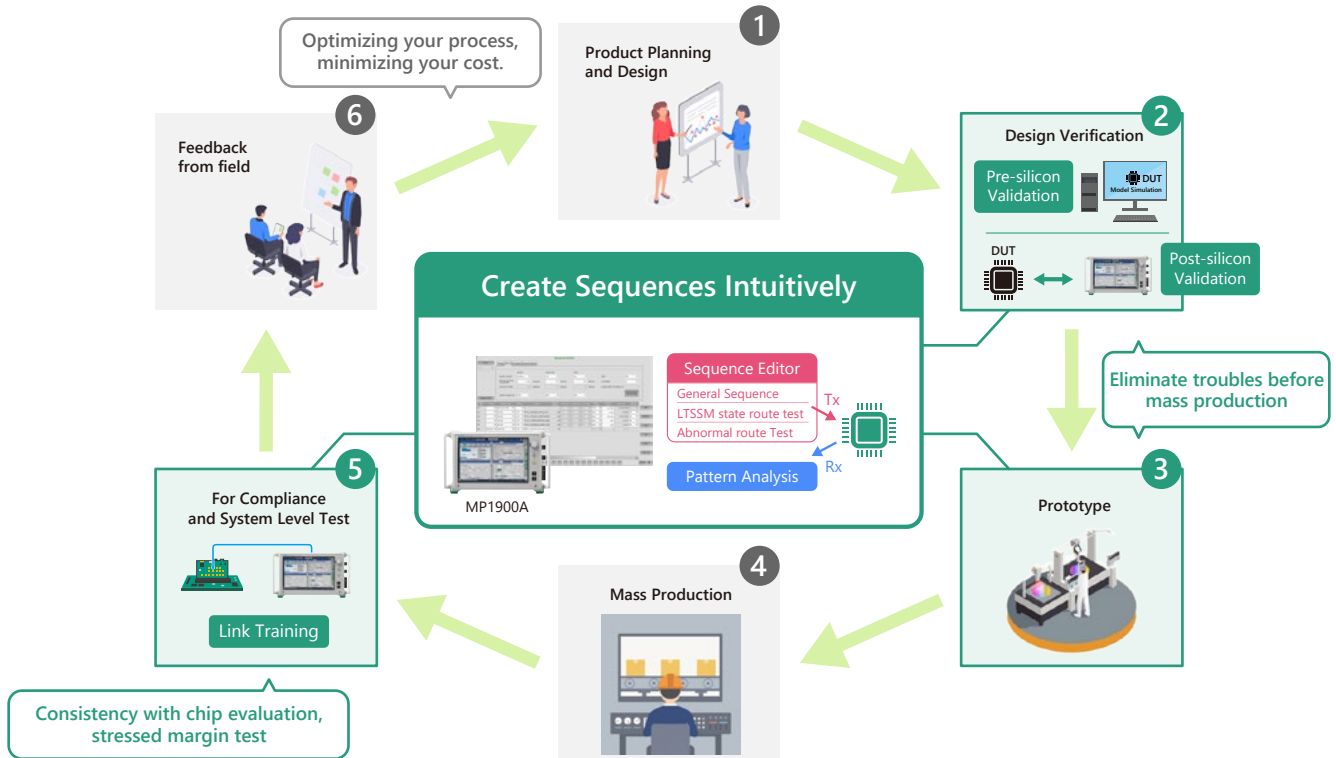
Reproduce Real-World Usage Environments using Sequence Editor to Facilitate Early Resolution of Potential Issues

Addressing High-Speed Bitrate Issues

Increasing bit-rate speeds make differentiating between physical layer errors and protocol errors more complex, which increases the burden of verification and debugging. Sequence Editor helps speed-up debugging by analyzing and isolating these errors efficiently.

Solving Challenges Beyond Compliance Testing in Multi-Channel Environments

By supporting not only 1 Lane but also 2- and 4-Lane configurations, Sequence Editor can reproduce both Compliance Test environments as well as actual market usage environments. This enables identification and resolution of potential issues in advance by reproducing load conditions according to real-world usage environments, thereby mitigating troubles after product launch.

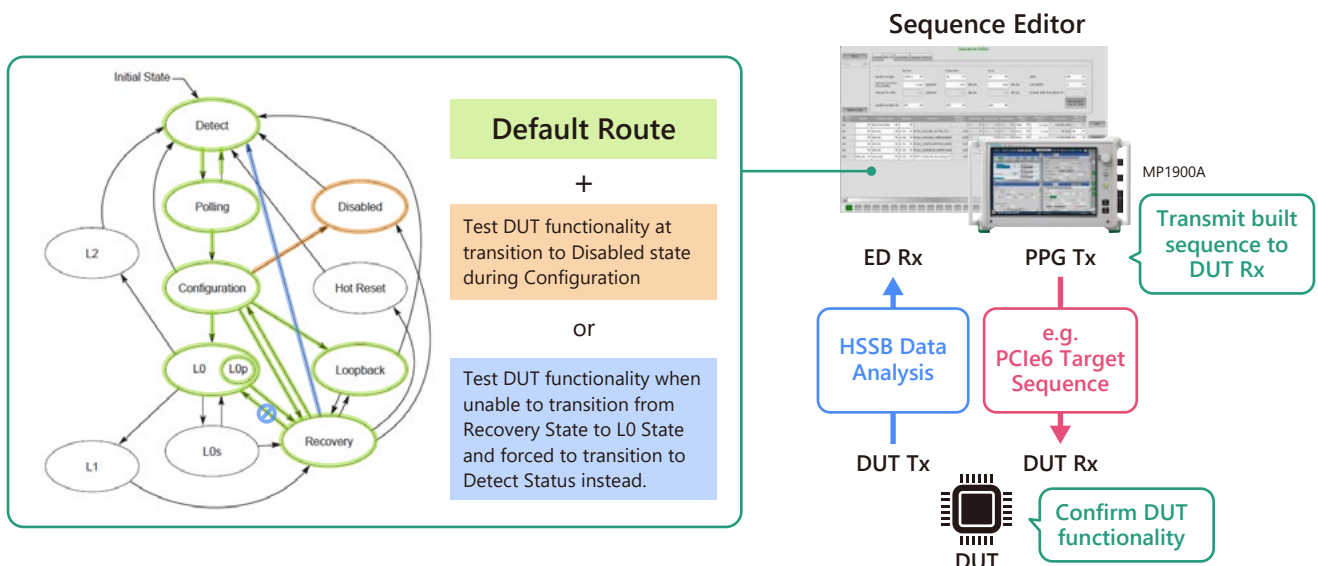


User-Friendly Sequence Editor Supporting PCIe 1 to 6, CXL2/3 and USB 3.2, with HSSB Data Analysis Function

Transmission Pattern Customization and Advanced Debugging Support

Users can use the Sequence Editor function freely to create and edit transmission patterns for PCIe 1-6 and USB 3.2.

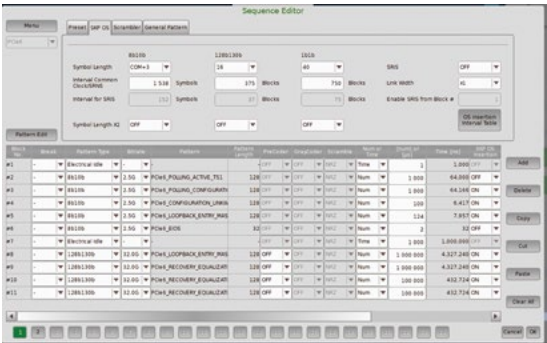
Users can reproduce actual Link Training behavior by using LTSSM logs and can debug Link Training easily by changing the conditions of states that are not operating normally. Data received from the DUT can be displayed easily using the HSSB Data Analysis function.



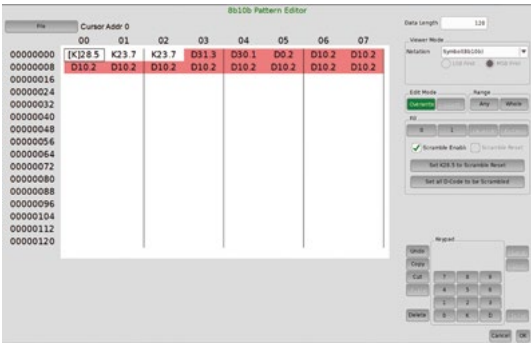
Sequence Editor (PCIe1 to 6, USB3.2, CXL2/3, Multi-channel) (cont'd)

Intuitive and Excellent Usability

Sequence Editor features a dedicated user interface for PCIe 1 to 6, CXL2/3 and USB 3.2, enabling intuitive sequence creation. Both symbol-level editing for 8b/10b, 128b/130b, 1b/1b, and NULL Flits, as well as scrambler settings for arbitrary symbols are easily configured. The ability to customize ordered set information and transmission counts and sequences makes simplifies creation of test cases, significantly contributing to higher test quality and reproduction of bugs.



Sequence Editor Screen



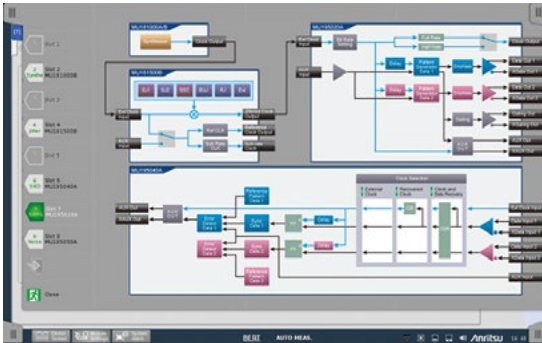
8b/10b Pattern Editor Screen (Scrambled)

Easy to Use Operability

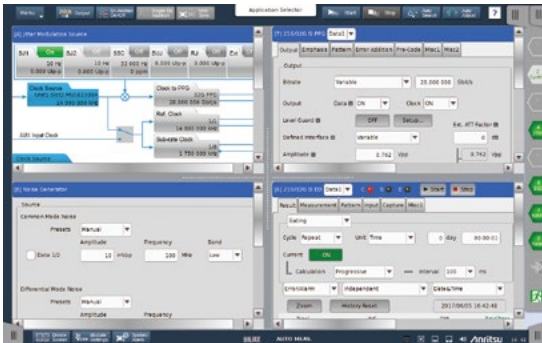
Improved Operability with New System View, User Interface, and Multi-windows

The MP1900A features easy intuitive operability based on a redesigned GUI and large 12.1-inch touch-panel LCD. Fast mistake-free settings help shorten measurement times.

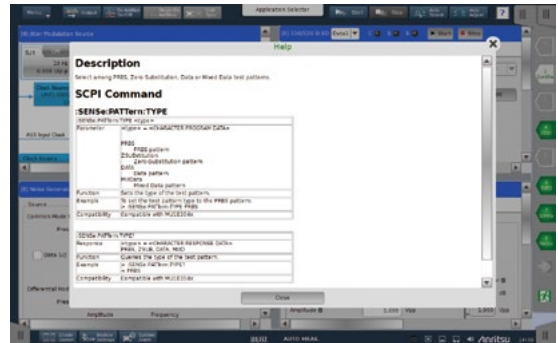
The newly developed system view displays system functions as easy-to-understand blocks, supporting smooth settings and easy operation of each module.



Four split screens help improve the efficiency of multi-channel measurements.



The Help function displays the remote commands corresponding to GUI operations, which simplifies automated system configurations.

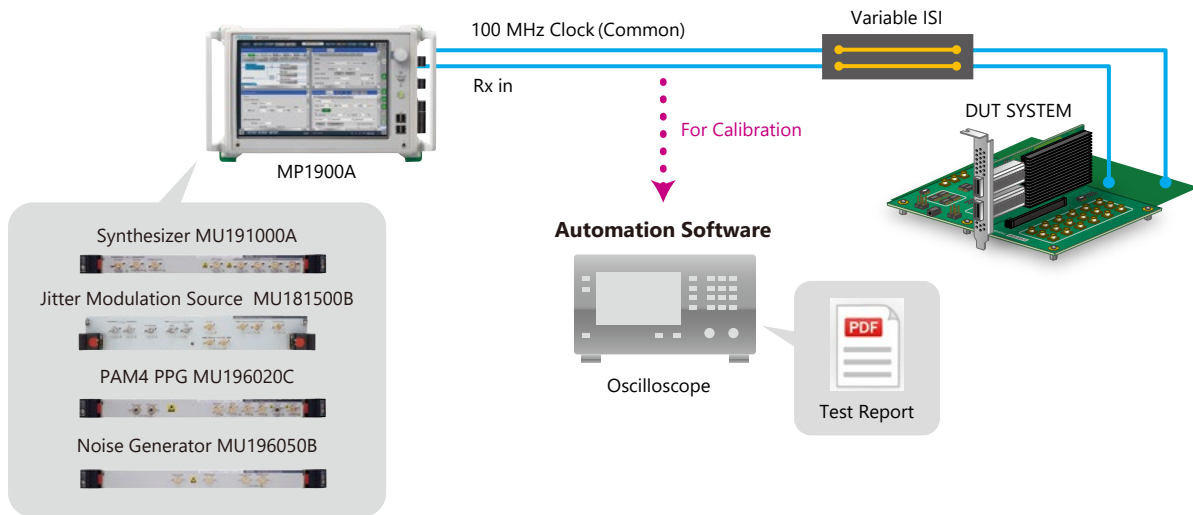


Application Examples

PCIe7 Base Specification Receiver Test

PCIe7, like PCIe6, continues to use the PAM4 signal format, while doubling the data rate from 64 GT/s to 128 GT/s. This makes the effects of channel loss and jitter more pronounced than ever and signal quality margins more stringent than for PCIe6. Evaluation based on the PCIe7 Base Specification requires measuring instruments capable of stably generating high-quality PAM4 signals.

PCIe7 Base Rx Test



Required Items

- Generation of high-quality waveforms that meet the PCIe7 requirements
- Jitter and noise injection tests
- Automation for shorter evaluation times and higher efficiency

Automation for Shorter Evaluation Times and Higher Efficiency

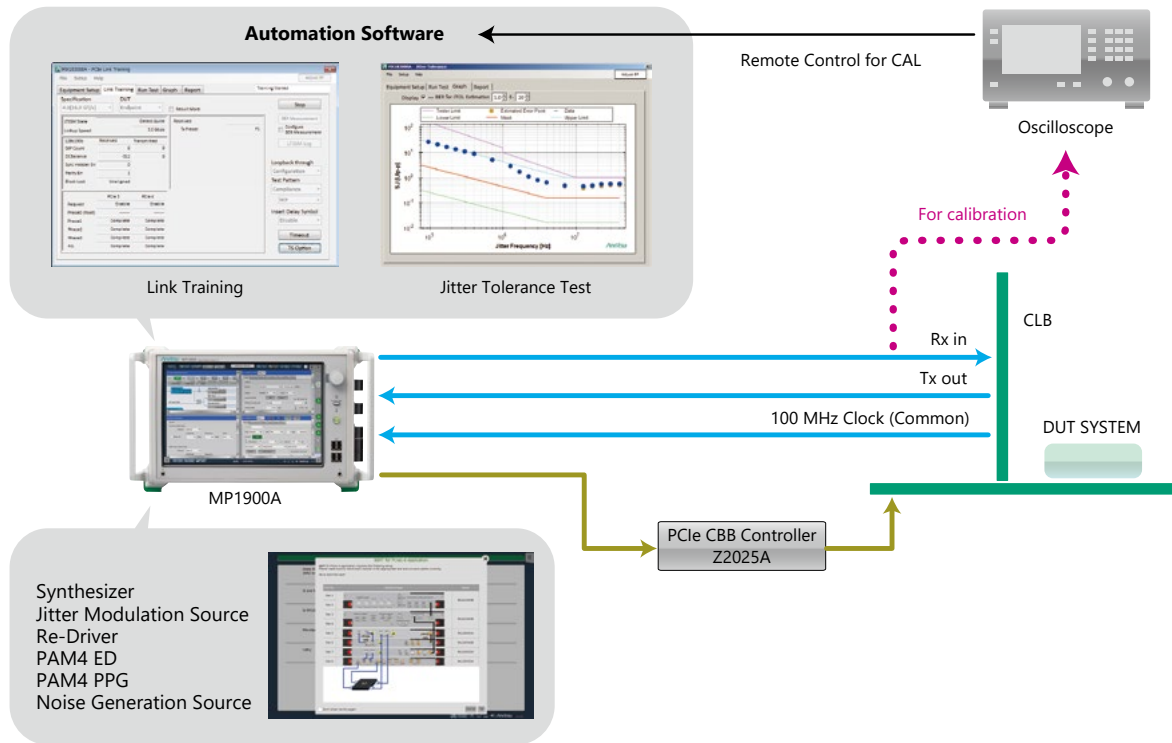
Provides the function to automate stress signal calibration and jitter tolerance tests using automation software.

Generation of High-quality Waveforms that Meet the PCIe7 Requirements

Generates high-quality waveforms with an SNDR of 35 dB, residual jitter of 108 fs, and Tr/Tf of 6.0 ps, supporting stable Rx tests.

Application Examples

PCIe 4/5/6 CEM Specification Receiver Test



Video

- [PCIe 6.0 Compliance Test](#)
- [PN Skew Evaluation Solution Demonstration Video](#)
- [PCIe® 6.0 RxLEQ Tests Demonstration Video](#)

Required Items

- Link Training function
- Jitter Tolerance Test
- Emphasis Effect Validation
- Supports Common/Separate Clock Architecture

PCI Express CEM Solution Features

- All-in-one support for Protocol Awareness PCIe 1 to 6 receiver tests
- Event Trigger Function for Tx/Rx Link Equalization Test
- 64.2 Gbit/s (32.1 Gbaud, PAM4) high-speed BERT
- Low-intrinsic-jitter and high-quality output waveform, high-sensitivity ED
- Link Training, Link Equalization and LTSSM analysis functions
- 4Tap Emphasis function
- CTLE and Clock Recovery functions
- CMI and DMI Noise addition, and SJ, RJ, BUJ, and SSC Jitter Addition functions
- Full automation including CBB control

PCIe CBB Controller Z2025A

The DUT must be reset and transitioned to the Initial state before starting Link Training.

The PCIe CBB Controller Z2025A fully automates control of Rx LEQ and Tx LEQ using the Power Reset and Power Cycle control pins implemented by PCIe CBB 4.0 (Compliance Base Board 4.0).

PCIe Re-Driver MU196060A

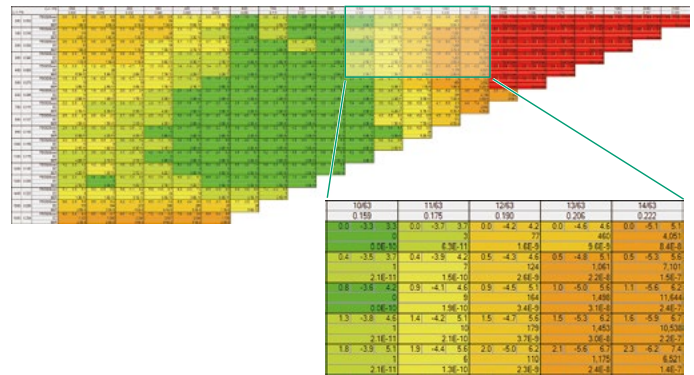
The Rx test requires establishment of a DUT return path. If the return-path physical loss is greater than about 18 dB (for PCIe5 NRZ), connection of an external equalizer is recommended since there is a risk of detecting errors in the return path.*

The return path can be established by using MU196060A.

*: The Re-Driver module (MU196060A) is required when using the PAM4 ED.

Matrix Scan Function

To secure high-quality communications with the Link partner, the best combination of the Tx-side EQ and Rx-side EQ must be selected. The Matrix scan function scans for the best Tx EQ setting at the RX to find the best setting automatically at the receiver.



Link Training Function (MX183000A-PL021/025/026)

The PCIe Rx test requires establishing a link between the test instrument and DUT with a transition to the LTSSM state before testing the DUT BER.

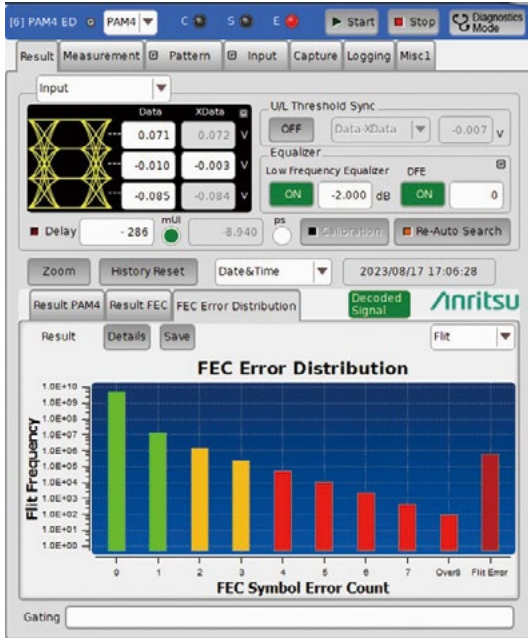
By using the PCIe Link Training option, the MP1900A establishes the necessary link required by the CEM Spec. for DUT BER measurement.

Additionally, the LTSSM Analysis function supported by this option facilitates easy troubleshooting if a link with the DUT is not established.

Application Examples

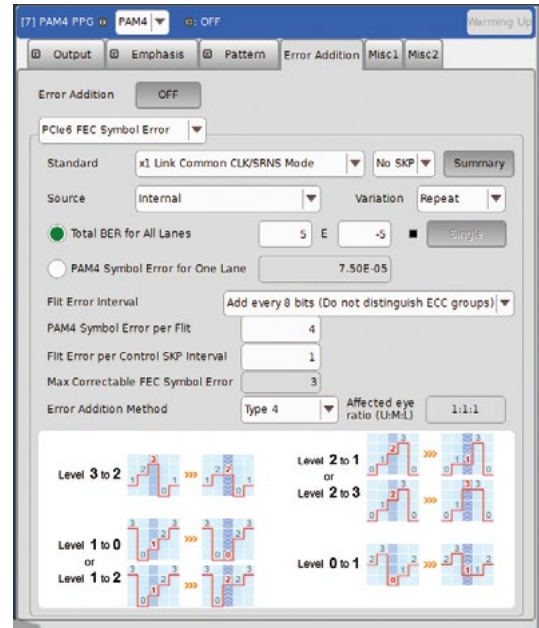
Real-time measurement of FEC Uncorrectable errors

FEC Error Distribution function for measurement and real-time display of correctable and uncorrectable errors. This allows accurate evaluation of the correction capability by FEC even at receiver tests with FBER (First Bit Error Rate) 1E-6 threshold.



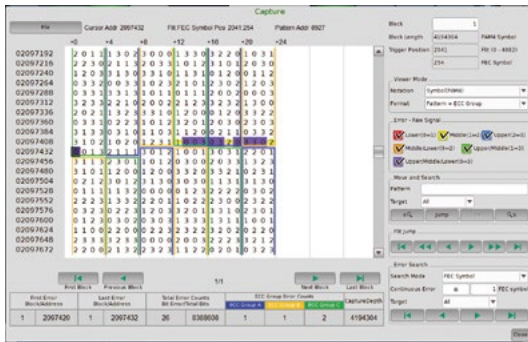
Supports verification of DUT error correction capability using error addition

PPG Error Addition function to add various types of error to FLIT (Flow Control Unit) data, helping verify the DUT FEC capability under stress conditions.



FEC Capture

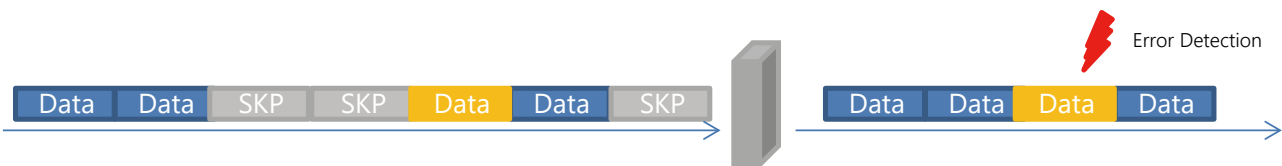
FEC Capture function to capture Burst and other errors causing FLIT loss, supporting analysis of infrequent system failures and identification of cause, which can be time-consuming otherwise.



SKP OS Filtering

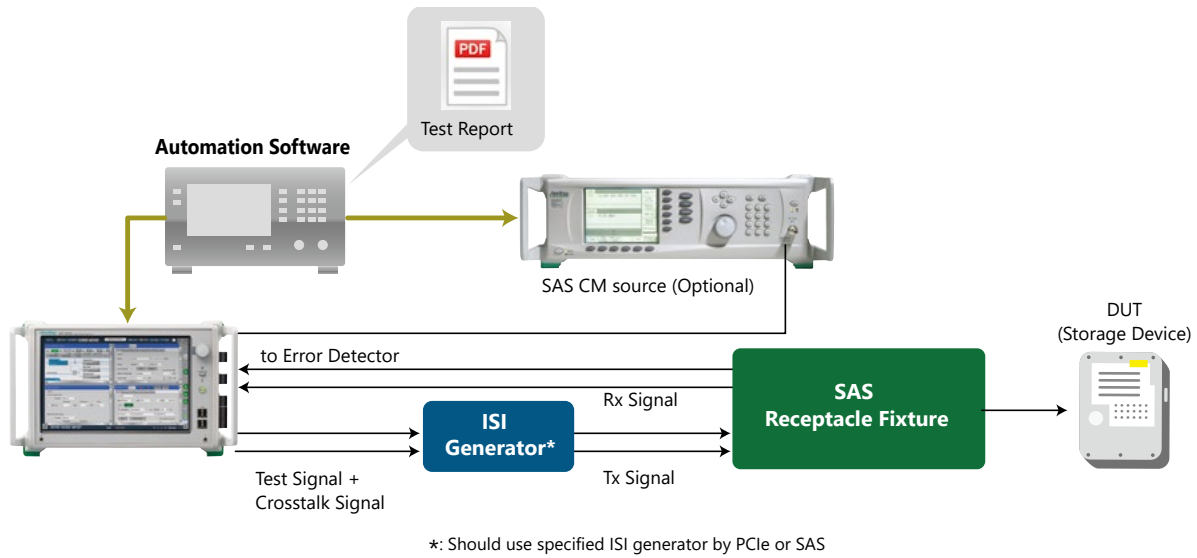
The SKP Symbol used to absorb frequency deviation must be excluded from the target BER measurement. The Error Detector automatically discriminates between Data and SKIP symbols to measure the true BER.

This function supports PCIe 1 to 6.



Application Examples

SAS-3/-4 Receiver Test



Required Functions

- 12 Gbit/s to 22.5 Gbit/s BERTS
- Stressed Signal Calibration and Test
- Jitter Margin Test

Wideband BERTS

The same configuration covers SAS-3 (12 Gbit/s), SAS-4 (22.5 Gbit/s) and PCIe 1 to 5 measurements.

Receiver Test

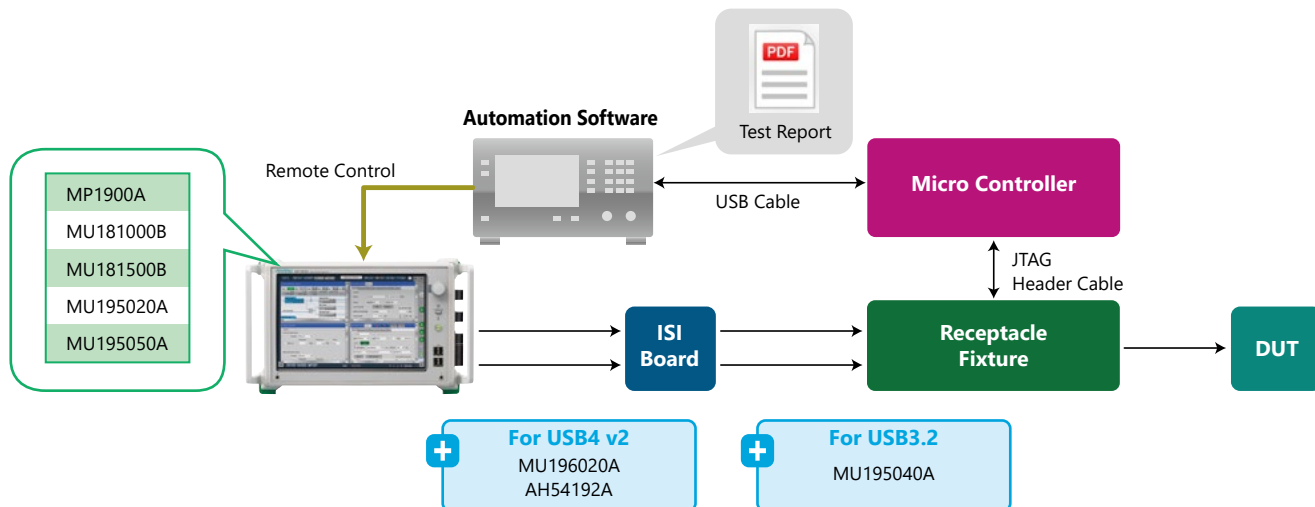
Stressed signal calibration and measurements can be automated using the automation software to shorten the design stage by cutting Compliance test times and improving measurement reproducibility.

Jitter Margin Test

The automation software supporting jitter tolerance tests helps simplify receiver performance evaluations required by storage, HBAs, and ICs.

Application Examples

USB4 v1, v2, Thunderbolt3/4 Receiver Test



Required Functions (USB4 v1, Thunderbolt3/4)

- 20 Gbit/s PPG
- Stressed Signal Calibration Function
- Jitter Tolerance Function

Required Functions (USB4 v2)

- USB4 v2 25.6 Gbaud (NRZ/PAM3)
- Stressed Signal Calibration Function
- Frequency Variation Profile Function

Supports USB Type-C

Supports specified bit rates.

USB4 v1 (NRZ)	20 Gbaud
USB4 v2 (NRZ/PAM3)	25.6 Gbaud
Thunderbolt3/4	20.625 Gbaud

Stressed Signal Calibration

Automation Software supports automatic stressed signal calibration as specified by USB Type-C.

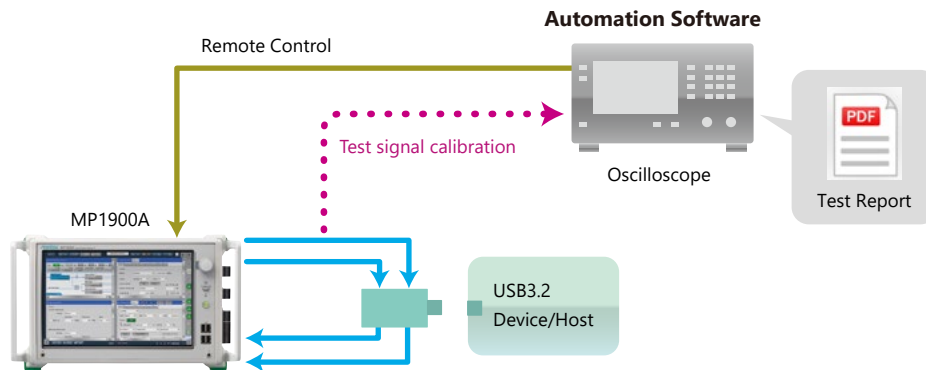
Stressed Signal Input Test

- Supports Rx BER measurements required by Host/Device compliance test
- Supports automatic Rx test using Tenlira scripts
- Supports automatic Pass/Fail measurement for Rx stressed signal tests

Receiver Test

Calibration, TER test (USB4 v2) and BER test (USB4 v1, Thunderbolt3/4) can both be automated using the automation software. Automation helps cut design verification times.

USB 3.2 Gen1/2 Receiver Test



Required Functions

- Loopback State Setting Function
- Jitter Tolerance Function
- Automatic Receiver Test Function
- Link Training Function

Link Training Function

Automated evaluation of BER required by the Compliance Test can be configured using the MX183000A and MX183000A-PL022/023 option.

- Supports transition to Loopback mode used for USB 3.2 Gen1/2 $\times 1$ and $\times 2$ device evaluation
- Supports troubleshooting using LTSSM analysis function when unable to transition to Loopback mode
- Detailed troubleshooting analysis is supported by changing the timeout for each state
- Supports easy troubleshooting when problems occur when changing timeout at each state by using LTSSM trigger to capture transient signals using oscilloscope when state does not transition normally

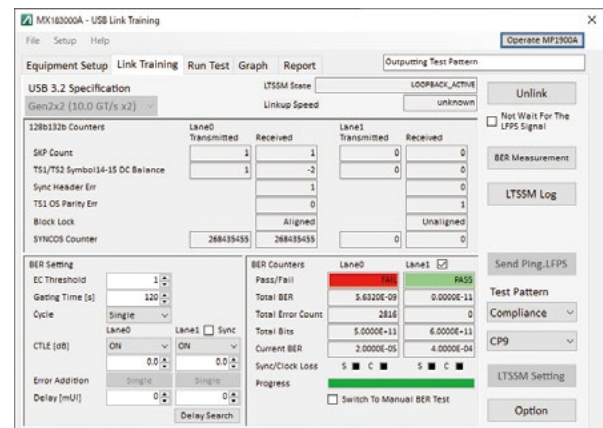
Receiver Jitter Tolerance Test

Jitter Tolerance tests can be automated using the MX183000A-PL001 software to help shorten the design validation time.

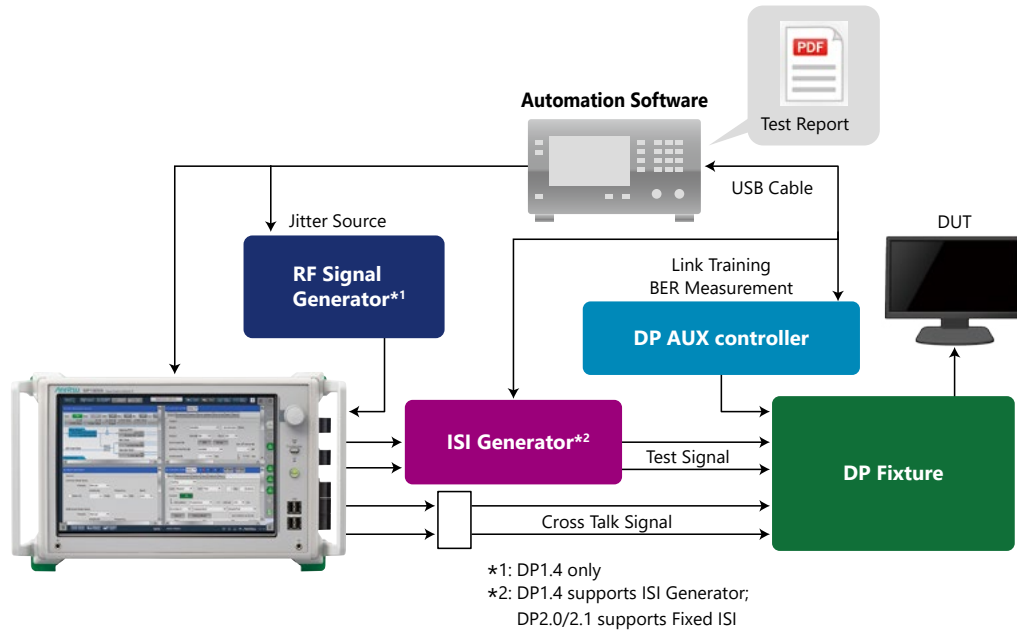
$\times 2$ Device Evaluation

Lane 0 and Lane 1 $\times 2$ devices can be evaluated simultaneously using the MX183000A-PL023.

Crosstalk effects can also be analyzed by impressing skew between lanes.



DisplayPort 1.4/2.0/2.1 Sink Test



Required Functions

- 2.7 Gbit/s to 20 Gbit/s PPG
- Stressed Signal Calibration and Test
- USB Type-C Alternative Mode Operation

Wideband PPG

One module covers RBR (1.62 Gbit/s)*, HBR (2.7 Gbit/s), HBR2 (5.4 Gbit/s), HBR3 (8.1 Gbit/s), UHBR10 (10 Gbit/s), UHBR13.5 (13.5 Gbit/s), and UHBR20 (20 Gbit/s).

Expandable up to 32 Gbit/s without hardware upgrade.

*: Can generate special RBR (1.62 Gbit/s) pattern

Sync Sensitivity Test

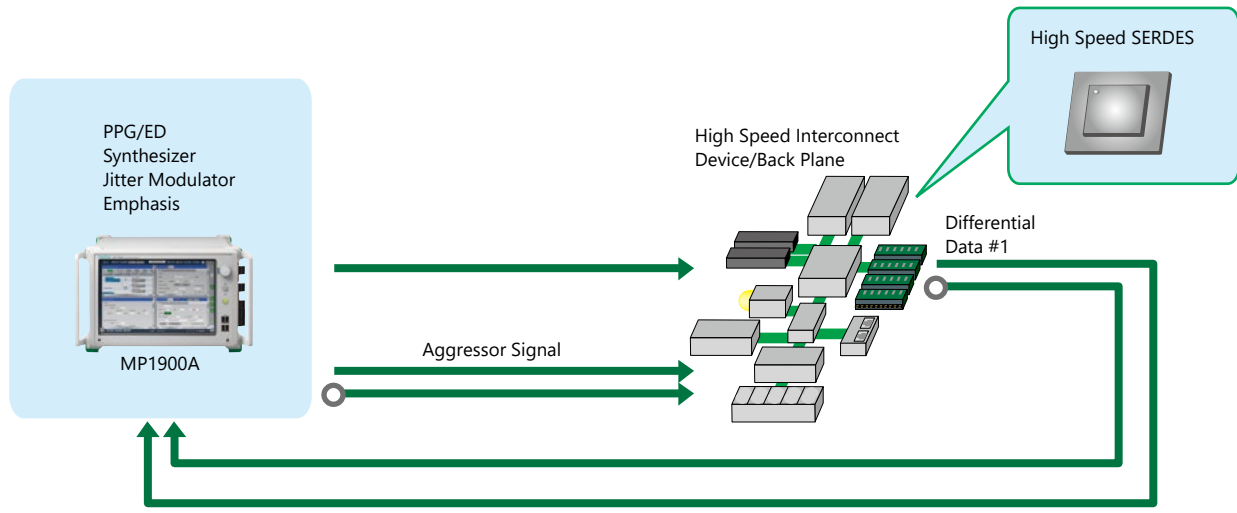
Stressed signal calibration and measurements can be automated using the automation software to shorten the design stage by cutting Compliance and Jitter Tolerance Margin test times and improving measurement reproducibility.

USB Type-C Alternative Mode

Measurement of the Alternative Mode transmitting Display Port signals using the Auto USB Type-C connector is supported.

Application Examples

High-speed Interconnect Evaluation



Required Test Items

- Multi-channel signal generation
- Jitter Tolerance test
- Emphasis efficiency check
- Crosstalk test

Multi-channel

Along with support for multi-channels, the bit rate of devices such as back planes of high-performance servers is becoming increasingly faster. The MP1900A supports generating both the Victim signal with controlling Emphasis and the Aggressor signal for crosstalk testing simultaneously. The MP1900A offers multi-channel measurements for TRx devices such as Transceiver, SERDES and Clock Data Recovery (CDR).

Jitter Tolerance Test

Jitter Tolerance tests supporting various standards can be run by simultaneously impressing SJ (2 tone), RJ, BUJ, and SSC up to 32.1 or 128 Gbit/s using the MX183000A-PL001 and MU185000B Jitter modulation sources.

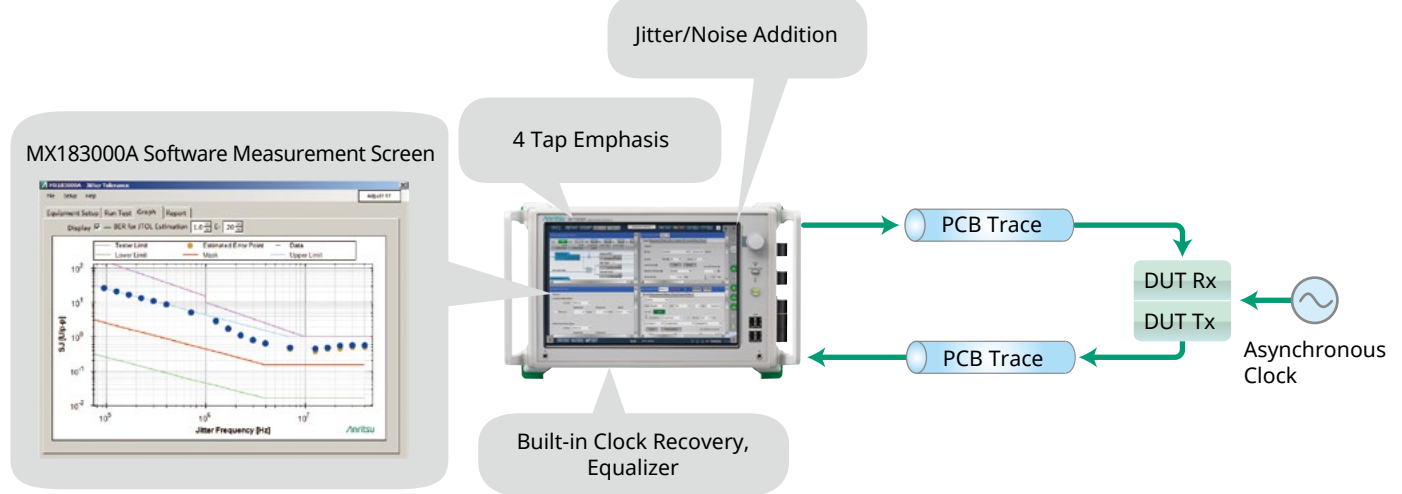
The Eye opening of signals passing through the back-plane is degraded by loss in the board traces.

Skew and Crosstalk Effect Check

Processing high speed digital signals requires both logic tests and actual equipment tests. The MP1900A supports both pattern synchronization and phase adjustment functions, permitting easy tests of Rx device skew tolerance and crosstalk effects.

Application Examples

PAM4 Signal Jitter Tolerance Test using One MP1900A



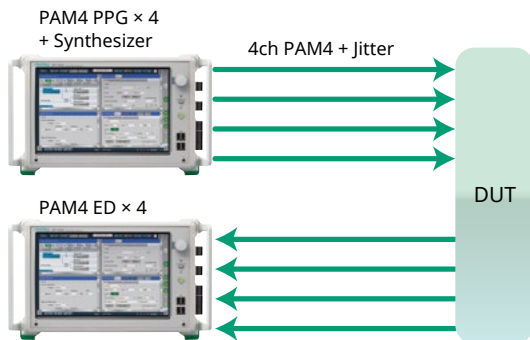
Required Items

- PAM4 BER measurement
- Jitter Tolerance Test

BER Measurements of 64-Gbaud PAM4 Signals

BER measurements can be performed in real-time using the PAM4 PPG and ED modules with no need for other external equipment*.

- All in one solution requiring no other external equipment
- Module with built-in clock recovery, equalizer
- Wide-range Emphasis function
- High-sensitivity data input
- Symbol BER evaluation



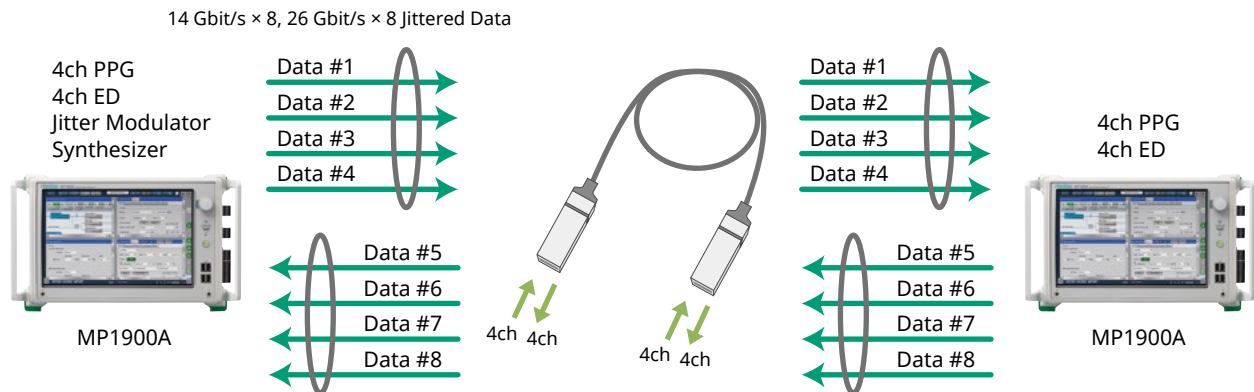
Jitter Tolerance Test

Testing the DUT receiver input stress tolerance requires BER measurements under severe conditions using a stressed signal with added jitter and noise. The all-in-one MP1900A series supports receiver stress tests for various interface specifications using the Jitter Modulation Source MU181500B for adding SJ, RJ, BUJ, and SSC simultaneously, the Jitter Tolerance Test MX183000A-PL001 software, and the Noise Generator MU195050A for adding CM/DM/White voltage noise. The MP1900A series provides strong support for high-quality signals prior to jitter and noise addition, as well as receiver stressed-signal tolerance tests using high-linearity jitter and noise addition functions.

*: Refer to the 32G/64G NRZ/PAM4 Signal Integrity Test Solution Catalog (MP1900A_64G-E-A-1) for details of PAM4 PPG/ED.

Application Examples

InfiniBand EDR (25.78G) AOC Evaluation



Required Test Items

- 8ch (4ch two ways) simultaneous BER measurement
- Crosstalk Test
- Jitter Tolerance Test
- Bathtub Jitter and Eye Diagram Analysis

8ch (4ch two ways) Simultaneous BER Measurement

The MP1900A supports up to eight PPG or ED channels simultaneously using SI PPG/ED modules. Additionally, up to four PPG or ED channels are supported simultaneously in one chassis using PAM4 PPG/ED modules.

QSFP Active Optical Cables (AOC) used by InfiniBand, etc., perform simultaneous transmission over a total of 8 channels using two-way transmissions over 4 channels. The MP1900A can incorporate up to 8 channels simultaneously in one main unit and can measure all channels at one time, offering excellent performance and shorter measurement times. Moreover, InfiniBand HDR measurement is also supported using PAM signals.

Jitter Tolerance Test

AOCs in data centers are using low input and output amplitude levels to cut power consumption costs, making it important to assure interconnectivity. With its high sensitivity data input and CTLE, the MU195040A supports reception of low-amplitude, low-Eye-opening Data signals and perform high-reproducibility DUT Jitter Tolerance tests.

Crosstalk Effect Confirmation

Implementing 20 Gbit/s class transmissions not only requires logic tests but also requires actual equipment verification tests. Since the MP1900A has both pattern synchronization and independent phase tuning for each channel, tests on items such as the effect of AOC crosstalk are implemented easily.

Bathtub Jitter and Eye Diagram Analysis

Bathtub Jitter Analysis (separate TJ, RJ, DJ) is supported by the built-in as standard Clock Delay function. Low bit error rates, such as 1E-12 and 1E-15, can also be estimated quickly from the change in bit error rate versus phase.

Automation Software Selection Guide

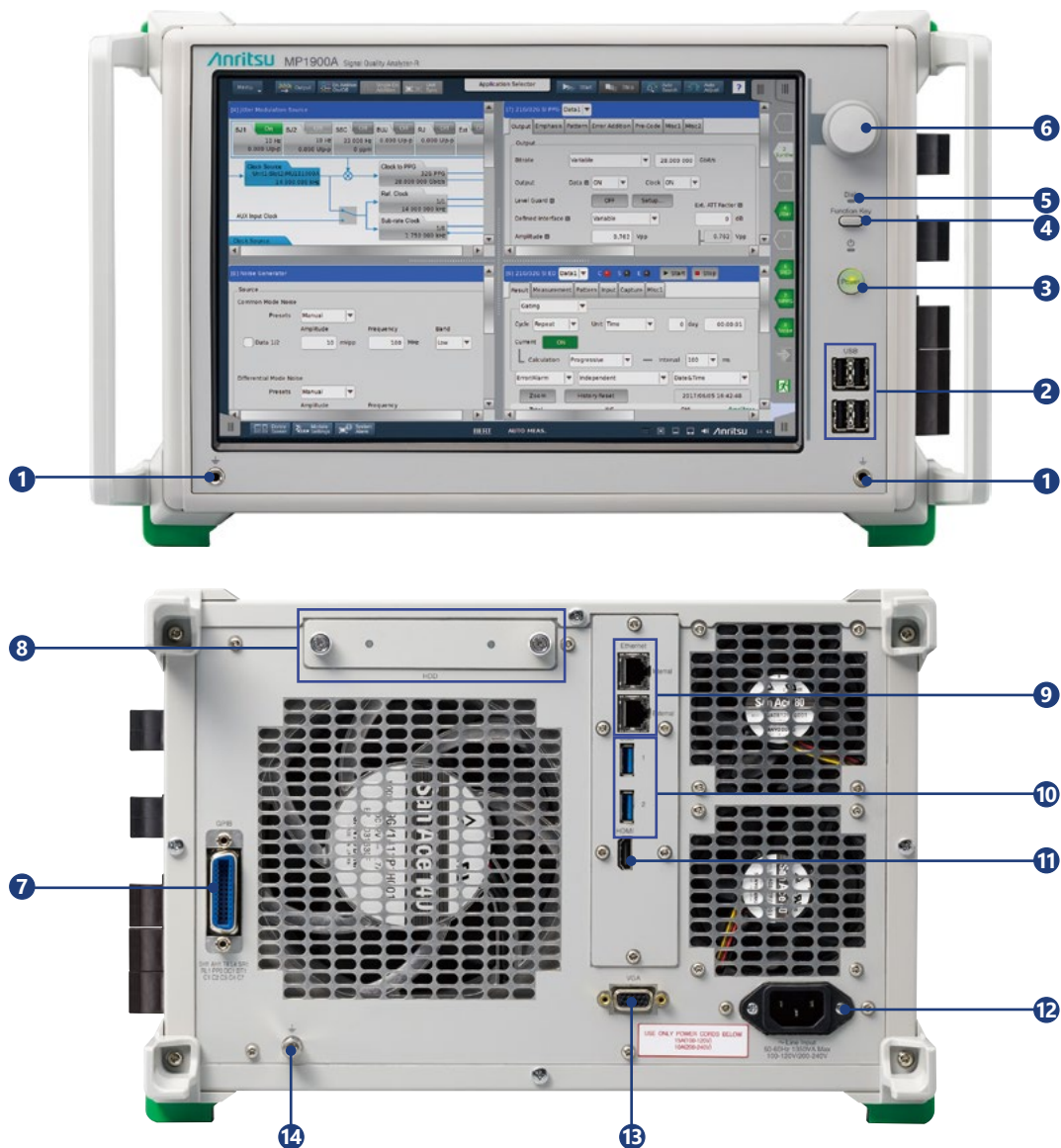
The MP1900A can execute the following receiver tests using automation software in combination with a real-time oscilloscope. Refer to the next page for option configurations required by the MP1900A. Refer to the Selection Guide (MP1900A-E-Z-1) for the supported combination of real-time oscilloscopes and automation software.

Interface Type	Compliance Test Item	
	Base Spec	Stressed Eye Test
PCIe3-7		
	CEM Spec*	Transmitter initial Tx Equalization Transmitter Link Equalization response (Tx LEQ) Receiver Link Equalization (Rx LEQ) PLL Bandwidth
USB3.2 Gen1/2	Transmitted Eye Test Receiver Jitter Tolerance Test	
USB Type-C (USB4, Thunderbolt3/4)	Receiver Test SJ Margin Test Amplitude Margin Test	
SAS-3/-4	Receiver Jitter Tolerance Test	
DP1.4/2.0/2.1	Sink Jitter Tolerance Test	

*: Supports PCIe3-6.

Signal Quality Analyzer-R MP1900A Panel Layout

Front/Rear Panel

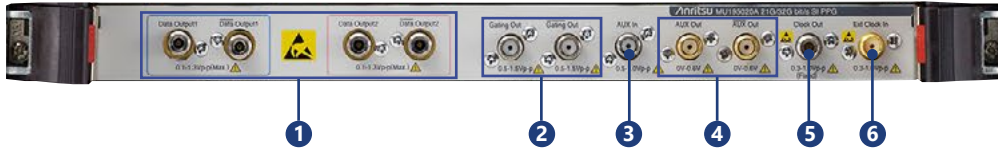


- 1 Ground Jack**
Wrist strap to discharge static electricity
- 2 USB Port**
Four USB2 ports for connecting peripherals
- 3 Power Switch**
Switches power on and off; Standby LED over power switch lights when power cord connected and Power switch set to off
- 4 Function Keys**
Keys for defining functions using software
- 5 HDD Access LED**
Lamp that lights during access to built-in HDD
- 6 Rotary Encoder**
Switch to increase/decrease numeric values by turning knob
- 7 GPIB**
GPIB Connector
- 8 HDD**
Slot for secondary 2.5" HDD
- 9 Ethernet Connector**
External: For Remote Control
(Internal: Reserved for future function expansion)
- 10 USB Port**
Two USB3.0 ports for peripherals
- 11 HDMI**
HDMI connector for displaying screens on external screen
- 12 Power Inlet**
Socket for connecting 3-pole power cord to supply 100 V(ac) to 12 V(ac) or 200 V(ac) to 240 V(ac) power
- 13 VGA**
VGA connector for displaying screens on external screen
- 14 Frame Ground Terminal**
Terminal for discharging electrostatic charges; connect DUT and common ground using ground strap

Signal Quality Analyzer-R MP1900A Panel Layout

Modules

21G/32G bit/s SI PPG MU195020A



- 1 Data Output, $\overline{\text{Data}}$ Output**
Connectors outputting differential Data and $\overline{\text{Data}}$ signals
- 2 Gating Out, $\overline{\text{Gating}}$ Out**
Repeat: Timing signal output
Burst: Timing signal output used at Burst
- 3 Aux In**
Auxiliary signal input connector
Either Error Injection or Burst can be selected.
- 4 Aux Out, $\overline{\text{Aux}}$ Out**
Auxiliary signal output connectors
Output of any of 1/N Clock, Pattern Sync, and Burst2 can be selected.
- 5 Clock Out**
Clock signal output connector
- 6 Ext Clock In**
Clock signal input connector

21G/32G bit/s SI ED MU195040A



- 1 Data Input, $\overline{\text{Data}}$ Input**
Input connectors for Data and $\overline{\text{Data}}$ signals
Supports both differential and single inputs
When the Clock Recovery MU195040A-x22 is installed, the clock is recovered from the signal input to Data Input1.
- 2 Aux In**
Auxiliary signal input connector
Any of External Mask, Burst, and Capture External Trigger can be selected.
- 3 Aux Out, $\overline{\text{Aux}}$ Out**
Auxiliary signal output connectors
Any of 1/N Clock, Pattern Sync, Error, Sync Gain can be output.
- 4 Ext Clock In**
Clock signal input connector

PAM4 PPG MU196020C



- 1 Data Output, $\overline{\text{Data}}$ Output**
Connectors outputting differential Data and $\overline{\text{Data}}$ signals
- 2 Gating Out**
Repeat: Timing signal output
Burst: Timing signal output used at Burst
- 3 Aux In**
Auxiliary signal input connector
Either Error Injection or Burst can be selected.
- 4 Aux Out, $\overline{\text{Aux}}$ Out**
Auxiliary signal output connectors
Output of any of 1/N Clock, Pattern Sync, and Burst2 can be selected.
- 5 Clock Out**
Clock signal output connector
- 6 Ext Clock In**
Clock signal input connector

Signal Quality Analyzer-R MP1900A Panel Layout

Modules

PAM4 ED MU196040B



1 Data Input, $\overline{\text{Data}}$ Input

Input connectors for Data and $\overline{\text{Data}}$ signals
Supports both differential and single inputs

2 Aux In

Auxiliary signal input connector
Any of External Mask, Burst, and Capture External Trigger can be selected.

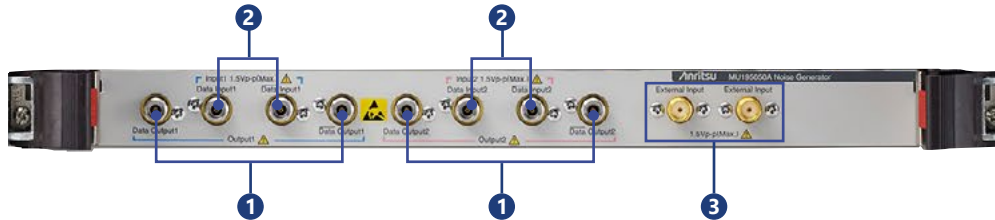
3 Aux Out, $\overline{\text{Aux}}$ Out

Auxiliary signal output connectors
Any of 1/N Clock, Pattern Sync, Error, Sync Gain can be output.

4 Ext Clock In

Clock signal input connector

Noise Generator MU195050A



1 Data Output, $\overline{\text{Data}}$ Output

Connector for outputting differential Data and $\overline{\text{Data}}$ Signal with added noise

* Input2 and Output2 are not used by the MU196020A

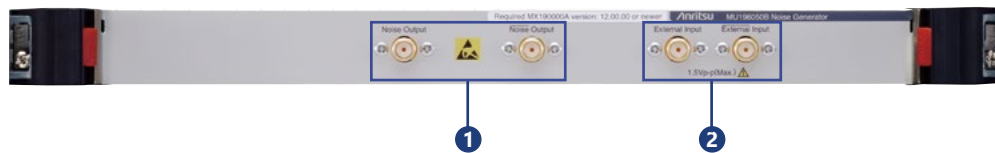
2 Data Input, $\overline{\text{Data}}$ Input

Connector for inputting Data and Data signal with added noise

3 External Input, $\overline{\text{External}}$ Input

External noise input connectors

Noise Generator MU196050B



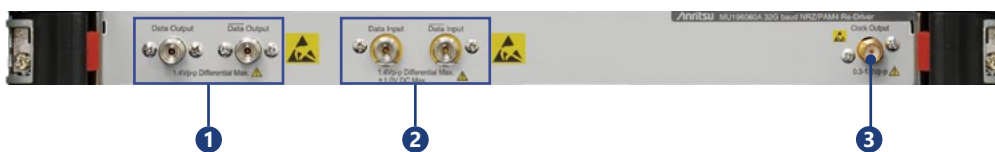
1 Noise Output, $\overline{\text{Noise}}$ Output

Connector for outputting differential Data and $\overline{\text{Data}}$ Signal with added noise

2 External Input, $\overline{\text{External}}$ Input

External noise input connectors

32G baud NRZ/PAM4 Re-Driver MU196060A



1 Data Output, $\overline{\text{Data}}$ Output

Connectors for outputting equalized differential Data and $\overline{\text{Data}}$ signals

2 Data Input, $\overline{\text{Data}}$ Input

Connectors for inputting differential Data and $\overline{\text{Data}}$ signals

3 Clock Output

Connector for outputting Clock signal recovered from input data

Signal Quality Analyzer-R MP1900A Panel Layout

Modules

Synthesizer MU191000A



- 1 10 MHz Ref Output**
Output 10 MHz clock for reference
- 2 10 MHz Ref Input**
Inputs 10 MHz clock for reference
- 3 100 MHz Ref Input**
Inputs 100 MHz clock for reference
- 4 AUX Output**
Output for auxiliary signal
- 5 Clock Output 1 to 4**
Outputs clocks

Jitter Modulation Source MU181500B



- 1 IQ Output**
Outputs IQ signal
- 2 Ext Jitter Input**
Inputs Jitter Modulation Source
- 3 Sub-rate Clock Output**
Differential Clock Output signal generated from 1/8 to 1/256-divided Clock Output based on any of following Clock inputs
• Ext Clock Input • Aux Input
- 4 Aux Input**
Inputs clock signal
- 5 Reference Clock Output**
Dual-system Clock Output signal generated from either 1/1, 1/2, or 1/4-divided Jitter Clock Output based on any of following Clock inputs
• Ext Clock Input • Aux Input
- 6 Jittered Clock Output**
Two outputs jitter modulated clock signal
- 7 Ext Clock Input**
Inputs external clock

Signal Quality Analyzer-R MP1900A Specifications

Refer to the [MP1900A Data Sheet](#) for detailed specifications.

Signal Quality Analyzer-R MP1900A

LCD		12.1" WXGA 1280 × 800
Remote Interface		GPIO, LAN
Module Slots		8
External Equipment Interface		USB × 6, VGA × 1, HDMI × 1
OS		Window 10
Power Supply		100 V(ac) to 120 V(ac), 200 V(ac) to 240 V(ac), 50 Hz to 60 Hz Power consumption: 1350 VA max.
Dimensions and Mass		340 (W) × 222.5 (H) × 451 (D) mm, 20 kg (excluding modules)
CE	EMC	2014/30/EU, EN61326-1, EN61000-3-2
	LVD	2014/35/EU, EN61010-1
	RoHS	2011/65/EU, (EU) 2015/863, EN IEC 63000: 2018
UKCA	EMC	S.I. 2016 No.1091, EN 61326-1, EN61000-3-2
	LVD	S.I. 2016 No.1101, EN 61010-1
	RoHS	S.I. 2012 No.3032, EN IEC 63000:2018

Synthesizer MU191000A

Clock Output	Number of Outputs: 4 Frequency Setting Range: 0.1 GHz to 16.05 GHz (Clock accuracy and stability depend on the internal reference clock of the MP1900A main unit or an external reference clock input.) Amplitude Level: 0.7 Vp-p ±0.3 Vp-p (0.4 Vp-p to 1.0 Vp-p) Connector: SMA (J), Termination: 50Ω/AC Coupling
10 MHz Reference Input	Frequency Range: 10 MHz ±2 ppm Connector: SMA (J), Termination: 50Ω/AC Coupling
10 MHz Reference Output	Level: 1.0 Vp-p ±0.3 Vp-p (0.7 Vp-p to 1.3 Vp-p) Connector: SMA (J), Termination: 50Ω/AC Coupling
100 MHz Reference Input	Frequency Range: 100 MHz with SSC 30 kHz to 33 kHz Center/Down Spread 0 to 5000 ppm Amplitude: 0.15 Vp-p to 1.45 Vp-p Connector: SMA (J), Termination: 50Ω/AC Coupling
AUX Output	SMA (J), Termination: 50Ω/AC Coupling (Always apply a 50Ω termination to ensure proper operation.)
Internal SSC Modulation	SSC 33 kHz Center/Down Spread Selectable OFF/1500 ppm/3000 ppm/5000 ppm Selectable (PCIe 1 to 7 supported)

12.5 GHz 4 Port Synthesizer MU181000B

Clock Output	Number of Output: 4 Frequency Range: 0.1 GHz to 12.5 GHz, Steps: 1 kHz/1 MHz Level: 0.4 Vp-p to 1 Vp-p (AC) Connector: SMA (J), Termination: 50Ω/GND
10 MHz Input	Frequency: 10 MHz ±10 ppm Level: 0.5 Vp-p to 2.0 Vp-p Connector: BNC, Termination: 50Ω/GND
10 MHz Output	Level: 1.0 Vp-p ±30% (AC) Connector: BNC, Termination: 50Ω/GND
100 MHz Reference Signal Input (SSC Extension MU181000B-002)	Outputs either 100 MHz with phase deviation x25, x50, or x80 frequency-multiplied clock from Clock Output connector Supports PCI Express Host Refclk input Modulation Frequency: 30 kHz to 33 kHz Level: 0.15 Vp-p to 1.3 Vp-p (AC) Connector: BNC

Signal Quality Analyzer-R MP1900A Specifications

Refer to the **MP1900A Data Sheet** for detailed specifications.

Jitter Modulation Source MU181500B

External Clock Input	Frequency Range: 0.800 000 GHz to 15.000 000 GHz Amplitude: 0.4 Vp-p to 1.0 Vp-p Connector: SMA (J), Termination: 50Ω/AC Coupling
Jittered Clock Output	Number of Output: 2 Amplitude: 0.4 Vp-p to 1.0 Vp-p Connector: SMA (f), Termination: 50Ω/AC Coupling
SJ1	Modulation Frequency: 10 Hz to 250 MHz Amplitude: 0 to 2000 UI @Modulation Frequency 10 kHz to 100 kHz 0 to 1 UI @Modulation Frequency 10 MHz to 250 MHz (Different depending on the operating bit rate)
Built-in SJ2	Modulation Frequency: 33 kHz, 87 MHz, 100 MHz, 210 MHz
Spread Spectrum Clocking (SSC)	Modulation Frequency: 28 kHz to 37 kHz Deviation: 0 to 7000 ppm
Random Jitter (RJ)	Bandwidth: 10 kHz to 1 GHz Amplitude: 0 to 0.5 UI (Different depending on the operating frequency)
Bounded Uncorrelated Jitter (BUJ)	PRBS Pattern Length: $2^n - 1$ ($n = 7, 9, 11, 15, 23, \text{ or } 31$) BUJ Rate: 0.1 Gbit/s to 3.2 Gbit/s, 4.9 Gbit/s to 6.25 Gbit/s, 9.8 Gbit/s to 12.5 Gbit/s Filter Type (LPF 3 dB Bandwidth): 50, 100, 200, 300, 500 MHz, Through Amplitude: 0 to 0.5 UI (Different depending on the operating frequency)
External Jitter	Bandwidth: 10 kHz to 1 GHz

Noise Generator MU196050B*1

Number of Channels	1
Frequency (DMI)	Sinusoidal wave: 2 GHz to 10 GHz
Amplitude (DMI*2)	0 to 200 mVp-p (Differential)
Output Control (DMI)	Switchable ON/OFF (DMI/CMI and External Input are mutually exclusive and selectable.) (DMI/CMI can be output simultaneously.)
Frequency (CMI*)	Sinusoidal wave Low Band: 100 MHz to 1 GHz High Band: 1 GHz to 6 GHz
Amplitude (CMI*2)	0 to 250 mVp-p (Single-ended)
Output Control (CMI)	Switchable ON/OFF (DMI/CMI and External Input are mutually exclusive and selectable.) (DMI/CMI can be output simultaneously.)

*1: △ Always use in combination with the Pick OFF Tee J1793A standard accessory.

*2: Connect a Coaxial Cable J1948A (0.4 m, SMA connector) and a Pick-off Tee J1793A (pick-off path) to the Noise Output, and define the measurement point at the end of the connection where a 34VKF50A and a Coaxial Cable J1821A (0.8 m, K connector) are connected to the OUT terminal of the J1793A.

Noise Generator MU195050A

Number of Channels	2
Insertion Loss	-3 dB
CMI: Common Mode Noise	0.1 GHz to 6 GHz: Sinusoidal wave
DMI: Differential Mode Noise	2 GHz to 10 GHz: Sinusoidal wave
White Noise	10 MHz to 10 GHz
Crest Factor	>5

21G/32G bit/s SI PPG MU195020A

Operation Rate (NRZ)	2.4 Gbit/s to 21 Gbit/s or 32.1 Gbit/s
Number of Channels	1 or 2
Output Amplitude	0.1 Vp-p to 1.3 Vp-p (Single-end) 0.2 Vp-p to 2.6 Vp-p (Differential)
Emphasis	10Tap
Channel Emulator	Normal: Emulates Insertion Loss using S-parameter data Inverse: Performs De-Emphasis compensation for S-parameter Insertion Loss S-Parameter file: S2P,S4P
ISI	Emulates ISI output using CEI-28G/25G Nyquist frequency loss setting Supports loss control in combination with ISI Board J1758A accessory Insertion Loss setting: 1.5 to 25 dB, 0.01 dB step, Nyquist frequency 0 to 25 dB, 0.01 dB step, 1/2 Nyquist frequency
Tr/Tf (20 to 80%)	12 ps (typ.)
Random Jitter	115 fs rms (typ.)
PCIe, USB Link Training	Supported (MX183000A-PL021/PL022/PL025)
Output Connector	K (J)

Signal Quality Analyzer-R MP1900A Specifications

Refer to the **MP1900A Data Sheet** for detailed specifications.

21G/32G bit/s SI ED MU195040A

Operation Rate (NRZ)	2.4 Gbit/s to 21 Gbit/s or 32.1 Gbit/s
Number of Channels	1 or 2
Input Attitude	0.05 Vp-p to 1.0 Vp-p (Single-End) 0.1 Vp-p to 2.0 Vp-p (Differential)
Input Sensitivity (Eye Height)	15 mV (28.1 Gbit/s, NRZ) 30 mV/Eye (28.1 Gbaud, PRBS15, PAM4)
CTLE	Peak Frequency: 14, 8, 4 GHz Gain: 0 to -12 dB
Clock Recovery	Yes, supports SSC
PCIe, USB Link Training	Supported (MX183000A-PL021/PL022/PL025)
Input Connector	K (J)

PAM4 PPG MU196020C

Operation Rate	When selecting the Expert BERT application: 2.4 Gbaud to 32.1/58.2/64.2 Gbaud When selecting the BERT for PCIe 1-7 application: 2.4 Gbaud to 64.2 Gbaud
Number of Output	1
Output Amplitude	NRZ: 70 mVp-p to 800 mVp-p, 2 mV step (Single-ended) PAM4: 70 mVp-p to 800 mVp-p, 1 mV step (Single-ended) PAM3: 48 mVp-p to 532 mVp-p, 1 mV step (Single-ended)
Coding	NRZ, PAM4, PAM3
Offset Reference	Vth
Offset	-2.0-Eye Amplitude/2 to +3.3-Eye Amplitude/2 Vth, 1 mV step (Single-ended)
Emphasis	4 Tap
Channel Emulator	<p>Normal: Emulates and outputs a waveform in which a transmission path equivalent to the loaded S-parameters is connected to the PPG output data signal.</p> <p>Inverse: Emulates and outputs a waveform in which the inverse characteristics of a transmission path equivalent to the loaded S-parameters are connected to the PPG output data signal.</p> <p>Intended for use in compensating for transmission path loss.</p> <p>The following graph shows typical limit values for compensable insertion loss. It does not guarantee that all responses emulated from S-parameter files will be compensated in the same manner as the characteristics shown in this graph.</p>
Independently Variable PAM4 3 Eye	Available, 20% to 50%, 1 mV step (in terms of eye amplitude) (PAM4 amplitude: 0/3 level defined as 100%)
PAM4 Pattern	Standards-compliant patterns for PAM4 mode QPRBS13-CEI, QPRBS31-CEI PRBS13Q, PRBS31Q, SSQRQ, Square Wave QPRBS13, JP03A, JP03B, Transmitter Linearity PRBS13Q(Infiniband), PRBS23Q, PRBS31Q(Infiniband) PRBS31Q(Fiber Channel) etc.
Error Addition	Bit, Error on MSB, Error on LSB, Error on LSB&MSB, RS-FEC Symbol Error, PCIe6 FEC Symbol Error
Tr/Tf (20 to 80%)	Typ. 6.0 ps at 32, 64 Gbaud, when using J1789A Typ. 7.0 ps at 32, 64 Gbaud, when using J1790A 100 GHz bandwidth sampling oscilloscope used
Output Connector	V Connector (J)
Low Residual Jitter (Intrinsic RJ)	≤ 108 fs rms Calculated by the RJ (rms) of the jitter analysis function using a 01 repetition pattern; specified at 64 Gbit/s.
Signal to noise and distortion ratio (SNDR)	PCIe7* (PAM4): typ. 35 dB

*: When performing calibration under the following conditions and removing the residual noise of the oscilloscope:
Amplitude: 0.8 Vp-p/Differential, J1793A Pick OFF Tee used, Test Pattern: PRBS13Q

Signal Quality Analyzer-R MP1900A Specifications

Refer to the [MP1900A Data Sheet](#) for detailed specifications.

PAM4 PPG MU196020A

Operation Rate (PAM4/NRZ)	2.4 Gbaud to 32.1/58.2/64.2 Gbaud (option selection)
No. of Channels	1
Output Amplitude	70 mVp-p to 800 mVp-p (Single-end) 140 mVp-p to 1600 mVp-p (Differential)
Offset	-2 V to +3.3 V
Emphasis	4 Tap, -20 to +20 dB
Channel Emulator	Generates waveform with insertion loss and simulates waveform with corrected insertion loss Set by loading S-Parameter file (S2 P, S4 P)
ISI	Simulates ISI generation waveform Set using loss (-8.00 to 8.00 dB) at CEI-specified Nyquist frequency Used in combination with channel board, such as J1800A/J1758A (optional accessories parts), or Noise Module MU195050A
Independently Variable PAM4 3 Eye	20 to 50% (PAM4 Amplitude 0/3 level = 100%)
PAM4 Pattern	SSPRQ, PRBS13Q, PRBS31Q, RS-FEC, etc.
PAM4 Pattern Error Addition	MSB Error, LSB Error, LSB&MSB Error, RS-FEC Symbol Error, PCIe6 FEC Symbol Error
Tr/Tf (20 to 80%)	8.5 ps (typ., NRZ)
Random Jitter	170 fs rms (typ., NRZ)
Output Connector	V (J)

PAM4 ED MU196040B

Operation Rates (PAM4/NRZ)	2.4 Gbaud to either 32.1 Gbaud, or 58.2 Gbaud (PAM4)/64.2 Gbaud (NRZ) (option selection)
No. of Channels	1
Input Amplitude	NRZ: $\leq 32.1\text{G}$: 0.05 Vp-p to 1.0 Vp-p, $> 32.1\text{G}$: 0.1 Vp-p to 1.0 Vp-p PAM4: $\leq 32.1\text{G}$: 0.3 Vp-p to 1.0 Vp-p, $> 32.1\text{G}$: 0.4 Vp-p to 1.0 Vp-p
Input Sensitivity (Eye Height)	NRZ: 19 mV @ 26.5625 Gbaud, 21 mV @ 53.125 Gbaud PAM4: 23 mV @ 26.5625 Gbaud, 36 mV @ 53.125 Gbaud
Clock Recovery (Option)	2.4 Gbaud to 32.1 Gbaud, 51 Gbaud to 58.2 Gbaud
Equalizer (Option)	Low-frequency Equalizer (≤ 1 GHz, 2 dB typ.) + DFE (1.4 dB typ.)
PAM4 Patterns	SSPRQ, PRBS13Q, PRBS31Q, etc.
PAM4 Counter	MSB, LSB, Symbol 0 to 3 (Option)
Input Connector	V (J)

32G baud NRZ/PAM4 Re-Driver MU196060A

Target Applications	PCIe 4.0: 16.0 Gbit/s, NRZ PCIe 5.0: 32.0 Gbit/s, NRZ PCIe 6.0: 32.0 Gbaud, PAM4 IEEE802.3bs 400GAUI-8 C2M: 26.5625 Gbaud, PAM4
Supported Plug-in Modules	MU196040B PAM4 ED MU195040A 21G/32G bit/s SI ED
Input Amplitude	PAM4: 0.40 to 0.80 Vp-p / Differential BER < 1E-8, 1E-12 (typ.), MCP, SSC 5300 ppm Down spread NRZ: 0.18 to 0.80 Vp-p / Differential BER < 1E-12, MCP, SSC 5300 ppm Down spread
Input/Output Connector	V (f)
LOSS Compensation	PAM4: 14 dB at 16.0 GHz, BER < 1E-6, 1E-9 (typ.), MCP, SSC 5300 ppm Down spread NRZ: 30 dB at 16.0 GHz, BER < 1E-12, MCP, SSC 5300 ppm Down spread
Clock Recovery (option)	With SSC support, PCIe 4.0, 5.0, 6.0

Signal Quality Analyzer-R MP1900A Ordering Information

When ordering, determine the configuration by referencing the selection guide (MP1900A-E-Z-1) and specify the type, model, name, and quantity. The names listed in the chart below are Order Names. The actual name of the item may differ from the Order Name.

MP1900A

Model/Order No.	Name
MP1900A	Main Frame *1 Signal Quality Analyzer-R
	Standard Accessories
G0342A	ESD DISCHARGER: 1 pc
J1211	POWER CORD. 3M: 1 pc
J1627A	GND connection cable: 1 pc
P0031A	USB Memory: 1 pc
Z0306A	Wrist Strap: 1 pc
–	RJ45 Cap (Cap for Ethernet Port): 1 pc
MX190000A	Signal Quality Analyzer-R Control Software*2
MX183000A	High-Speed Serial Data Test Software*3, *4
	Retrofit Option
MP1900A-110	Windows10 Upgrade Retrofit*5
	Maintenance Service
MP1900A-ES310	Three Years Extended Warranty Service
MP1900A-ES510	Five Years Extended Warranty Service

*1: The Windows 10 OS will be installed in all orders from July 1, 2020.

*2: Standard software pre-installed in Signal Quality Analyzer-R MP1900A

*3: Trial software pre-installed in Signal Quality Analyzer-R MP1900A for extending functions with 30-day free trial period following first launch. When requiring the official version after the 30-day trial period, obtain the official license by purchasing the separate MX183000A-PLxx software license. Refer to the software license.

*4: The PAM4 Control function is bundled with the MX183000A as a standard function and can be used without a license.

*5: MP1900A main units running Windows Embedded Standard 7 are retrofitted to Windows 10 using a hardware upgrade. Anritsu destroys the unnecessary, post-upgrade Windows Embedded Standard 7 parts.
For details, contact our sales representative.

MU191000A

Model/Order No.	Name
MU191000A	Module Synthesizer
	Standard Accessories
J1341A	OPEN: 3 pcs
J1632A	TERMINATOR: 5 pcs
J1624A	COAXIAL CABLE 0.3M (SMA connector): 4 pcs
J1717A	COAXIAL ADAPTOR (SMA-P, SMA-J): 5 pcs
	Optional Accessories
J1759A	BNC-SMA Connector Cable (1 m)
	Maintenance Service
MU191000A-ES310	Three Years Extended Warranty Service
MU191000A-ES510	Five Years Extended Warranty Service

MU181000B

Model/Order No.	Name
MU181000B	Module 12.5 GHz 4port Synthesizer
	Standard Accessories
J1624A	Coaxial Cable 0.3 m (SMA): 4 pcs
	Option
MU181000B-002	SSC Extension
	Retrofit Option
MU181000B-102	SSC Extension Retrofit
	Maintenance Service
MU181000B-ES310	Three Years Extended Warranty Service
MU181000B-ES510	Five Years Extended Warranty Service

MU181500B

Model/Order No.	Name
MU181500B	Module Jitter Modulation Source
	Standard Accessories
J1624A	Coaxial Cable 0.3 m (SMA): 1 pc
J1508A	BNC-SMA Connector Cable (30 cm): 2 pcs
J1137	Terminator: 6 pcs
J1341A	Open: 2 pcs
Z0897A	MP1800A Manual CD: 1 pc
Z0918A	MX180000A Software CD: 1 pc
	Maintenance Service
MU181500B-ES310	Three Years Extended Warranty Service
MU181500B-ES510	Five Years Extended Warranty Service

MU196050B

Model/Order No.	Name
MU196050B	Module Noise Generator
	Standard Accessories
J1717A	COAXIAL ADAPTOR (SMA-P, SMA-J): 4 pcs
J1632A	TERMINATOR: 2 pcs
J1341A	Open: 2 pcs
J1948A	Coaxial Skew Matched Cable Pair (0.4 m, SMA Connector): 1 set
J1793A	Pick OFF Tee: 2 pcs
	Optional Accessories
34VKF50A	Fixed Adapter (V-M, K-F)
J1821A	Coaxial Skew Matched Cable Pair (0.8 m, K Connector)
	Maintenance Service
MU196050B-ES310	Three Years Extended Warranty Service
MU196050B-ES510	Five Years Extended Warranty Service

MU195050A

Model/Order No.	Name
MU195050A	Module Noise Generator
	Standard Accessories
J1632A	Terminator (SMA): 4
J1359A	Coaxial Adapter (K-P, K-J, SMA): 4
J1717A	COAXIAL ADAPTOR (SMA-P, SMA-J): 2
J1341A	Open: 6
J1746A	Skew Match Pair Semrigid Cable (K connector, Data Input1): 1 set
J1747A	Skew Match Pair Semrigid Cable (K connector, Data Input2): 1 set
J1792A	Skew Match Pair Semrigid Cable (V-K connector, MU196020A PPG Output to MU195050A Noise Data Input1): 1 set
	Option
MU195050A-001	White Noise
	Retrofit Option
MU195050A-101	White Noise Retrofit
	Maintenance Service
MU195050A-ES310	Three Years Extended Warranty Service
MU195050A-ES510	Five Years Extended Warranty Service

Signal Quality Analyzer-R MP1900A Ordering Information

When ordering, determine the configuration by referencing the selection guide (MP1900A-E-Z-1) and specify the type, model, name, and quantity.

MU196060A*15

Model/Order No.	Name
MU196060A	Module 32G baud NRZ/PAM4 Re-Driver
	Standard Accessories
J1916A	OPEN (V): 4 pcs
J1341A	OPEN (SMA): 1 pc
J1898A	Coaxial Cable Set for MU196060A: 1 set
	[J1917A Coaxial Semi-rigid Cable: 1
	J1932A Coaxial Skew Matched Cable Pair (0.8 m, V Connector): 1]
MU196060A-001	Option Clock Recovery for SSC
MU196060A-301	Retrofit Option Clock Recovery for SSC Retrofit
MU196060A-ES310	Maintenance Service Three Years Extended Warranty Service
MU196060A-ES510	Five Years Extended Warranty Service

MU195020A

Model/Order No.	Name
MU195020A	Module 21G/32G bit/s SI PPG
	Standard Accessories
J1632A	Terminator (SMA): 5 pcs
J1341A	Open: 2 pcs
J1359A	Coaxial Adapter (K-P, K-J, SMA): 1 pc
J1717A	COAXIAL ADAPTOR (SMA-P, SMA-J): 6 pcs
MU195020A-001	Option 32G bit/s Extension
MU195020A-010	1ch Data Output
MU195020A-020	2ch Data Output
MU195020A-011	1ch 10Tap Emphasis
MU195020A-021	2ch 10Tap Emphasis
MU195020A-030	1ch Data Delay
MU195020A-031	2ch Data Delay
MU195020A-040	1ch Variable ISI
MU195020A-041	2ch Variable ISI
MU195020A-050	Sequence Editor Function*6
MU195020A-051	Sequence Editor Function PCIe 5 Extension*6
MU195020A-101	Retrofit Options 32G bit/s Extension Retrofit
MU195020A-111	1ch 10Tap Emphasis Retrofit
MU195020A-121	2ch 10Tap Emphasis Retrofit
MU195020A-130	1ch Data Delay Retrofit
MU195020A-131	2ch Data Delay Retrofit
MU195020A-140	1ch Variable ISI Retrofit
MU195020A-141	2ch Variable ISI Retrofit
MU195020A-340	1ch Variable ISI Retrofit
MU195020A-341	2ch Variable ISI Retrofit
MU195020A-350	Sequence Editor Function Retrofit
MU195020A-351	Sequence Editor Function PCIe 5 Extension Retrofit
J1632A	Opt-x10 Accessories Terminator (SMA): 2
J1359A	Coaxial Adapter (K-P, K-J, SMA): 2
J1632A	Opt-x20 Accessories Terminator (SMA): 4
J1359A	Coaxial Adapter (K-P, K-J, SMA): 4
MU195020A-ES310	Maintenance Service Three Years Extended Warranty Service
MU195020A-ES510	Five Years Extended Warranty Service

MU196020C*13

Model/Order No.	Name
MU196020C	Module PAM4 PPG
	Standard Accessories
J1632A	TERMINATOR: 4 pcs
J1889A	Terminator (V Connector): 2 pcs
J1341A	OPEN: 2 pcs
J1359A	COAXIAL ADAPTOR (K-P,K-J,SMA): 1 pc
J1717A	COAXIAL ADAPTOR (SMA-P,SMA-J): 5 pcs
MU196020C-001	Option 32G baud*
MU196020C-002	58G baud*
MU196020C-003	64G baud*
MU196020C-011	4Tap Emphasis
MU196020C-030	Data Delay
MU196020C-040	Adjustable ISI
MU196020C-042	FEC Pattern Generation
MU196020C-043	FEC Error Insertion for PCIe6
MU196020C-045	USB4 Gen4 Pattern Generation
MU196020C-050	Inter-Module Synchronization
MU196020C-112	Retrofit Options 32G to 58G baud Retrofit
MU196020C-113	32G to 64G baud Retrofit
MU196020C-123	58G to 64G baud Retrofit
MU196020C-111	4Tap Emphasis Retrofit
MU196020C-130	Data Delay Retrofit
MU196020C-140	Adjustable ISI Retrofit
MU196020C-142	FEC Pattern Generation Retrofit
MU196020C-143	FEC Error Insertion for PCIe6 Retrofit
MU196020C-145	USB4 Gen4 Pattern Generation Retrofit
MU196020C-150	Inter-Module Synchronization Retrofit
MU196020C-340	Adjustable ISI Retrofit
MU196020C-342	FEC Pattern Generation Retrofit
MU196020C-343	FEC Error Insertion for PCIe6 Retrofit
MU196020C-345	USB4 Gen4 Pattern Generation Retrofit
MU196020C-ES310	Maintenance Service Three Years Extended Warranty Service
MU196020C-ES510	Five Years Extended Warranty Service

*: Select any one

*6: Option 050 supports PCIe 1 to 4, and USB 3.2 ×1. Option 051 supports PCIe 5. Option 050 is required when adding Option 051.

Signal Quality Analyzer-R MP1900A Ordering Information

When ordering, determine the configuration by referencing the selection guide (MP1900A-E-Z-1) and specify the type, model, name, and quantity.

MU196020A*15

Model/Order No.	Name
MU196020A	Module PAM4 PPG
	Standard Accessories
J1632A	TERMINATOR: 4
J1889A	TERMINATOR (V): 2
J1341A	OPEN: 2
J1359A	COAXIAL ADAPTOR (K-P,K-J,SMA): 1
J1717A	COAXIAL ADAPTOR(SMA-P,SMA-J): 5
	Option
MU196020A-001	32G baud*
MU196020A-002	58G baud*
MU196020A-003	64G baud*
MU196020A-011	4Tap Emphasis
MU196020A-030	Data Delay
MU196020A-040	Adjustable ISI
MU196020A-042	FEC Pattern Generation
MU196020A-043	FEC Error Insertion for PCIe6
MU196020A-045	USB4 Gen4 Pattern Generation
MU196020A-050	Inter-Module Synchronization
MU196020A-051	Sequence Editor Function
MU196020A-052	Sequence Editor Function for Multi-channel
MU196020A-056	Sequence Editor Function PCIe 6 and CXL 3 Flits Extension*7
MU196020A-060	PCIe6 LEQ
	Retrofit Options
MU196020A-112	32G to 58G baud Extension Retrofit
MU196020A-113	32G to 64G baud Retrofit
MU196020A-123	58G to 64G baud Retrofit
MU196020A-111	4Tap Emphasis Retrofit
MU196020A-130	Data Delay Retrofit
MU196020A-140	Adjustable ISI Retrofit
MU196020A-142	FEC Pattern Generation Retrofit
MU196020A-145	USB4 Gen4 Pattern Generation Retrofit
MU196020A-150	Inter-Module Synchronization Retrofit
MU196020A-160	PCIe6 LEQ Retrofit
MU196020A-156	Sequence Editor Function PCIe 6 and CXL 3 Flits Extension Retrofit*7
MU196020A-340	Adjustable ISI Retrofit
MU196020A-342	FEC Pattern Generation Retrofit
MU196020A-343	FEC Error Insertion for PCIe6 Retrofit
MU196020A-345	USB4 Gen4 Pattern Generation Retrofit
MU196020A-351	Sequence Editor Function Retrofit
MU196020A-352	Sequence Editor Function for Multi-channel Retrofit
MU196020A-356	Sequence Editor Function PCIe 6 and CXL 3 Flits Extension Retrofit*7
MU196020A-360	PCIe6 LEQ Retrofit*8
	Maintenance Service
MU196020A-ES310	Three Years Extended Warranty Service
MU196020A-ES510	Five Years Extended Warranty Service

*7: Option 051 is required when adding Option 056.

*8: Order when MU196020A serial number is 6272477551 or later

*: Select any one

MU195040A

Model/Order No.	Name
MU195040A	Module 21G/32G bit/s SI ED
	Standard Accessories
J1632A	Terminator (SMA): 2
J1341A	Open: 1
J1717A	COAXIAL ADAPTOR (SMA-P, SMA-J): 4
	Option
MU195040A-001	32G bit/s Extension
MU195040A-010	1ch ED
MU195040A-020	2ch ED
MU195040A-011	1ch CTLE
MU195040A-021	2ch CTLE
MU195040A-022	Clock Recovery
	Retrofit Options
MU195040A-101	32G bit/s Extension Retrofit
MU195040A-111	1ch CTLE Retrofit
MU195040A-121	2ch CTLE Retrofit
MU195040A-122	Clock Recovery Retrofit
	Opt-x10 Accessories
J1341A	Open: 3
J1359A	Coaxial Adapter (K-P, K-J, SMA): 2
J1887A	Fixed Attenuator (6 dB, K Connector): 2
	Opt-x20 Accessories
J1341A	Open: 5
J1359A	Coaxial Adapter (K-P, K-J, SMA): 4
J1887A	Fixed Attenuator (6 dB, K Connector): 4
	Maintenance Service
MU195040A-ES310	Three Years Extended Warranty Service
MU195040A-ES510	Five Years Extended Warranty Service

Signal Quality Analyzer-R MP1900A Ordering Information

When ordering, determine the configuration by referencing the selection guide (MP1900A-E-Z-1) and specify the type, model, name, and quantity.

MU196040B*15

Model/Order No.	Name
MU196040B	Module PAM4 ED
	Standard Accessories
J1632A	TERMINATOR: 2
J1889A	TERMINATOR (V): 2
J1341A	OPEN: 2
J1359A	COAXIAL ADAPTOR (K-P.K-J,SMA): 1
J1717A	COAXIAL ADAPTOR (SMA-P.SMA-J): 3
J1888A	Fixed Attenuator 6 dB: 2
	Option
MU196040B-001	32G baud (2.4G to 32.1G)*
MU196040B-002	58G baud (NRZ: 2.4G to 64.2G, PAM4: 2.4G to 58.2G)*
MU196040B-005	64G baud*10
MU196040B-011	Equalizer
MU196040B-021	29G baud Clock Recovery (2.4G to 29G)*9
MU196040B-022	32G baud Clock Recovery (2.4G to 32.1G)*9
MU196040B-023	58G baud Clock Recovery Extension (51G to 58.2G)*9
MU196040B-041	SER Measurement
MU196040B-042	FEC Analysis
MU196040B-043	FEC Analysis for PCIe6
MU196040B-051	PCIe Sequence Editor Pattern Analysis
	Retrofit Options
MU196040B-111	Equalizer Retrofit
MU196040B-112	32G to 58G baud Extension Retrofit
MU196040B-115	32G to 64G baud Extension Retrofit*10
MU196040B-121	29G baud Clock Recovery Retrofit
MU196040B-122	32G baud Clock Recovery Retrofit
MU196040B-123	58G baud Clock Recovery Extension Retrofit
MU196040B-124	32G baud Clock Recovery Extension Retrofit
MU196040B-125	58G to 64G baud Extension Retrofit*10
MU196040B-141	SER Measurement Retrofit
MU196040B-341	SER Measurement Retrofit
MU196040B-342	FEC Analysis Retrofit
MU196040B-343	FEC Analysis for PCIe6 Retrofit
MU196040B-351	PCIe Sequence Editor Pattern Analysis Retrofit
	Maintenance Service
MU196040B-ES310	Three Years Extended Warranty Service
MU196040B-ES510	Five Years Extended Warranty Service

*9: Select at least one option; either Option 021 or 022 is required when adding Option 023.

*10: There are software restrictions when using 64G baud.
For details, consult our business sales representative.

*: Select any one

Software License

Model/Order No.	Name
MX183000A	High-Speed Serial Data Test Software
MX183000A-PL001	Jitter Tolerance Test
MX183000A-PL011	PCIe Link Sequence
MX183000A-PL021	PCIe Link Training*11
MX183000A-PL022	USB Link Training*12
MX183000A-PL023	USB 3.2 × 2 Link Training*12
MX183000A-PL025	PCIe 5 Link Training*11
MX183000A-PL026	PCIe 6 Link Training*11
MX183000A-PL031	DUT Error Counts Import

*11: PL021 supports PCIe 1 to 4.

PL025 supports PCIe 5.

PL026 supports PCIe 6.

Requires PL021 to add PL025.

Requires PL021 and PL025 to add PL026.

*12: PL022 supports USB 3.2 × 1. PL023 supports USB 3.2 × 2. PL022 is required to add PL023.

On Using VISA*13

The National Instruments™ (NI hereafter) NI-VISA*14 software must be installed to use the MX183000A (this product hereafter). We recommend using NI-VISA saved on the product USB memory stick.

Customers may only use NI-VISA saved on the product memory stick. NI-VISA on the memory stick may not be used for other applications with other products.

When uninstalling this product from the controller PC, etc., also uninstall NI-VISA from the USB memory.

*13: Abbreviation for Virtual Instrument Software Architecture. This is I/O software for remote control of measuring instruments via GPIB, Ethernet and USB interfaces.

*14: NI-VISA was developed by National Instruments for VXI Plug&Play Alliance standards compliant I/O interfaces.
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Signal Quality Analyzer-R MP1900A Ordering Information

When ordering, determine the configuration by referencing the selection guide (MP1900A-E-Z-1) and specify the type, model, name, and quantity.

Optional Accessories

Model/Order No.	Name
J1900A	Passive Low Frequency Equalizer
G0447A	PCIe6 External Re-Driver
J1947A	Bessel Filter
J1632A	Terminator (SMA)
J1889A	TERMINATOR (V)
J1678A	ESD Protection Adapter-K
J1679A	ESD Protection Adapter-V
J1359A	Coaxial Adapter (K-P, K-J, SMA)
34VFK50	Fixed Adapter (V-F, K-M)*15
34VKF50	Fixed Adapter (V-M, K-F)*15
41KC-3	Fixed Attenuator 3 dB
41KC-6	Fixed Attenuator 6 dB
41KC-10	Fixed Attenuator 10 dB
41KC-20	Fixed Attenuator 20 dB
41VA-3	Fixed Attenuator 3 dB
41VA-6	Fixed Attenuator 6 dB
41VA-10	Fixed Attenuator 10 dB
41VA-20	Fixed Attenuator 20 dB
J1887A	Fixed Attenuator (6 dB, K Connector)
J1888A	Fixed Attenuator (6 dB, V Connector)
J1758A	ISI Board
J1800A	ISI Board V
K261	DC Block
K240C	Precision Power Divider
V240C	Fixed Power divider
J1510A	Pick OFF Tee (K)
J1793A	Pick OFF Tee (V)
K241C	Power Splitter
J1748A	Power Splitter (1.5 GHz to 18 GHz, SMA, using MU195020A × 4 to MU181500B connection)
J1624A	COAXIAL CABLE 0.3 m (SMA connector)
J1342A	COAXIAL CABLE 0.8 m (APC3.5 connector)
J1439A	Coaxial cable (0.8 m, K connector)
J1625A	Coaxial Cable 1 m (SMA connector)
J1449A	Measurement kit (J1324A × 2, J1439A × 2, J1625A × 1)
J1550A	Coaxial skew match cable (0.8 m, APC3.5 connector)
J1551A	Coaxial skew match cable (0.8 m, K connector)
J1728A	Electrical Length Specified Coaxial Cable (0.4 m, K connector)*15
J1759A	BNC-SMA Connector Cable (1 m)
J1741A	Electrical Length Specified Coaxial Cable (0.8 m, K Connector)*15
J1789A	Electrical Length Specified Coaxial Cable (0.4 m, V connector)*15
J1790A	Electrical Length Specified Coaxial Cable (0.8 m, V connector)*15
J1792A	Skew match pair semirigid cable (V-K connector, MU196020A PPG Output to MU195050A Noise Data Input1)
J1821A	Coaxial Skew Matched Cable Pair (0.8 m, K Connector)
J1898A	Coaxial Cable Set for MU196060A
J1917A	Coaxial Semi-rigid Cable
J1932A	Coaxial Skew Matched Cable Pair (0.8 m, V Connector)
J1948A	Coaxial Skew Matched Cable Pair (0.4 m, SMA Connector)
J1761A	PCIe Reference Clock Cable Kit
Z2025A	PCIe CBB Controller
Z2029A	PCIe Reference Clock Buffer

Model/Order No.	Name
AH54192A	56Gbaud Differential Linear Amplifier
W3911AE	MP1900A Operation Manual
W3913AE	MX190000A Operation Manual
W3813AE	MX183000A Operation Manual
W3915AE	MU195020/40/50A Operation Manual
W3976AE	MU196020/40A OPERATION MANUAL
B0576A	Blank Panel
B0736A	Front Cover (For MP1900A)
B0737A	Carrying Case (For MP1900A, with B0736A)
B0738A	Rack Mount Kit (For MP1900A)
Z1746A	Stylus
Z0541A	USB Mouse
J0008	GPIO CABLE, 2.0 m
Z0917A	Shielded LAN Cable, 5 m
Z1953A	Gigabit Ethernet Switch (5 Port)
Z0306A	Wrist Strap
Z1964A	Torque Wrench (Right Angle)

Signal Quality Analyzer-R MP1900A Ordering Information

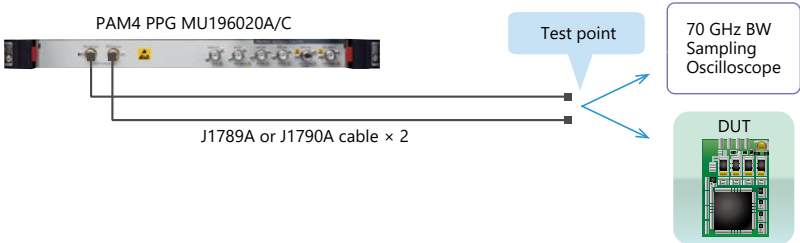
When ordering, determine the configuration by referencing the selection guide (MP1900A-E-Z-1) and specify the type, model, name, and quantity.

J1815A MP1900A PCIe Measurement Component Set

The following table lists the component set required by the PCIe 3/4/5 Tx/Rx LEQ test.

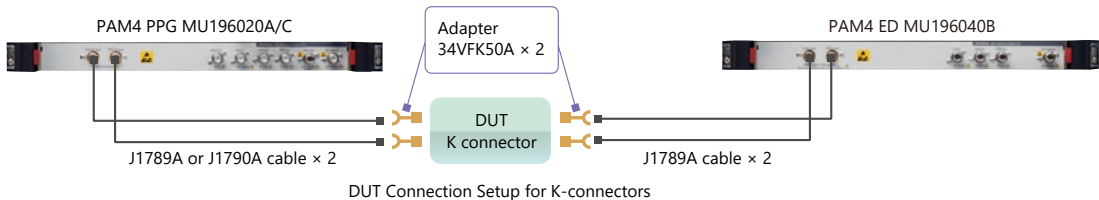
Item	Description	Qty.	Remarks		
Optional Accessories	MP1900A PCIe Measurement Component Set	1	J1815A		
			Accessories		Qty. Comment
			Coax skew match cable, 0.8 m K connector		4 Junflon J12J103220-00-1
			AE-TMC-10205		2 Coax cable, 1 m, SMA connector
			PICK OFF TEE		2 Anritsu 3-68231
			SMPF-SMAJ-TFLEX-10CM-5PS		3 SMP to SMA adapter cable
			BNC-SMA cable		2
			K261		2 DC Block
			K241C		2 Power Splitter

*15: We recommend using either the J1789A or J1790A as the coaxial cable for the MU196020A/C data output. Recommend using coaxial cable J1789A for MU196040B Data IN. The MU196020A/C data output specifications are defined based on the performance observed using a 70-GHz bandwidth oscilloscope connected as shown below.



Solution except above

The MU196020A/C Data OUT and MU196040B Data IN connectors, and the J1789A/J1790A cables all use V-connectors. Consequently, for K-connectors, use 34VFK50 adapters as shown in the following figure.



PCIe and Ethernet (26.5625 Gbaud) Solution

VK adapter

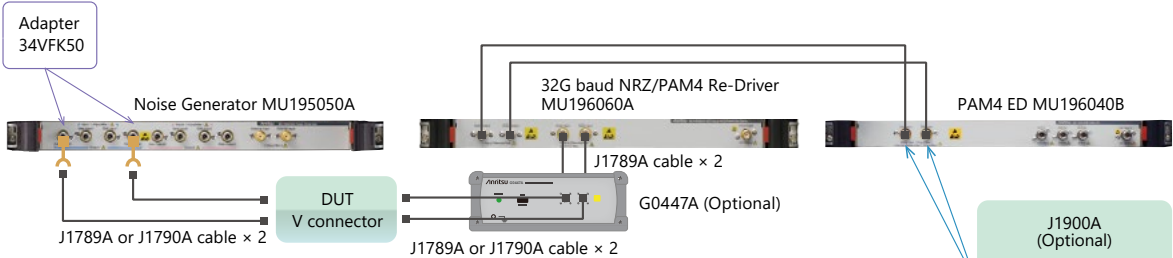
Use the 34VFK50 or 34VFK50 adapter that matches the DUT connector shape, as shown below.

MU195050A: K connector output

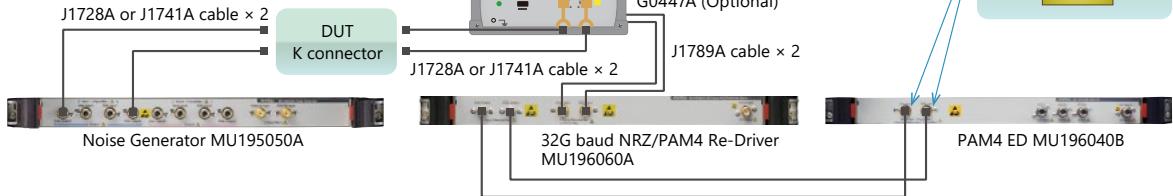
MU196060A: V connector input

- When the DUT connector shape is V and a V cable is used: **Two 34VFK50 adapters**
- When the DUT connector shape is K and a K cable is used (e.g., PCIe5 CEM Fixture): **Two 34VFK50 adapters**
- When used in combination with an SI ED: **Two separate 34VFK50 adapters** in addition to the above

With V-conector DUT



With K-conector DUT



G0447A

Install the G0447A between DUT and MU196060A, as shown below. Connect the G0447A and MU196060A using the J1789A.

J1900A

Connect the J1900A to Data Input and Data Input of the MU196040B, as shown below.

For details of the G0447A and J1900A, contact us.



Specifications are subject to change without notice.

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