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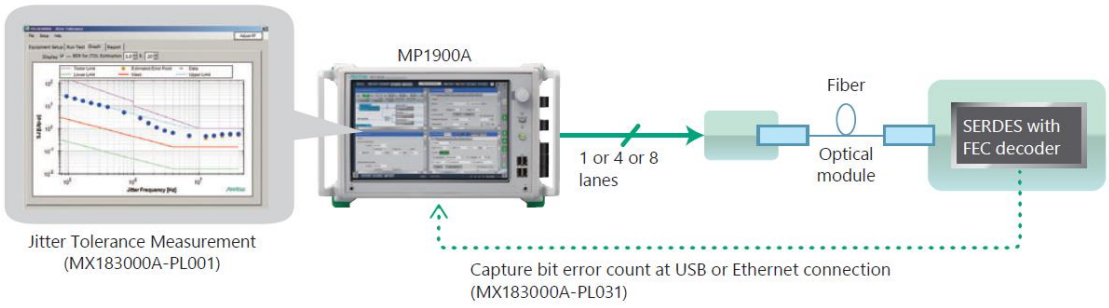
# Jitter Tolerance Test Using Multi-channel FEC Patterns

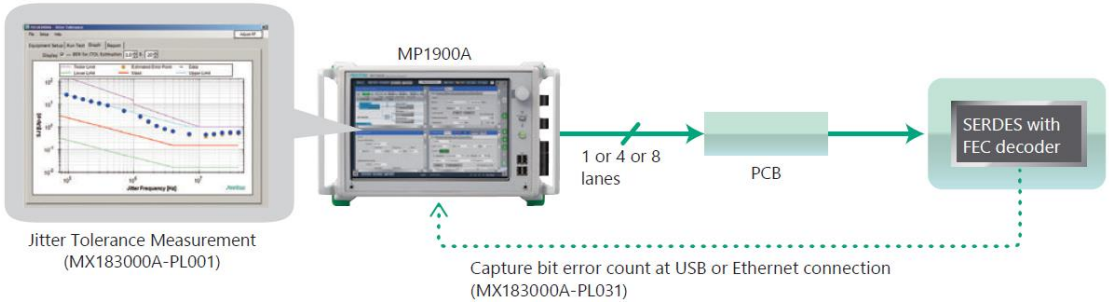
Signal Quality Analyzer-R MP1900A
PAM4 PPG MU196020A
Jitter Tolerance Test MX183000A-PL001
DUT Error Counts Import MX183000A-PL031

Increasing the transmission speed for implementing large capacity traffic such as 100G/400G presumes use of FEC to guarantee transmission quality. In addition, research into multilane transmission, such as 4- and 8-lane transmissions, as well as PAM4 signalling is in progress. Consequently, transmission quality testing requires multilane FEC patterns as well as confirmation of error rates at passage through optical modules, such as QSFP, QSFP-DD, and OSFP. Anritsu's MP1900A BERT with pulse pattern generator (PPG) provides all-in-one support for multilane FEC pattern generation and jitter addition for 400GbE PAM4 signals. Testing is performed by generating 1-, 4-, and 8-channel FEC patterns and using the DUT internal counter data for jitter tolerance tests.

**Evaluating Optical FEC Signal Transmission**




**Evaluating Electrical FEC Signal Transmission**




- Generates 1-, 4-, and 8-channel FEC patterns depending on number of modules inserted in MP1900A
- Measures jitter tolerance using FEC pattern; impresses jitter on FEC pattern, reads DUT internal FEC Decode result (Uncorrected codeword/Corrected codeword) via Ethernet or USB Interface, and measures DUT jitter tolerance using FEC pattern
- Inserts variable Burst Error into FEC pattern; confirms DUT FEC function by inserting correctable bit errors and detectable uncorrectable bit errors

[Target Application] 50GbE, 100GbE, 200GbE, 400GbE, IEEE 802.3bs, 802.3cd

## Typical Specification/Selection Guide

| Model/Name | Item | Specification |
|---|---|---|
| MU196020A-042<br>FEC Pattern Generation | Required option for generating FEC pattern | |
| | FEC Pattern Generation | RS-FEC Scrambled Idle Pattern<br>PAM4:<br>50G 1 Lane (26.5625 Gbaud, 50 GBASE-KR/CR/SR/FR/LR)<br>100G 1 Lane (53.125 Gbaud, 400 GBASE-DR)<br>200G 4 Lanes (26.5625 Gbaud, 200 GBASE-SR4/DR4/FR4/LR4)<br>400G 4 Lanes (53.125 Gbaud, 400 GBASE-DR4)<br>400G 8 Lanes (26.5625 Gbaud, 400 GBASE-FR8/LR8)<br>NRZ:<br>25G 1 Lane (25.78125 Gbaud, 25 GBASE-KR/CR/SR/LR/ER)<br>100G 4 Lanes (25.78125 Gbaud, 100 GBASE-KR4/CR4 /SR4 ) |
| | Error Addition | Burst: 1 to 256 bits contiguous Error (NRZ), 1 to 256 Symbol contiguous Error<br>Rate: E-3 to E-12<br>Symbol error per codeword: 1 to 20 |
| MU196020A-050<br>Inter-Module Synchronization | Required option for generating multilane patterns using multiple MU196020A units | |
| | Inter-module Synchronized Bit Skew | Baud Rate ≤32.1 GBaud: Accurate generation up to 1UI<br>Baud Rate >32.1 GBaud: Accurate generation up to 5UI |
| | Phase Setting Range | –64,000 to +64,000 mUI (independent setting for each channel) |
| | Phased Setting Resolution | 2 mUI (independent setting for each channel) |
| MX183000A-PL031<br>DUT Error Counts Import | Required option for capturing DUT error count via Ethernet or USB interface | |
| | Connection | Ethernet or USB |
| | Detection | Error Rate, Error Count, Alarm |
| | Jitter Tolerance | Yes, but requires MX183000A-PL001 Jitter Tolerance Test |

The following table lists typical MP1900A module and option configurations for evaluating multiple lanes.

| Category | Model/Name | 50G/100GbE<br>1 lane | 200GbE<br>4 lanes | 400GbE<br>4 lanes |
|---|---|---|---|---|
| Main Unit | MP1900A Signal Quality Analyzer-R | 1 | 1 | 1 |
| Synthesizer | MU181000B 12.5GHz 4port Synthesizer | 1 | 1 | 1 |
| Jitter | MU181500B Jitter Modulation Source | 1 | 1 | 1 |
| PPG | MU196020A PAM4 PPG | 1 | 4 | 4 |
| | MU196020A-001 32G baud | 1 | 4 | |
| | MU196020A-002 58G baud | | | 4 |
| | MU196020A-011 4Tap Emphasis | 1 | 4 | 4 |
| | MU196020A-030 Data Delay | | 4 | 4 |
| | MU196020A-042 FEC Pattern Generation | 1 | 4 | 4 |
| | MU196020A-050 Inter-Module Synchronization | | 4 | 4 |
| Software | MX183000A PL-001 Jitter Tolerance Test | 1 | 1 | 1 |
| | MX183000A PL-031 DUT Error Counts Import | 1 | 1 | 1 |

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