Signal Quality Analyzer
MP1900A/MP1800A Series
64 Gbaud PAM4 DAC Overview

**Features**
- Operating baud rate: DC to 64 Gbaud
- Half-rate Data and Clock inputs
- High quality and low Intrinsic Jitter waveform
- Differential output: 0.7 Vp-p typ. (single-end)
- Amplitude control: >6 dB
- Jitter transparency
- Adjustable Duty cycle
- I/O Interface: DC-coupled
- Power consumption: <8.5 W
- Size: 210 (W) x 88 (H) x 230 (D) mm

**Applications**
- PAM4 Signal generation
- 200GbE/400GbE, CEI-56G, Fibre Channel
- Telecom high-speed transmissions
<table>
<thead>
<tr>
<th>Name/Model</th>
<th>Qty</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal Quality Analyzer</td>
<td>1</td>
<td>Requires 2 x 2ch PPG (MU195020A) and MU181000A/B + MU181500B option</td>
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<tr>
<td>MP1900A</td>
<td></td>
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<tr>
<td>or MP1800A</td>
<td></td>
<td>Requires 2 x 2ch PPG (MU183020A) or 4ch PPG (MU183021A) (2 x 2ch PPG recommended for BER and Jitter tests) and MU181000A/B + MU181500B option</td>
</tr>
<tr>
<td>G0374A 64 Gbaud PAM4 DAC</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Power Cord</td>
<td>1</td>
<td>Standard accessory</td>
</tr>
<tr>
<td>Sampling Oscilloscope</td>
<td>1</td>
<td>86100D (86118A 70 GHz Head + 86107A Time base)</td>
</tr>
<tr>
<td>Coaxial Cables</td>
<td></td>
<td></td>
</tr>
<tr>
<td>J1612A (specified electrical length, 80 cm, Individual delay difference of ≤3 ps)</td>
<td>4</td>
<td>4 Data inputs, standard accessory</td>
</tr>
<tr>
<td>J1611A (130 cm)</td>
<td>1</td>
<td>Clock input, standard accessory</td>
</tr>
<tr>
<td>34VV50 Adapter or J1655A (20 cm)</td>
<td>1</td>
<td>DAC output to scope (V-connector, 20 cm or shorter cable)</td>
</tr>
<tr>
<td>J1625A (1 m) or J1342A (80 cm)</td>
<td>2</td>
<td>Scope trigger Clock</td>
</tr>
<tr>
<td>V210 Terminator</td>
<td>1</td>
<td>For unused DAC output</td>
</tr>
<tr>
<td>41V-6 6 dB Attenuator</td>
<td>1</td>
<td>For scope input</td>
</tr>
<tr>
<td>J1678A ESD Protection Adapter-K</td>
<td>(5)</td>
<td>For Data and Clock inputs</td>
</tr>
</tbody>
</table>

* Duty Cycle Distortion, pulse width difference between even and odd bits, adjustable using CLKref voltage
Coaxial Cable Connections (64G x 2ch Combination)

- Example for 56 Gbaud operation

- J1612A 80 cm x4, Data Inputs
- D1A
- D1B

- Ch1
- Ch2

- MU195020A or MU18302xA

- 28 Gbps

- J1611A 130 cm Full-rate Clock (28 GHz)
- D0A
- D0B

- Ch3
- Ch4

- AUX Output (1/64 Clock Output)

- 2nd MU195020A/MU183020A CK Output, Divided MU181000A CK Output or MU181000B CK Output

- Time Base

- Trigger

- Scope

- V6 dB

- Terminate

Anritsu envision: ensure
G0374A Block Diagram

Data Input (MSB) D1A, D1B

Data Input (LSB) D0A, D0B

Clock Input

G0374A

6 dB Attenuator

6 dB Attenuator

6 dB Attenuator

6 dB Attenuator

64Gbaud DAC

MUX

DAC

MUX

CLKref

VEE

Vamp1

Vamp2

GND

D1A

D1B

D0A

D0B

Data Output

5 dB Attenuator

5 dB Attenuator

5 dB Attenuator
Setting Procedure (1/3)

1. Connect power cords of instruments to grounded power outlet.
2. Connect coaxial cables between the G0374A, SQA, and scope.
   (Use J1678A for Data and Clock inputs of G0374A to prevent ESD and EOS damage.)
3. Power-up G0374A.
4. Set Combination Setting to 64Gx2ch Combination.
   - For MP1900A mainframe and two MU195020A sets, click Module Settings button at bottom of GUI screen and click Combination setting button on Module Settings screen. Select 64Gx2ch Combination on Inter module combination setting.
   - For two MU183020A sets, click Combination Setting button at top of GUI screen and select 64Gx2ch Combination at Channel Synchronization as Combination function between modules.
   - For MU183021A, select 64Gx2ch Combination at Combination setting on Misc2 tab.
5. Set all Data output **Amplitude** to **1.0 Vp-p** and **Offset** to **Vth 0V**. The Grouping Setting function is useful when configuring multiple channels with the same settings.
   - For MP1900A mainframe and two MU195020A sets, click Module Settings button at bottom of GUI screen and click Module Grouping button on Module Settings screen. Set Output and Pattern of PPG Slot 1 and Slot 2 to ON. This shares the output amplitude, offset, and pattern settings of Data1 with the other Data outputs. Click [Execute] at [Module Grouping] to reflect the settings at Inter module grouping.
   - For two MU183020A sets, click “Setting…” button at Grouping setting on Misc2 tab of both PPGs and select “Output” checkbox. This shares the output amplitude and offset settings of Data1 with Data2.
   - For MU183021A, click “Setting…” button at Grouping setting on Misc2 tab and select “Data1-4” from Group dropdown list and select “Output” checkbox. This shares the output amplitude and offset settings of Data1 with Data2.
6. Set MU195020A or MU18302xA AUX output to 1/64 Clock output for scope trigger.
7. Set MU195020A or MU18302xA Clock output to full rate for Clock input of DAC.
8. Set Vamp1 and Vamp2 to maximum and set Data Duty to 0.
9. Turn on SQA output.
10. For two MU195020A and MU183020A sets at the Data1 setting screens of both PPGs, or for MU183021A at Data1 setting screen, set pattern to “Data” and bit length of 16 bits (0001 1011 0010 0111) and confirm that output waveform repeats 01230213 over.
11. Set same Delay value for all Data inputs and adjust so 01230213 is output. We recommend adjusting in 0.1UI units and setting Delay to the center of the proper adjustment range because the proper adjustment range is about 0.5UI (/period).
12. Set pattern to PRBS15 and monitor waveform using time-base trigger.
13. Adjust DCD (pulse width difference between even and odd bits) using Data Duty control.
Setting Procedure (3/3)

- The adjustment procedures in steps 10 and 11 are required when the bit rate is changed.
- To change to NRZ signal:
  - When using MP1900A mainframe and two MU195020A sets, click Module Settings button at bottom of GUI screen and click Combination setting button on Module Settings screen. Select 2CH Combination on Inter module combination setting. Click [Execute] at [Module Grouping] to reflect the settings at Inter module grouping.
  - When using two MU183020A sets, click Combination Setting button at top of GUI screen and set Channel Synchronization to 2ch Combination as Combination function between modules.
  - For MU183021A, change to 2ch CH Sync at Misc2 tab.

This will align the start bit positions for each 2ch Combination pattern used for MSB and LSB input, and the PRBS15 NRZ waveform can be confirmed when output is set to On because the pattern is set to the PRBS15 default.

![Diagram showing start bit position for both MSB and LSB at PRBS15]

NRZ for converted pattern at PRBS15
Typical Waveform at Setting

Pattern setting “0001 1011 0010 0111”
“01230213” observed

Magnified “01230213”
Typical Waveforms (1/2)

Vamp1 and Vamp2 set to maximum

Adjust amplitude using Vamp1 and Vamp2 control
Typical Waveforms (2/2)
64 Gbaud: Sample waveform before adjusting DCD using Data Duty

56 Gbaud: Sample waveform before adjusting DCD using Data Duty

Adjust Data Duty
Setting Procedure for NRZ 2Tap Emphasis (1/2)

After completing the previous settings, monitor the NRZ signal and use the following procedure to add Emphasis.

1. Change the D0A and D0B input cable connections in slide 4 as shown below.
Setting Procedure for NRZ 2Tap Emphasis (2/2)

2. Set Combination Setting to the same settings as at NRZ output (see slide 8).
3. Set the same patterns at the Data1, 2 and Data 3, 4 combinations as set at 2ch Combination.
4. Set the Data3, 4 pattern Logic to NEG.
5. Add 1UI to the Delay setting of Data4 (PPG output connected to D0A input).

56 Gbaud 2Tap Emphasis, sample waveform

64 Gbaud, PRBS $2^7$-1 pattern

64 Gbaud, 16 bit “11...00...” pattern
# MP1900A/MP1800A Setting for Each Waveform Pattern

<table>
<thead>
<tr>
<th>Output</th>
<th>PPG Settings</th>
<th>G0374A Settings</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Modulation</td>
<td>Baud Rate</td>
<td>Composition</td>
<td>Combination Setting</td>
</tr>
<tr>
<td>PAM4</td>
<td>&gt;32.1G</td>
<td>2ch</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>2.4 to 32.1G</td>
<td>2ch</td>
<td>2ch Combination</td>
</tr>
<tr>
<td></td>
<td>4.8 to 64G</td>
<td>2ch x 2 slot or 4ch</td>
<td>64G x 2ch Combination</td>
</tr>
<tr>
<td></td>
<td>4ch</td>
<td>4ch Combination</td>
<td>-</td>
</tr>
<tr>
<td>NRZ</td>
<td>4.8 to 64G</td>
<td>2ch</td>
<td>2ch Combination</td>
</tr>
<tr>
<td></td>
<td>2ch x 2 slot</td>
<td>2ch Comb. and 2ch CH Sync.</td>
<td>2.0 V Vth 0 V</td>
</tr>
<tr>
<td></td>
<td>4ch</td>
<td>2ch Comb. and 2ch CH Sync.</td>
<td>1.0 V Vth 0 V</td>
</tr>
<tr>
<td>NRZ with Emphasis</td>
<td>4.8 to 64G</td>
<td>2ch x 2 slot</td>
<td>2ch Comb. and 2ch CH Sync.</td>
</tr>
<tr>
<td></td>
<td>4ch</td>
<td>2ch Comb. and 2ch CH Sync.</td>
<td>-</td>
</tr>
</tbody>
</table>