



Supplementary Explanation of MP1825B-002 Full and Half-Rate Clock Operation

Signal Quality Analyzer MP1800A Series
4 Tap Emphasis MP1825B

The MP1825B options are as follows.

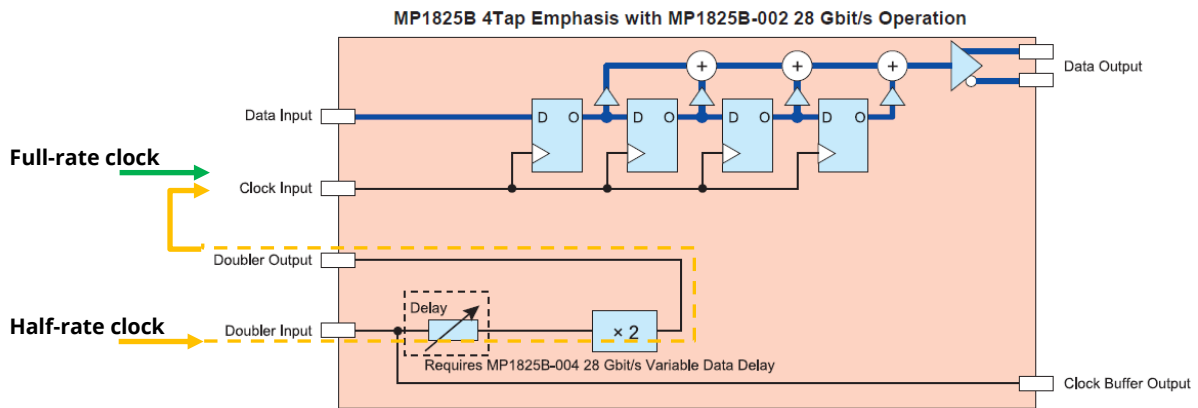
No.	Main Frame	Bit Rate	Data Delay
1	MP1825B 4Tap Emphasis	MP1825B-001 14 Gbit/s Operation	MP1825B-003 14 Gbit/s Variable Data Delay
2			
3		MP1825B-001 14 Gbit/s Operation	MP1825B-003 14 Gbit/s Variable Data Delay
4		MP1825B-005 14.1 Gbit/s Extension	
5		MP1825B-002 28 Gbit/s Operation	MP1825B-004 28 Gbit/s Variable Data Delay
6		MP1825B-002 28 Gbit/s Operation	
7		MP1825B-006 32.1 Gbit/s Extension	

This document describes the full and half-rate clock operation up to 28.1 Gbit/s of the MP1825B with the MP1825B-002 option. Two clock-rate operation options can be selected: full-rate clock, and half-rate clock.

At full-rate clock operation, the full-rate clock is connected to Clock Input as shown in the following diagram.

At half-rate clock operation, the half-rate clock is connected to Doubler Input which creates a full-rate clock from the half-rate clock and outputs it from Doubler Output. The output of Doubler Output is connected to Clock Input.

The MP1825B-004 Variable Data Delay option is supported only by the half-rate clock operation.



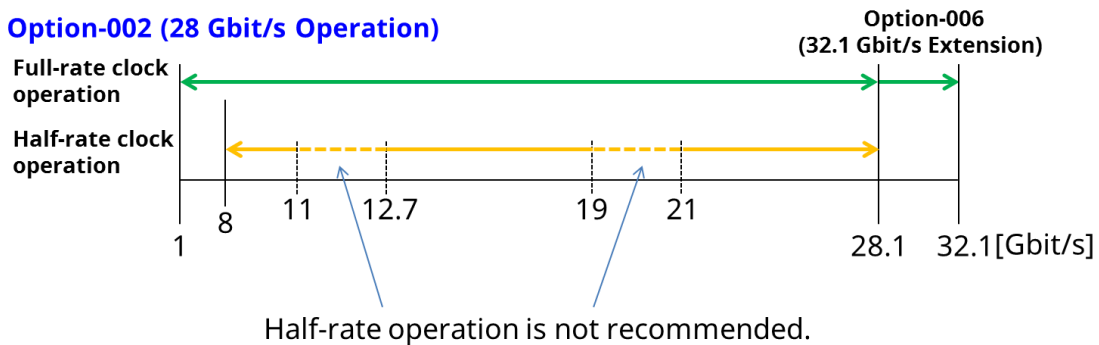
The MP1825B-002 operation bit rate specification differs according to whether full-rate or half-rate clock operation is used.

Operation bit rate specification

Full-rate clock operation: 1 to 28.1 Gbit/s

Half-rate clock operation: 8 to 28.1 Gbit/s

The half-rate clock operation can be used when using the Variable Data Delay function (MP1825B-004), but the half-rate clock operation range of the MP1825B-002 has two restricted bandwidths: from 11 to 12.7 Gbit/s, and from 19 to 21 Gbit/s, where jitter transparency is not maintained fully. Consequently, Anritsu recommends using full-rate clock operation in these two

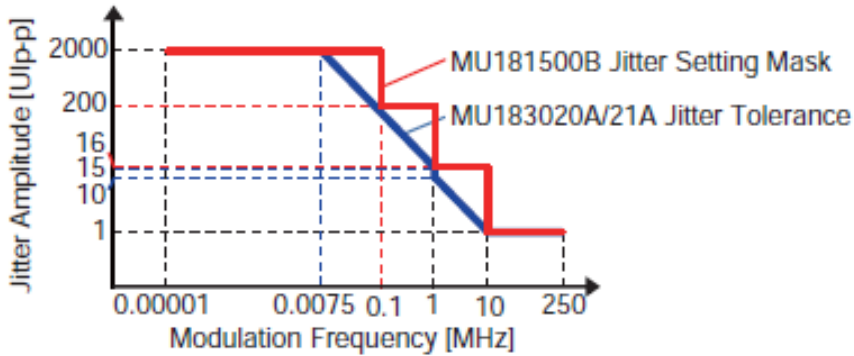


ranges.

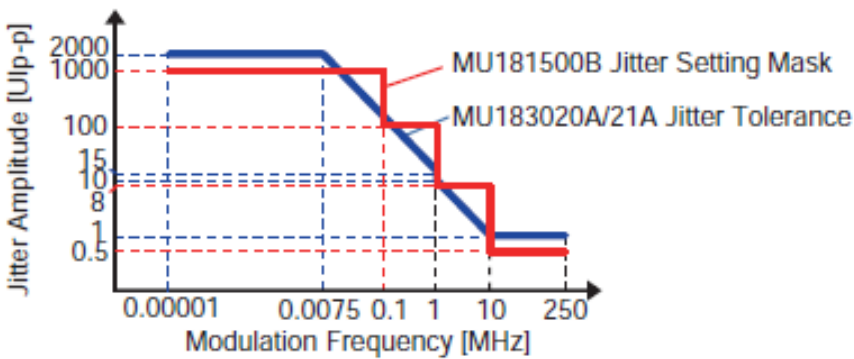
Note:

- When setting the full-rate clock, the SJ amplitude setting range of the MU181500B changes according to the bit rate. (For details, refer to the MP1800A series catalog or the MU181500B specifications.)
- The following figures are from the catalog. As an example, when the bit rate is higher than 15 Gbit/s, the maximum jitter amplitude setting (MU181500B Jitter Setting Mask) at the SJ Modulation frequency 250 MHz is 1 UIp-p compared to 0.5 UIp-p when the bit rate is less than 15 Gbit/s.

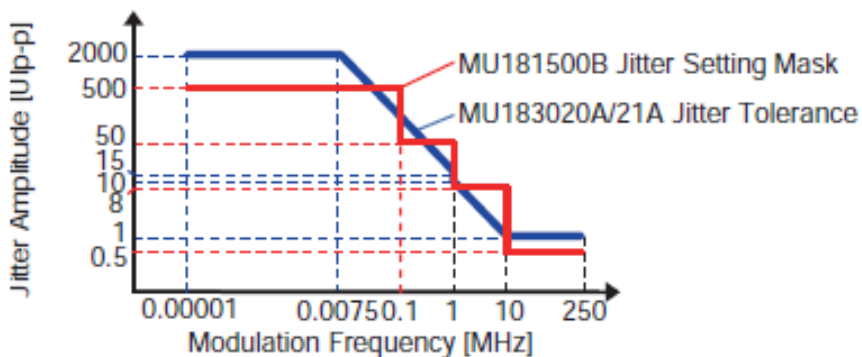
Full rate Clock Out setting, Bit-rate: 15 Gbit/s to 32.1 Gbit/s
Half rate Clock Out setting, Bit-rate: 2.4 Gbit/s to 32.1 Gbit/s



Full rate Clock Out setting, Bit-rate: 4 Gbit/s to 15 Gbit/s



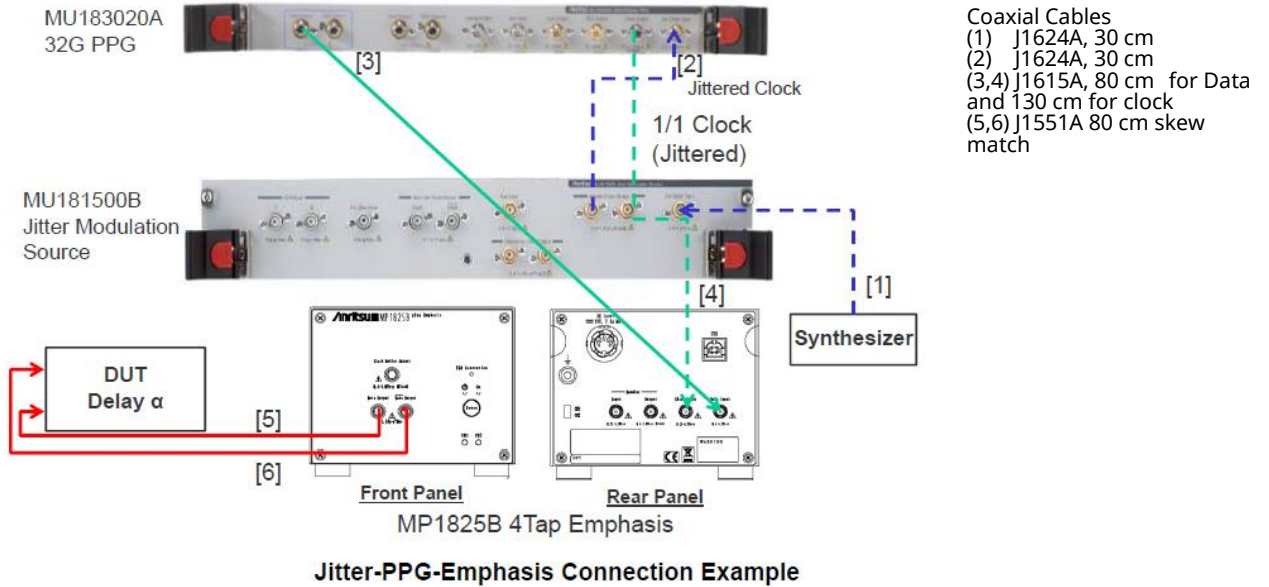
Full rate Clock Out setting, Bit-rate: 2.4 Gbit/s to 4 Gbit/s



Note:

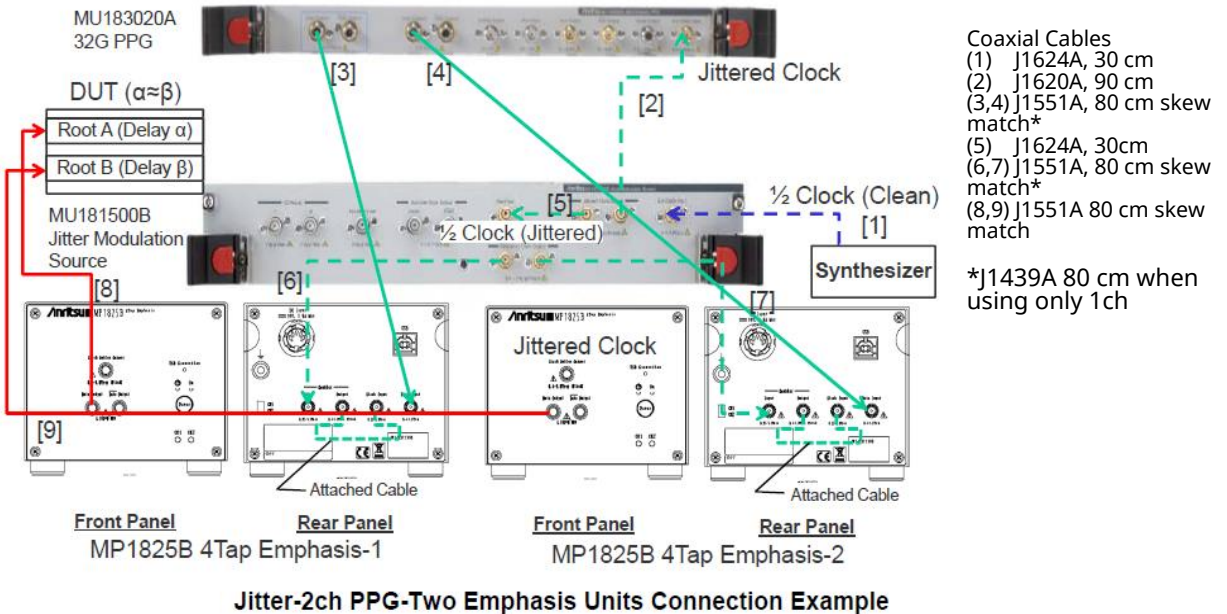
To test by adding transparent jitter to the MP1825B data output, the cables must be connected correctly between the MU183020A, MU181500B and MP1825B for both full-rate and half-rate clock operation. (For details, refer to Appendix B "Connection Example for Jitter Measurement" in the MP1825B operation manual. The following figures are from the operation manual.)

Connection diagram for full-rate clock operation



Connection diagram for half-rate clock operation

The MP1825B x2ch connections are shown. The connection at the "MP1825B 4Tap Emphasis-2" side is not required when using only 1ch.



Note:

When switching Output Off \rightarrow On after adjusting the delay of the MP1825B Data output, operation of the Data/Clock phase adjustment function of the PPG connected to each MP1825B may cause a half-bit phase shift in the MP1825B Data output. When the MP1825B cx 2ch signal is PAM4-combined at half-rate clock operation, either perform the test without switching Off \rightarrow On so the 2ch skew does not drift, or perform the test after re-confirming the 2ch skew again after switching Off \rightarrow On.

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