The Forefront of Ultra-High-Speed Interconnect Development

Test Solutions Supporting Advanced Technologies

Qualitas Semiconductor Co., Ltd.

Enhancing signal integrity verification for high-speed interconnects using Anritsu's Vector Network Analyzer (VNA)

Improving the development efficiency of PHY IP solutions while ensuring quality and reliability

Overview

Qualitas Semiconductor Co., Ltd. (hereinafter "Qualitas"), a leading company headquartered in South Korea, develops and provides advanced PHY IP solutions for high-speed interconnects. PHY IP refers to physical-layer design blocks that handle the transmission and reception of digital signals in high-speed interfaces, such as PCI Express® (PCIe®) and USB.

Data transmission speeds are continually increasing in high-speed interconnects, making signal integrity requirements increasingly stringent. So simply verifying a chip is no longer sufficient. It is now essential to comprehensively evaluate the entire interconnect channel, including the printed circuit boards (PCBs), chip packages, and sockets that connect the chip to the PCB. As a result, building a verification environment capable of performing these verifications has become a critical challenge.

To address these challenges, Qualitas started using Anritsu's ShockLine™ MS46524B, which is a vector network analyzer (VNA). And by establishing a verification environment that enables highly accurate and repeatable evaluations of signal integrity across the entire system, including PHY IP, Qualitas has significantly improved the quality and reliability of its IP solutions.

In an interview with Dr. Jaeyoung Kim, the executive director of R&D Center at Qualitas, this article explains the technical challenges the company has faced, its efforts to enhance the verification environment, the key factors behind selecting Anritsu's solution, and its technology strategy for the next generation of interface standards.

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Dr. **Jaeyoung Kim**, executive director of R&D Center at Qualitas

— Could you tell us about your business and its core strengths?

Qualitas is a semiconductor design company specializing in developing PHY IP for high-speed interconnect applications. Its portfolio includes a wide range of high-value PHY IP solutions, such as SerDes, PCIe, Universal Chiplet Interconnect Express (UCIe), Ethernet, Mobile Industry Processor Interface (MIPI), and USB SuperSpeed+. These PHY IP solutions have been adopted by many of its customers as core components that ensure signal integrity across various high-speed communication standards.

Our company's key strengths lie in its advanced signal integrity technologies and highly accurate circuit design capabilities that are optimized for leading-edge process nodes. To maintain stable operations even as circuits continue to increase in speed and density, we place strong emphasis on the implementation conditions from the design stage onward. Specifically, we employ a holistic design approach that considers the entire interconnect channel, including packages, PCBs, and sockets. In addition, we have developed a large portfolio of "silicon-proven IPs" whose performance has been verified on actual silicon, enabling the delivery of highly reliable IP solutions.

Building on this strong technical foundation, we have established numerous supply agreements with leading companies in major semiconductor markets, including the United States, China, and Japan, and we have accumulated extensive verification data and mass-production experience. By reducing the design burden on customers while contributing to shorter development cycles and more stable mass production, we have positioned ourselves as a trusted technology partner in growth areas, such as next-generation AI, data centers, automotive applications, and chiplet-based systems.

— Why is signal integrity verification becoming more important?

Major interfaces, such as PCIe, UCIe, USB, and Ethernet, continue to increase in speed with each new generation. As a result, the tolerance for signal integrity has rapidly decreased, and parasitic effects, such as channel loss, reflections, crosstalk, and impedance mismatches, now have a direct impact on the overall operations of systems. Consequently, conventional verification approaches that focus solely on chips no longer ensure signal integrity in real-world applications.

The signal integrity of high-speed signals is determined by the entire interconnect structure, such as the internal package wiring, PCB trace length, dielectric properties, layer stack-up, and via structures, as well as the sockets and connectors. As signal transmission speeds increase, even slight differences in these structures can lead to significant degradation in signal quality. Therefore, without verifying an environment that closely reflects the actual implementation, it becomes difficult to guarantee that the system will perform as expected under real operating conditions. While standalone chip evaluations are satisfactory, system-level implementation often reveals reflections and discontinuities, which can erode the operating margin and lead to marginal operation. So the scope of verification must be expanded from just the chip to the entire interconnect channel, including the packages, PCBs, and connectors. Ensuring signal integrity now requires optimization of the complete channel.

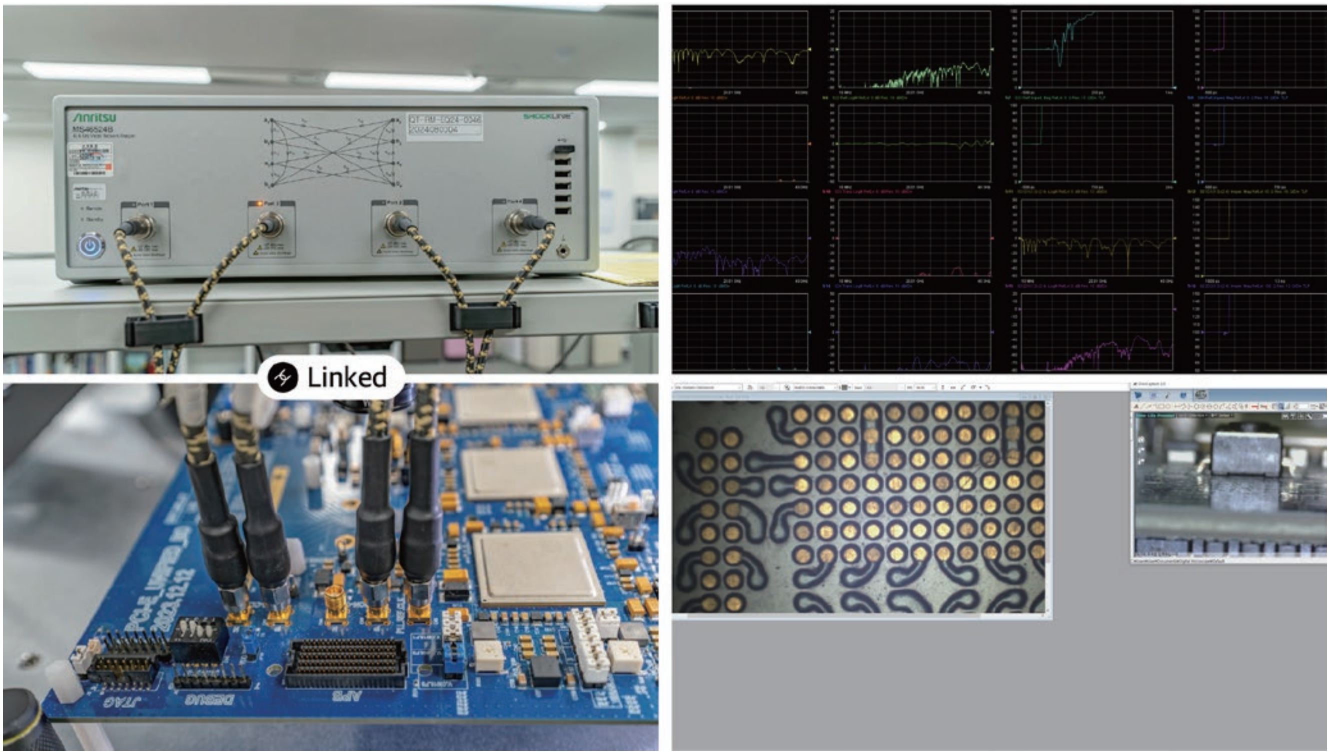
— Could you tell us about the limitations you faced with conventional approaches?

With high-speed interconnect development, we found that conventional simulation-based approaches could not fully reproduce the signal degradation that occurs after a system has been implemented. Even very small differences in package structures or PCB trace lengths can increase loss, reflections, and crosstalk, significantly impacting the operation of PHY IP. However, these implementation-dependent effects are inherently difficult to model, and in many cases, they cannot be sufficiently reproduced or detected through just simulations.

Consequently, problems remain latent during the design phase and are only identified during actual measurements, triggering cascading changes to the design, PCB, and test fixtures in later stages and resulting in substantial rework. In addition, an increasing number of global customers began to demand rigorous reliability verification, based on actual measurement data. So it became clear that the conventional simulation-centric approach had reached its limits and was no longer sufficient to meet customer requirements.

— Why did you select Anritsu's MS46524B?

In response to these challenges, we began shifting away from a simulation-centric approach toward upfront verification under conditions that closely reflect actual implementations. And to address next-generation interface standards and increasingly



ShockLine™ VNA MS46524B

Measurement Screen

The high-speed interconnect verification environment at Qualitas

diverse package structures, establishing a verification environment that is capable of quantitatively verifying signal integrity under realistic implementation conditions was urgently needed. So we decided to introduce a VNA.

After comparing products from multiple vendors, the primary reasons we selected Anritsu's MS46524B were its measurement stability at high frequencies and its flexibility in adapting to the complexity of real-world interconnect implementation conditions. In verification environments where probe-based measurements and coaxial measurements are mixed, measurement conditions tend to vary, making it difficult to maintain repeatability.
However, during pre-evaluations, the MS46524B demonstrated stable and highly repeatable measurement results under such conditions, and we evaluated this as a key advantage over competing products.

In addition, the MS46524B supports high-resolution time domain reflectometry (TDR) measurements with a resolution of less than 10 picoseconds, enabling visualization of impedance variations within interconnect structures, which is essential for verifying fine package structures and high-speed signal paths. It also provides a significant benefit in terms of scalability for future technologies.

— What have you achieved by introducing the MS46524B?

After introducing the VNA, we created an environment that enables efficient verification of different structures, such as PCBs, packages, and test chips, on a single platform. Using differential S-parameter measurements, we can accurately characterize insertion loss, reflection characteristics, and differential transmission behavior. In addition, differential TDR measurements allow us to intuitively identify impedance discontinuities and issues related to fine structures in the time domain. By combining these measurement techniques, we have been able to rapidly identify the root causes of issues and streamline the feedback between design and verification.

Anritsu's proprietary software has also enabled us to automate and standardize the measurement workflow, significantly improving verification efficiency. And the lead time for generating quality reports and submitting results to customers has been reduced, allowing us to meet the verification speed and quality standards required by global customers. As a result, we have improved our ability to identify issues at the design stage, which has reduced the need for rework in the later phases of development. This has enabled us to achieve both higher IP design quality and shorter times to market.

— What challenges did you face when building the high-speed interconnect verification environment, and how did you address them?

High-speed interconnect verification required significantly more trial and error than we expected, particularly in probe-based, non-coaxial measurements, such as probe-to-coax and probe-to-probe configurations. When evaluating ball-pad packages or fine PCB patterns, even slight variations in probe contact conditions or alignment can directly affect measurement results, making it difficult to establish accurate reference planes and ensure measurement repeatability.

To address these challenges, we applied the four-port configuration of the MS46524B to build a consistent measurement setup that supports both probe-to-coax and probe-to-probe measurements. In addition, we applied Type-E network extraction techniques, which isolate and compensate for known network elements in the measurement path, and de-embedding techniques that mathematically remove parasitic effects caused by probes and cables. This enabled us to establish a verification environment that is capable of accurately extracting the intrinsic characteristics of the device under test (DUT).

Another major challenge in probe-based verification of high-speed interconnects was minimizing discrepancies between measurement environments and actual system implementations. Conventional pad-level verifications often failed to sufficiently reflect the impact of PCB layouts and package structures on signal integrity, resulting in cases where measured characteristics did not match real-world behavior. As interconnect speeds continue to increase, these discrepancies have grown, making it difficult to achieve sufficient verification accuracy using traditional methods alone.

To overcome this issue, we design evaluation boards (EVBs) that faithfully replicate not only pad-level structures but also actual PCB layouts and package configurations, and we perform probe-based measurements on these boards. Furthermore, by combining differential S-parameter measurements and TDR measurements in probe-to-coax and probe-to-probe environments, we quantitatively compare and analyze differences between measurement results. This approach enables us to accurately capture implementation-dependent effects from the perspectives of the frequency- and time-domains.

By conducting multifaceted probe-based measurements that consider implementation conditions, we can now gain advanced insight into signal integrity behavior that closely reflects real system environments. This has significantly improved the accuracy of behavior predictions in customer environments and enhanced the reliability of our IP solutions.

— How do you utilize de-embedding technology in your verification process, and what benefits does it provide?

In high-speed interconnect verification, measurement fixtures, such as probes and cables, can significantly affect signal integrity. As a result, the accuracy with which the intrinsic characteristics of the DUT can be extracted has a major impact on the overall verification accuracy. To address this challenge, we use the four-port measurement configuration of the MS46524B to extract the S-parameters of external elements in the measurement path in advance, and then we apply de-embedding processing to remove their influence.

The de-embedding approach we emphasize is a correction technique that mathematically removes the effects of cables, probes, and other elements included in the measurement system so that only the DUT’s intrinsic characteristics are extracted. This has enabled us to obtain key signal integrity parameters, such as insertion loss, impedance variations, and reflection characteristics, with high accuracy. In particular, for high-loss channels and packages with fine structures, the presence or absence of de-embedding can significantly affect the resolution of the measurement results, making it an essential step in the verification process.

The high-accuracy measurement data obtained through this process is used as valuable feedback during the PHY IP design phase, and this directly contributes to more precise design improvements, higher quality, and shorter development cycles. For Qualitas, de-embedding technology is indispensable for meeting the stringent quality requirements of the next-generation interface standards.

High-speed interconnect PHY IP verification in action

— What impact has the verification environment had on the quality of your PHY IP and your future technology development strategy?

By establishing a signal integrity verification environment centered on the MS46524B, we have built a framework that enables quantitative upfront verification of system-level transmission characteristics, including packages, PCBs, and test chips. As a result, the repeatability of high-frequency measurements has improved significantly, allowing us to consistently ensure PHY IP quality from the early stages of design.

In addition, the use of Anritsu's customized software has advanced the automation and standardization of measurement workflows, which has reduced the variability of verification activities. This has enabled us to obtain reliable feedback in shorter cycles and establish a process for rapidly providing the measurement data required for quality reporting and ramping up mass production. As a result, our ability to meet the demanding requirements of global customers has been further strengthened.

This verification environment, which we are already using as a foundation for quality assurance in the current development of PHY IP, will continue to play a critical role in our future technology strategy. By flexibly supporting increasingly diverse package structures, as well as next-generation high-speed standards, such as UCIe and PCIe Gen6, the environment enables a continuous cycle of enhancing technical capabilities while simultaneously improving the development speed and quality for next-generation IPs. For Qualitas, this environment represents an indispensable foundation for maintaining long-term signal integrity competitiveness and strengthening its presence in the global market.

— Could you tell us about your future verification environment for next-generation high-speed interfaces?

For next-generation interfaces, we anticipate that the requirements for accuracy and repeatability in signal integrity verification will become even more stringent due to increasingly complex package structures, the widespread adoption of chiplet architectures, and further increases in data rates. In response, we are continuing to enhance our verification environment to keep pace with these evolving technology trends.

Specifically, we plan to further expand our probe-based measurement environment, centered on the MS46524B, and to develop it into a platform that is capable of wider bandwidth and higher-precision differential measurements. In addition, by strengthening its integration with our proprietary verification software, we aim to establish workflows that can consistently deliver highly repeatable measurement results, even for increasingly complex package and interconnect structures.

Furthermore, to enhance our readiness for next-generation high-speed standards, such as UCIe and PCIe Gen6, we are advancing our measurement methodologies, calibration processes, and data analysis procedures. At the same time, we are actively participating in industry-standardization activities and joint research with external partners, which is contributing to the creation of verification models and evaluation metrics that are suited to future interface specifications. Through these initiatives, we aim to continuously improve the overall accuracy of signal integrity verification and sustainably strengthen the competitiveness required for next-generation product development.

— What elements are necessary for high-speed interconnect IP vendors to strengthen their competitiveness in the global market?

To enhance competitiveness in the global market, it is no longer sufficient to provide PHY IP that merely meets industry standards. With the latest interfaces becoming increasingly high-speed and high-density, stable operations in real system environments are crucial. As a result, it has become essential to demonstrate signal quality across the entire interconnect, including packages, PCBs, and sockets, based on actual measurement data.

At Qualitas, we perform upfront verification that faithfully reproduces implementation environments from the early stages of development. By using measurements such as differential S-parameters and TDR, we have established a framework that enables us to present objective data showing how our PHY IP behaves under real operating conditions. In addition, our highly reliable measurement environment, which incorporates the MS46524B, enables us to rapidly deliver verification results that meet the stringent requirements of global customers, which provides us with a significant competitive advantage.

— What aspects of your collaboration with Anritsu were particularly impressive?

What stood out most in our collaboration with Anritsu was the hands-on, practical support we received when facing technical challenges. Rather than simply supplying measurement equipment, Anritsu took the time to gain a deep understanding of our verification environment and workflows, and proactively provided technical support tailored to our specific challenges.

High-frequency measurements involve many complex steps, and they require expert judgment. To address this, Anritsu also worked closely with us on the joint development of customized software that enables automation and standardization of measurement procedures, making these processes more efficient and reliable. As a result, variability in probe-based verification work was significantly reduced, leading to major improvements in measurement repeatability and overall operational efficiency.

Through this close collaboration, we were able to build a relationship with Anritsu that goes beyond the conventional equipment-supplier model. And we have established a reliable, long-term technical partnership that is aimed at jointly advancing verification technologies for next-generation interfaces, which we consider to be the most significant outcome of our collaboration.