Multi-channel high speed solution

Signal Quality Analyzer
MP1800A Series

32G Solutions (NRZ / PAM4)
64G Solutions (NRZ / PAM4)
High speed serial bus solutions
Multi-channel SQA Solution

Product Overview
- Multichannel 20 to 30 Gbit/s is key technology for high-end computers, servers, and 100G / 400G network communications.
- 28 GBaud PAM4 is major technology for 100G / 400G communications. 53G NZR / 53GBaud PAM4 development has started toward the realization of 400 GbE.
NRZ / PAM4 standards

- 25G / 50G / 200GbE / 400GbE standardization are on going.
- PAM4 becomes major technology for various standards.
- Most of PAM4 actual baud-rate is 26.6G.
- To assure PAM4 signal Integrity, PAM4 BER measurement is key factors.

<table>
<thead>
<tr>
<th>Optical Interface</th>
<th>Electrical Interface (OIF-CEI)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard</td>
<td>Format</td>
</tr>
<tr>
<td>400G BASE-SR16</td>
<td>100m</td>
</tr>
<tr>
<td>400G BASE-DR4</td>
<td>500m</td>
</tr>
<tr>
<td>400G BASE-FR8</td>
<td>2km</td>
</tr>
<tr>
<td>400G BASE-LR8</td>
<td>10km</td>
</tr>
<tr>
<td>200G BASE-SR8*</td>
<td>100m*</td>
</tr>
<tr>
<td>200G BASE-SR4*</td>
<td>100m*</td>
</tr>
<tr>
<td>200G BASE-FR4*</td>
<td>2km*</td>
</tr>
<tr>
<td>200G BASE-LR4*</td>
<td>10km*</td>
</tr>
<tr>
<td>100G BASE-SR10</td>
<td>100m/150m</td>
</tr>
<tr>
<td>100G BASE-SR2*</td>
<td>100m*</td>
</tr>
<tr>
<td>100G BASE-SR4</td>
<td>70/100m</td>
</tr>
<tr>
<td>100G SWDM</td>
<td>400m</td>
</tr>
<tr>
<td>100G PSM4</td>
<td>500m</td>
</tr>
<tr>
<td>100G CWDM4/CLR4</td>
<td>2km</td>
</tr>
<tr>
<td>100G BASE-LR4</td>
<td>10km</td>
</tr>
<tr>
<td>100G BASE-ER4</td>
<td>40km</td>
</tr>
<tr>
<td>100G BASE-CR4</td>
<td>10km</td>
</tr>
<tr>
<td>100G BASE-KR4</td>
<td>20km</td>
</tr>
<tr>
<td>100G BASE-KP4</td>
<td>10km</td>
</tr>
<tr>
<td>50G BASE-SR*</td>
<td>100m</td>
</tr>
<tr>
<td>50G BASE-FR*</td>
<td>2km</td>
</tr>
<tr>
<td>50G BASE-LR</td>
<td>10km</td>
</tr>
<tr>
<td>25G BASE-SR</td>
<td>100m</td>
</tr>
<tr>
<td>25G BASE-FR</td>
<td>2km</td>
</tr>
<tr>
<td>25G BASE-LR</td>
<td>10km</td>
</tr>
</tbody>
</table>

*: Under discussion
Feature of Anritsu high speed PAM4 / NRZ solutions

- Flexible upgradability: Singe channel to Multi channels, PAM4 (Up to 64Gbit/s)
- High quality waveform: Low intrinsic jitter (300 fs @ 28.1Gbps with clock pattern).
- High input sensitivity: 56G/64G DEMUX MP1862A (Typ.25 mV@56.2 Gbps)
  28G/32G ED MU18304xB (Typ.10 mV@28.1 Gbps)
- Jitter transparent NRZ / PAM4 solutions with various types of jitters
Features of 32G All-in-One Jitter BERT

- Wideband bit rates from 2.4 to 32.1 Gbit/s
- 1 Tbit/s synchronous BERT: 8ch PPG in one box and 4 boxes synchronization
- High-input-sensitivity ED at 10 mV (typical, single-end, Eye Height)
- Integrated Clock Recovery option with complete jitter tolerance test
- PAM4 generation and BER measurement

Various Signal Integrity Analysis Functions
- Jitter Tolerance (with MX183000A) SJ = 1UI @ fm: 250 MHz
- 4Tap Emphasis with MP1825B
- Crosstalk testing with individual variable delay

Excellent Signal Quality and Rx Sensitivity
- Low intrinsic jitter: 300 fs
- Fast Tr / Tf: 12 ps
- Wide output amplitude range 0.5 to 3.5 V p-p
- High input sensitivity: 10 mV
- PAM4 / PAM8 generation (MZ1834A/MZ1838A)
- PAM4 BER Measurement

Supports Data Patterns for Various Applications
- PAM4 PRBS, Gray code etc.
- Burst signal test
- 256 Mbits / ch max. user programmable pattern CJTPAT, CJPAT, K28.5 etc.
- Pre-coding, de-coding DQPSK, DP-QPSK
Features of 56G / 64G All-in-One jitter BERT

- Low intrinsic Jitter: $R_J = 200$ fs rms (typical)
- Variable amplitude: 0.5 to 3.5 Vp-p
- Full jitter components generation $R_J$, BUJ, Dual tone SJ, SSC.
  SJ generation 0.55 UI @ fm 250 MHz

- High Input sensitivity: 25 mV (typical, single-end, EYE height)
- Bathtub Analysis as well as Eye Margin, Eye Diagram auto measurement
- Automatic jitter tolerance test with MX181500A software

- PAM4 signal generation up to 64GBaud with DAC Box (G0374A)
- 56 Gbaud PAM4 BER measurement up to PRBS15

- 56 Gbit/s signal EYE opening recovery by J1646A (6 dB passive equalizer)
Multi-channel SQA Solution

28G / 32G Solution
Module Lineup

■ 28G/32G PPG/ED Module
MU183020A 28G/32G bit/s PPG (1ch or 2ch)

MU183021A 28G/32G bit/s 4ch PPG

■ 28G/32G BERT Typical Configurations

MP1800A
Max. 6 Slots

28G/32 G Jitter BERT
- 32G PPG 1ch or 2ch
- 32G ED 1ch or 2ch
- Synthesizer (2 Slots)
- Jitter Generator (2 Slots)

28G/32G 4ch BERT
- 32G PPG 4ch (2 Slots)
- 32G ED 4ch (2 Slots)
- Synthesizer (2 Slots)

28G/32G 8ch Jitter BERT (2 Box)
- 32G PPG 4ch (2 Slots)
- 32G ED 4ch (2 Slots)
- Jitter (2 Slots)
- Synthesizer (2 Slots)

MU183040B 28G/32G bit/s High Sensitivity ED (1ch or 2ch)

MU183041B 28G/32G bit/s High Sensitivity 4ch
Features (1) Waveform Quality

- **Low-Jitter, High-Quality Waveforms with Output $\leq 3.5$ Vp-p**

Output waveform at 28 Gbit/s, 2.0 Vp-p (MU183020A-012)

Output waveform at 28 Gbit/s, 3.5 Vp-p (MU183020A-013)

28 Gbit/s, PPG Intrinsic RJ rms
Using sampling oscilloscope with 50 GHz bandwidth and $<100$ fs rms intrinsic jitter
Features (2) Rx Input Sensitivity

- **World’s Best Input Sensitivity Error Detector (MU183040B/MU183041B)**
  - EYE amplitude sensitivity: 15 mVp-p (typ., 28.1 Gbit/s, single-end), ≤25 mVp-p (28.1 Gbit/s, single-end)
  - EYE Height sensitivity: 10 mVp-p (typ., 28.1 Gbit/s, single-end)

- **Passive Equalizer**
  - Insertion before ED recovers EYE opening by correcting transmission-path losses
  - Combination with MU183040B/MU183041B High Sensitivity ED supports Jitter Tolerance tests of physical devices with narrow Eye Opening

- **Jitter Tolerance Testing for Async SERDES by embedded Clock Recovery**
  - Loop bandwidth: Bit rate/1667, Bit rate/2578, 1 MHz to 17 MHz*
  - Supports clock recovery and high input sensitivity

*Opt-022
Features (3) Skew testing by synchronous PPGs

- **Individual Variable Data Skew for Each Channel**
  - Built-in PPG Data Delay option supports independent phase control for each channel

  ![Max. 8ch synchronization and individual variable delay](image)

- **Crosstalk Test**
  - High-accuracy control of data synchronized between channels in 1 mUI steps supports accurate validation of DUT crosstalk characteristics
Features (4) Jitter generation capability

- **Jitter Tolerance Test up to 32.1 Gbit/s**
  - RJ / SJ (2 tone) / BUJ / SSC generation
  - Automatic Jitter Tolerance test using MX183000A
    - SJ: 2000UI max., 1UI @ fm = 250 MHz
    - Shorten measurement time by estimating low error rate result
  - Half-period Jitter (F/2 Jitter) generation using MU183020A PPG

![MU181500B Jitter Modulation Source Setting Screen](image1)

![MX183000A PL001 Jitter Tolerance Test Software Result Screen](image2)

- **Sine-Wave Jitter**
- **Random Jitter**
- **Bounded Uncorrelated Jitter**
- **Half-Period Jitter (HPJ, F/2 Jitter)**

![Graph showing Low Intrinsic Jitter](image3)

(Enhanced MP1800A)

Before Enhancement

(measured value using 50-GHz band sampling oscilloscope with Residual Jitter of <100 fs)
Features (5) Emphasis capability

- **4Tap Emphasis Signal Generator up to 32.1 Gbit/s (with MP1825B)**
  - High quality Emphasis signal of Low Jitter and steep Tr/Tf
  - Setting by Pre-emphasis, De-emphasis, Co-efficient
Features (6) Various Analysis functions

Eye Contour Measurement

EYE Margin Measurement

PAM BER Measurement

Bathtub Jitter Measurement

Q Measurement
Features (7) Supports various data patterns

• **PAM4 Patterns**
  – PRBS13Q, GreyPRBS13Q, SSPR, JP03A, JP03B, Square wave

• **DQPSK, DP-QPSK Pre-coding**
  – DQPSK, DPQPSK Pre-code signal generation

• **Burst Signal Test**
  – Supports optical circulation loop test
  – Burst disable time up to 1uS (Typical)

• **Maximum 256 Mbit/ch Programmable Data Pattern**
  – Generates any pattern for applications, such as CJTPAT, CJPAT, K28.5

• **Pseudo random Patterns (PRBS)**
  – $2^n-1$ (n = 7, 9, 10, 11, 15, 20, 23, 31)

• **Zero-Substitution Pattern**
  – Suitable for clock recovery contiguous “0” / “1” tolerance test
  – Incremental number of “0” / “1” inside of PRBS pattern up to PRBS23
Features (8) Frequent used items on one screen

- **Customize screen**
  - For easy operation, you can select up to 18 items on one screen.
  - Selected items can be saved / recall from internal memory.
PAM Features (1) PAM signal generation

- **PAM4/PAM8 Generation (MZ1834A/MZ1838A 4/8 PAM Converter)**
  - PAM4 Differential signal generation: MZ1834A + PPG 2ch
  - PAM8 Differential signal generation: MZ1838A + PPG 3ch
  - Wideband 32.1 Gbaud rate
  - High-quality EYE opening, high-speed Tr/Tf
  - PAM Control GUI: Adjustable PPG Data Output for setting PAM signal levels
PAM Features (2) Various PAM4 patterns

- 32GBaud PAM4 Patterns
  - Pattern files used for PAM4 signal generation/BER measurement have been added.
  - Select Edit after setting Test Pattern to Data. [1]
  - The following PAM4 Data Patterns can be selected from the Pattern Editor file list.[2]

Using Combination Mode for PPG_CH1 and PPG_CH2 to generate above PAM4 patterns. Using Independent Mode for ED to measure above PAM4 patterns.

<table>
<thead>
<tr>
<th>Pattern</th>
<th>PPG1 Pattern file</th>
<th>PPG2 Pattern file</th>
<th>ED Top EYE Pattern</th>
<th>ED Middle EYE Pattern</th>
<th>ED Bottom EYE Pattern</th>
</tr>
</thead>
<tbody>
<tr>
<td>PRBS13Q</td>
<td>PRQS13Q_TX1.txt</td>
<td>PRQS13Q_TX2.txt</td>
<td>PRBS13Q_Upper.txt</td>
<td>PRBS13Q_Middle.txt</td>
<td>PRBS13Q_Lower.txt</td>
</tr>
<tr>
<td>GrayPRBS13Q</td>
<td>GrayPRBS13Q_TX1.txt</td>
<td>GrayPRBS13Q_TX2.txt</td>
<td>GrayPRBS13Q_Upper.txt</td>
<td>GrayPRBS13Q_Middle.txt</td>
<td>GrayPRBS13Q_Lower.txt</td>
</tr>
<tr>
<td>PRQS10</td>
<td>PRQS10_TX1.txt</td>
<td>PRQS10_TX2.txt</td>
<td>PRQS10_Upper.txt</td>
<td>PRQS10_Middle.txt</td>
<td>PRQS10_Lower.txt</td>
</tr>
<tr>
<td>SSPR</td>
<td>SSPR_TX1.txt</td>
<td>SSPR_TX2.txt</td>
<td>SSPR_Upper.txt</td>
<td>SSPR_Middle.txt</td>
<td>SSPR_Lower.txt</td>
</tr>
<tr>
<td>JP03B</td>
<td>JP03B.txt</td>
<td>JP03B.txt</td>
<td>JP03B.txt</td>
<td>JP03B.txt</td>
<td>JP03B.txt</td>
</tr>
<tr>
<td>Squarewave</td>
<td>Squarewave.txt</td>
<td>Squarewave.txt</td>
<td>Squarewave.txt</td>
<td>Squarewave.txt</td>
<td>Squarewave.txt</td>
</tr>
</tbody>
</table>
PAM Features (3) PAM4 BER Measurement

- PAM4 BER measurement with high input sensitivity ED
  - Two ways of BER measurement
    - Sequential PAM4 respective sub eyes BER measurement with single ED
    - Parallel PAM4 sub eyes BER measurement with 3 EDs.
    - Auto Search function for each PAM4 sub eyes
PAM Features (4) PAM4 Analysis functions

- **Analysis functions**
  - PAM4 sub eyes analysis for Top, Middle, and Bottom respectively.
  - Auto-measurement functions are:
    - Eye Contour
    - Eye Margin
    - Bathtub
    - Q Analysis
PAM Features (5) Typical waveforms

Conditions
Input: 3.5 Vp-p, 1.75 Vp-p, PRBS31
Output: 832 mVp-p, 170 mV/div, 10.0 ps/div

25.78125 Gbaud Rate

28.1 Gbaud Rate
# 28G/32G PPG Specifications

<table>
<thead>
<tr>
<th>Item</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Operating Bit Rate</strong></td>
<td>2.4 to 28.1 Gbit/s</td>
</tr>
<tr>
<td></td>
<td>2.4 to 32.1 Gbit/s (Option)</td>
</tr>
<tr>
<td><strong>Data Output</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Number of Outputs</strong></td>
<td>MU183020A</td>
</tr>
<tr>
<td></td>
<td>1ch 2 ports (Data/xData) (Option)</td>
</tr>
<tr>
<td></td>
<td>2ch 4 ports (Data1/xData1, Data2/xData2) (Option)</td>
</tr>
<tr>
<td></td>
<td>MU183021A</td>
</tr>
<tr>
<td></td>
<td>4ch 8 ports (Data1/xData1, Data2/xData2, Data3/xData3, Data4/xData4)</td>
</tr>
<tr>
<td><strong>Amplitude</strong></td>
<td>500 mV to 2.0 Vp-p/2 mV step (Option)</td>
</tr>
<tr>
<td></td>
<td>500 mV to 3.5 Vp-p/2 mV step (Option)</td>
</tr>
<tr>
<td><strong>Offset</strong></td>
<td>-2.0 to +3.3 Voh/1 mV step</td>
</tr>
<tr>
<td><strong>Crosspoint Adjust</strong></td>
<td>20% to 80%/0.1% step @ 28 Gbit/s, 32 Gbit/s</td>
</tr>
<tr>
<td><strong>Clock Output</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Number of Outputs</strong></td>
<td>1</td>
</tr>
<tr>
<td><strong>Amplitude</strong></td>
<td>0.3 Vp-p min. 1.0 Vp-p max.</td>
</tr>
<tr>
<td><strong>Frequency</strong></td>
<td>Selectable clock of 1/1 or 1/2 of bit rate</td>
</tr>
<tr>
<td><strong>Data Delay</strong></td>
<td>Option</td>
</tr>
<tr>
<td><strong>Range</strong></td>
<td>-1000 to +1000 mUI/2 mUI step</td>
</tr>
<tr>
<td><strong>Pattern Generation</strong></td>
<td></td>
</tr>
<tr>
<td><strong>PRBS</strong></td>
<td>2^n-1 (n = 7, 9, 10, 11, 15, 20, 23, 31), Mark Ratio 1/2, Logic POS/NEG</td>
</tr>
<tr>
<td><strong>Programmable DATA</strong></td>
<td>2 to 268,435,456 bits/1 bit step, Mark Ratio 1/2, Logic POS/NEG</td>
</tr>
<tr>
<td><strong>Aux Outputs</strong></td>
<td>Divided Clock, Pattern Sync.</td>
</tr>
</tbody>
</table>
# 28G/32G ED Specifications (1/2)

<table>
<thead>
<tr>
<th>Item</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Bit Rate</td>
<td>2.4 to 28.1 Gbit/s, 2.4 to 32.1 Gbit/s (Option)</td>
</tr>
<tr>
<td>Data Input</td>
<td>MU183040A/B</td>
</tr>
<tr>
<td>Number of Inputs</td>
<td>1ch 2 ports (Data/xData) (Option)</td>
</tr>
<tr>
<td></td>
<td>2ch 4 ports (Data1/xData1, Data2/xData2) (Option)</td>
</tr>
<tr>
<td></td>
<td>MU183041A/B</td>
</tr>
<tr>
<td></td>
<td>4ch 8 ports (Data1/xData1, Data2/xData2, Data3/xData3, Data4/xData4)</td>
</tr>
<tr>
<td>Input Amplitude/Sensitivity*</td>
<td></td>
</tr>
<tr>
<td></td>
<td>MU183040B/MU183041B</td>
</tr>
<tr>
<td>Input Amplitude*</td>
<td>0.05 Vp-p to 1.0 Vp-p</td>
</tr>
<tr>
<td>Sensitivity*</td>
<td>EYE Amplitude</td>
</tr>
<tr>
<td></td>
<td>15 mVp-p (typ.), ≤25 mVp-p</td>
</tr>
<tr>
<td></td>
<td>EYE Height</td>
</tr>
<tr>
<td></td>
<td>10 mVp-p (typ.)</td>
</tr>
<tr>
<td>Clock Input</td>
<td>MU183040B/MU183041B</td>
</tr>
<tr>
<td>Number of Inputs</td>
<td>1</td>
</tr>
<tr>
<td>Amplitude</td>
<td>0.3 Vp-p min., 1.0 Vp-p max.</td>
</tr>
<tr>
<td>Frequency</td>
<td>1/2 of bit rate</td>
</tr>
<tr>
<td>Clock Delay</td>
<td>−1000 to +1000 mUI/2 mUI step</td>
</tr>
<tr>
<td>Pattern Detection</td>
<td>2^n-1 ( n = 7, 9, 10, 11, 15, 20, 23, 31) , Mark Ratio 1/2, Logic POS/NEG</td>
</tr>
<tr>
<td>Programmable DATA</td>
<td>2 to 268,435,456 bits/1 bit step, Mark Ratio 1/2, Logic POS/NEG</td>
</tr>
<tr>
<td>Aux Outputs</td>
<td>Divided clock, Pattern Sync.</td>
</tr>
<tr>
<td>Analysis Functions</td>
<td>Auto Search, Auto Adjust, Bathtub Jitter, EYE Diagram, EYE Margin, Auto Search PAM Mode, Q-value measurement, Eye Contour, PAM BER Measurement</td>
</tr>
</tbody>
</table>

* Input amplitude is a range where Auto Adjust function operates. Input sensitivity is the minimum input amplitude which becomes error free.
# 28G/32G ED Specifications (2/2)

<table>
<thead>
<tr>
<th>ITEM</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock Recovery Options</td>
<td>Clock Recovery from ch1 Data input, internal distribution to each channel*¹</td>
</tr>
<tr>
<td>Operating Bit Rate</td>
<td>Opt-x22: 2.4 to 28.1 Gbit/s</td>
</tr>
<tr>
<td></td>
<td>Opt-x23: 25.5 to 32.1 Gbit/s (requires MU183040B/41B-001)</td>
</tr>
<tr>
<td>Maximum Number of Consecutive Zeros</td>
<td>72 bits (Zero Substitution 2¹⁵)</td>
</tr>
<tr>
<td>Lock Range for Data Clock Recovery</td>
<td>Opt-x22: ±200 ppm</td>
</tr>
<tr>
<td></td>
<td>Opt-x23: ±100 ppm</td>
</tr>
<tr>
<td>Target Loop Band</td>
<td>Opt-x22: Selectable from bit rate/1667, bit rate/2578, Jitter Tolerance*², and variable</td>
</tr>
<tr>
<td></td>
<td>Variable: 3 MHz to 17 MHz/1 MHz steps*³</td>
</tr>
<tr>
<td></td>
<td>Opt-x23: Selectable from bit rate/1667, bit rate/2578 and Jitter Tolerance*²</td>
</tr>
</tbody>
</table>

*1: MU183041B-023 recovers Clock from ch1 Data input and distributes to ch1 and ch2. Also recovers Clock from ch3 Data input and distributes to ch3 and ch4.

*2: Jitter Tolerance setting makes widest loop band and enables Jitter Tolerance measurement.

*3: Upper setting band depends on bit rate: 17 MHz at 28.1 Gbit/s
Main Applications (Interconnects) (1/2)

• **28G Ultra high speed Interconnect evaluation**

  - Jitter Tolerance Testing
  - Compensate for PCB trace losses
  - Crosstalk effect testing
  - Dual tone SJ/RJ/BUJ/SSC Jitter Tolerance
  - Measuring small amplitude with high-sensitivity ED SERDES measurement with clock recovery
  - Emphasis generation
  - Timing control and skew control between channels
Main Applications (Interconnects) (2/2)

- **Infiniband FDR(14G) / EDR(26G) AOC Evaluation**

- **8ch (4ch end-to-end) BER** → 8ch simultaneous testing
  Measuring small swing signal with high-sensitivity ED

- **Crosstalk effect test** → Timing control and skew control between channels

- **Jitter Tolerance test for CDR** → SJ/RJ/BUJ/SSC Jitter Tolerance

- **Output waveform test** → TJ/DJ/RJ/Bathtub Jitter,
  EYE Contour (BER contour mask) analysis
Main Applications (CFP2/CFP4)

- **CFP2/CFP4 Evaluation**

  - Crosstalk effect test
  - 25 x 4λ BER
  - EAM Direct drive
  - Jitter Tolerance test for CDR

  ➔ Timing control and skew control between channels
  ➔ All-in-one 4ch simultaneous testing
  ➔ Measuring small swing signal with high-sensitivity ED
  ➔ 3.5 Vp-p Data out, variable Crosspoint
  ➔ SJ Jitter Tolerance (MU181000 with jitter option can generate SJ)

Dual-tone-SJ/RJ/BUJ/SSC are available with using MU181500B Jitter Modulation Unit.
Main Applications (DP-QPSK, DQPSK)

- **32G DP-QPSK Evaluation**
  - Pre-coding signal generation
  - Optical output waveform optimization
  - Timing control between channels
  - Modulator input level tolerance
  → Synchronized DP-QPSK, DQPSK signal
  → Crosspoint adjustment
  → Precision data delay
  → 3.5 Vp-p Data out, variable Amplitude

- **DQPSK Evaluation**
Multi-channel SQA Solution

56G / 64G Solution
Module Lineup

MP1861A
56G/64G bit/s MUX

MP1862A
56G/64G bit/s DEMUX

J1646A
Passive Equalizer 6dB (V connector)

Standard Configurations

MP1800A Max. 6 slot

56G/64G Jitter BERT
- 32G PPG 2ch
- 32G ED 2ch
- Synthesizer (2 Slots)
- Jitter Generator (2 Slots)
- 64G MUX
- 64G DEMUX

MP1861A
MP1862A

56G/64G 2ch BERT
- 32G PPG 4ch or 32G PPG 2ch x 2
- 32G ED 4ch or 32G ED 2ch x 2
- 4Port Synthesizer (2 Slots)
- 64G MUX
- 64G DEMUX

56G/64G 4ch BERT (2 box)
- 32G PPG 4ch or 32G PPG 2ch x 2
- 32G ED 4ch or 32G ED 2ch x 2
- 4Port Synthesizer (2 Slots)
- 64G MUX
- 64G DEMUX
Features (1) Waveform Quality

- Low-Jitter, High-quality Waveform MUX

50 Gbit/s, 3.5 Vp-p Output Waveform (MP1861A-013)
Features (2) Rx Sensitivity and Equalizer

- **High-sensitivity DEMUX**
  - Sensitivity: 25 mV (typ.) (56.2 Gbit/s, single-end, EYE Height, PRBS31)
  - ≤40 mV (56.2 Gbit/s, single-end, EYE Height, PRBS31)
  - 30 mV (typ.) (64.2 Gbit/s, single-end, EYE Height, PRBS31)

- **Passive equalizer**
  - Put passive equalizer upstream of MP1862A 56/64G bit/s DEMUX
  - Compensate transmission path losses, recovery of EYE Opening then possible to measure BER and execute jitter tolerance

 ![Before](image1.png)

 ![After](image2.png)

 ![S21 dB vs Frequency](image3.png)

 **J1646A Passive Equalizer 6dB S21**
Features (3) Jitter generation and tolerance test

- Full jitter components generation: Dual tone SJ, RJ, BUJ, SSC, Half Period Jitter
- Automatic jitter tolerance measurements
  - SJ up to 2000 UI or 0.55 UI high-frequency SJ at 250 MHz (at 56.2Gbps).
  - Low intrinsic jitter: 275 fs rms. (typical).

![Generate Various types of jitters](image)

![MX181500A Jitter/Noise Tolerance Test Software](image)

![Jitter Generation Mask](image)

- Sine Wave Jitter (SJ)
- Random Jitter (RJ)
- Bounded Uncorrelated Jitter (BUJ)
- Half Period Jitter (Even/Odd Jitter)
Features (4) Synchronous operation

- **4ch Synchronization in one mainframe**
  - Ultra high speed synchronized data streams up to 4ch MP1861A 56G / 64G MUX by one MP1800A.

- **Crosstalk Tests**
  - Installing MUX Data Delay option offers independent phase control for each channel.
  - High accurate phase delay setting in 4mUI steps.
Features (5) Various analysis functions

**Bathtub Jitter Measurement**

**EYE Diagram Measurement**

**EYE Margin Measurement**
Features (6) Various data patterns

• **Burst Signal Tests**
  ✓ Supports application evaluation using burst signals, such as optical circulation loop test
  ✓ Burst disable time up to 1uS (Typical)

• **Max 512 Mbit/ch Programmable Data Pattern**
  ✓ Generates any pattern for applications, such as CJTPAT, CJPAT, K28.5

• **Pseudorandom Patterns (PRBS)**
  ✓ $2^{n-1}$ $(n = 7, 9, 10, 11, 15, 20, 23, 31)$

• **Zero Substitution Patterns**
  ✓ Suitable for clock recovery contiguous 1s and 0s tolerance testing

• **Mixed Patterns**
### 56G/64G bit/s MUX/DEMUX specifications

#### MP1861A 56G/64G bit/s MUX

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Bit Rate</strong></td>
<td>8 to 56.2 Gbit/s 8 to 64.2 Gbit/s (MP1861A-001)</td>
</tr>
<tr>
<td>No. of Channels</td>
<td>1ch, Up to 4ch parallel synchronization by connecting to MP1800A</td>
</tr>
<tr>
<td><strong>Amplitude</strong></td>
<td>0.5 to 2.5 Vp-p (≤56.2 Gbit/s, MP1861A-011)</td>
</tr>
<tr>
<td></td>
<td>1.0 to 2.5 Vp-p (&gt;56.2 Gbit/s, MP1861A-011)</td>
</tr>
<tr>
<td></td>
<td>0.5 to 3.5 Vp-p (≤56.2 Gbit/s, MP1861A-013)</td>
</tr>
<tr>
<td></td>
<td>1.0 to 3.5 Vp-p (&gt;56.2 Gbit/s, MP1861A-013)</td>
</tr>
<tr>
<td><strong>Intrinsic Random Jitter</strong></td>
<td>RJ = 200 fs rms (typ.)</td>
</tr>
<tr>
<td><strong>Half Period Jitter</strong></td>
<td>20 Steps</td>
</tr>
</tbody>
</table>

#### MP1862A 56G/64G bit/s DEMUX

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Bit Rate</strong></td>
<td>8 to 56.2 Gbit/s 8 to 64.2 Gbit/s (MP1861A-001)</td>
</tr>
<tr>
<td>No. of Channels</td>
<td>1ch, Up to 4ch parallel synchronization by connecting to MP1800A</td>
</tr>
<tr>
<td><strong>Amplitude</strong></td>
<td>0.125 to 1.0 Vp-p</td>
</tr>
<tr>
<td><strong>Sensitivity</strong></td>
<td>25 mV (typ.), ≤40 mV (EYE height, PRBS31, single-ended)</td>
</tr>
</tbody>
</table>
Main Applications (Interconnect)

- **56 Gbit/s Band High Speed Semiconductor Chip Measurements**

- **56 / 64 Gbit/s BER Measurements** ➔ For SERDES, Clock Data Recovery (CDR), etc.
- **Jitter Tolerance Tests** ➔ Supports dual tone SJ, RJ, BUJ, SSC, etc., Jitter Tolerance tests for CEI-56G
- **Input Sensitivity Tests** ➔ Wide variable amplitude range 0.5 to 3.5 Vpp (56G, with installed MP1861A-013 option)
- **Bathtub Jitter Measurements** ➔ TJ / RJ / DJ separation
Main Applications (Transmitter)

- **200 GbE, 56G × 4 lane evaluation**  ➔  Supports EML and optical module evaluations for 200G / 400GbE
- **EML evaluation**  ➔  Direct EML driving using variable output function up to 3.5 Vp-p
- **Confirming skew and crosstalk effects**  ➔  Pattern Sync and Variable Phase functions support easy verification of Rx device skew tolerance, crosstalk effects
- **Auto search functions**  ➔  Data and Clock phase auto alignment
Multi-channel SQA Solution

56G / 64GBaud PAM4 Solution
64Gbaud PAM4 DAC features

G0374A 64Gbaud PAM4 DAC
- Wide Operating Range: DC to 64 Gbaud
- Generates 64 Gbaud PAM4 signal using half rate 32 Gbit/s x 4 input signals
- 1.4 Vp-p (differential, Typ.) output
- Amplitude, duty and Upper / Lower / Middle amplitude ratio control by manual
- Low output Jitter performance of only 300 fs (rms)
- NRZ, PAM4 signal control and jitter addition
64Gbaud PAM4 generation block diagram

MP1800A
Signal Quality Analyzer

G0374A
64Gbaud PAM4 DAC

32Gbit/s Data1A,B(MSB)

32 GHz Clock input

32 Gbit/s Data0A,B(LSB)

DUT
or Scope

4ch 32G PPG
MU183020A 32G 2ch PPG x2
MU181000A/B Synthesizer

64 Gbaud PAM4
Data output
Typical waveform from 64Gbaud PAM4 DAC

- **PAM4 Output Waveforms** (41 V -6 ATT +3 4 V V50 Adapter + 70-GHz Band Oscilloscope)

<table>
<thead>
<tr>
<th>64 Gbaud</th>
<th>56 Gbaud</th>
<th>28 Gbaud</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1.png" alt="Waveform" /></td>
<td><img src="image2.png" alt="Waveform" /></td>
<td><img src="image3.png" alt="Waveform" /></td>
</tr>
</tbody>
</table>

- **NRZ Output Waveforms** (41 V -6 ATT +3 4 V V50 Adapter + 70-GHz Band Oscilloscope)

<table>
<thead>
<tr>
<th>64 Gbaud</th>
<th>56 Gbaud</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image4.png" alt="Waveform" /></td>
<td><img src="image5.png" alt="Waveform" /></td>
</tr>
</tbody>
</table>
Block diagram for jitter injection

G0374A 64Gbaud PAM4 DAC has jitter transparency. So jitter stress test is possible on top of PAM4 signal.

Recommended cables: Data Cables 80 cm (J1612A x4) Clock Cable 130 cm (J1611A)
56Gbaud PAM4 BER measurement

- Support 56Gbaud PAM4 BER measurement with PRBS15

MU183020A
32G 2ch PPG x2

MU181000B
Synthesizer

MP1800A
Signal Quality Analyzer

MU183040B
32G 2ch ED

28 GHz Clock

28 Gbit/s Data1A,B(MSB)

G0374A
64Gbaud PAM4 DAC

64 Gbaud PAM4

28 Gbit/s Data0A,B(LSB)

MP1862A
64G DEMUX

MP1862A measures 3 sub eyes BER respectively.
Multi-channel SQA Solution

High Speed Serial Bus Solution
- Thunderbolt Gen3
- USB3.1 Gen1 / Gen2
- PCIe Gen4
Agenda

1. TBT solution
2. USB solution
3. PCIe solution
Thunderbolt Overview

**What is Thunderbolt (TBT)?**
- 10.3125 Gbps for Gen1 & Gen2, 2 x 20.625 Gbps for Gen3.
- Integrated multiple applications through ALT mode (TBT, USB, DP).
- Power delivery up to 100 W

**Anritsu Solution**
- MP1800A SQA is the first authorized BERT by Intel.
- MS46322A VNA is also authorized by Intel.
- Anritsu collaborate with GRL (Granite River Labs Inc.) to provide automated solution.
- GRL is one of the authorized test house for TBT by Intel.
  GRL: HQ in Santa Clara US.
- High repeatability one button calibration and Rx test based on Thunderbolt CTS (Compliance Test Specification).
2.2.3 Pattern Generator
Generate Thunderbolt signal with a variety of patterns, clock jitter, data waveform (eye diagram) and amplitude characteristics.

**Required Test Equipment Capabilities**
- Data rates ≥ 20.625 Gbps
- Data patterns: PRBS15, PRBS31, Square wave
- Differential swing range: 0 – 2Vp-p in 10mV steps
- Rise Time ≥ 10 ps (20%-80%)
- Intrinsic jitter < 400 fs RMS

**Recommended Test Equipment #1**
- Anritsu MP1800A
  - MP1800A Signal Quality Analyzer
  - MP1800A-002 Ethernet
  - MP1800A-007 OS Upgrade to Windows7
  - MP1800A-014 2-Slot for PPG and/or ED
  - MP1800A-032 32Gbit/s PPG and/or ED support
  - MU181000A 12.5GHz Synthesizer
  - MU181000A-001 Jitter modulation
  - MU181500B Jitter Modulation Source
  - MU183020A 28G/32G bit/s PPG
  - MU183020A-012 1ch 2V Data Output
  - MU183020A-030 1ch Data Delay
  - MP1825B 4Tap Emphasis
  - MP1825B-002 28Gbit/s operation
  - J1551A Coaxial Skew match cable (0.8m, K connector)
  - J1439A Coaxial Cable 0.8m, K connector
  - J1611A Coaxial Cable 1.3m, K connector

2.2.4 Network Analyzer
**Required Test Equipment Capabilities**
- 2 ports used simultaneously
- At least 1MHz – 13GHz bandwidth
- Dynamic range > 50db

**Recommended Test Equipment #3**
- Anritsu MS46322A VNA
- Option: MS46322A-020
Thunderbolt Receiver tolerance test setup

**Case 1 (TP2):**
- **Host/Device RX (DUT)**
- **TBT Plug**
- **Emphasis**
- **PPG**
- **Crosstalk source**
- **SJ**, **RJ**, **SSC**

**Case 2 (TP3EQ):**
- **Host/Device RX (DUT)**
- **Cable (2m) -12dB@5GHz**
- **TBT Plug**
- **PCB -3.5dB@5GHz**
- **Emphasis**
- **PPG**
- **Crosstalk source**
- **SJ**, **RJ**, **SSC**

- **CM injection**
Thunderbolt Receiver tolerance calibration setup

Test case 1 (TP2)
Thunderbolt Receiver tolerance calibration setup

Test case 2 (TP3EQ)
Thunderbolt calibration procedure (1/2)

1. Set inner eye amplitude (700 mVpp differential)

2. Find minimum DDJ from 16 presets for emphasis

3. CM noise phase adjustment
Thunderbolt calibration procedure (2/2)

4. CM noise
   During CM calibration, MP1825B output set to off. After calibrated CM, CM should be turn off.

5. RJ calibration
   Only RJ set to on during RJ calibration.

6. SJ calibration
   Calibrate at 5 different SJ frequencies
   Only SJ set to on during SJ calibration.

7. TJ calibration
   Set calibrated CM, RJ and SJ value on.
   Final value should be adjusted by RJ value.
   Adjusted TJ values should be saved respectively.
TBT3 Rx test configuration at TP3EQ

- **Control PC**: Including Alpine Ridge Host
  - Type-C Cable
- **DUT**: Alpine Ridge DP Device
- **Type-C Cable**
  - 10G: 1.8 m
  - 20G: 0.5 m

**Components**:
- **MG3740A**
- **MP1800A 32G PPG**
- **Jittered Data**
- **MP1825B 4tap emphasis**
- **K241C**
- **J1510A**
- **K261**
- **Skew Matched Pair Cables**
- **Receptacle Fixture**
- **K-SMP Adapter**
- **Data**
- **xData**

**Signals**:
- **Aggressor 1/8 Clock**
  - 800 mVp-p, Diff.
Thunderbolt automated test solution by GRL

Test point settings

Calibration & Test item

Target values for each settings
Agenda

1. TBT solution
2. USB solution
3. PCIe solution
USB 3.1 Gen1 & Gen2 Solution

What is USB3.1?
- New connector: Type C
- Two speed (Gen1: 5Gbps, Gen2: 10Gbps)
- Part of Intel TBT chip (Alpine Ridge)

Anritsu solution
- Link Generation (MX183000A)
- Automated calibration and JTOL (GRL)
- USB Adaptor with BER measurement function

Features ➔
Simple, easy Go / No Go test
Support USB3.1 Gen1 & Gen2 Host / Device receiver test
Full automatic calibration and test in loopback mode
Receiver test with compliance test pattern
Test procedure

1. Calibrating stressed waveform by GRL software

2. Setting DUT in loopback mode by MX183000A software

   LFPS (Low Frequency Periodic Signaling)
   Low Freq (10M-20Mbps) communication between USB devices.
   Change USB internal state (LTSSM) to loopback

   For Rx tolerance test, DUT must be in loopback state.
   MX183000A can control state transition automatically.

3. BER measurement by external USB adaptor
USB 3.1 Gen1&Gen2 loop back link generation

MX183000A

![USB 3.1 Gen1&Gen2 loop back link generation](image)
USB 3.1 Gen1&Gen2 Calibration software (GRL)
USB compliance test block diagram

MP1800A, MX183000A
MU183020A 32G PPG

Data out +
Clock out
AUX out+
Gating out
(for LPFS detection)
AUX in

J1615A
(Pair Cable
0.8m for Data,
1.3m for clock)

J1343A(1.0m)

J1343A(1.0m)

J1343A(1.0m)

J1349A(0.3m)

J1349A(0.3m)

Ethernet

Data In
Clock In

Dataout +
Dataout -

MP1825B Emphasis

ARTEK USB TEST ADAPTOR

LFPS TX+
LFPS TX-

AUX

GATING

LFPS RX

LFPS RX+
LFPS RX-

Analyzing
BER

J1510A
Pick OFF Tee

J1551A
(0.8m Phase
matched Pair)

J1551A
(0.8m Phase
matched Pair)

Test Fixture
for DUT

J1551A
(0.8m Phase
matched Pair)

J1551A
(0.8m Phase
matched Pair)
Test points

Gen2 Test points
Confirm error free at 1E-10 (Tentative)
SJ: 17 ps +/- 10% at 50 MHz
   17 ps +/- 10% at 7.5 MHz
   37 ps +/- 10% at 4.0 MHz
   87 ps +/- 5% at 2.0 MHz
   203 ps +/- 5% at 1.0 MHz
   476 ps +/- 5% at 500 MHz

Gen1 Test points
Confirm error free at 1E-10
SJ: 40 ps +/- 10% at 33 MHz
   40 ps +/- 10% at 20 MHz
   40 ps +/- 10% at 10 MHz
   40 ps +/- 10% at 4.9 MHz
   100 ps +/- 5% at 2.0 MHz
   200 ps +/- 5% at 1.0 MHz
   400 ps +/- 5% at 500 kHz

MX183000A
- BER measurement
- Pass / Fail display
Agenda

1. TBT solution
2. USB solution
3. PCIe solution
PCI Express Solution

Anritsu target market for PCIe
- Multi application interface high speed semiconductor
  PCIe + 100GbE,
  PCIe + Thunderbolt,
  PCIe + Thunderbolt + USB3.1

Anritsu solution
- Based on PCIe Gen4 Base specification revision 0.5
- Link capability (MX183000A) and Automated Cal & JTOL (GRL)
Different PCIe architecture

Case 1: Common Clock Architecture

Case 2: Data Clocked Architecture

Case 3: Separate Ref Clock Architecture
Two improvements will be implemented (1/2)

**SKP ordered set**

- Different frequency clock between two PCIe devices

![Diagram of different clock architectures between two PCIe devices]

- PCIe TX generates SKP ordered set randomly / automatically

Also in loopback mode, TX generates SKP into transmitting data. → ED incoming data is different from PPG transmitted data

→ Future Anritsu solution will support “SKP ordered set”.
Two improvements will be implemented (2/2)

SSC (Spread Spectrum Clocking)

SSC: Change carrier frequency slowly to save EMI
PCIe: 5000 ppm, 33 kHz, Triangle waveform

Future Anritsu solution will support SSC data Error Detection
Current Anritsu PCIe Solution

![Diagram showing Common Clock Architecture with PCIe Device A and Device B connected through Ref clock]

Anritsu+GRL-PCIE4-BASE-RXA Key Features

**Totally Automated** PCIe 4.0 Rx Base Spec Test using Anritsu equipment
- Perform Receiver Jitter Tolerance test at the push of a button
- Reduce technical risk using an industry-accepted calibration methodology
- Achieve consistent results with rapid test execution
PCle Gen4 Calibration points

![Diagram of PCle Gen4 Calibration points]

Table 9-8: Stressed Jitter Eye Parameters

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>2.5 GT/s</th>
<th>5.0 GT/s</th>
<th>8.0 GT/s</th>
<th>16.0 GT/s</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{RX-LAUNCH}$</td>
<td>Generator launch voltage</td>
<td>800-1200</td>
<td>800-1200</td>
<td>800-1200</td>
<td>800-1200</td>
<td>mV PP</td>
</tr>
<tr>
<td>$T_{RX-U1}$</td>
<td>Unit Interval</td>
<td>400</td>
<td>200</td>
<td>125</td>
<td>62.5</td>
<td>ps</td>
</tr>
<tr>
<td>$T_{RX-ST}$</td>
<td>Eye width at TP2P</td>
<td>&lt;0.4</td>
<td>&lt;0.32</td>
<td>0.30</td>
<td>0.30</td>
<td>UI</td>
</tr>
<tr>
<td>$T_{RX-ST-SJ}$</td>
<td>Swept Sj</td>
<td>33 kHz</td>
<td>33 kHz</td>
<td>Figure 9-29, Figure 9-30</td>
<td>Figure 9-29, Figure 9-30</td>
<td>UI PP</td>
</tr>
<tr>
<td>$T_{RX-ST-RJ}$</td>
<td>Random Jitter</td>
<td>TBD</td>
<td>TBD</td>
<td>3.0 (max)</td>
<td>~1.0 (max)</td>
<td>ps RMS</td>
</tr>
<tr>
<td>$V_{RX-DIFF-INT}$</td>
<td>Differential noise</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>mV PP</td>
</tr>
<tr>
<td>$V_{RX-CM-INT}$</td>
<td>Common mode noise</td>
<td>150</td>
<td>150</td>
<td>150</td>
<td>150</td>
<td>mV PP</td>
</tr>
</tbody>
</table>

Post Processing Scripts:
- Rx pkg model
- Behavioral CTLE/DFE
- Behavioral CDR

15 mV / .3 UI at E-12 BER
PCIe base spec calibration test setup for TP1

Real time scope
PCIe base spec calibration test setup for TP2

Real time scope
PCIe Gen4 Base spec calibration procedure

1. Emphasis eye amplitude calibration
2. De-emphasis and Pre-shoot calibration
3. RJ, SJ calibration
4. ISI loss calibration
5. CMI, DMI calibration
6. Stressed eye calibration
PCIe base spec receiver tolerance test setup
PCIe Gen4 base spec automated solution (GRL)

Test List (Calibration) for PCIe Gen4 including Upstream and Downstream for All TP2 channel type (Short, Medium, Long) calibration
PCIe Gen4 base spec automated solution (GRL)

1) Select Rx Test

2) Run Tests (Go / No Go at test points)

3) Generate Report
PCIe Gen1 to 4 loop back link generation (Anritsu)

MX183000A

- Sets DUT in loop back mode
- PCIe Gen 1 to Gen4
- Jitter tolerance “margin” test
Anritsu PCIe Solution operation procedure

1. Calibrate waveform by GRL SW

2. Set DUT in loop back mode

3. Jitter tolerance test for two options:
   AAA) Anritsu margin test
   BBB) GRL Go / No Go test
Anritsu / GRL PCIe Solution features

GRL-PCIE4-BASE-RXA Key Features
Automate PCIe 4.0 Rx Base Spec Test using Anritsu equipment
Perform Receiver Jitter Tolerance test at the push of a button
Reduce technical risk using an industry-accepted calibration methodology
Achieve consistent results with rapid test execution

MX183000A Key Features
Establish loop back mode for PCIe Gen1 to Gen4
Jitter tolerance margin test
Supporting also USB3.1 Gen1 (5Gbps) & Gen2 (10Gbps)

Application Specifications
• Data Rates: 16 GT/s
• Supported Receiver Test: Common Clock Architecture without SSC
• This application is compatible with:
  – Keysight 32 GHz Oscilloscope (DSAX or newer series)
  – Anritsu MP1800A Signal Quality Analyzer
  – Artek CLE-1000 A2 Variable ISI Channel
Appendix
History of Anritsu BERTS

1977 - 1999

- 2 Gbit/s/1977
- 3 Gbit/s/1990
- 10 Gbit/s/1990
- 12.5 Gbit/s/1994
- 12.5 Gbit/s x 4ch PPG/1995
- 3.2 Gbit/s/1998
- 1600+ Sales

2000 - 2005

- 12.5 Gbit/s x 4ch/2001
- 12.5 Gbit/s x 4ch PPG/1995
- MP1800A Flexible architecture
- MP2100B BERTWave 10 Gbit/s BERT&Scope

2005 - 2010

- 56 Gbit/s MUX/DEMUX
- Small Remote BOX
- Bit Rate Extension
- Multichannel Bit Rate Extension
- Built-in Scope

Today to future

- Broadband
- Jitter Analysis

>43.5 Gbit/s

≤43.5 Gbit/s

≤12.5 Gbit/s

≤3.2 Gbit/s

43.5 Gbit/s BERT System

43.5 Gbit/s MUX/DEMUX

Keep evolving!
Signal Quality Analyzer
MP1800A Series

**Solution:**
- 10/25/32/64 Gbit/s device tests

**Features:**
- Easy support for latest applications by adding functions matching customers’ TTM due to flexible/scalable modular architecture
- Unique Jitter and Emphasis functions, high sensitivity, built-in Clock Recovery, and PAM signal generation for 32G applications

BERTWave
MP2100B Series

**Solution:**
- 10 Gbit/s BER tests, EYE Pattern measurements

**Features:**
- All-in-one solution supporting BERT and Scope
- BERT expansion up to 4 channels
- Fast remote control and high-speed Eye Mask tests
- Compact design (180 mm deep)