Anritsu envision:ensure

Product Introduction

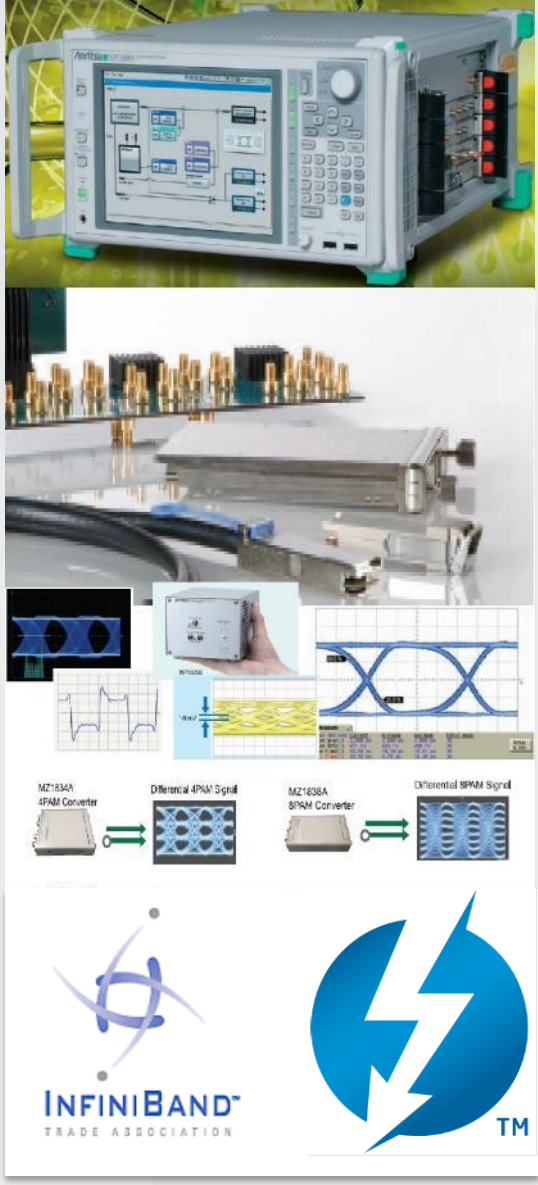
Multi-channel high speed solution

Signal Quality Analyzer
MP1800A Series

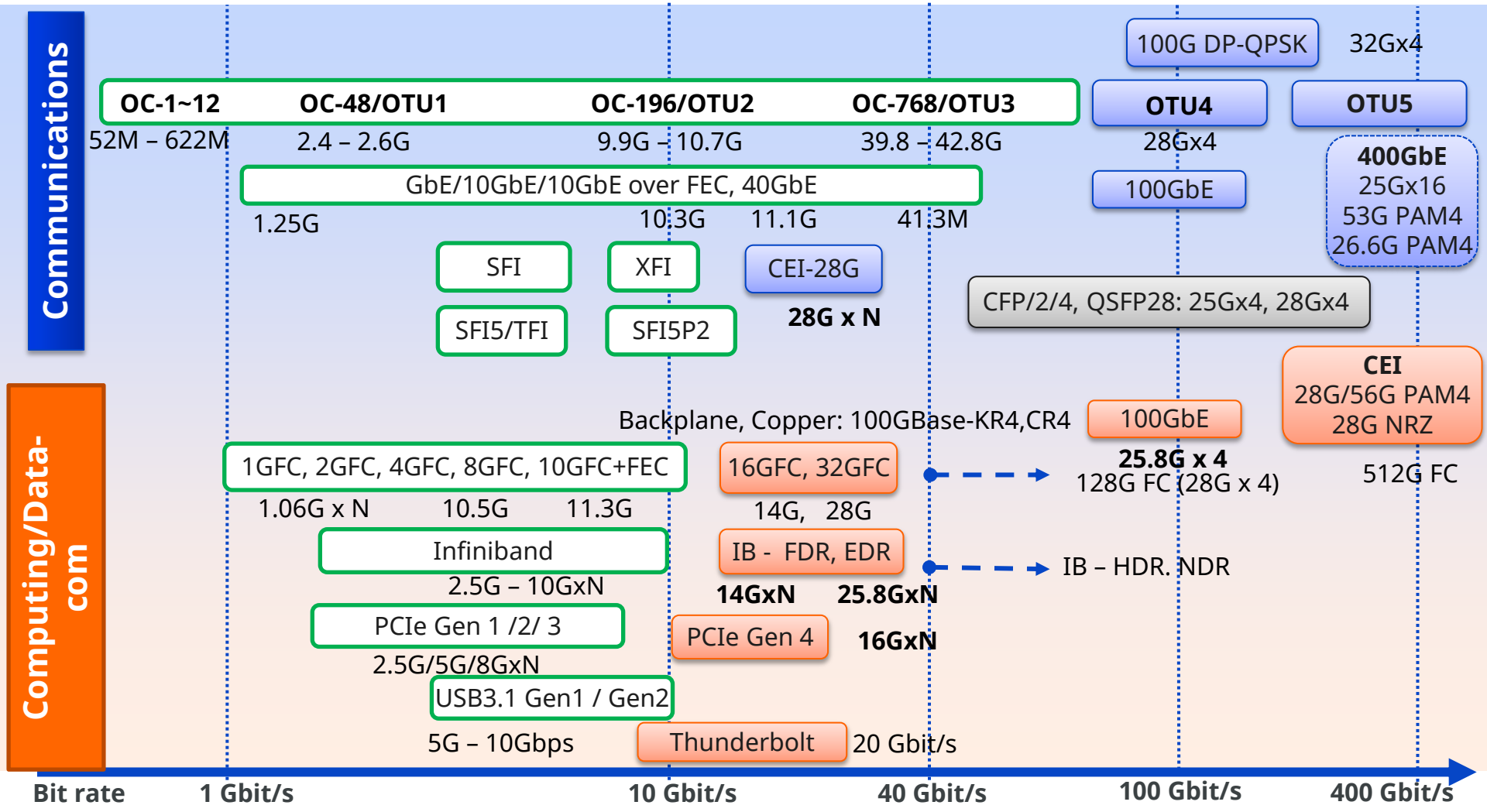
32G Solutions (NRZ / PAM4)
64G Solutions (NRZ / PAM4)
High speed serial bus solutions

Multi-channel SQA Solution

Product Overview



Technology trends



- **Multichannel 20 to 30 Gbit/s is key technology for high-end computers, servers, and 100G / 400G network communications.**
- **28 GBaud PAM4 is major technology for 100G / 400G communications.**
  53G NZR / 53GBaud PAM4 development has started toward the realization of 400 GbE.

NRZ / PAM4 standards

- 25G / 50G / 200GbE / 400GbE standardization are on going.
- PAM4 becomes major technology for various standards.
- Most of PAM4 actual baud-rate is 26.6G.
- To assure PAM4 signal Integrity, PAM4 BER measurement is key factors.

Optical Interface

Standard		Distance	Format	Baud-rate
400G	400G BASE-SR16	100m	NRZ	26.6G
	400G BASE-DR4	**500m**	**PAM4**	**53.1G**
	400G BASE-FR8	**2km**	**PAM4**	**26.6G**
	400G BASE-LR8	**10km**	**PAM4**	**26.6G**
200G	200G BASE-SR8*	100m*	NRZ	26.6G
	200G BASE-SR4*	**100m***	**PAM4**	**26.6G**
	200G BASE-FR4*	**2km***	**PAM4**	**26.6G**
	200G BASE-LR4*	**10km***	**PAM4**	**26.6G**
100G	100G BASE-SR10	100m/150m	NRZ	10.3G
	100G BASE-SR2*	**100m***	**PAM4**	**26.6G**
	100G BASE-SR4	70/100m	NRZ	25.8G
	100G SWDM	400m	NRZ	25.8G
	100G PSM4	500m	NRZ	25.8G
	CWDM4/CLR4	2km	NRZ	25.8G
	100G BASE-LR4	10km	NRZ	25.8G
	100G BASE-ER4	40km	NRZ	25.8G
	100G BASE-CR4		NRZ	25.8G
	100G BASE-KR4		NRZ	25.8G
	100G BASE-KP4		**PAM4**	**13.6G**
50G	**50G BASE-SR***	**100m**	**PAM4**	**26.6G**
	50G BASE-FR*	**2km**	**PAM4**	**26.6G**
	50G BASE-LR	**10km**	**PAM4**	**26.6G**
25G	25G BASE-SR	100m	NRZ	25.8G
	25G BASE-FR	2km	NRZ	25.8G
	25G BASE-LR	10km	NRZ	25.8G

Electrical Interface

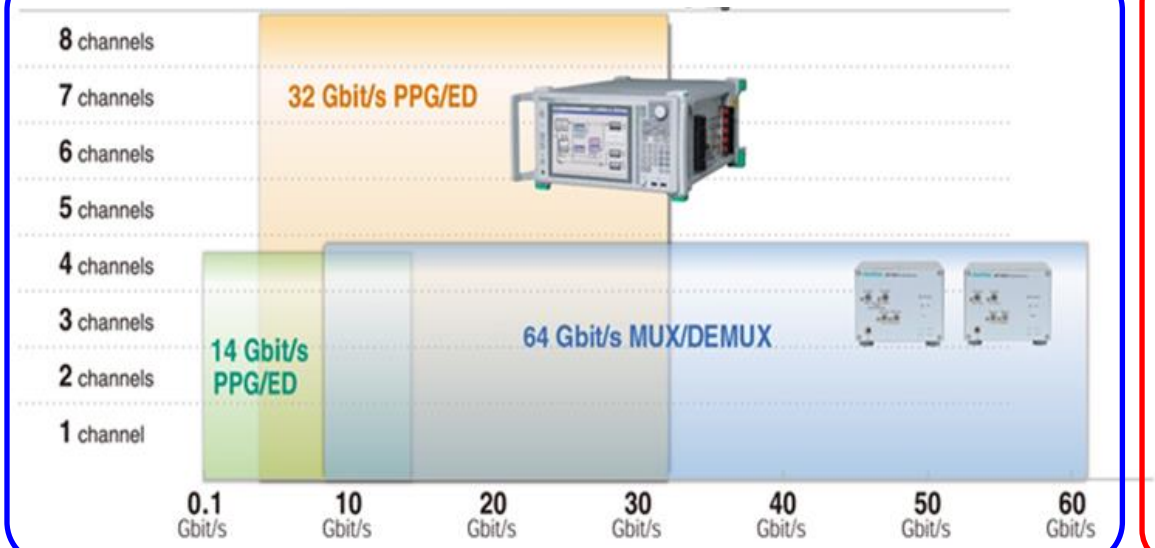
Electrical Interface (OIF-CEI)		Format	Baud-rate
400G	CDAUI-16	NRZ	25.8G
	CDAUI-8	**PAM4**	**26.6G**
200G	CCAUI-8	NRZ	25.8G
	CCAUI-4	**PAM4**	**26.6G**
100G	CAUI-10	NRZ	10.3G
	CAUI-4	NRZ	25.8G
50G	**50GAUI**	**PAM4**	**26.6G**
25G	25GAUI	NRZ	25.8G

***: Under discussion**

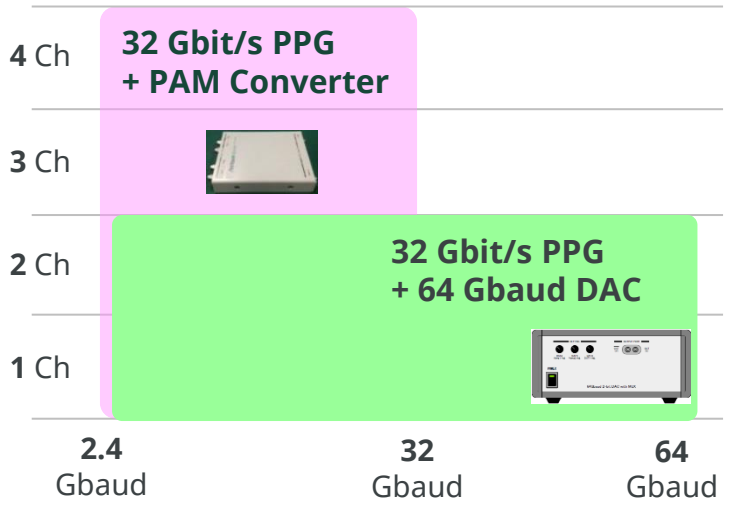
Feature of Anritsu high speed PAM4 / NRZ solutions

- Flexible upgradability: Singe channel to Multi channels, PAM4 (Up to 64Gbit/s)
- High quality waveform: Low intrinsic jitter (300 fs @ 28.1Gbps with clock pattern).
- High input sensitivity: 56G/64G DEMUX MP1862A (Typ.25 mV@56.2 Gbps)
  28G/32G ED MU18304xB (Typ.10 mV@28.1 Gbps)
- Jitter transparent NRZ / PAM4 solutions with various types of jitters

Multi-channel NRZ solutions



Multi-channel PAM4 solutions



Features of 32G All-in-One Jitter BERT

- ✓ Wideband bit rates from 2.4 to 32.1 Gbit/s
- ✓ 1 Tbit/s synchronous BERT : 8ch PPG in one box and 4 boxes synchronization
- ✓ High-input-sensitivity ED at 10 mV (typical, single-end, Eye Height)
- ✓ Integrated Clock Recovery option with complete jitter tolerance test
- ✓ PAM4 generation and BER measurement

Various Signal Integrity Analysis Functions

- TJ/DJ/RJ/J2/J9/Bathtub Jitter, Eye Diagram, Eye Margin auto-measurement
- Jitter Tolerance (with MX183000A)
  SJ = 1UI @ fm: 250 MHz
- 4Tap Emphasis with MP1825B
- Crosstalk testing with individual variable delay

Excellent Signal Quality and Rx Sensitivity

- Low intrinsic jitter: 300 fs
  Fast Tr / Tf : 12 ps
- Wide output amplitude range
  0.5 to 3.5 V p-p
- High input sensitivity: 10 mV
- PAM4 / PAM8 generation
  (MZ1834A/MZ1838A)
- PAM4 BER Measurement

Supports Data Patterns for Various Applications

- PAM4 PRBS, Gray code etc.
- Burst signal test
- 256 Mbits / ch max. user programmable pattern CJTPAT, CJPAT, K28.5 etc.
- Pre-coding, de-coding DQPSK, DP-QPSK

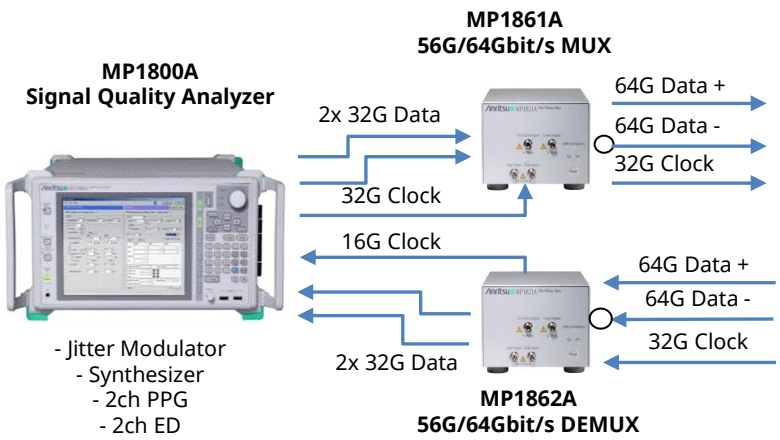
Features of 56G / 64G All-in-One jitter BERT

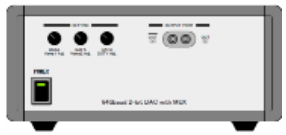
- **Low intrinsic Jitter: RJ = 200 fs rms（typical）**
- **Variable amplitude: 0.5 to 3.5 Vp-p**
- **Full jitter components generation RJ, BUJ, Dual tone SJ, SSC.**
  SJ generation 0.55 UI @ fm 250 MHz

- **High Input sensitivity: 25 mV (typical, single-end, EYE height)**
- **Bathtub Analysis as well as Eye Margin, Eye Diagram auto measurement**
- **Automatic jitter tolerance test with MX181500A software**

- **PAM4 signal generation up to 64GBaud with DAC Box (G0374A)**
- **56 Gbaud PAM4 BER measurement up to PRBS15**

- **56 Gbit/s signal EYE opening recovery by J1646A (6 dB passive equalizer)**



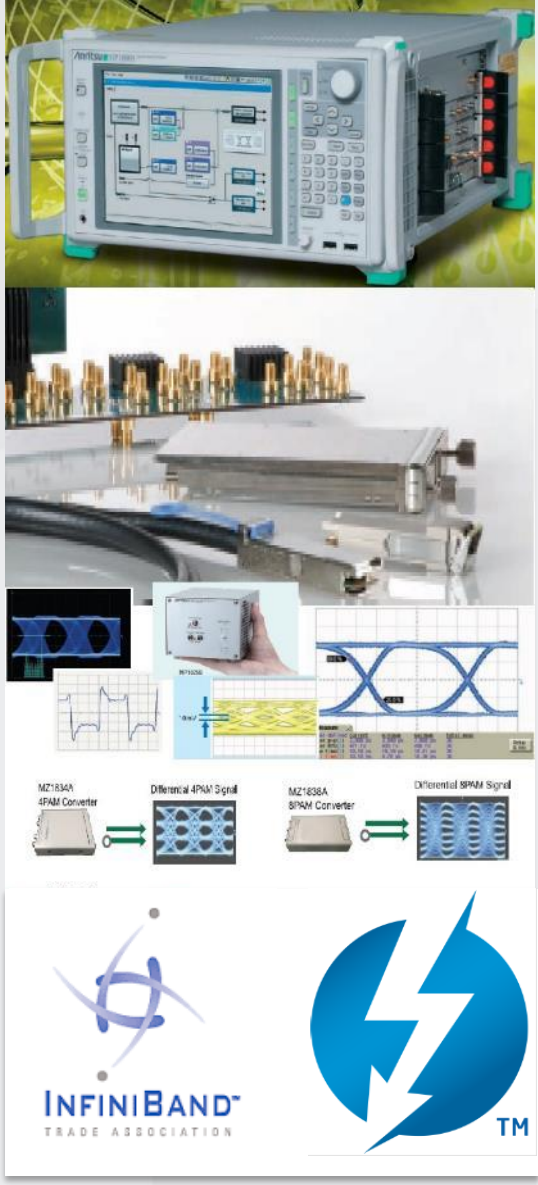


G0374A
64Gbaud PAM4 DAC

J1646A
Passive Equalizer
6 dB(V connector)

Multi-channel SQA Solution

28G / 32G Solution



Module Lineup

■ 28G/32G PPG/ED Module

MU183020A 28G/32G bit/s PPG (1ch or 2ch)

MU183040B 28G/32G bit/s High Sensitivity ED (1ch or 2ch)

MU183021A 28G/32G bit/s 4ch PPG

MU183041B 28G/32G bit/s High Sensitivity 4ch

■ 28G/32G BERT Typical Configurations

MP1800A

Max. 6 Slots

28G/32 G Jitter BERT

- 32G PPG 1ch or 2ch
- 32G ED 1ch or 2ch
- Synthesizer (2 Slots)
- Jitter Generator (2 Slots)

28G/32 G 4ch BERT

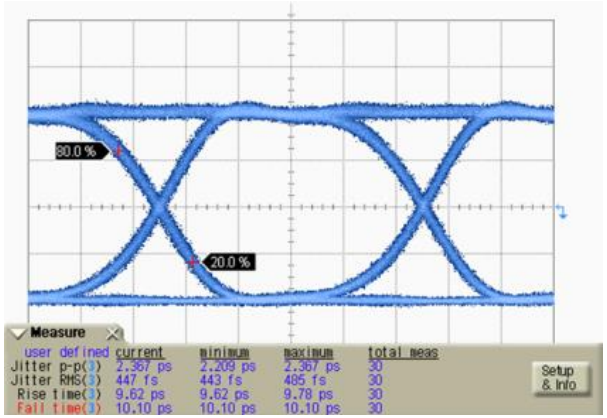
- 32G PPG 4ch (2 Slots)
- 32G ED 4ch (2 Slots)
- Synthesizer (2 Slots)

28G/32G 8ch Jitter BERT (2 Box)

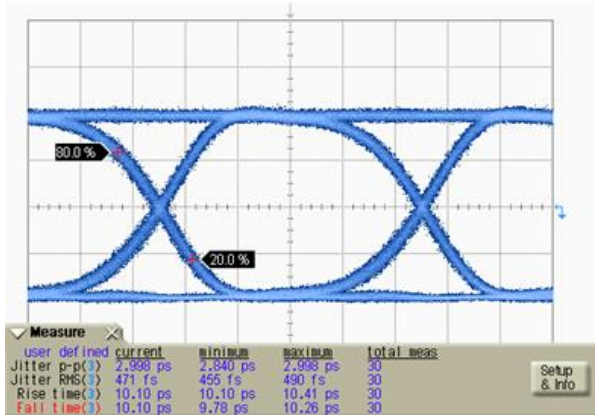
- 32G PPG 4ch (2 Slots)
- 32G ED 4ch (2 Slots)
- 32G PPG 4ch (2 Slots)
- 32G ED 4ch (2 Slots)
- Jitter (2 Slots)
- Synthesizer (2 Slots)

Features (1) Waveform Quality

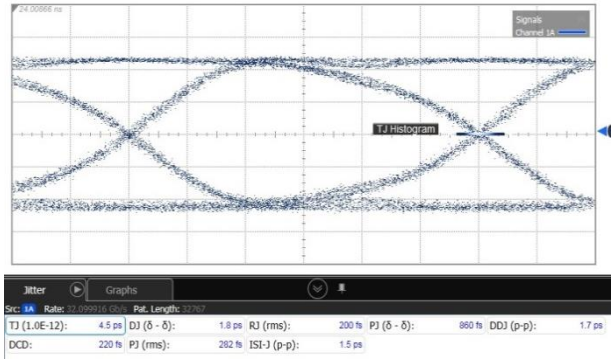
- **Low-Jitter, High-Quality Waveforms with Output ≤3.5 Vp-p**



Output waveform at 28 Gbit/s, 2.0 Vp-p (MU183020A-012)



Output waveform at 28 Gbit/s, 3.5 Vp-p (MU183020A-013)

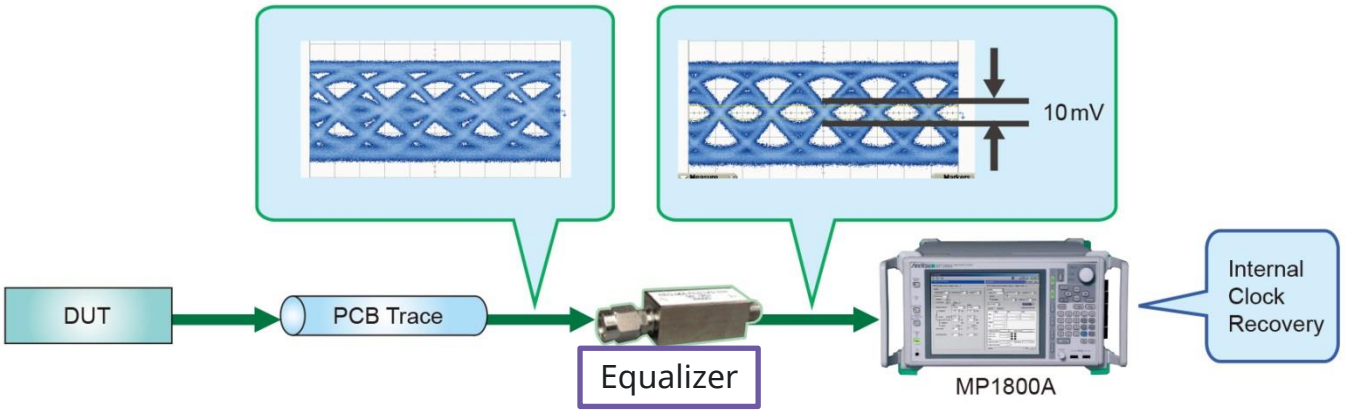


28 Gbit/s, PPG Intrinsic RJ rms

Using sampling oscilloscope with 50 GHz bandwidth and <100 fs rms intrinsic jitter

Features (2) Rx Input Sensitivity

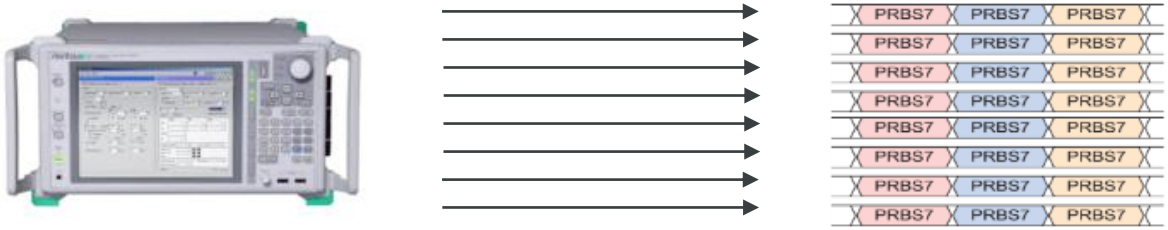
- **World's Best Input Sensitivity Error Detector (MU183040B/MU183041B)**
  - EYE amplitude sensitivity: 15 mVp-p (typ., 28.1 Gbit/s, single-end), ≤25 mVp-p (28.1 Gbit/s, single-end)
  - EYE Height sensitivity: 10 mVp-p (typ., 28.1 Gbit/s, single-end)
- **Passive Equalizer**
  - Insertion before ED recovers EYE opening by correcting transmission-path losses
  - Combination with MU183040B/MU183041B High Sensitivity ED supports Jitter Tolerance tests of physical devices with narrow Eye Opening
- **Jitter Tolerance Testing for Async SERDES by embedded Clock Recovery**
  - Loop bandwidth: Bit rate/1667, Bit rate/2578, 1 MHz to 17 MHz* ***Opt-022**
  - Supports clock recovery and high input sensitivity



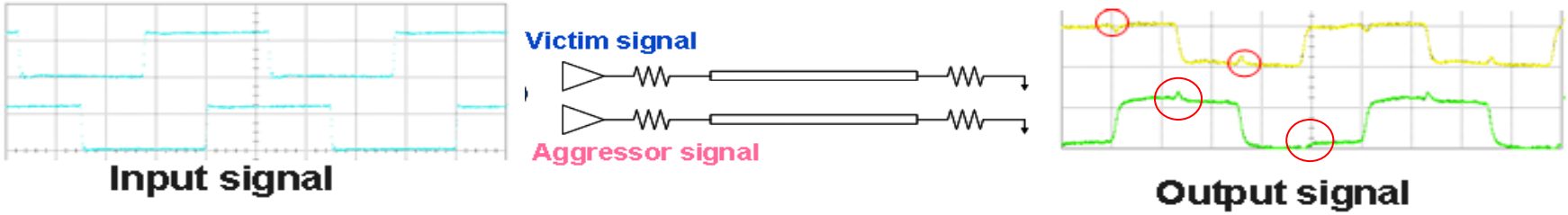
Features (3) Skew testing by synchronous PPGs

- **Individual Variable Data Skew for Each Channel**
  - Built-in PPG Data Delay option supports independent phase control for each channel

Max. 8ch synchronization and individual variable delay

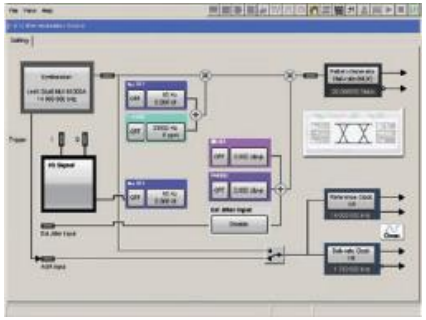


- **Crosstalk Test**
  - High-accuracy control of data synchronized between channels in 1 mUI steps supports accurate validation of DUT crosstalk characteristics

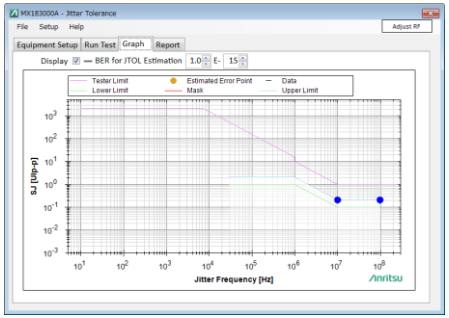


Features (4) Jitter generation capability

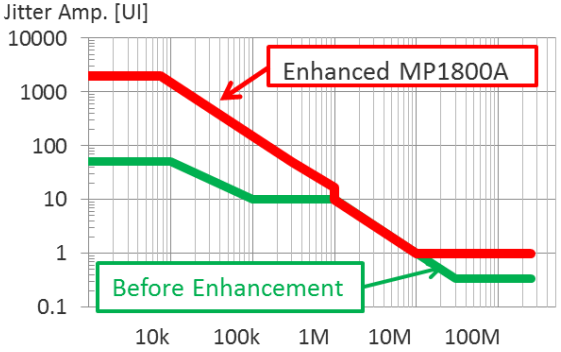
- **Jitter Tolerance Test up to 32.1 Gbit/s**
  - RJ / SJ (2 tone) / BUJ / SSC generation
  - Automatic Jitter Tolerance test using MX183000A
    - SJ: 2000UI max., 1UI @ fm = 250 MHz
    - Shorten measurement time by estimating low error rate result
  - Half-period Jitter (F/2 Jitter) generation using MU183020A PPG



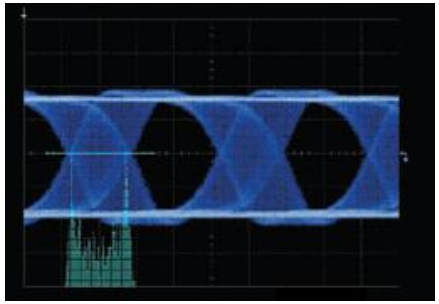
MU181500B Jitter Modulation Source Setting Screen



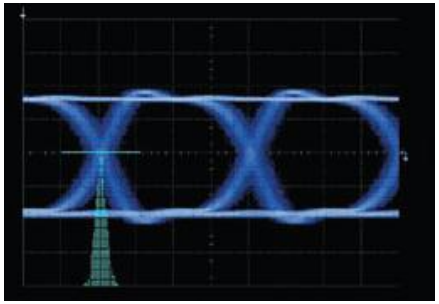
MX183000A PL001 Jitter Tolerance Test Software Result Screen



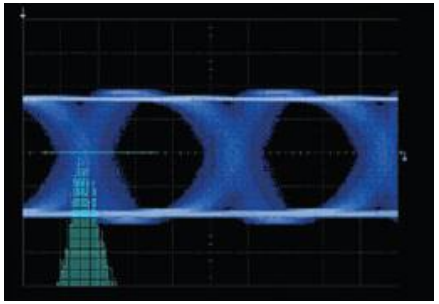
Low Intrinsic Jitter
(measured value using 50-GHz band sampling oscilloscope with Residual Jitter of <100 fs)



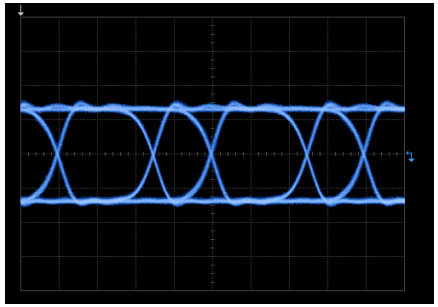
Sine-Wave Jitter



Random Jitter



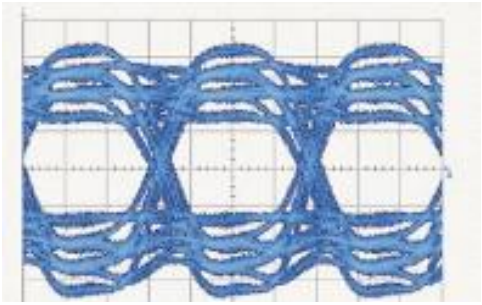
Bounded Uncorrelated Jitter



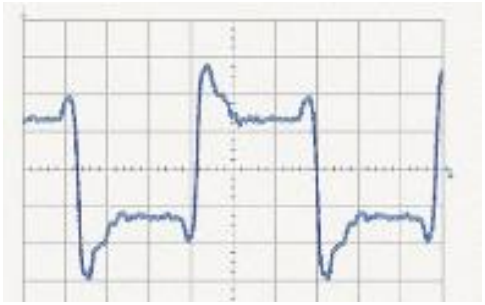
Half-Period Jitter (HPJ, F/2 Jitter)

Features (5) Emphasis capability

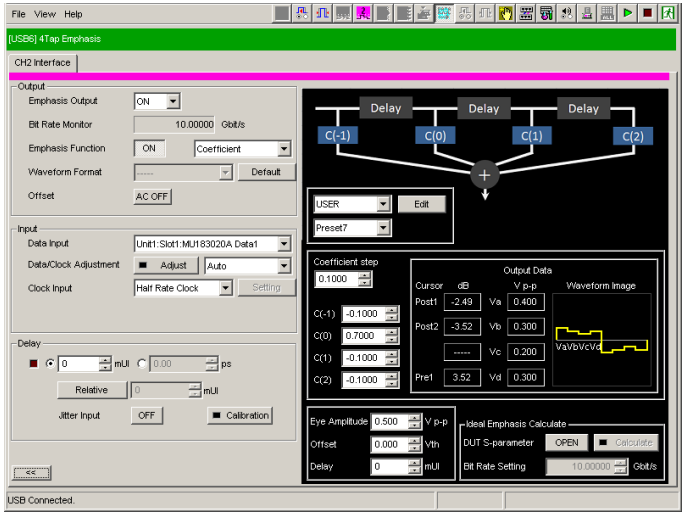
- **4Tap Emphasis Signal Generator up to 32.1 Gbit/s (with MP1825B)**
  - ✓ High quality Emphasis signal of Low Jitter and steep Tr/Tf
  - ✓ Setting by Pre-emphasis, De-emphasis, Co-efficient

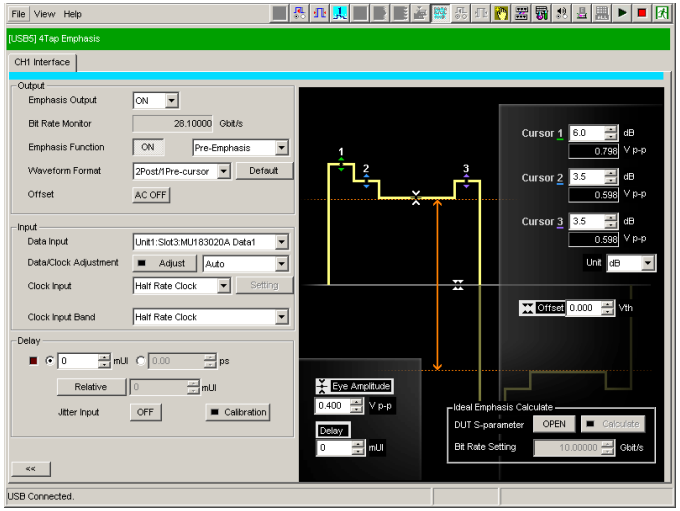


Waveform with PRBS31 Test Pattern



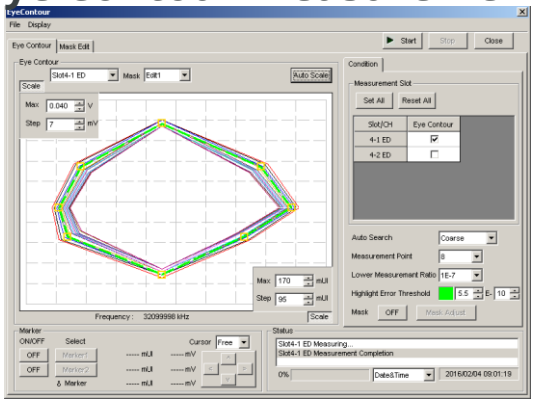
Waveform with FF00 Test Pattern



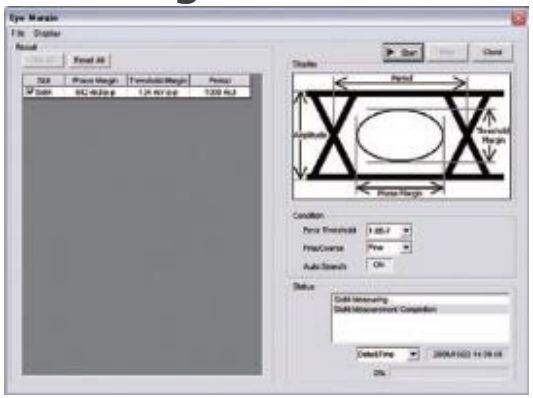


Features (6) Various Analysis functions

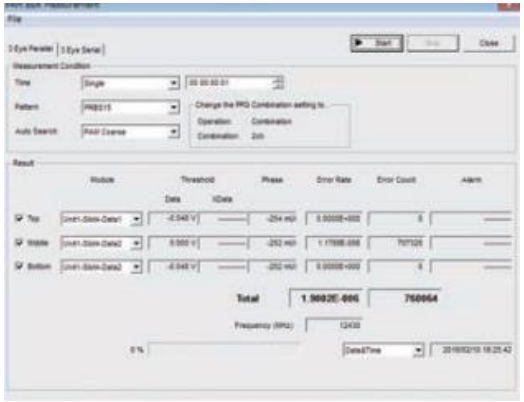
Eye Contour Measurement



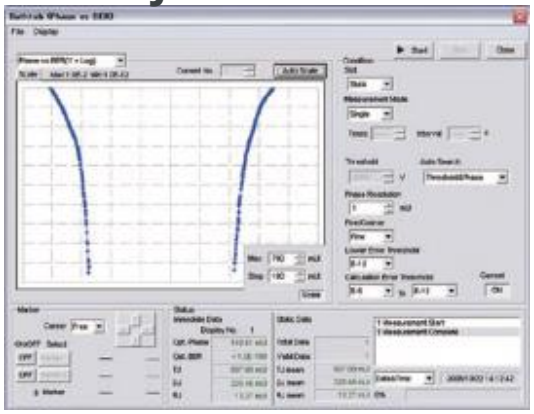
EYE Margin Measurement



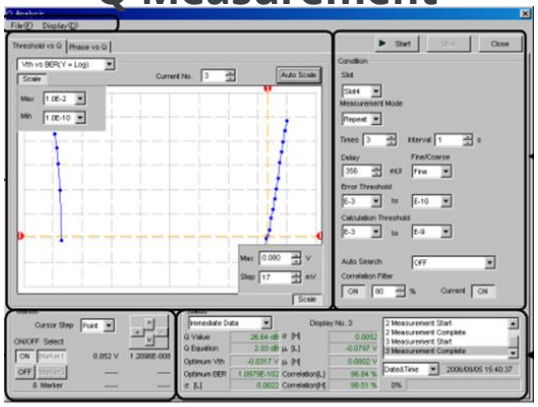
PAM BER Measurement



Bathtub Jitter Measurement



Q Measurement

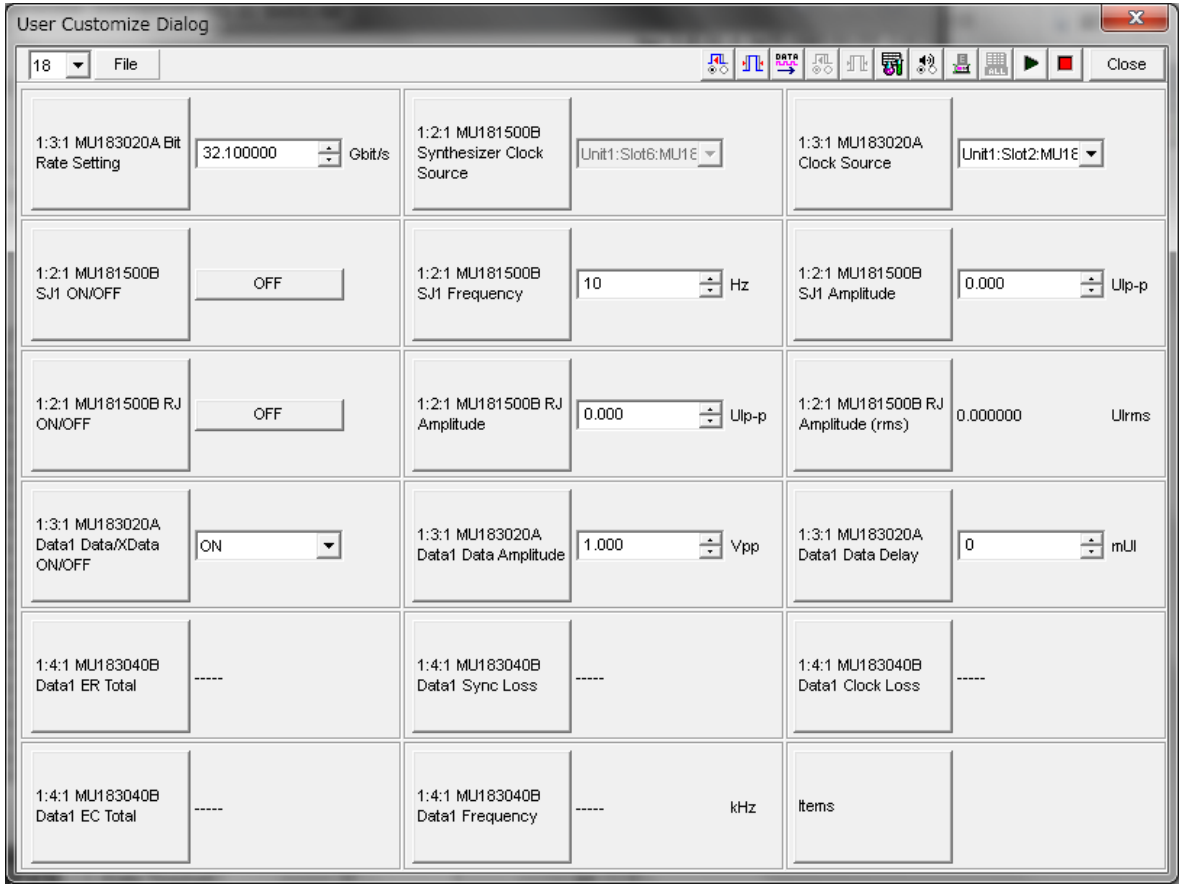


Features (7) Supports various data patterns

- PAM4 Patterns
  - PRBS13Q, GreyPRBS13Q, SSPR, JP03A, JP03B, Square wave
- DQPSK, DP-QPSK Pre-coding
  - DQPSK, DPQPSK Pre-code signal generation
- Burst Signal Test
  - Supports optical circulation loop test
  - Burst disable time up to 1uS (Typical)
- Maximum 256 Mbit/ch Programmable Data Pattern
  - Generates any pattern for applications, such as CJTPAT, CJPAT, K28.5
- Pseudo random Patterns (PRBS)
  - 2^n–1 (n = 7, 9, 10, 11, 15, 20, 23, 31)
- Zero-Substitution Pattern
  - Suitable for clock recovery contiguous “0” / “1” tolerance test
  - Incremental number of “0” / “1” inside of PRBS pattern up to PRBS23

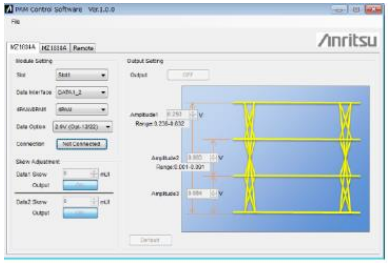
Features (8) Frequent used items on one screen

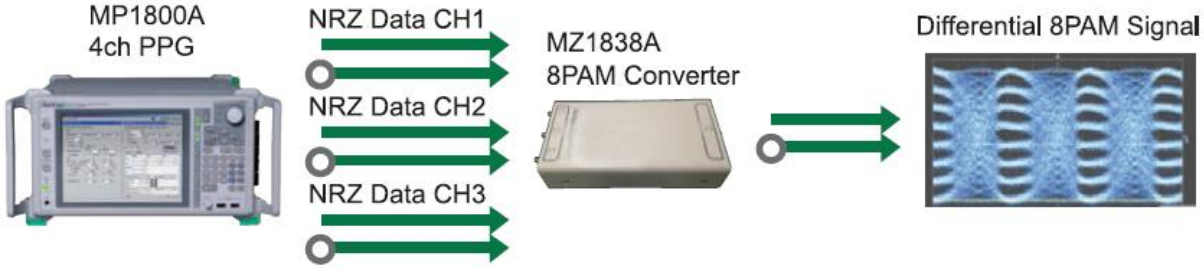
- **Customize screen**
  - For easy operation, you can select up to 18 items on one screen.
  - Selected items can be saved / recall from internal memory.

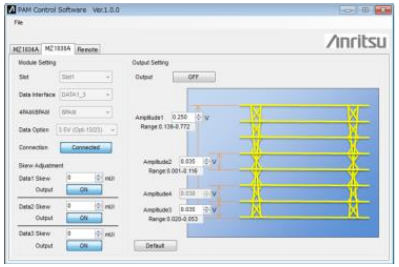


PAM Features (1) PAM signal generation

- **PAM4/PAM8 Generation (MZ1834A/MZ1838A 4/8 PAM Converter)**
  - PAM4 Differential signal generation: MZ1834A + PPG 2ch
  - PAM8 Differential signal generation: MZ1838A + PPG 3ch
  - Wideband 32.1 Gbaud rate
  - High-quality EYE opening, high-speed Tr/Tf
  - PAM Control GUI: Adjustable PPG Data Output for setting PAM signal levels

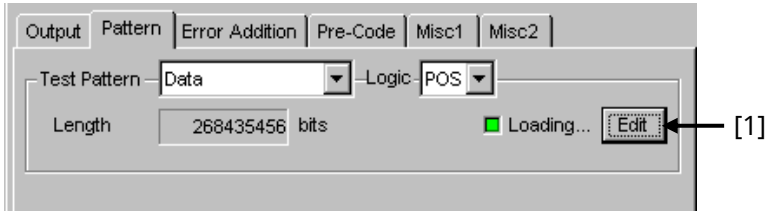


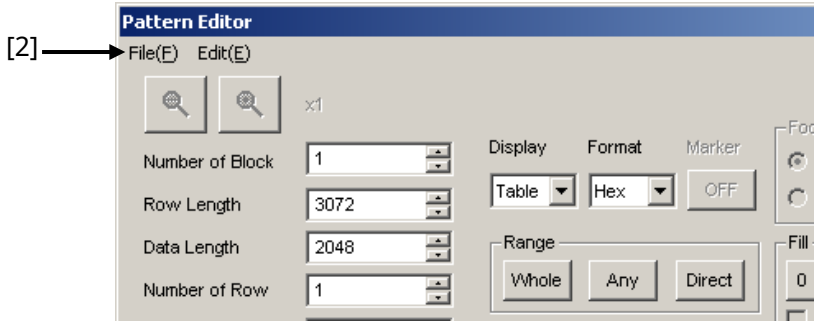




PAM Features (2) Various PAM4 patterns

- 32GBaud PAM4 Patterns
  - Pattern files used for PAM4 signal generation/BER measurement have been added.
  - Select Edit after setting Test Pattern to Data. [1]
  - The following PAM4 Data Patterns can be selected from the Pattern Editor file list.[2]



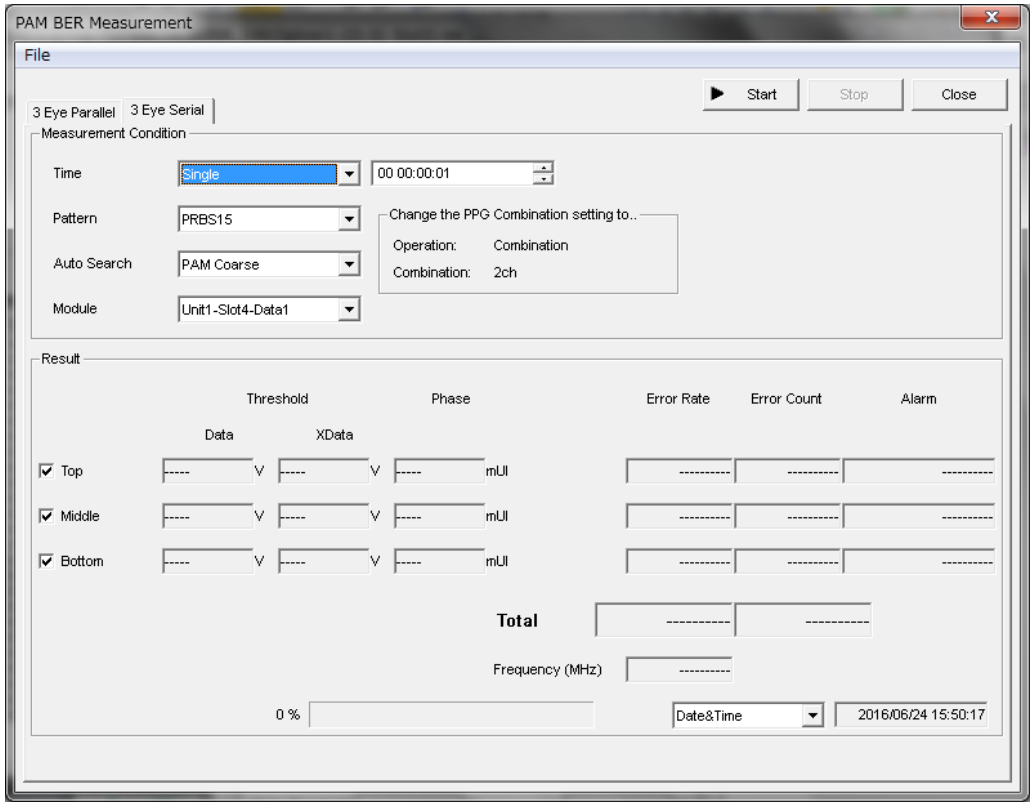


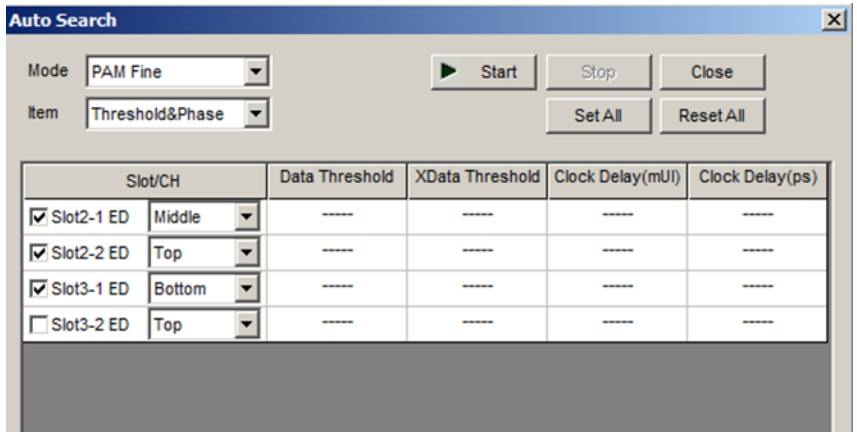
Pattern	PPG1 Pattern file	PPG2 Pattern file	ED Top EYE Pattern	ED Middle EYE Pattern	ED Bottom EYE Pattern
PRBS13Q	PRQS13Q_TX1.txt	PRQS13Q_TX2.txt	PRBS13Q_Upper.txt	PRBS13Q_Middle.txt	PRBS13Q_Lower.txt
GrayPRBS13Q	GrayPRBS13Q_TX1.txt	GrayPRBS13Q_TX2.txt	GrayPRBS13Q_Upper.txt	GrayPRBS13Q_Middle.txt	GraeyPRBS13Q_Lower.txt
PRQS10	PRQS10_TX1.txt	PRQS10_TX2.txt	PRQS10_Upper.txt	PRQS10_Middle.txt	PRQS10_Lower.txt
SSPR	SSPR_TX1.txt	SSPR _TX2.txt	SSPR_Upper.txt	SSPR_Middle.txt	SSPR_Lower.txt
JP03A	JP03A.txt	JP03A.txt	JP03A.txt	JP03A.txt	JP03A.txt
JP03B	JP03B.txt	JP03B.txt	JP03B.txt	JP03B.txt	JP03B.txt
Squarewave	Squarewave.txt	Squarewave.txt	Squarewave.txt	Squarewave.txt	Squarewave.txt

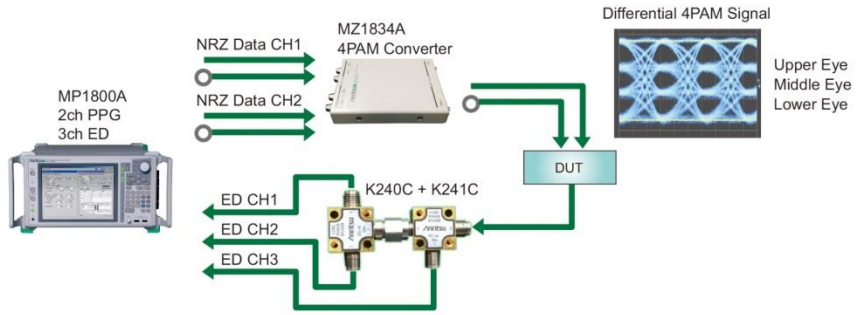
Using Combination Mode for PPG_CH1 and PPG_CH2 to generate above PAM4 patterns.
Using Independent Mode for ED to measure above PAM4 patterns.

PAM Features (3) PAM4 BER Measurement

- PAM4 BER measurement with high input sensitivity ED
  - **Two ways of BER measurement**
    - **Sequential PAM4 respective sub eyes BER measurement with single ED**
    - **Parallel PAM4 sub eyes BER measurement with 3 EDs.**
    - **Auto Search function for each PAM4 sub eyes**

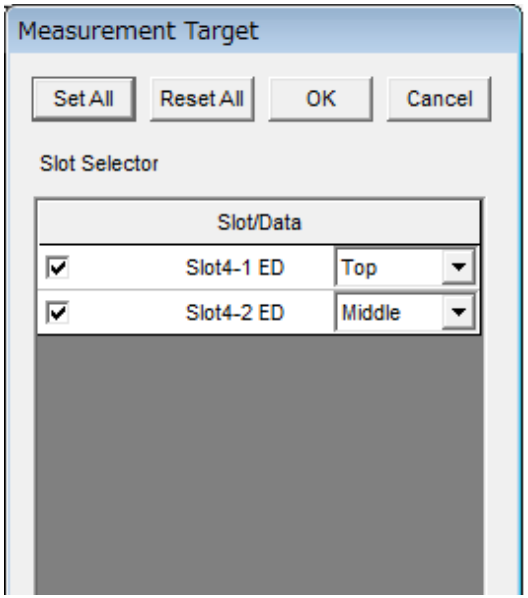


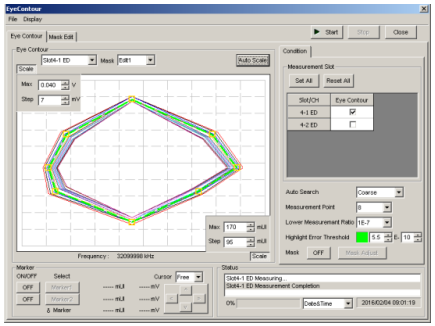


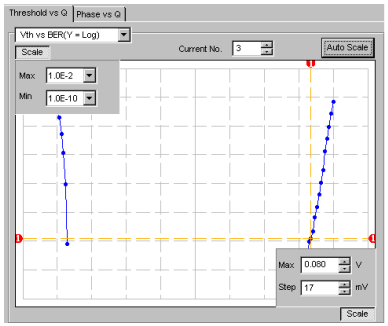


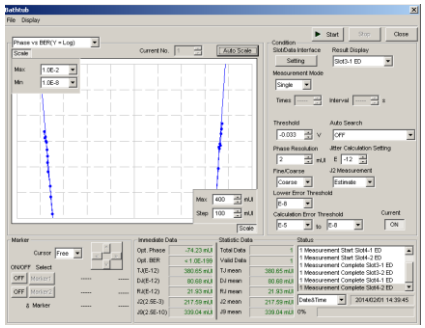
PAM Features (4) PAM4 Analysis functions

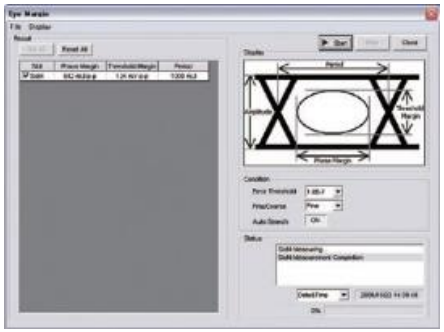
- Analysis functions
  - PAM4 sub eyes analysis for Top, Middle, and Bottom respectively.
  - Auto-measurement functions are:
    - Eye Contour
    - Eye Margin
    - Bathtub
    - Q Analysis







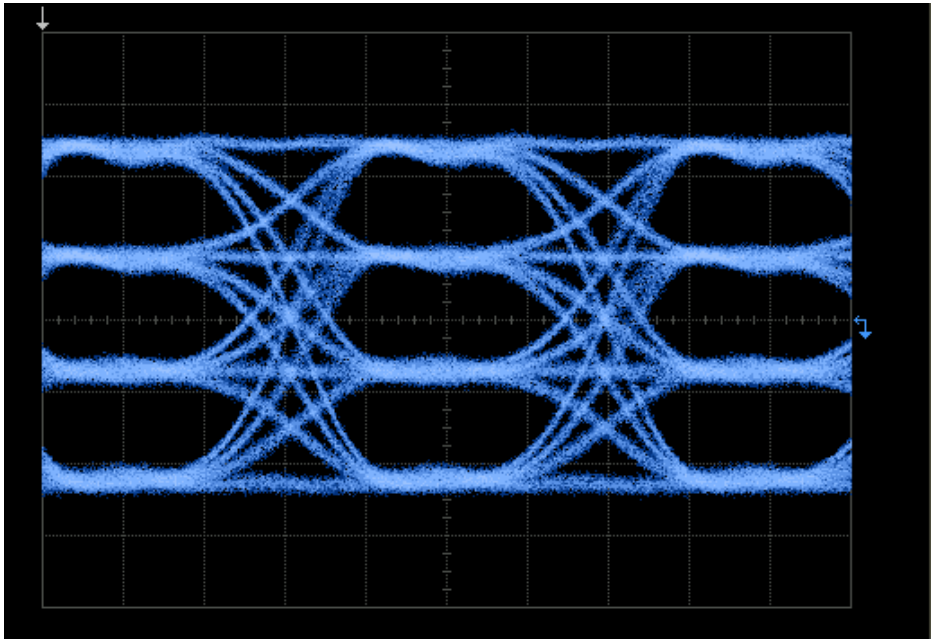




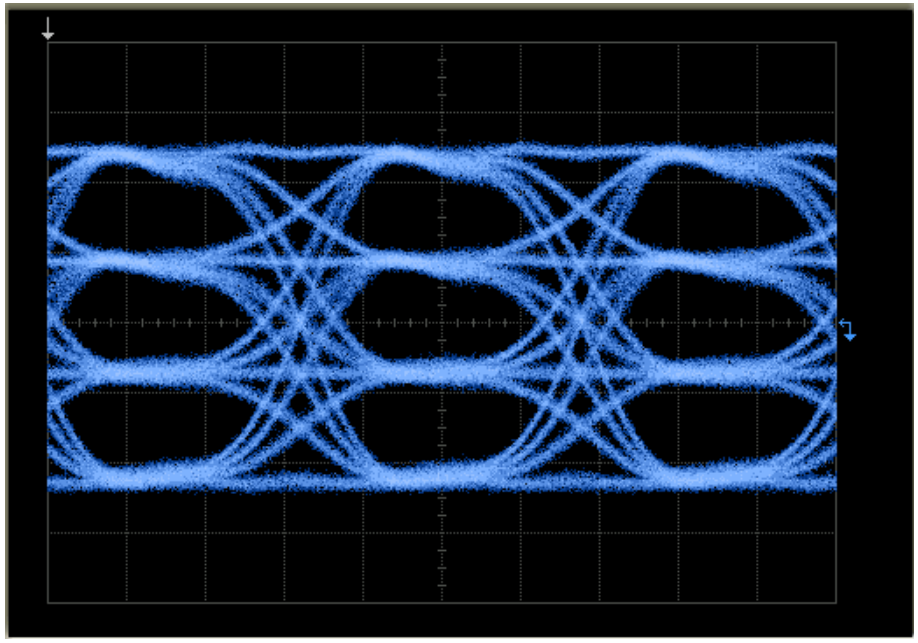
PAM Features (5) Typical waveforms

Conditions

Input: 3.5 Vp-p, 1.75 Vp-p, PRBS31
Output: 832 mVp-p, 170 mV/div, 10.0 ps/div



25.78125 Gbaud Rate



28.1 Gbaud Rate

28G/32G PPG Specifications

Item	Specification
Operating Bit Rate	2.4 to 28.1 Gbit/s 2.4 to 32.1 Gbit/s (Option)
Data Output	
Number of Outputs	MU183020A 1ch 2 ports (Data/xDdata) (Option) 2ch 4 ports (Data1/xData1, Data2/xData2) (Option) MU183021A 4ch 8 ports (Data1/xData1, Data2/xData2, Data3/xData3, Data4/xData4)
Amplitude	500 mV to 2.0 Vp-p/2 mV step (Option) 500 mV to 3.5 Vp-p/2 mV step (Option)
Offset	–2.0 to +3.3 Voh/1 mV step
Crosspoint Adjust	20% to 80%/0.1% step @ 28 Gbit/s, 32 Gbit/s
Clock Output	
Number of Outputs	1
Amplitude	0.3 Vp-p min. 1.0 Vp-p max.
Frequency	Selectable clock of 1/1 or 1/2 of bit rate
Data Delay	Option
Range	–1000 to +1000 mUI/2 mUI step
Pattern Generation	
PRBS	2^n-1 (n = 7, 9, 10, 11, 15, 20, 23, 31), Mark Ratio 1/2, Logic POS/NEG
Programmable DATA	2 to 268,435,456 bits/1 bit step, Mark Ratio 1/2, Logic POS/NEG
Aux Outputs	Divided Clock, Pattern Sync.

28G/32G ED Specifications (1/2)

Item	Specification
Operating Bit Rate	2.4 to 28.1 Gbit/s, 2.4 to 32.1 Gbit/s (Option)
Data Input	
Number of Inputs	MU183040A/B 1ch 2 ports (Data/xData) (Option) 2ch 4 ports (Data1/xData1, Data2/xData2) (Option) MU183041A/B 4ch 8 ports (Data1/xData1, Data2/xData2, Data3/xData3, Data4/xData4
Input Amplitude/ Sensitivity*	
Clock Input	
Number of Inputs	1
Amplitude	0.3 Vp-p min.,1.0 Vp-p max.
Frequency	1/2 of bit rate
Clock Delay	
Range	–1000 to +1000 mUI/2 mUI step
Pattern Detection	
PRBS	2^n-1 (n = 7, 9, 10, 11, 15, 20, 23, 31) , Mark Ratio 1/2, Logic POS/NEG
Programmable DATA	2 to 268,435,456 bits/1 bit step, Mark Ratio 1/2, Logic POS/NEG
Aux Outputs	Divided clock, Pattern Sync.
Analysis Functions	Auto Search, Auto Adjust, Bathtub Jitter, EYE Diagram, EYE Margin, Auto Search PAM Mode, Q-value measurement, Eye Contour, PAM BER Measurement

		MU183040B/MU183041B
Input Amplitude*		0.05 Vp-p to 1.0 Vp-p
Sensitivity*	EYE Amplitude	15 mVp-p (typ.), ≤25 mVp-p
	EYE Height	10 mVp-p (typ.)

* Input amplitude is a range where Auto Adjust function operates. Input sensitivity is the minimum input amplitude which becomes error free.

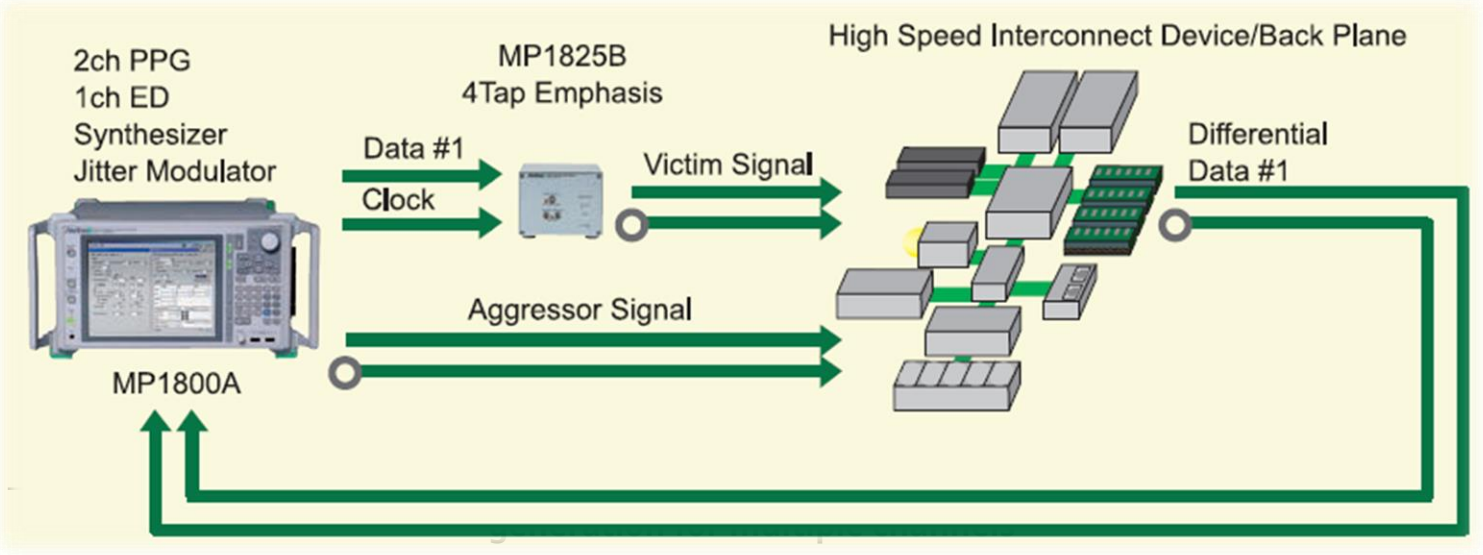
28G/32G ED Specifications (2/2)

ITEM	Specification
Clock Recovery Options	Clock Recovery from ch1 Data input, internal distribution to each channel*1
Operating Bit Rate	Opt-x22: 2.4 to 28.1 Gbit/s Opt-x23: 25.5 to 32.1 Gbit/s (requires MU183040B/41B-001)
Maximum Number of Consecutive Zeros	72 bits (Zero Substitution 2^{15})
Lock Range for Data Clock Recovery	Opt-x22: ±200 ppm Opt-x23: ±100 ppm
Target Loop Band	Opt-x22: Selectable from bit rate/1667, bit rate/2578, Jitter Tolerance*2, and variable Variable: 3 MHz to 17 MHz/1 MHz steps*3 Opt-x23: Selectable from bit rate/1667, bit rate/2578 and Jitter Tolerance*2

*1: MU183041B-023 recovers Clock from ch1 Data input and distributes to ch1 and ch2. Also recovers Clock from ch3 Data input and distributes to ch3 and ch4.
*2: Jitter Tolerance setting makes widest loop band and enables Jitter Tolerance measurement.
*3: Upper setting band depends on bit rate: 17 MHz at 28.1 Gbit/s

Main Applications (Interconnects) (1/2)

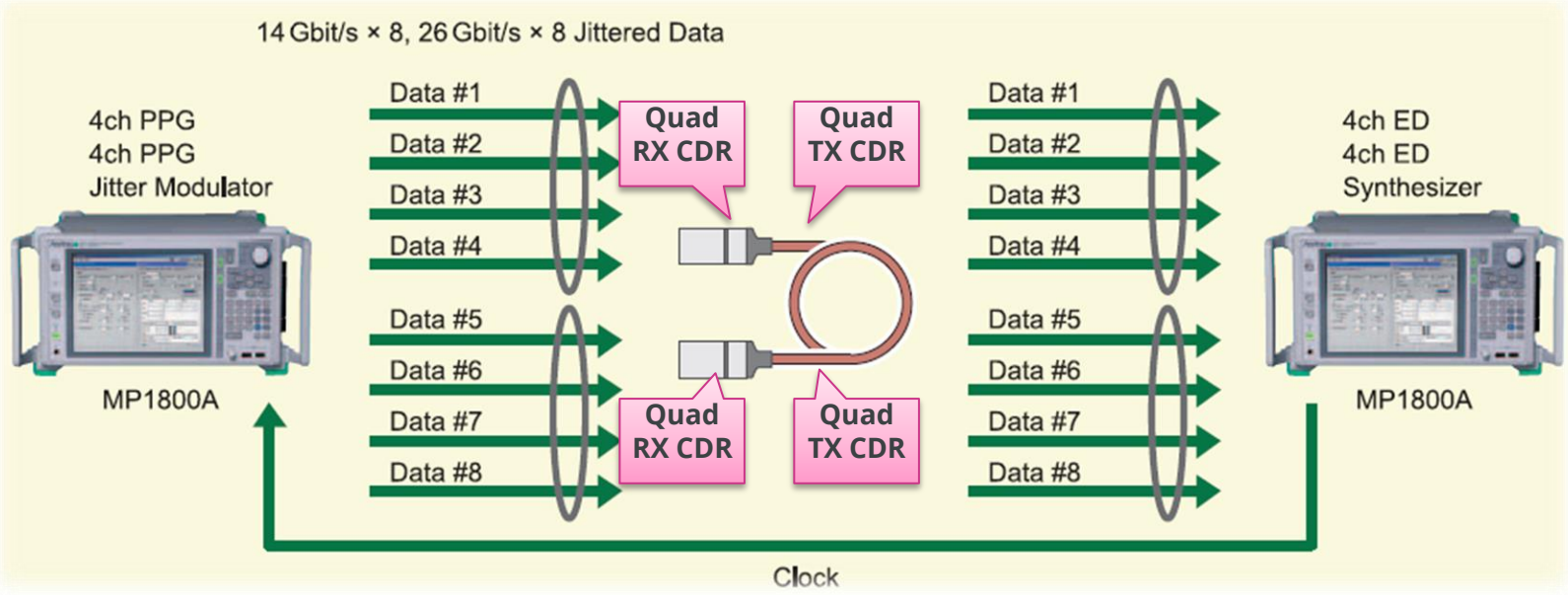
- **28G Ultra high speed Interconnect evaluation**



- **Jitter Tolerance Testing** → **Dual tone SJ/RJ/BUJ/SSC Jitter Tolerance**
  Measuring small amplitude with high-sensitivity
  ED SERDES measurement with clock recovery
- **Compensate for PCB trace losses** → **Emphasis generation**
- **Crosstalk effect testing** → **Timing control and skew control between channels**

Main Applications (Interconnects) (2/2)

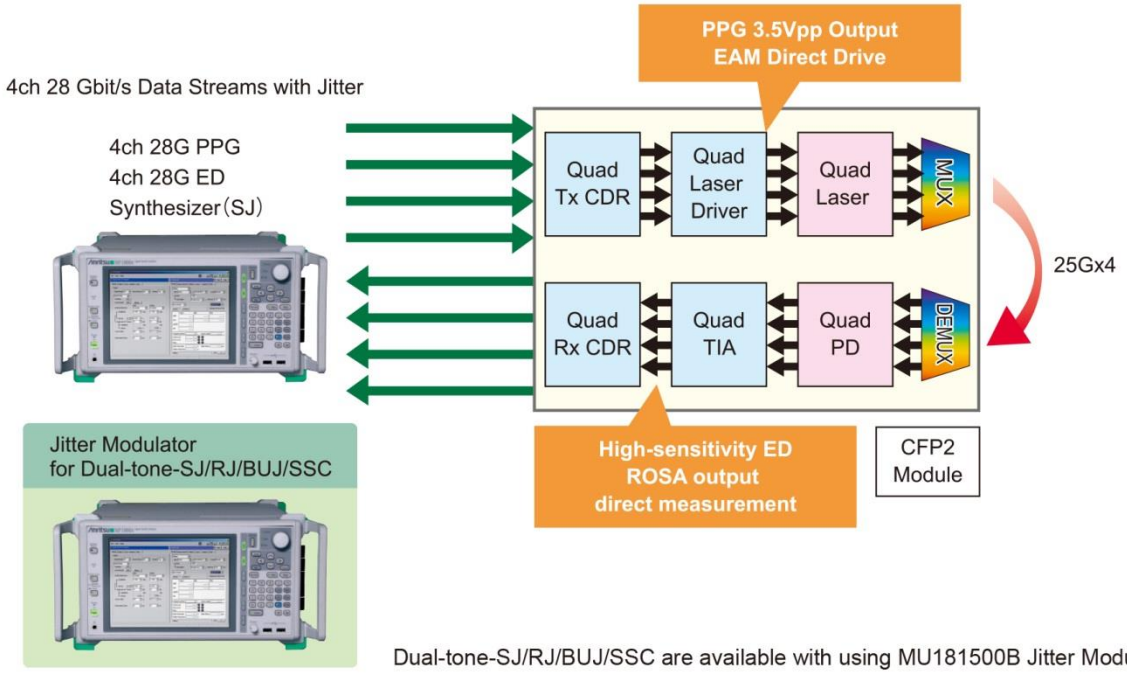
- **Infiniband FDR(14G) / EDR(26G) AOC Evaluation**



– 8ch (4ch end-to-end) BER	→	8ch simultaneous testing Measuring small swing signal with high-sensitivity ED
– Crosstalk effect test	→	Timing control and skew control between channels
– Jitter Tolerance test for CDR	→	SJ/RJ/BUJ/SSC Jitter Tolerance
– Output waveform test	→	TJ/DJ/RJ/Bathtub Jitter, EYE Contour (BER contour mask) analysis

Main Applications (CFP2/CFP4)

- **CFP2/CFP4 Evaluation**

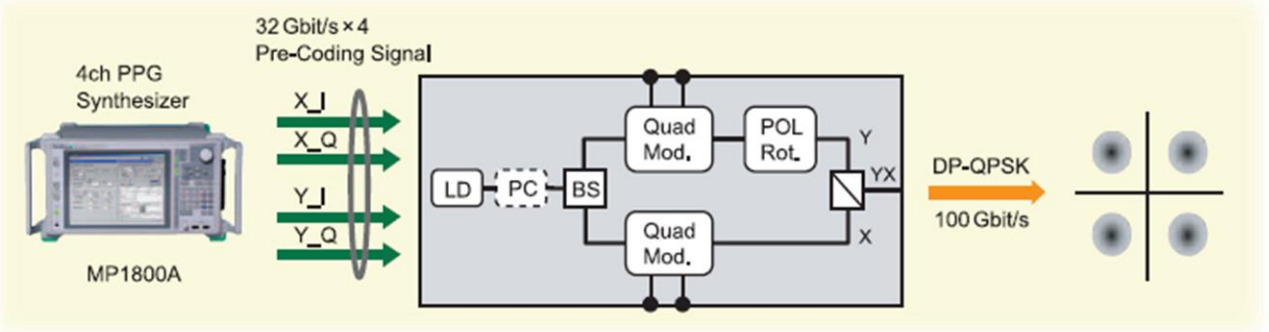


Dual-tone-SJ/RJ/BUJ/SSC are available with using MU181500B Jitter Modulation Unit.

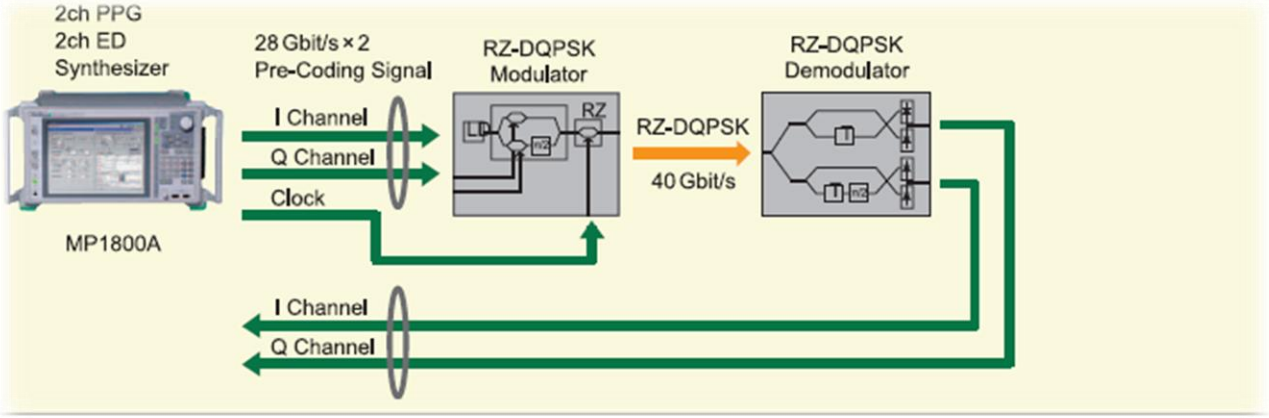
- **Crosstalk effect test** → **Timing control and skew control between channels**
- **25 x 4λ BER** → **All-in-one 4ch simultaneous testing**
  Measuring small swing signal with high-sensitivity ED
- **EAM Direct drive** → **3.5 Vp-p Data out, variable Crosspoint**
- **Jitter Tolerance test for CDR** → **SJ Jitter Tolerance (MU181000 with jitter option can generate SJ)**

Main Applications (DP-QPSK, DQPSK)

- **32G DP-QPSK Evaluation**



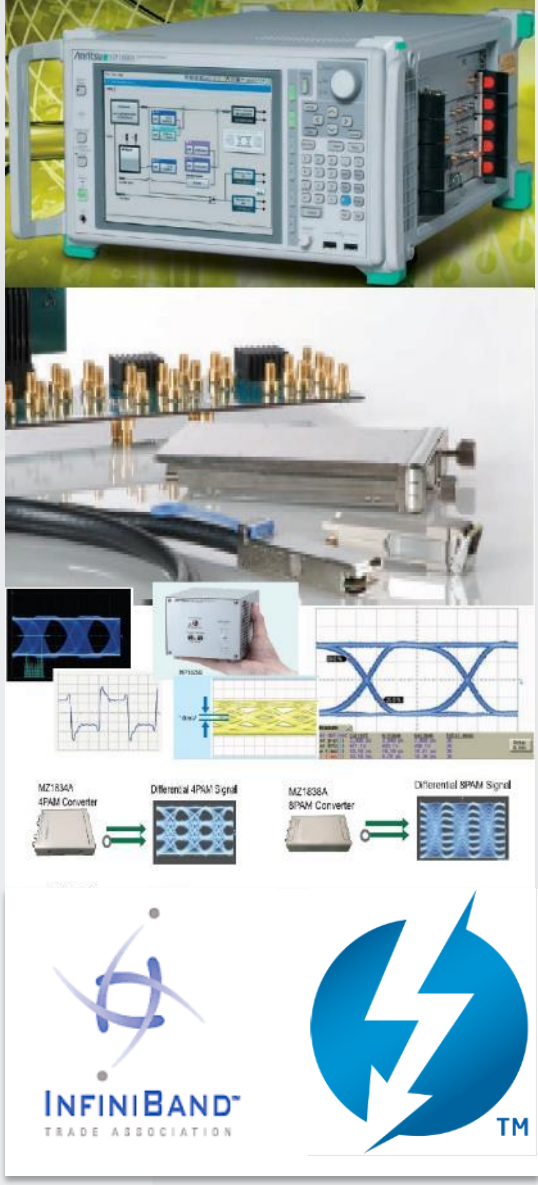
- **DQPSK Evaluation**



- Pre-coding signal generation → Synchronized DP-QPSK, DQPSK signal
- Optical output waveform optimization → Crosspoint adjustment
- Timing control between channels → Precision data delay
- Modulator input level tolerance → 3.5 Vp-p Data out, variable Amplitude

Multi-channel SQA Solution

56G / 64G Solution



Module Lineup

MP1861A
56G/64G bit/s MUX

MP1862A
56G/64G bit/s DEMUX

J1646A
Passive Equalizer 6dB
(V connector)

Standard Configurations

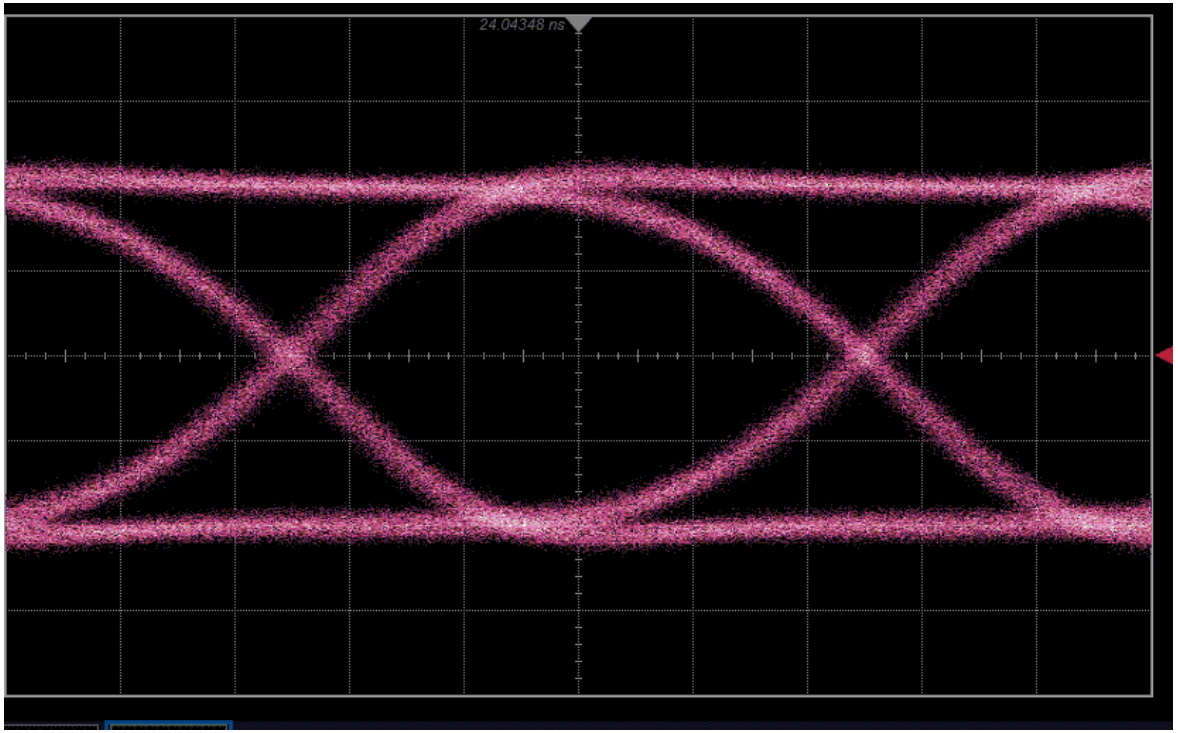
MP1800A Max. 6 slot

MP1861A **MP1862A**

56G/64G Jitter BERT	56G/64G 2ch BERT	56G/64G 4ch BERT (2 box)	
32G PPG 2ch	32G PPG 4ch or 32G PPG 2ch x 2	32G PPG 4ch or 32G PPG 2ch x 2	32G ED 4ch or 32G ED 2ch x 2
32G ED 2ch			
Synthesizer (2 Slots)	32G ED 4ch or 32G ED 2ch x 2	32G PPG 4ch or 32GPPG 2ch x 2	32G ED 4ch or 32G ED 2ch x 2
Jitter Generator (2 Slots)	4Port Synthesizer (2 Slots)	4Port Synthesizer (2 Slots)	
64G MUX	64G MUX	64G MUX	64G DEMUX
64G DEMUX	64G MUX	64G MUX	64G DEMUX
	64G DEMUX	64G MUX	64G DEMUX
	64G DEMUX	64G MUX	64G DEMUX

Features (1) Waveform Quality

- Low-Jitter, High-quality Waveform MUX



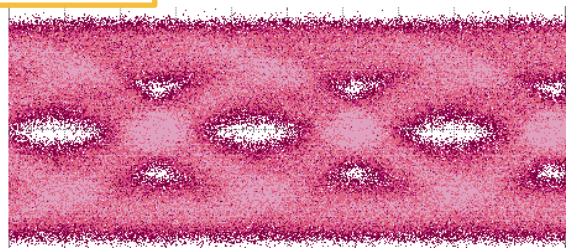
50 Gbit/s, 3.5 Vp-p Output Waveform (MP1861A-013)

Features (2) Rx Sensitivity and Equalizer

- **High-sensitivity DEMUX**
  - ✓ Sensitivity: 25 mV (typ.) (56.2 Gbit/s, single-end, EYE Height, PRBS31)
    ≤40 mV (56.2 Gbit/s, single-end, EYE Height, PRBS31)
    30 mV (typ.) (64.2 Gbit/s, single-end, EYE Height, PRBS31)
- **Passive equalizer**
  - ✓ Put passive equalizer upstream of MP1862A 56/64G bit/s DEMUX
  - ✓ Compensate transmission path losses, recovery of EYE Opening then possible to measure BER and execute jitter tolerance

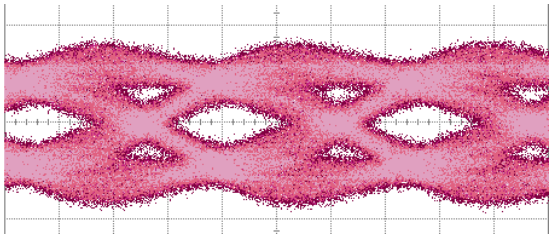
Before

※70 mV/div

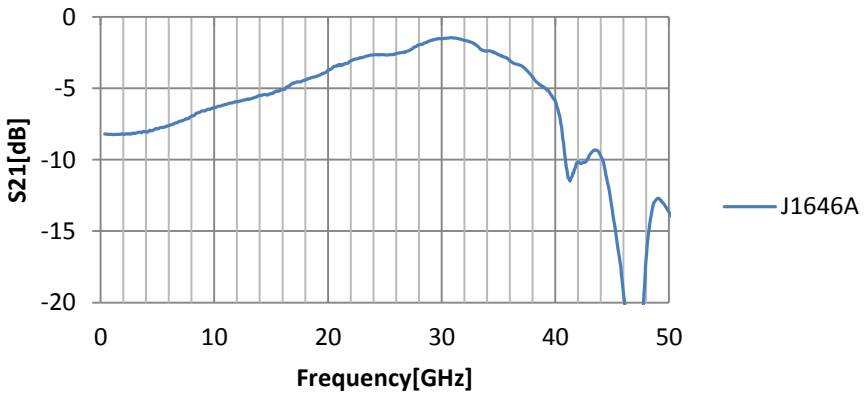


After

※50 mV/div

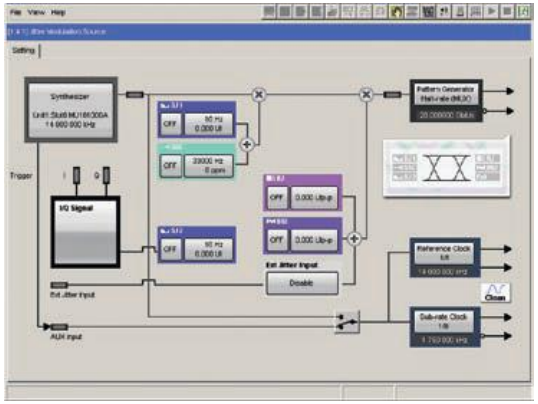


J1646A Passive Equalizer 6dB S21

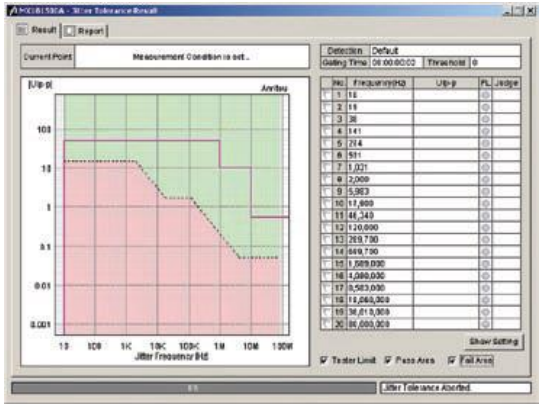


Features (3) Jitter generation and tolerance test

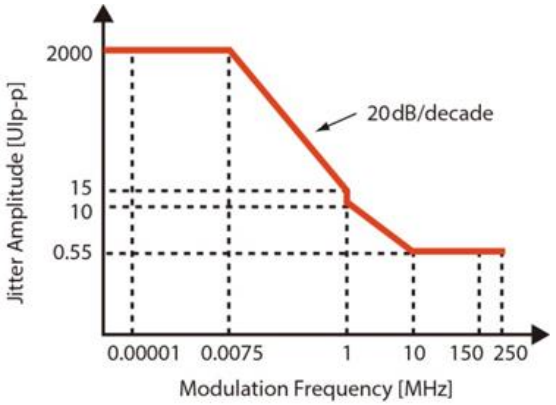
- Full jitter components generation: Dual tone SJ, RJ, BUJ, SSC, Half Period Jitter
- Automatic jitter tolerance measurements
  - ✓ SJ up to 2000 UI or 0.55 UI high-frequency SJ at 250 MHz (at 56.2Gbps).
  - ✓ Low intrinsic jitter: 275 fs rms. (typical).



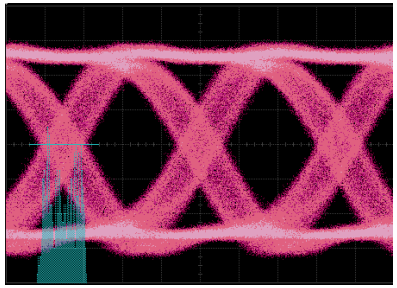
Generate Various types of jitters



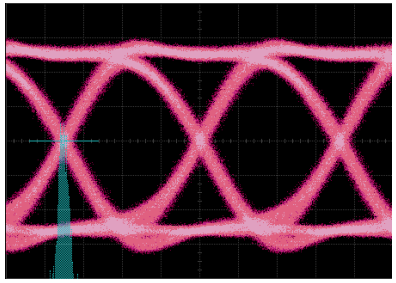
MX181500A Jitter/Noise Tolerance Test Software



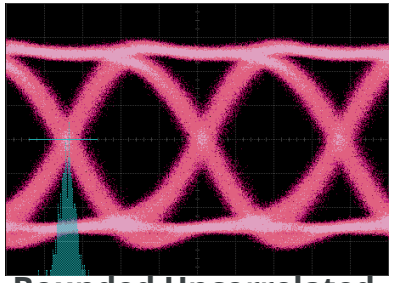
Jitter Generation Mask



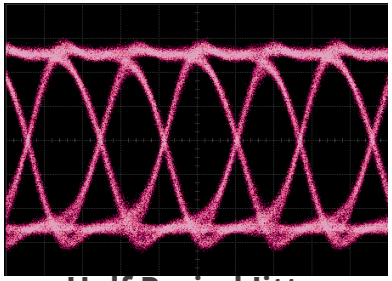
Sine Wave Jitter (SJ)



Random Jitter (RJ)



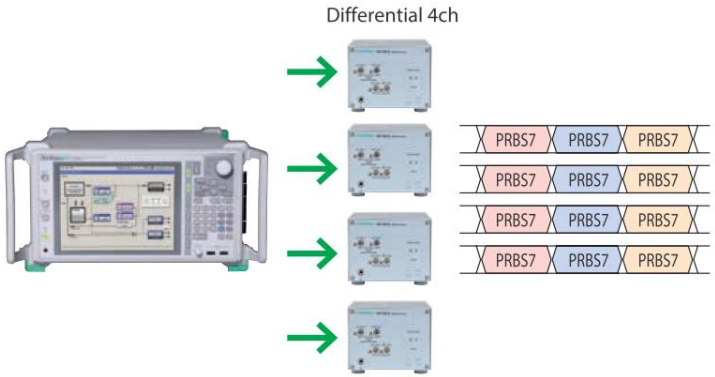
Bounded Uncorrelated Jitter (BUJ)



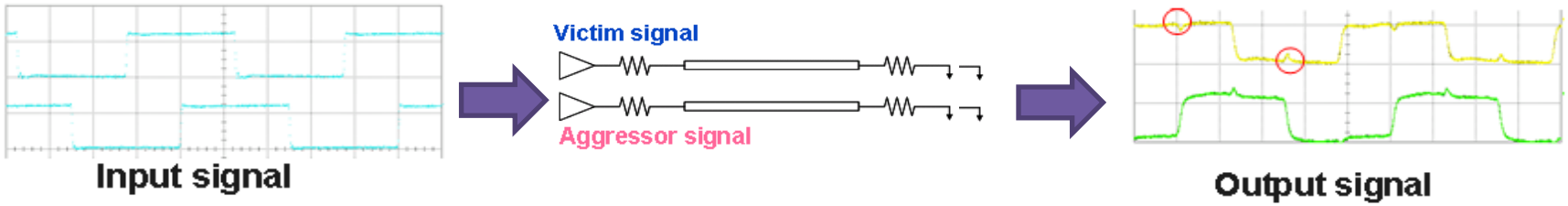
Half Period Jitter (Even/Odd Jitter)

Features (4) Synchronous operation

- **4ch Synchronization in one mainframe**
  - ✓ Ultra high speed synchronized data streams up to 4ch MP1861A 56G / 64G MUX by one MP1800A.

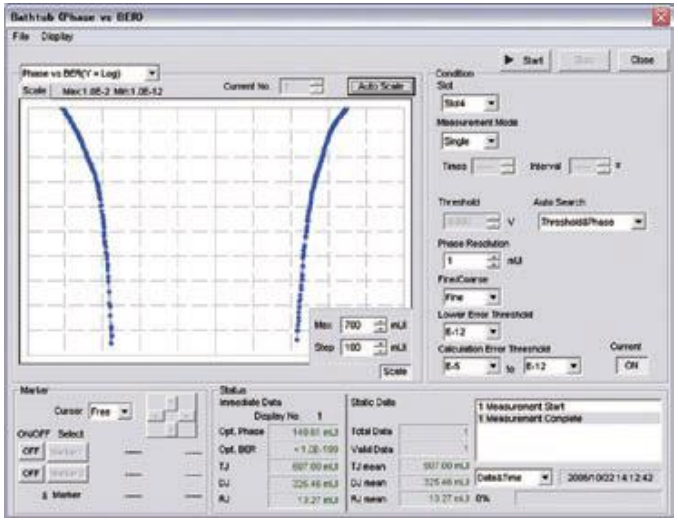


- **Crosstalk Tests**
  - ✓ Installing MUX Data Delay option offers independent phase control for each channel.
  - ✓ High accurate phase delay setting in 4mUI steps.

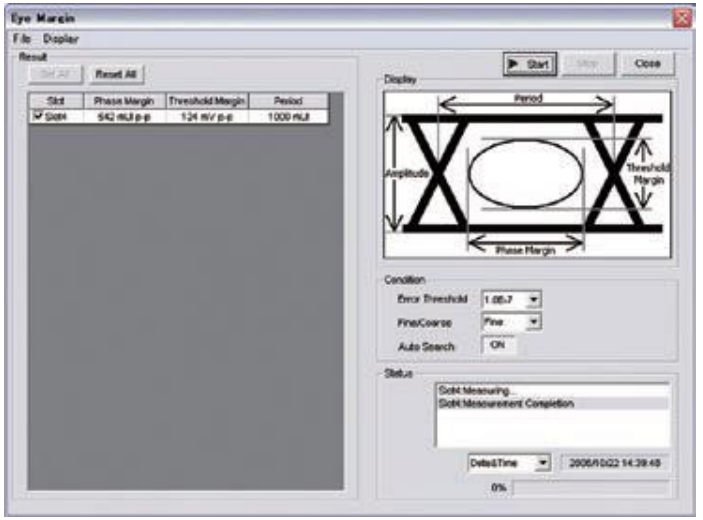


Features (5) Various analysis functions

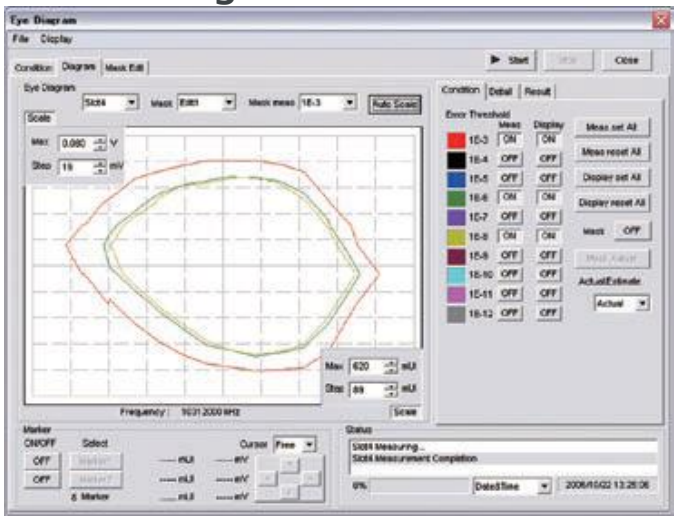
Bathtub Jitter Measurement



EYE Margin Measurement



EYE Diagram Measurement



Features (6) Various data patterns

- **Burst Signal Tests**
  - ✓ Supports application evaluation using burst signals, such as optical circulation loop test
  - ✓ Burst disable time up to 1uS (Typical)
- **Max 512 Mbit/ch Programmable Data Pattern**
  - ✓ Generates any pattern for applications, such as CJTPAT, CJPAT, K28.5
- **Pseudorandom Patterns (PRBS)**
  - ✓ 2^{n-1} (n = 7, 9 , 10 , 11 , 15 , 20 , 23 , 31)
- **Zero Substitution Patterns**
  - ✓ Suitable for clock recovery contiguous 1s and 0s tolerance testing
- **Mixed Patterns**

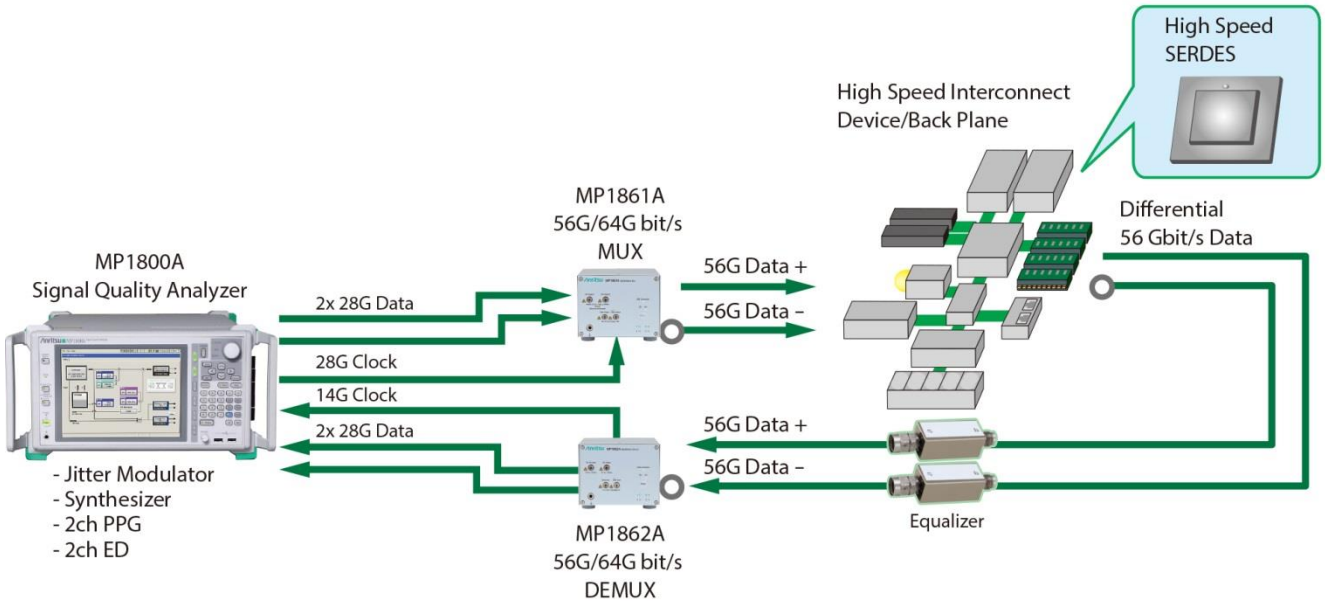
56G/64G bit/s MUX/DEMUX specifications

MP1861A 56G/64G bit/s MUX	
Bit Rate	8 to 56.2 Gbit/s 8 to 64.2 Gbit/s (MP1861A-001)
No. of Channels	1ch, Up to 4ch parallel synchronization by connecting to MP1800A
Amplitude	0.5 to 2.5 Vp-p（≤56.2 Gbit/s, MP1861A-011） 1.0 to 2.5 Vp-p（>56.2 Gbit/s, MP1861A-011） 0.5 to 3.5 Vp-p（≤56.2 Gbit/s, MP1861A-013） 1.0 to 3.5 Vp-p（>56.2 Gbit/s, MP1861A-013）
Intrinsic Random Jitter	RJ = 200 fs rms（typ.）
Half Period Jitter	20 Steps

MP1862A 56G/64G bit/s DEMUX	
Bit Rate	8 to 56.2 Gbit/s 8 to 64.2 Gbit/s (MP1861A-001)
No. of Channels	1ch, Up to 4ch parallel synchronization by connecting to MP1800A
Amplitude	0.125 to 1.0 Vp-p
Sensitivity	25 mV (typ.), ≤40 mV (EYE height, PRBS31, single-ended)

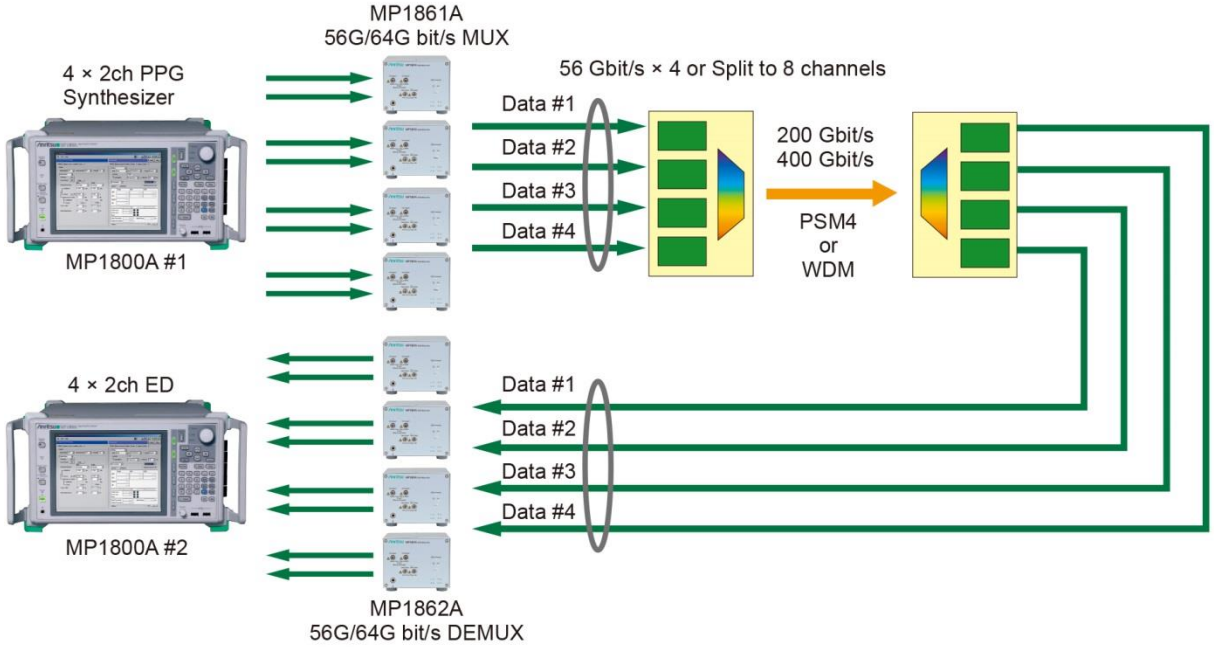
Main Applications (Interconnect)

- **56 Gbit/s Band High Speed Semiconductor Chip Measurements**



- 56 / 64 Gbit/s BER Measurements → For SERDES, Clock Data Recovery(CDR), etc.
- Jitter Tolerance Tests → Supports dual tone SJ, RJ, BUJ, SSC, etc., Jitter Tolerance tests for CEI-56G
- Input Sensitivity Tests → Wide variable amplitude range 0.5 to 3.5 Vpp (56G, with installed MP1861A-013 option)
- Bathtub Jitter Measurements → TJ / RJ / DJ separation

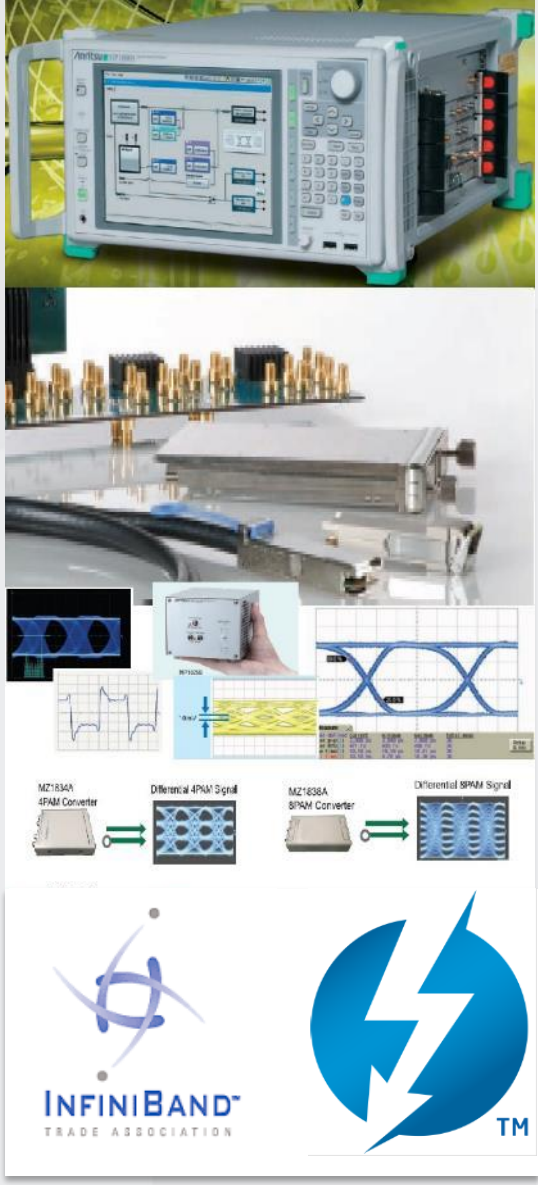
Main Applications (Transmitter)



- 200 GbE, 56G × 4 lane evaluation → Supports EML and optical module evaluations for 200G / 400GbE
- EML evaluation → Direct EML driving using variable output function up to 3.5 Vp-p
- Confirming skew and crosstalk effects → Pattern Sync and Variable Phase functions support easy verification of Rx device skew tolerance, crosstalk effects
- Auto search functions → Data and Clock phase auto alignment

Multi-channel SQA Solution

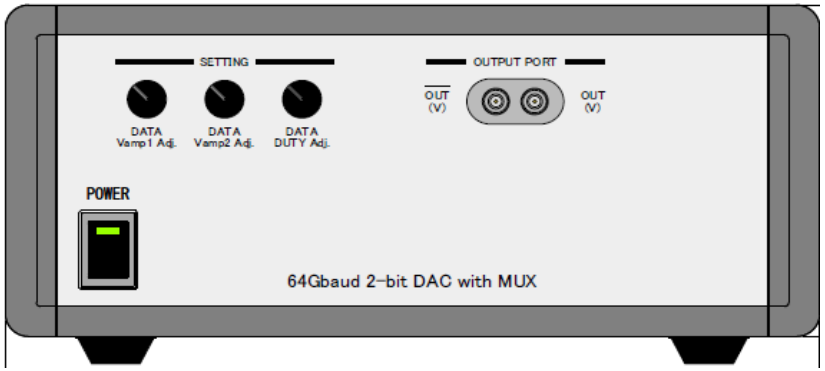
56G / 64GBaud PAM4 Solution



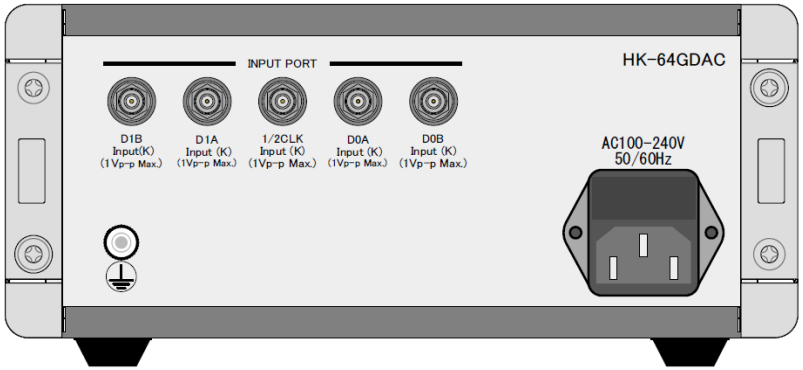
64Gbaud PAM4 DAC features

G0374A 64Gbaud PAM4 DAC

- Wide Operating Range: DC to 64 Gbaud
- Generates 64 Gbaud PAM4 signal using half rate 32 Gbit/s x 4 input signals
- 1.4 Vp-p (differential, Typ.) output
- Amplitude, duty and Upper / Lower / Middle amplitude ratio control by manual
- Low output Jitter performance of only 300 fs (rms)
- NRZ, PAM4 signal control and jitter addition

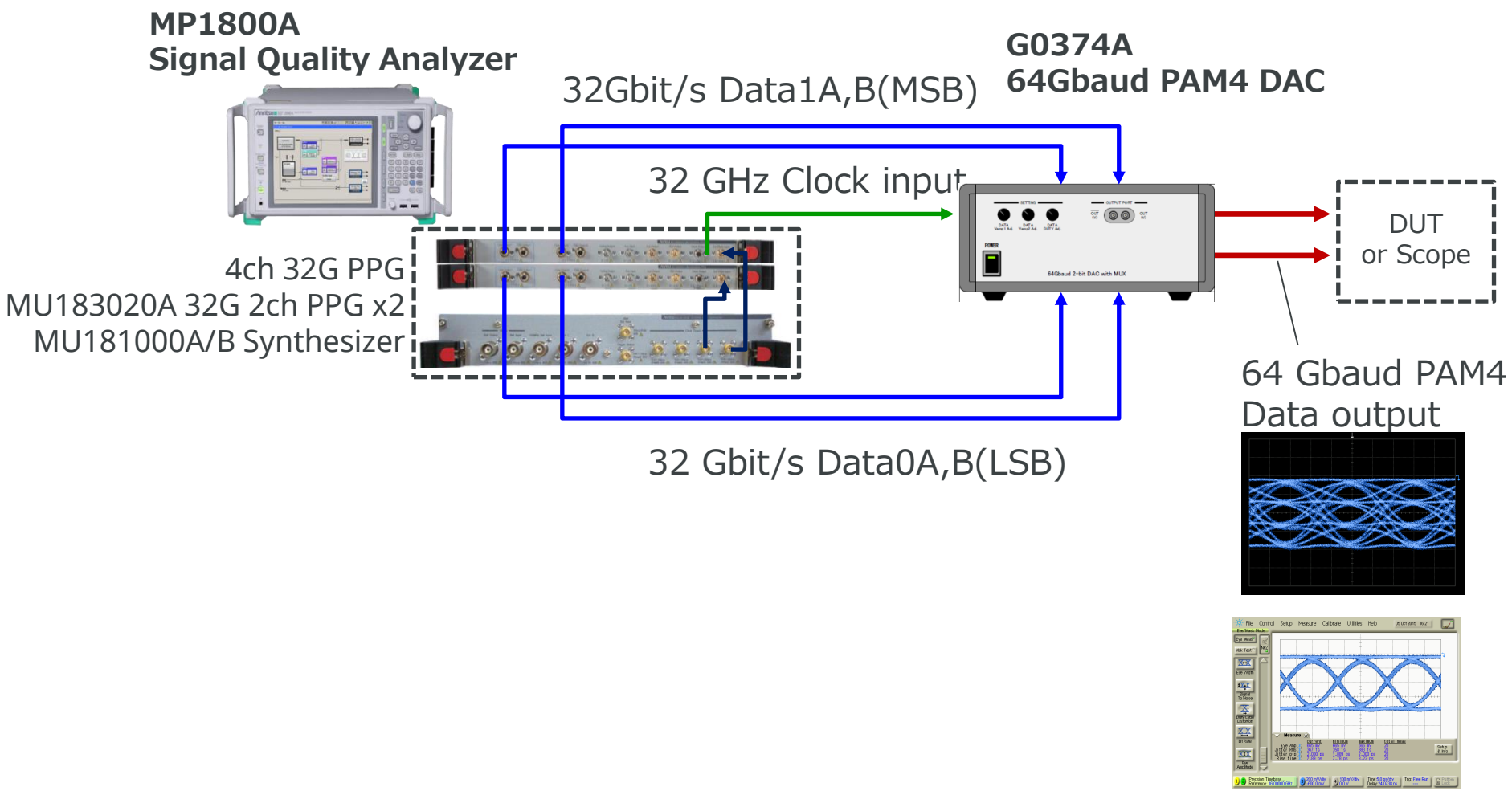


Front View



Rear View

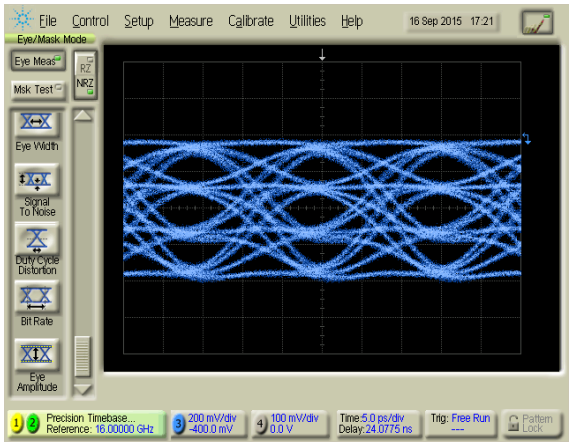
64Gbaud PAM4 generation block diagram



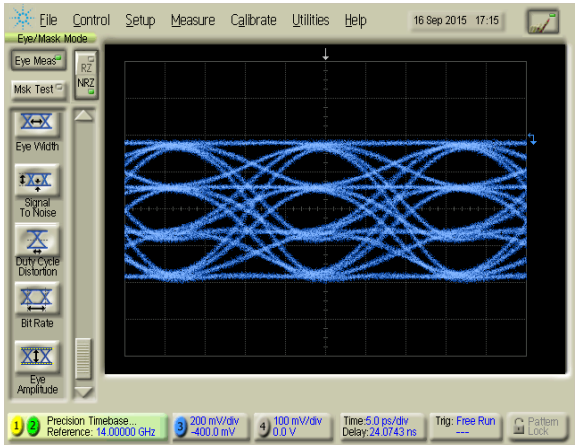
Typical waveform from 64Gbaud PAM4 DAC

➢ PAM4 Output Waveforms (41 V -6 ATT +3 4 V V50 Adapter + 70-GHz Band Oscilloscope)

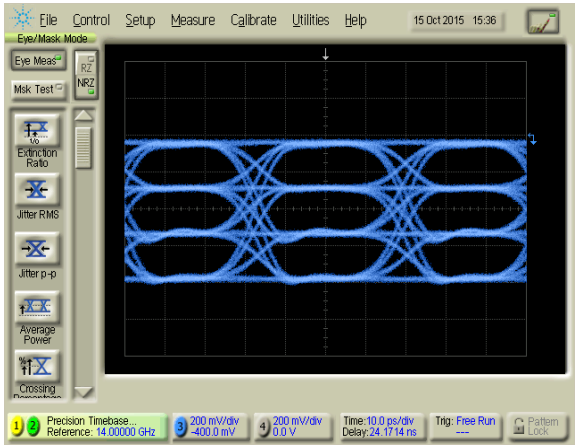
64 Gbaud



56 Gbaud

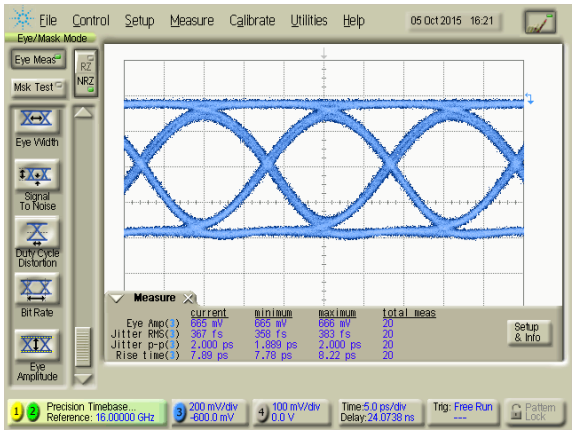


28 Gbaud

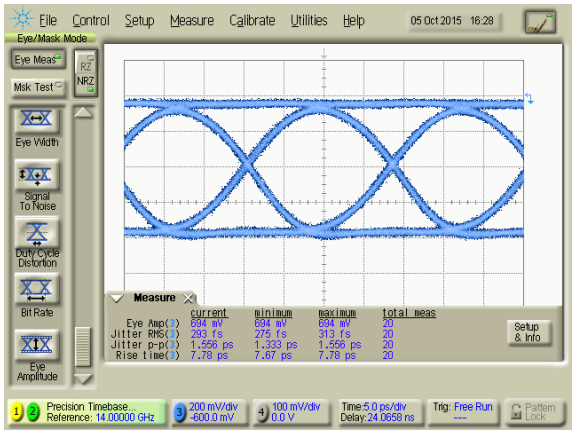


➢ NRZ Output Waveforms (41 V -6 ATT +3 4 V V50 Adapter + 70-GHz Band Oscilloscope)

64 Gbaud

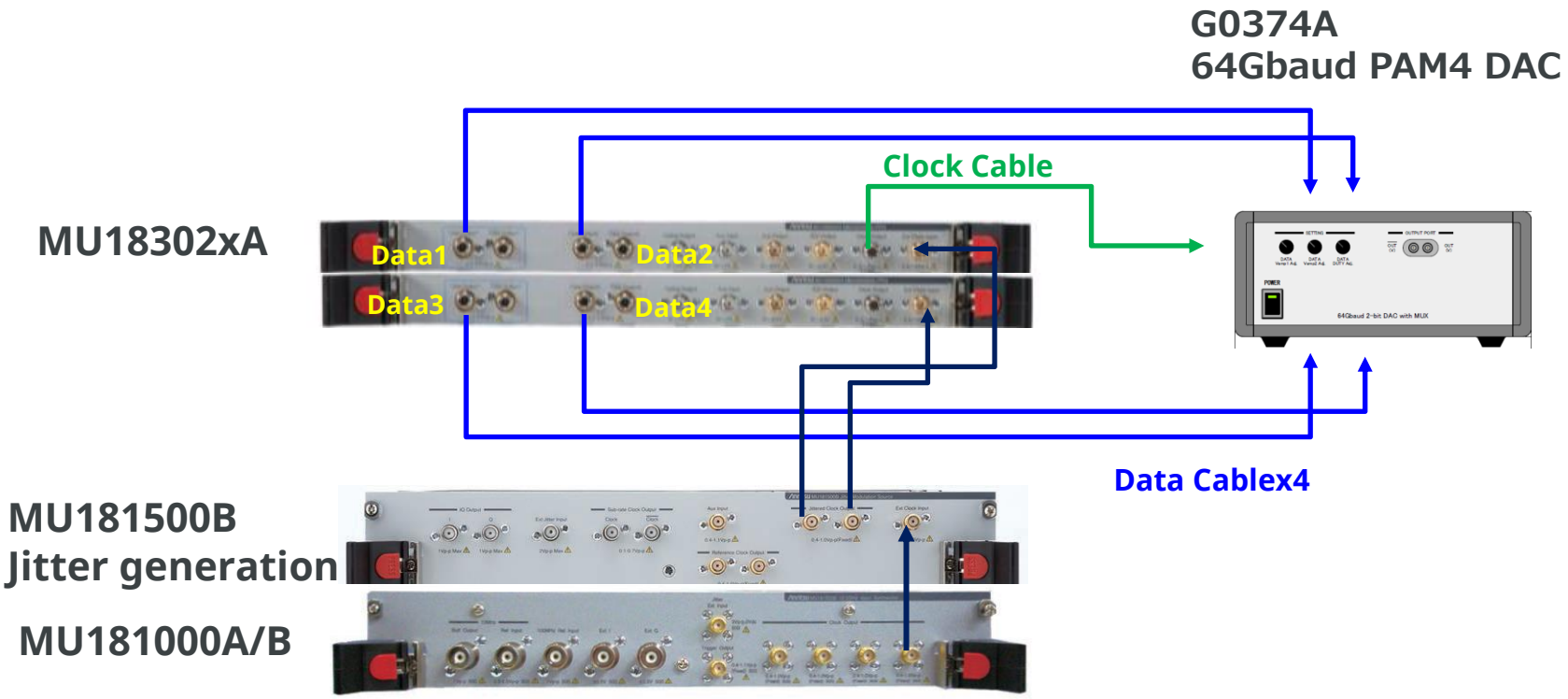


56 Gbaud



Block diagram for jitter injection

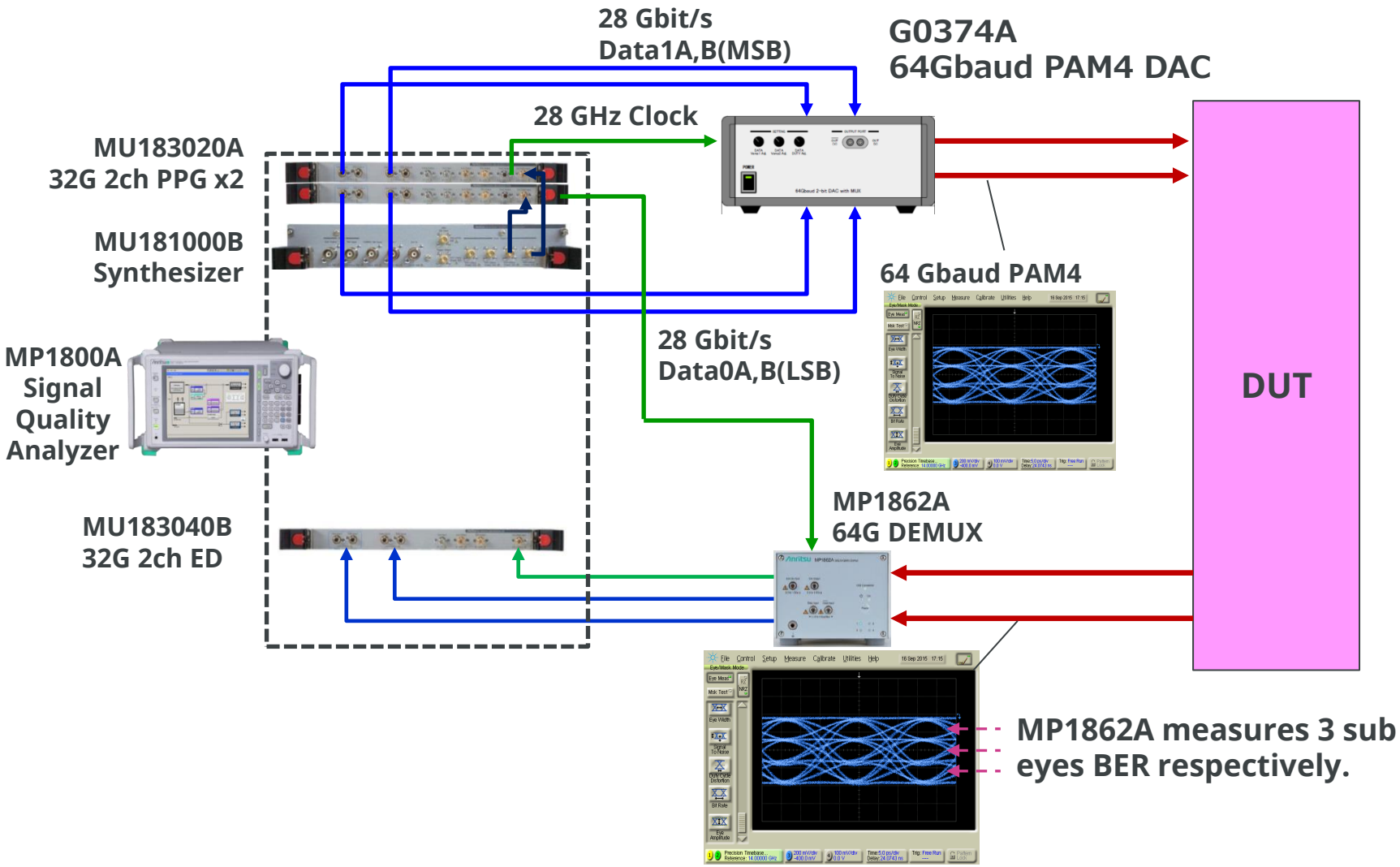
G0374A 64Gbaud PAM4 DAC has jitter transparency.
So jitter stress test is possible on top of PAM4 signal.



Recommended cables: Data Cables 80 cm (J1612A x4)
Clock Cable 130 cm (J1611A)

56Gbaud PAM4 BER measurement

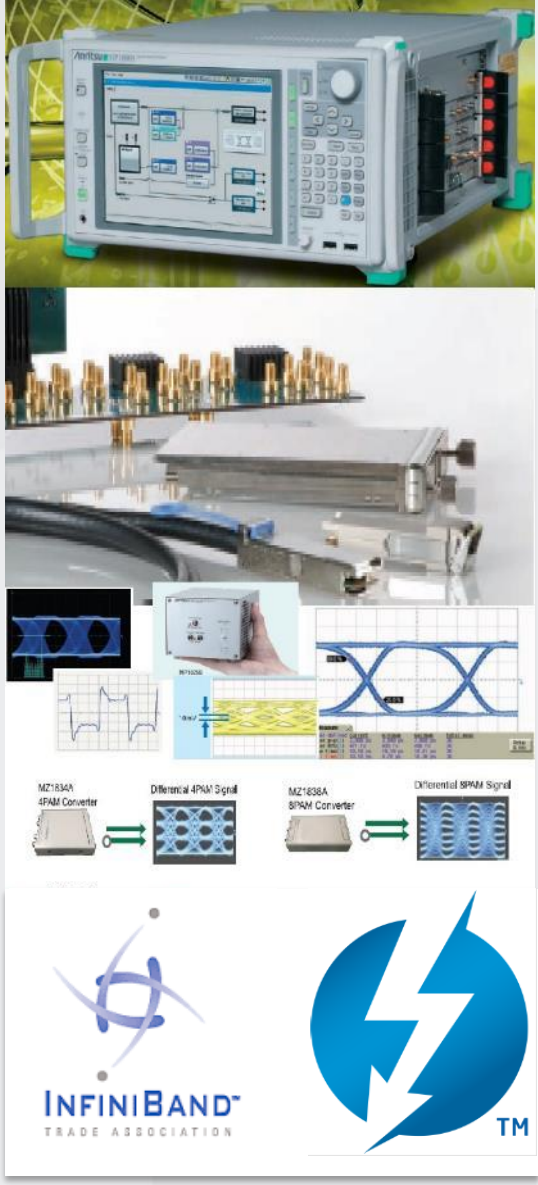
- Support 56Gbaud PAM4 BER measurement with PRBS15



Multi-channel SQA Solution

High Speed Serial Bus Solution

- Thunderbolt Gen3
- USB3.1 Gen1 / Gen2
- PCIe Gen4



Agenda

1. **TBT solution**
2. USB solution
3. PCIe solution

Thunderbolt Overview

What is Thunderbolt (TBT)?

- 10.3125 Gbps for Gen1 & Gen2, 2 x 20.625 Gbps for Gen3.
- Integrated multiple applications through ALT mode (TBT, USB, DP)
- Power delivery up to 100 W

Anritsu Solution

- MP1800A SQA is the first authorized BERT by Intel.
- MS46322A VNA is also authorized by Intel.
- Anritsu collaborate with GRL (Granite River Labs Inc.) to provide automated solution.
- GRL is one of the authorized test house for TBT by Intel.
  GRL: HQ in Santa Clara US.
- High repeatability one button calibration and Rx test based on Thunderbolt CTS (Compliance Test Specification).

MP1800A #1 Recommended Test Equipment

2.2.3 Pattern Generator

Generate Thunderbolt signal with a variety of patterns, clock jitter, data waveform (eye diagram) and amplitude characteristics.

Required Test Equipment Capabilities

- Data rates ≥ 20.625 Gbps
- Data patterns: PRBS15, PRBS31, Square wave
- Differential swing range: 0 – 2Vp-p in 10mV steps
- Rise Time ≥ 10 ps (20%-80%)
- Intrinsic jitter ≤ 400 fS RMS

Recommended Test Equipment #1

- Anritsu MP1800A
  - MP1800A Signal Quality Analyzer
  - MP1800A-002 Ethernet
  - MP1800A-007 OS Upgrade to Windows7
  - MP1800A-014 2-Slot for PPG and/or ED
  - MP1800A-032 32Gbit/s PPG and/or ED support
  - MU181000A 12.5GHz Synthesizer
  - MU181000A-001 Jitter modulation
  - MU181500B Jitter Modulation Source
  - MU183020A 28G/32G bit/s PPG
  - MU183020A-012 1ch 2V Data Output
  - MU183020A-030 1ch Data Delay
  - MP1825B 4Tap Emphasis
  - MP1825B-002 28Gbit/s operation
  - J1551A Coaxial Skew match cable (0.8m, K connector)
  - J1439A Coaxial Cable 0.8m, K connector
  - J1611A Coaxial Cable 1.3m, K connector

2.2.4 Network Analyzer

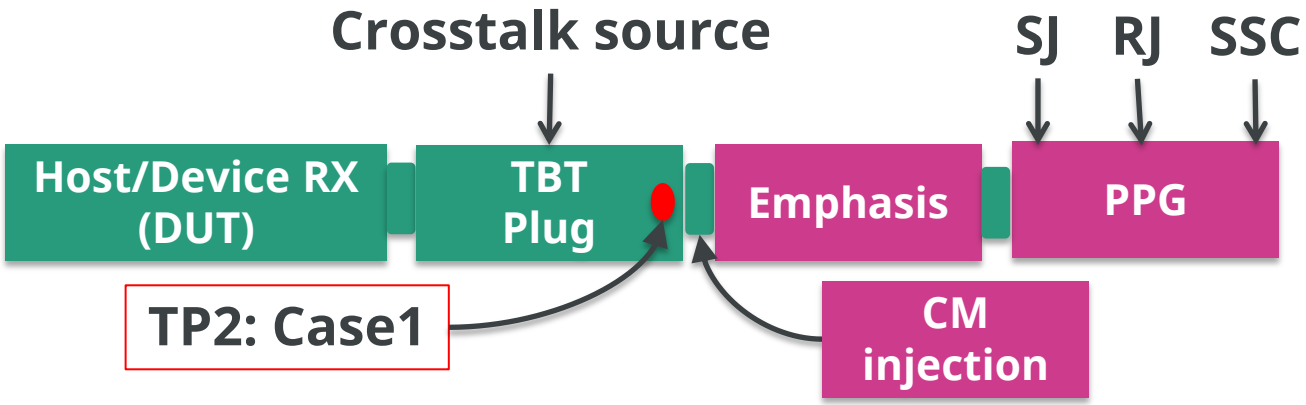
Required Test Equipment Capabilities

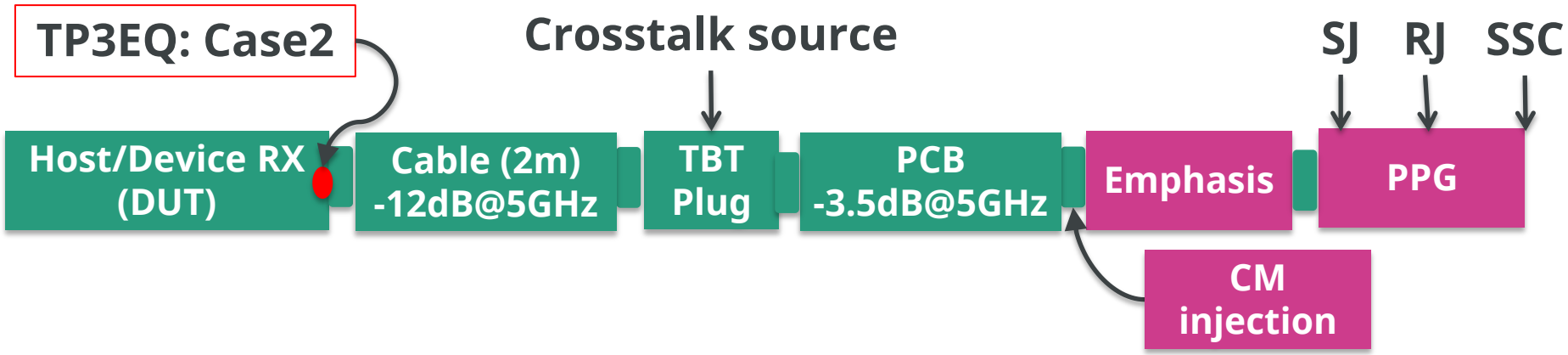
- 2 ports used simultaneously
- At least 1MHz – 13GHz bandwidth
- Dynamic range > 50db

Recommended Test Equipment #3

- Anritsu MS46322A VNA
- Option: MS46322A-020

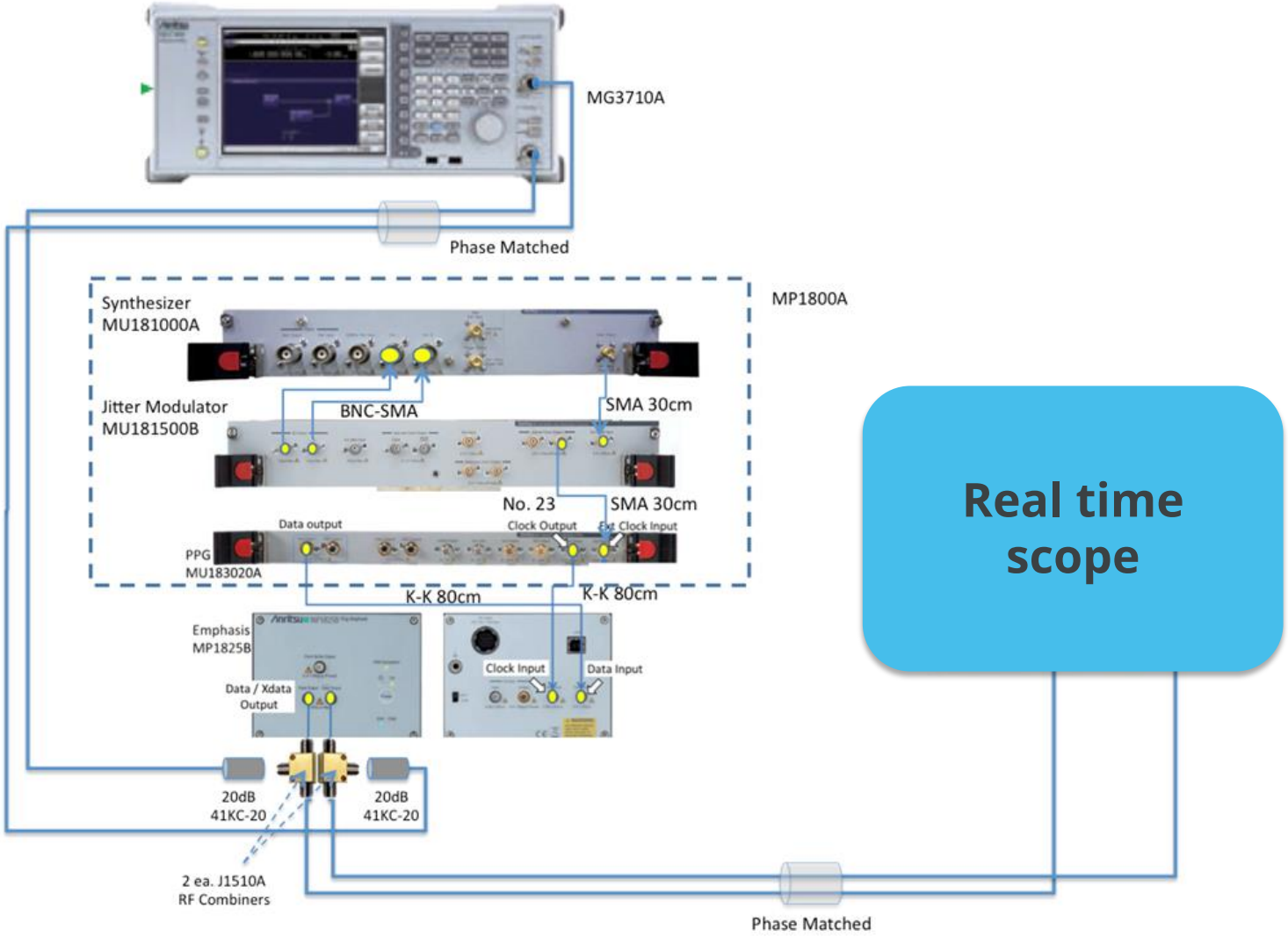
Thunderbolt Receiver tolerance test setup





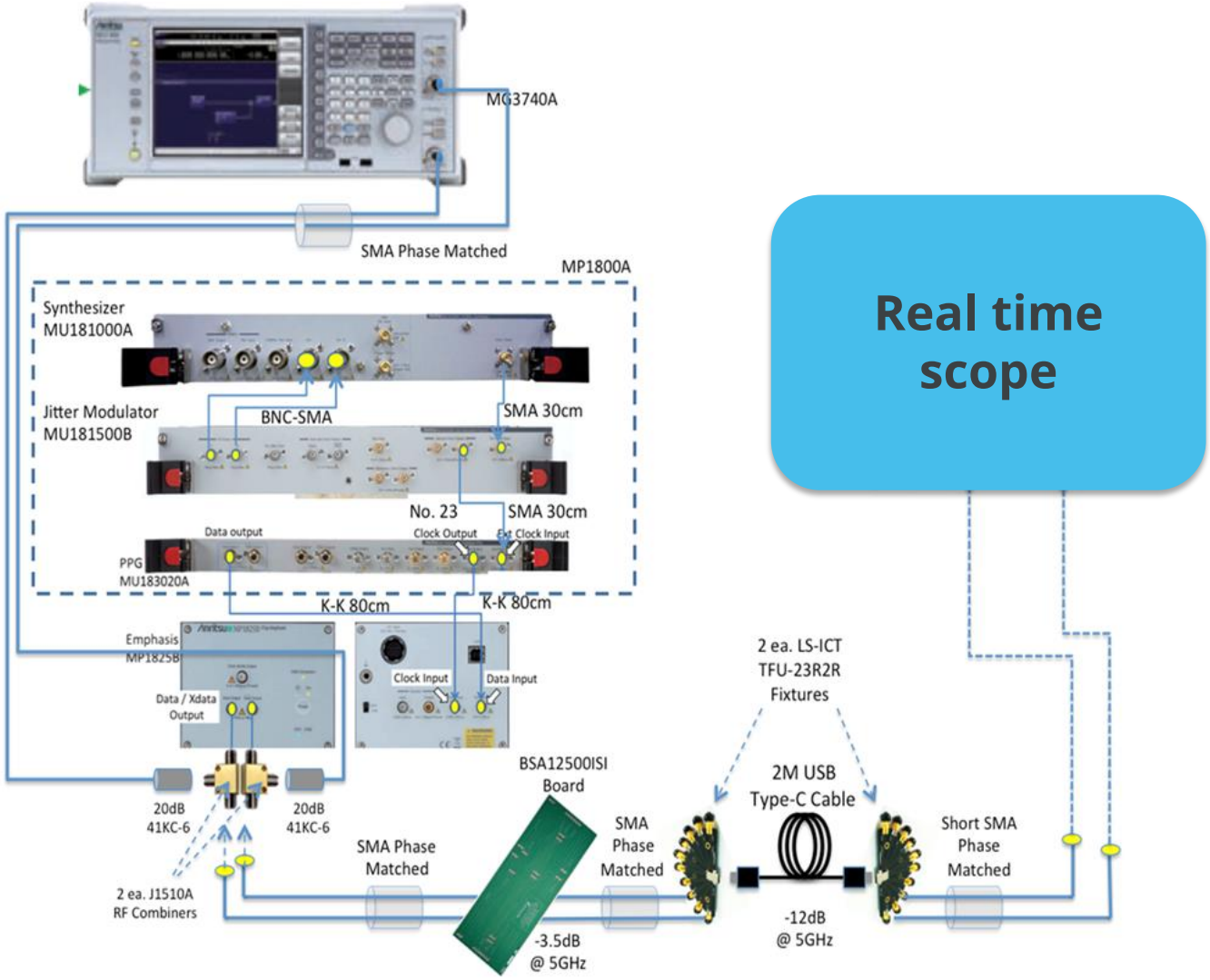
Thunderbolt Receiver tolerance calibration setup

Test case 1 (TP2)



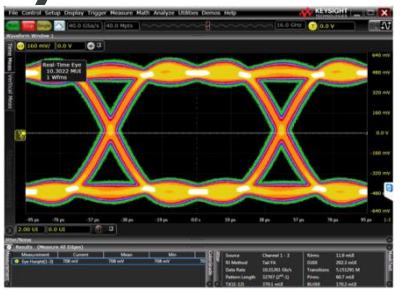
Thunderbolt Receiver tolerance calibration setup

Test case 2 (TP3EQ)

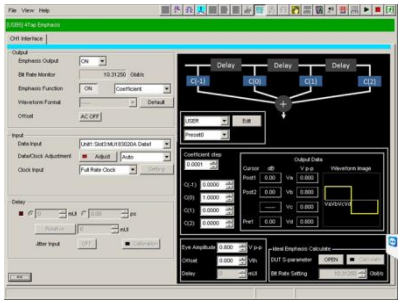


Thunderbolt calibration procedure (1/2)

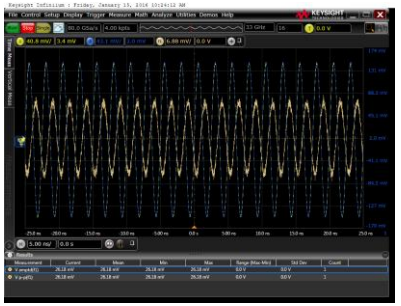
1. Set inner eye amplitude (700 mVpp differential)



2. Find minimum DDJ from 16 presets for emphasis



3. CM noise phase adjustment



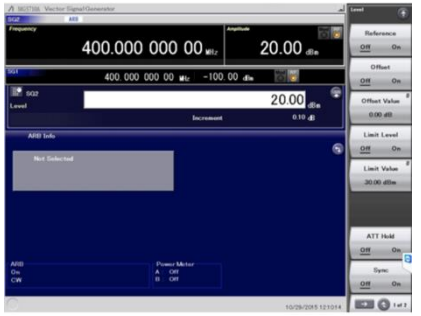
Thunderbolt calibration procedure (2/2)

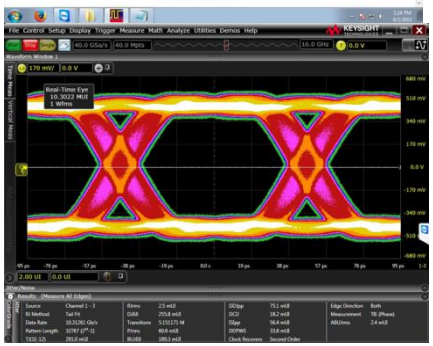
4. CM noise
   During CM calibration, MP1825B output set to off.
   After calibrated CM, CM should be turn off.

5. RJ calibration
   Only RJ set to on during RJ calibration.

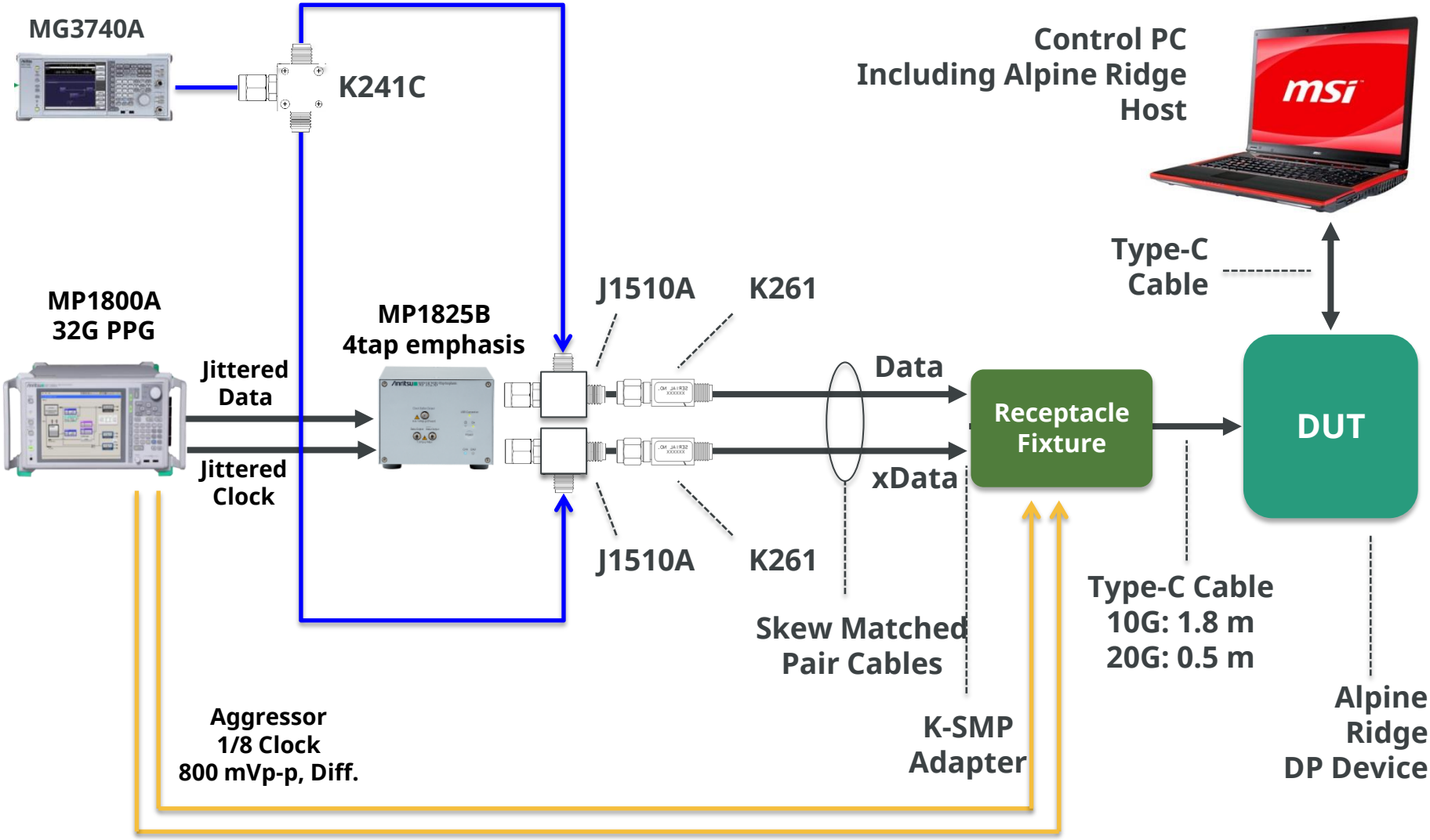
6. SJ calibration
   Calibrate at 5 different SJ frequencies
   Only SJ set to on during SJ calibration.

7. TJ calibration
   Set calibrated CM, RJ and SJ value on.
   Final value should be adjusted by RJ value.
   Adjusted TJ values should be saved respectively.



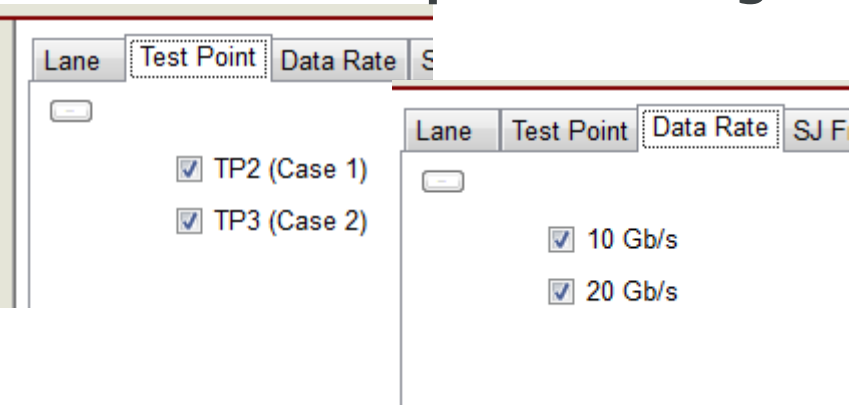


TBT3 Rx test configuration at TP3EQ

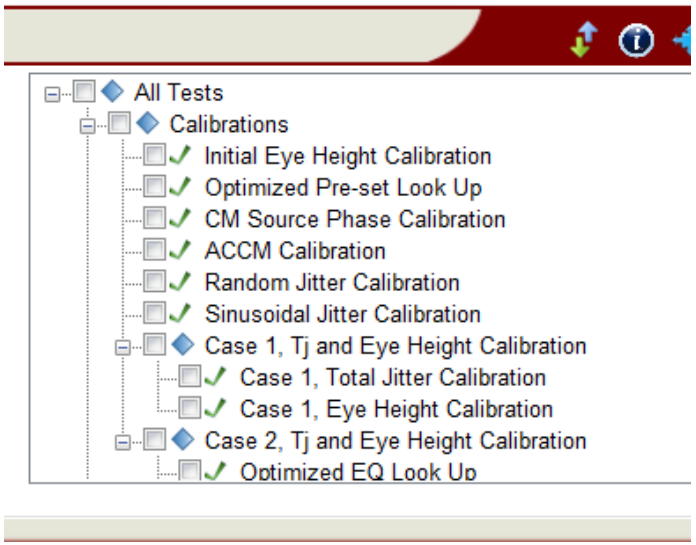


Thunderbolt automated test solution by GRL

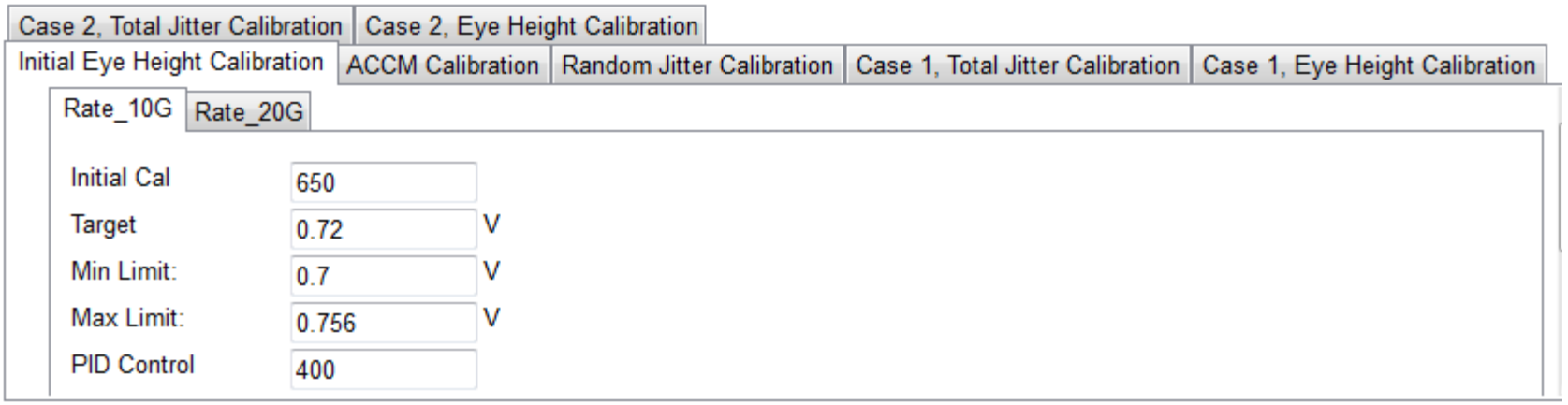
Test point settings



Calibration & Test item



Target values for each settings



Agenda

1. TBT solution
2. **USB solution**
3. PCIe solution

USB 3.1 Gen1 & Gen2 Solution

What is USB3.1?

- New connector: Type C
- Two speed (Gen1: 5Gbps, Gen2: 10Gbps)
- Part of Intel TBT chip (Alpine Ridge)

Anritsu solution

- Link Generation (MX183000A)
- Automated calibration and JTOL (GRL)
- USB Adaptor with BER measurement function

Features ➔

Simple, easy Go / No Go test
Support USB3.1 Gen1 & Gen2 Host / Device receiver test
Full automatic calibration and test in loopback mode
Receiver test with compliance test pattern

Test procedure

1. Calibrating stressed waveform by GRL software

2. Setting DUT in loopback mode by MX183000A software

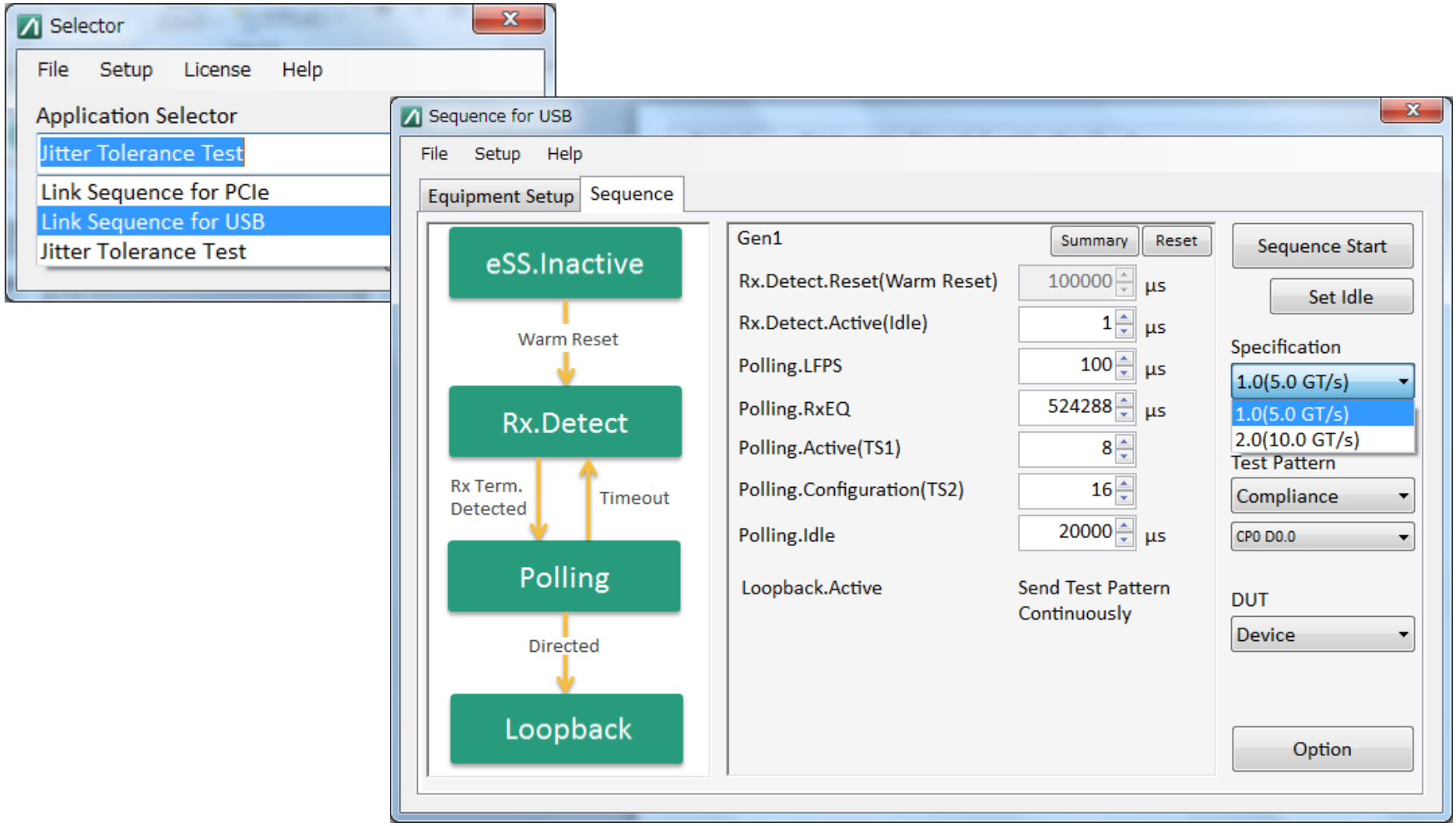
   LFPS (Low Frequency Periodic Signaling)
   Low Freq (10M-20Mbps) communication between USB devices.
   Change USB internal state (LTSSM) to loopback

   For Rx tolerance test, DUT must be in loopback state.
   MX183000A can control state transition automatically.

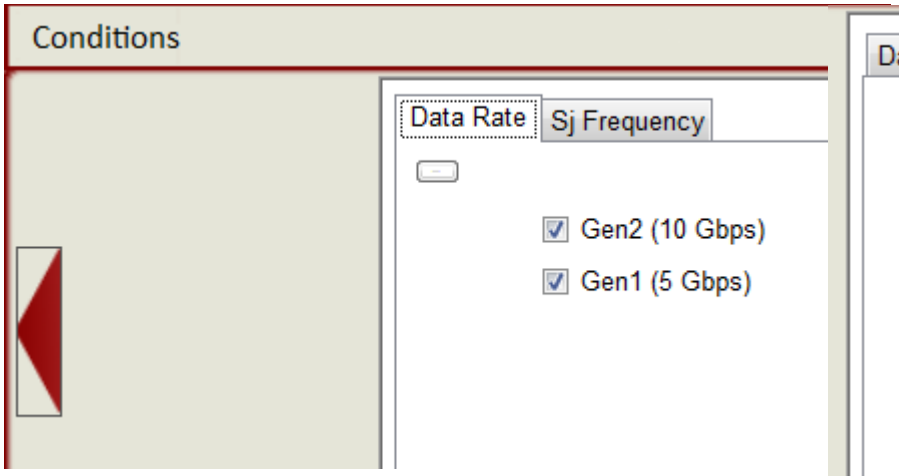
3. BER measurement by external USB adaptor

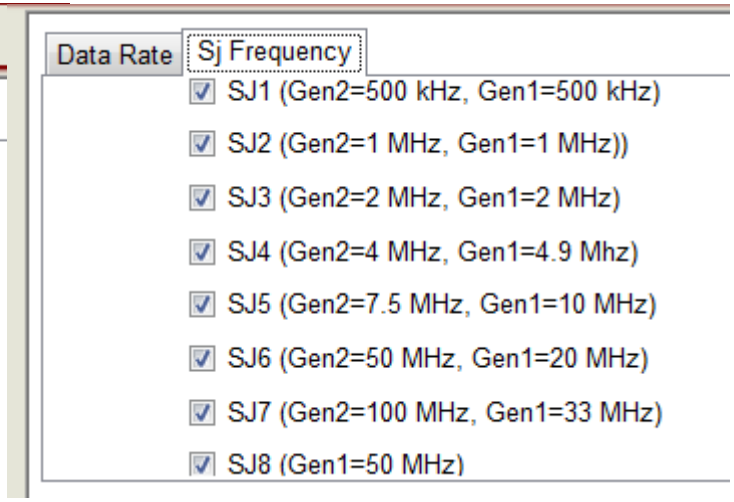
USB 3.1 Gen1&Gen2 loop back link generation

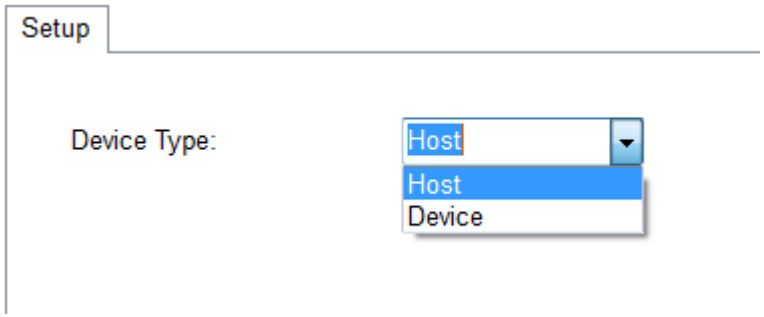
MX183000A

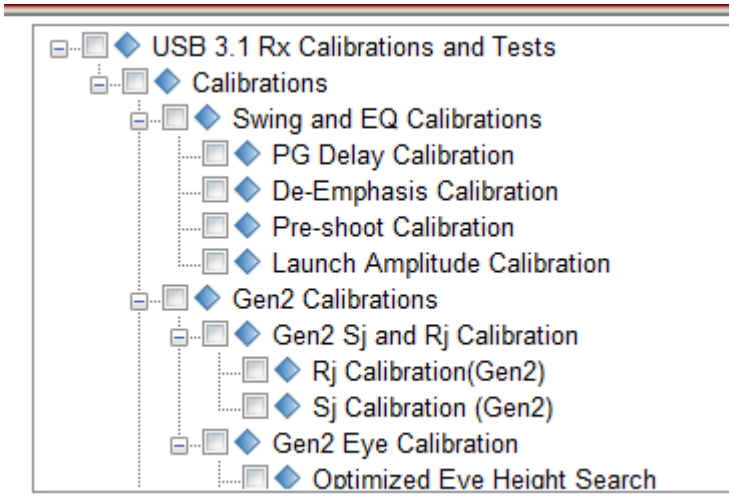


USB 3.1 Gen1&Gen2 Calibration software (GRL)

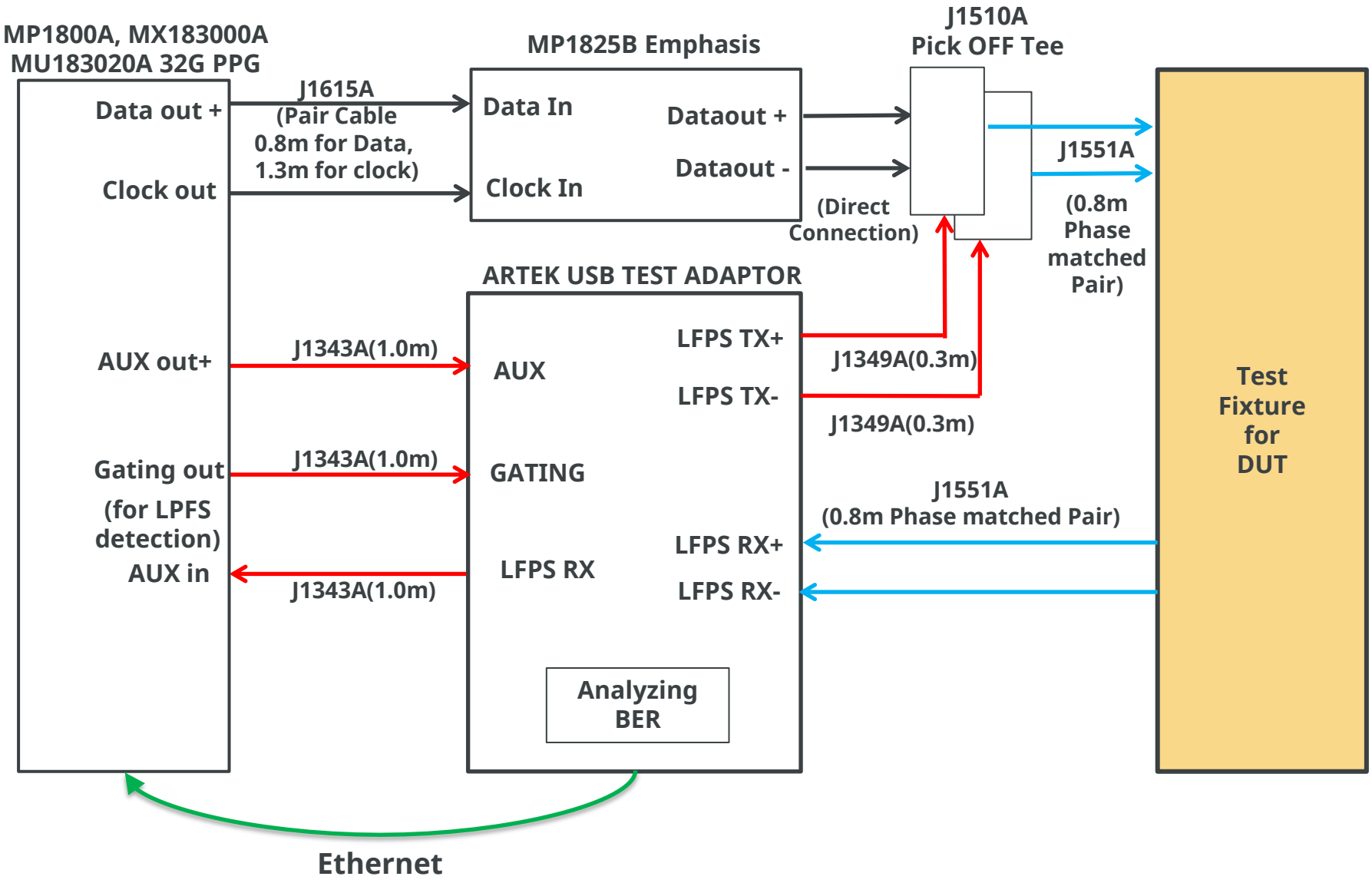








USB compliance test block diagram

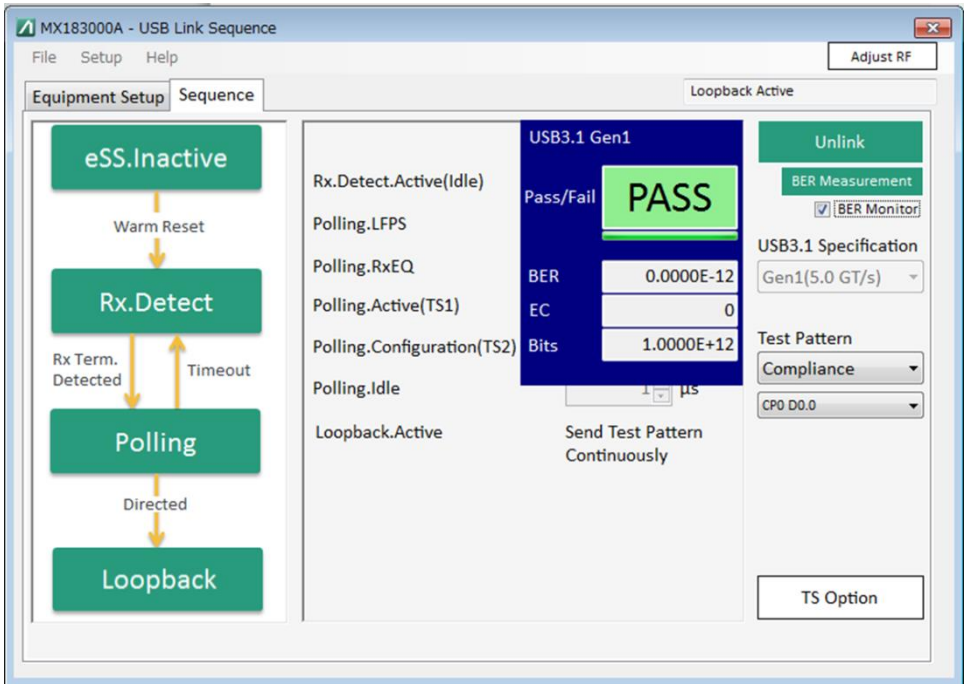


Test points

Gen2 Test points
Confirm error free at 1E-10 (Tentative)
SJ: 17 ps +/- 10% at 50 MHz
17 ps +/- 10% at 7.5 MHz
37 ps +/- 10% at 4.0 MHz
87 ps +/- 5% at 2.0 MHz
203 ps +/- 5% at 1.0 MHz
476 ps +/- 5% at 500 MHz

Gen1 Test points
Confirm error free at 1E-10
SJ: 40 ps +/- 10% at 33 MHz
40 ps +/- 10% at 20 MHz
40 ps +/- 10% at 10 MHz
40 ps +/- 10% at 4.9 MHz
100 ps +/- 5% at 2.0 MHz
200 ps +/- 5% at 1.0 MHz
400 ps +/- 5% at 500 kHz

MX183000A
- BER measurement
- Pass / Fail display



Agenda

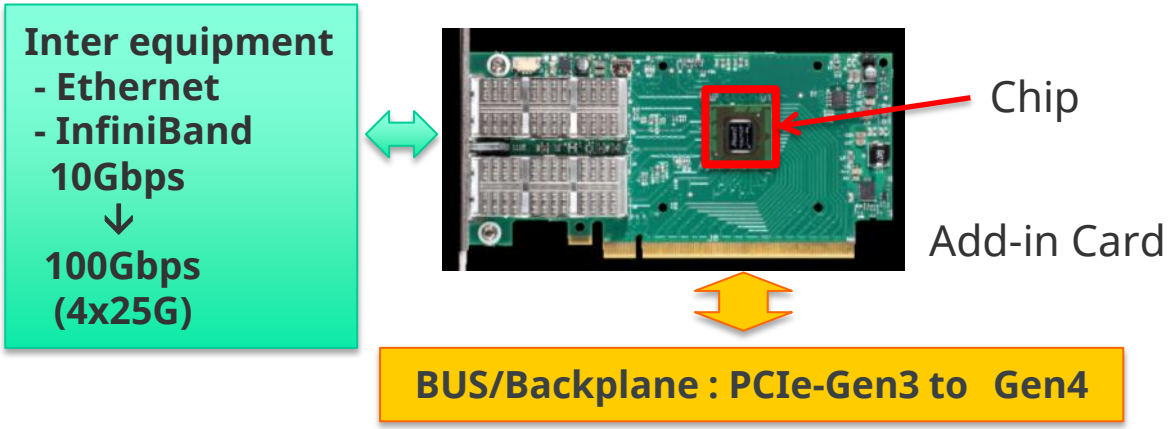
1. TBT solution
2. USB solution
3. **PCIe solution**

PCI Express Solution

Anritsu target market for PCIe

- Multi application interface high speed semiconductor

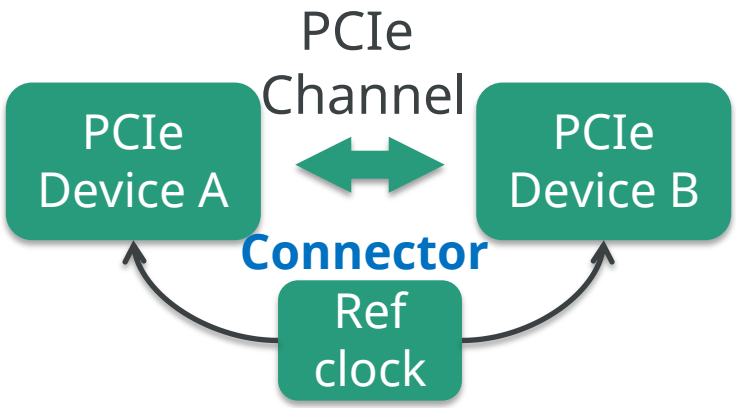
PCIe + 100GbE,
PCIe + Thunderbolt,
PCIe + Thunderbolt + USB3.1



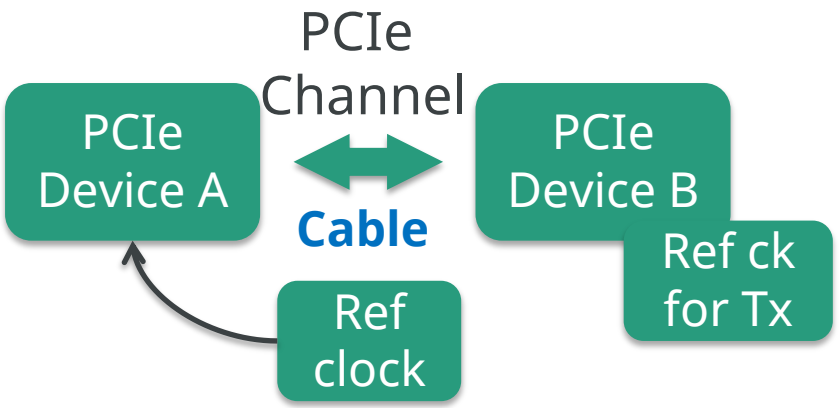
Anritsu solution

- Based on PCIe Gen4 Base specification revision 0.5
- Link capability (MX183000A) and Automated Cal & JTOL (GRL)

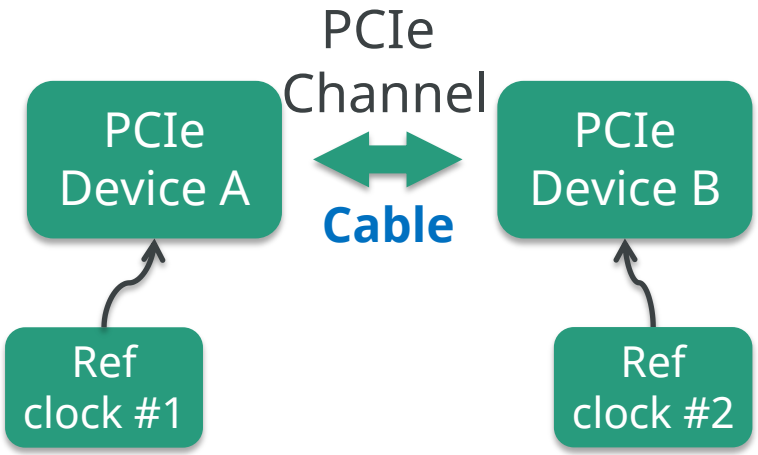
Different PCIe architecture



Case 1: Common Clock Architecture



Case 2: Data Clocked Architecture

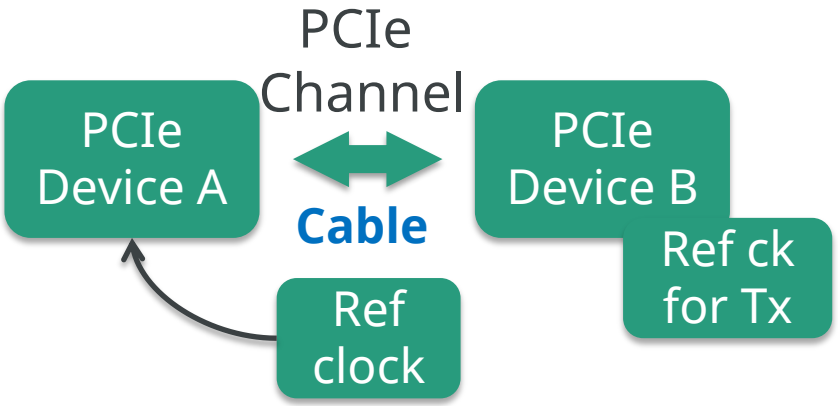


Case 3: Separate Ref Clock Architecture

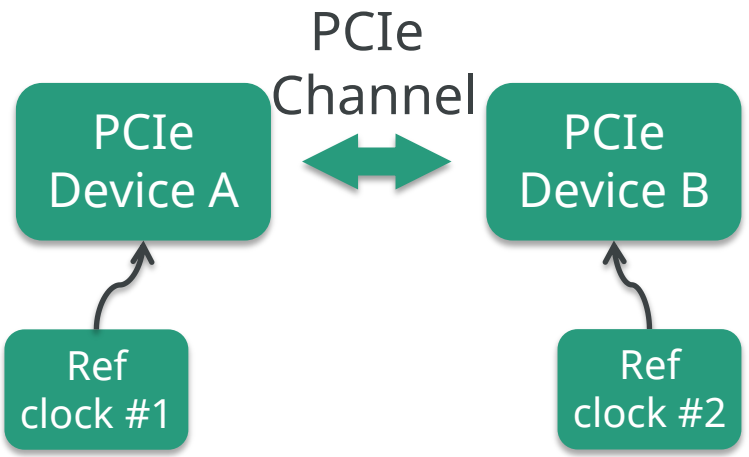
Two improvements will be implemented (1/2)

SKP ordered set

- Different frequency clock between two PCIe devices



Data Clocked Architecture



Separate Ref Clock Architecture

- PCIe TX generates SKP ordered set randomly / automatically

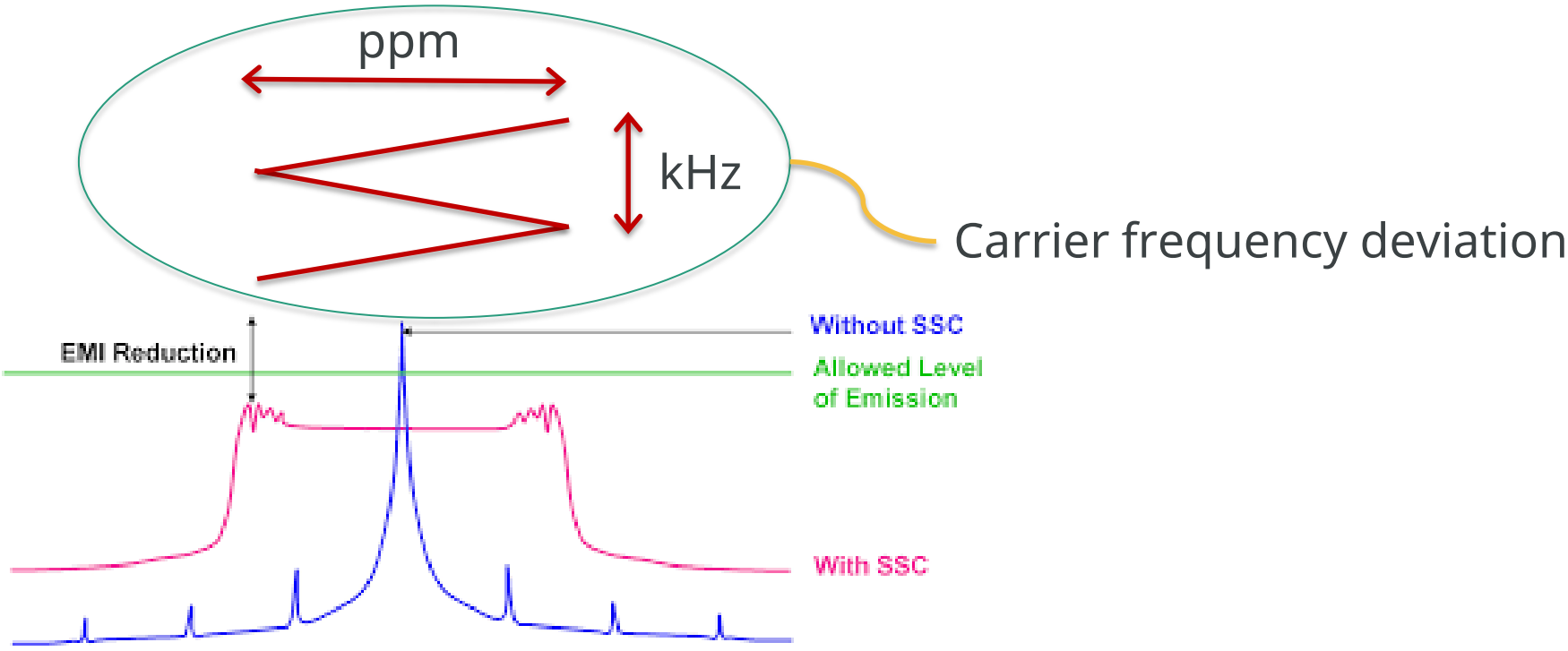
Also in loopback mode, TX generates SKP into transmitting data.
→ ED incoming data is different from PPG transmitted data

➔ Future Anritsu solution will support “SKP ordered set ”.

Two improvements will be implemented (2/2)

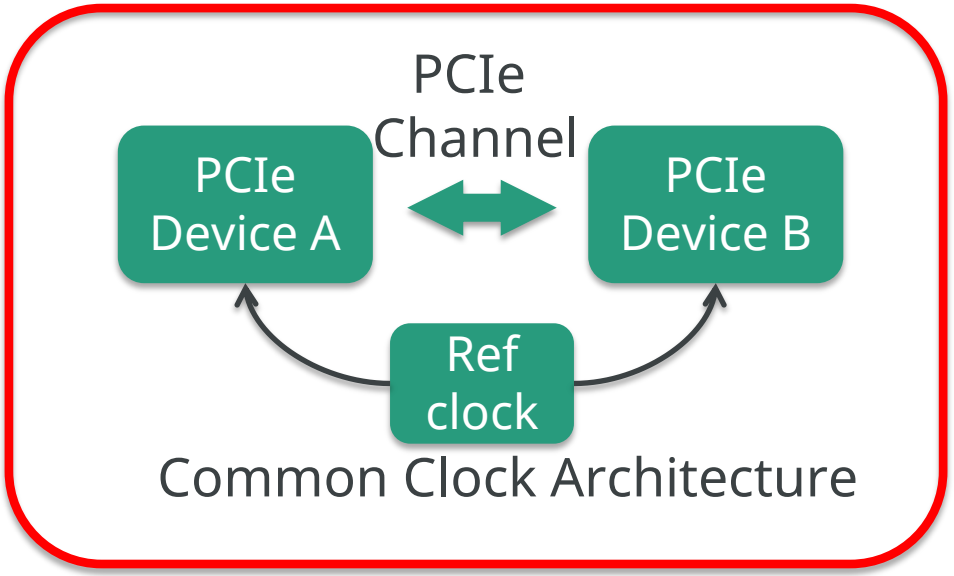
SSC (Spread Spectrum Clocking)

SSC: Change carrier frequency slowly to save EMI
PCIe: 5000 ppm, 33 kHz, Triangle waveform



➔ Future Anritsu solution will support SSC data Error Detection

Current Anritsu PCIe Solution



Current Anritsu Solution
without SSC condition

Anritsu+GRL-PCIE4-BASE-RXA Key Features

Totally Automated PCIe 4.0 Rx Base Spec Test using Anritsu equipment

Perform Receiver Jitter Tolerance test at the push of a button

Reduce technical risk using an industry-accepted calibration methodology

Achieve consistent results with rapid test execution

PCIe Gen4 Calibration points

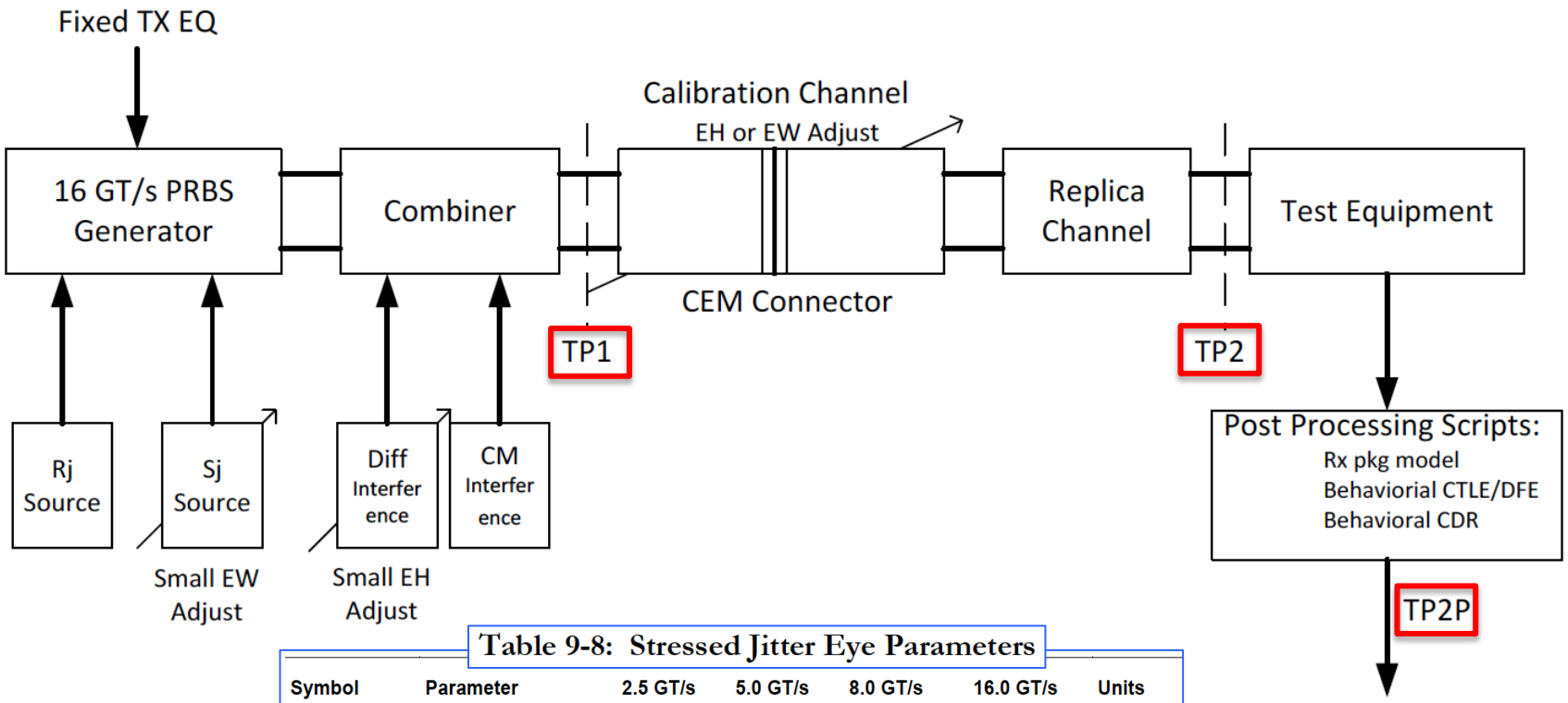
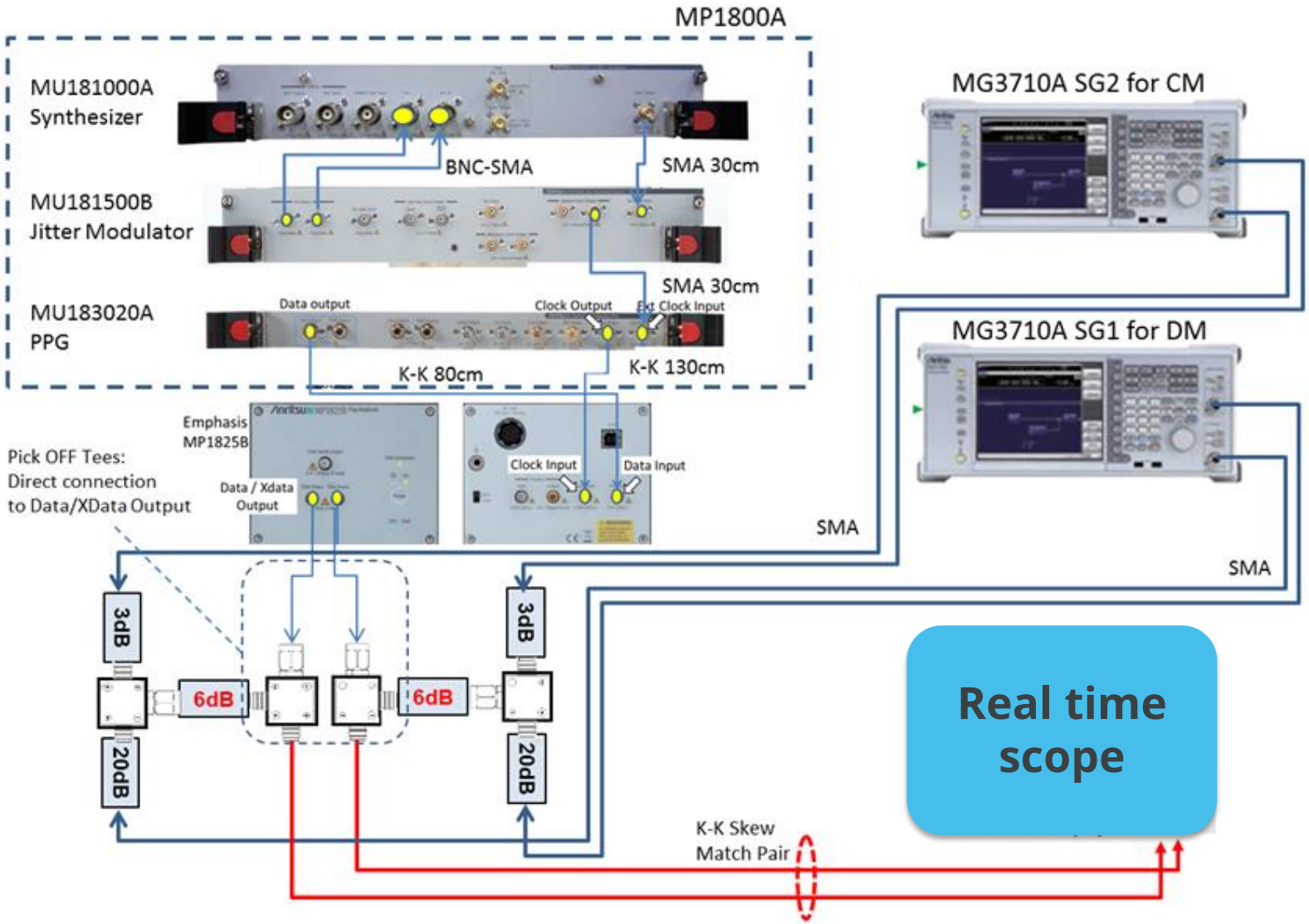


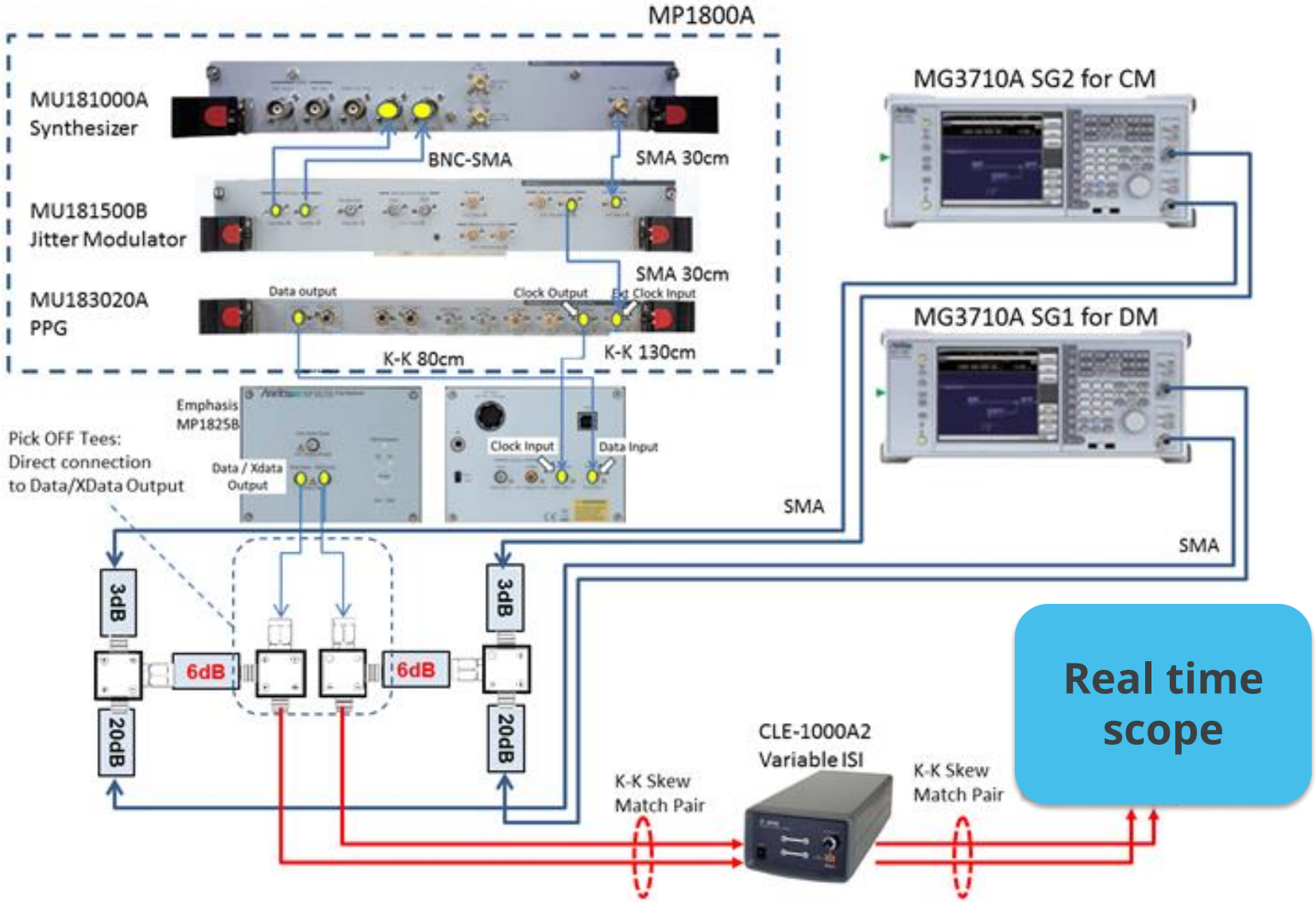
Table 9-8: Stressed Jitter Eye Parameters

Symbol	Parameter	2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	Units
$V_{RX-LAUNCH}$	Generator launch voltage	800-1200	800-1200	800-1200	800-1200	mV PP
T_{RX-UI}	Unit Interval	400	200	125	62.5	ps
T_{RX-ST}	Eye width at TP2P	<0.4	<0.32	0.30	0.30	UI
$T_{RX-ST-SJ}$	Swept Sj	33 KHz spur only	33 KHz spur only	Figure 9-29, Figure 9-30	Figure 9-29, Figure 9-30	UI PP
$T_{RX-ST-RJ}$	Random Jitter	TBD	TBD	3.0 (max)	~1.0 (max)	ps RMS
$V_{RX-DIFF-INT}$	Differential noise	TBD	TBD	TBD	TBD	mV PP
$V_{RX-CM-INT}$	Common mode noise	150	150	150	150	mV PP

PCIe base spec calibration test setup for TP1

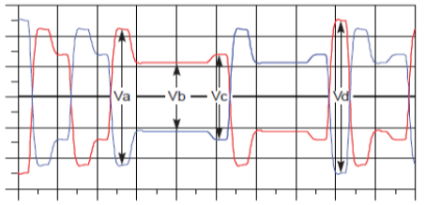


PCIe base spec calibration test setup for TP2

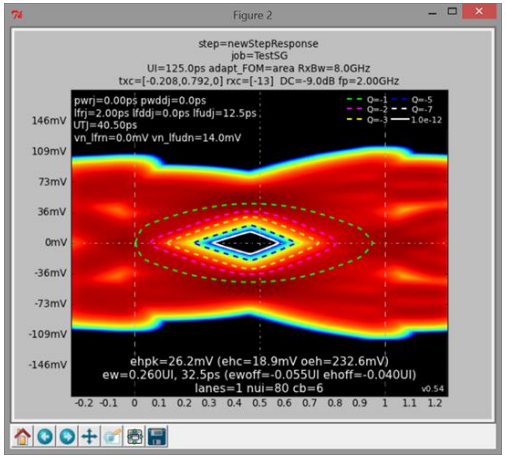


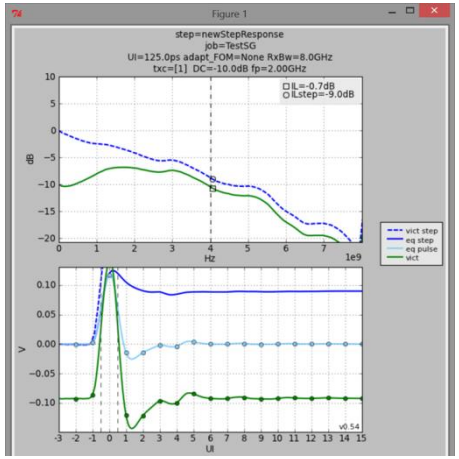
PCIe Gen4 Base spec calibration procedure

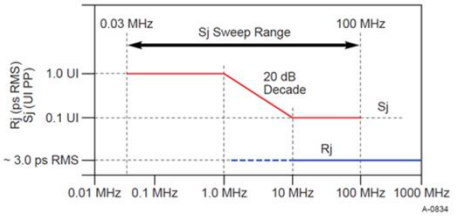
1. Emphasis eye amplitude calibration
2. De-emphasis and Pre-shoot calibration
3. RJ, SJ calibration
4. ISI loss calibration
5. CMI, DMI calibration
6. Stressed eye calibration



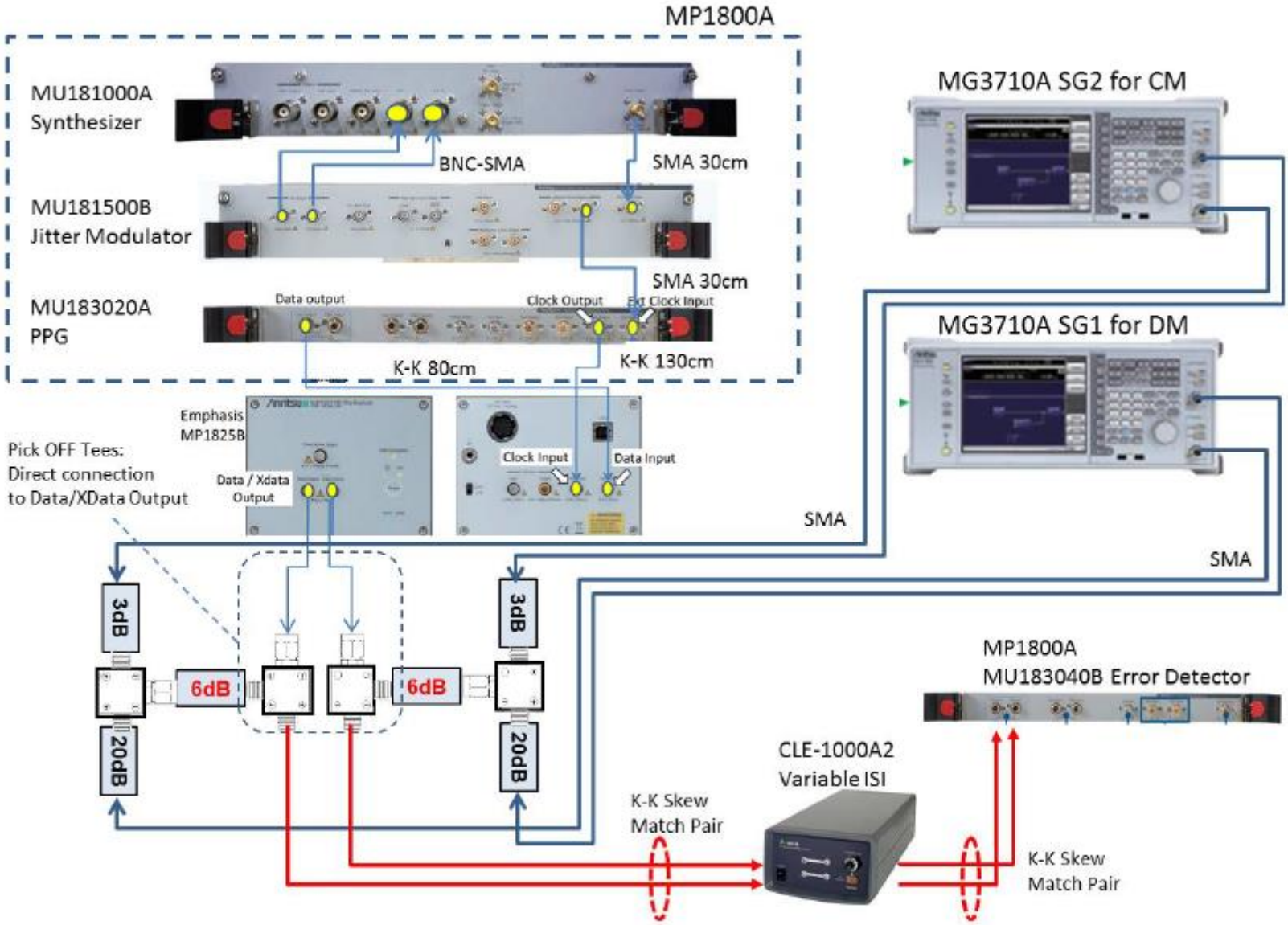
De-emphasis = $20\log_{10}$ Vb/Va
Preshoot = $20\log_{10}$ Vc/Vb
Boost = $20\log_{10}$ Vd/Vb



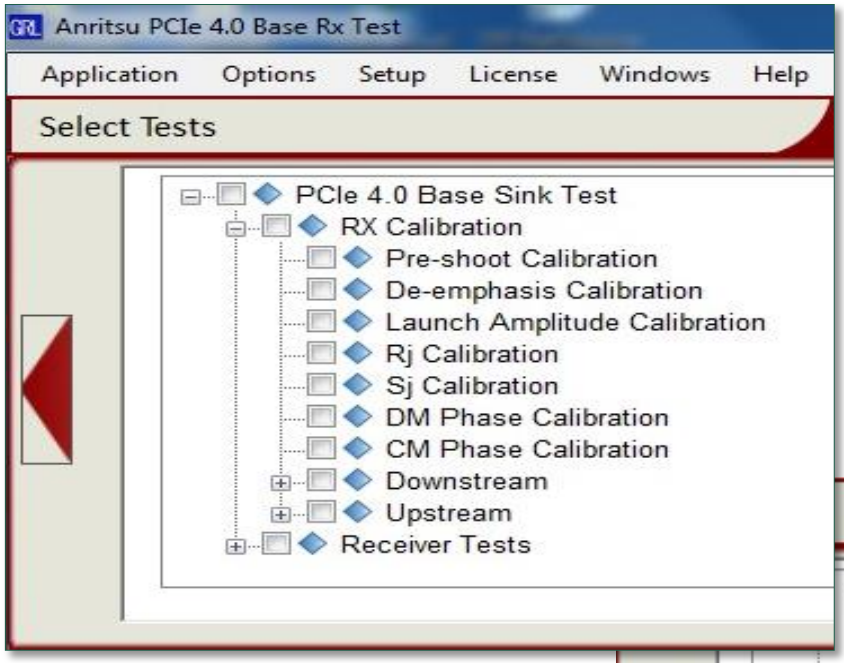




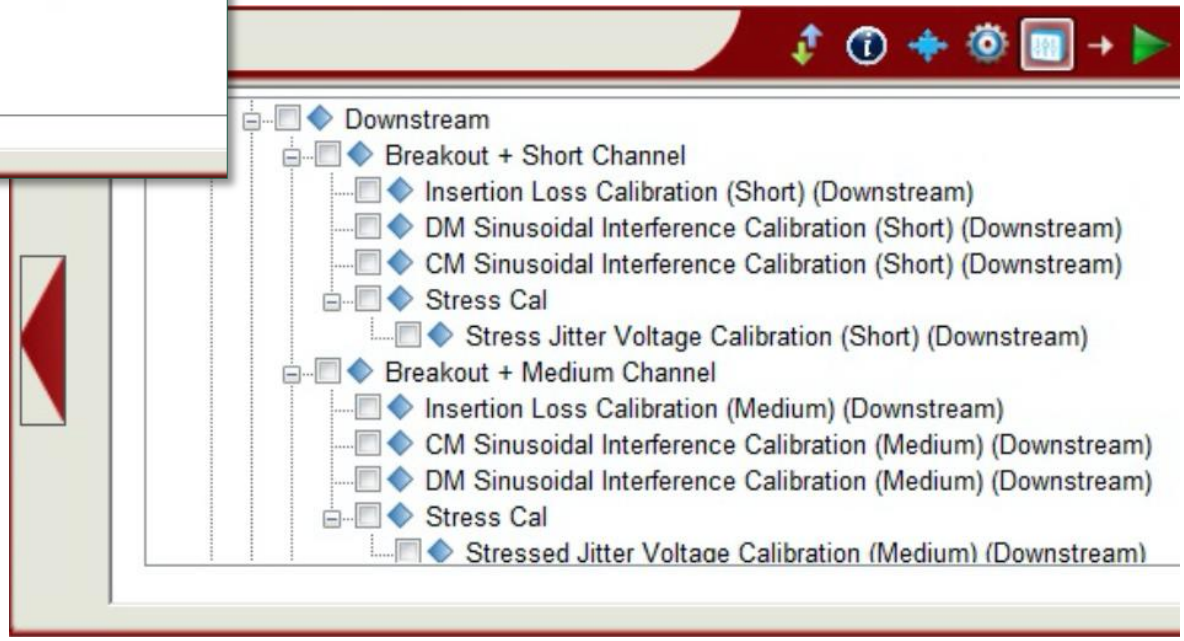
PCIe base spec receiver tolerance test setup



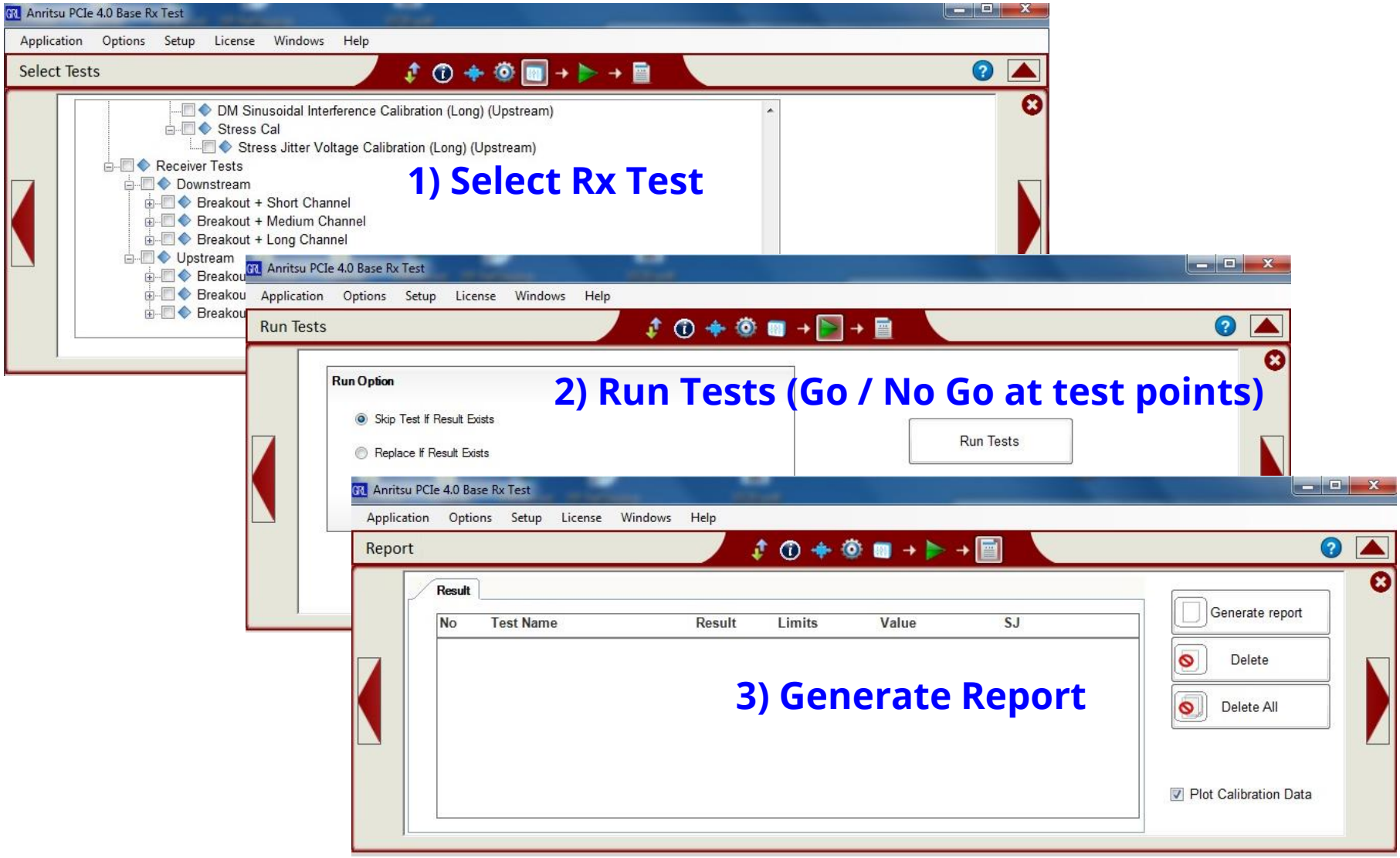
PCIe Gen4 base spec automated solution (GRL)



Test List (Calibration) for PCIe Gen4 including Upstream and Downstream for All TP2 channel type (Short, Medium, Long) calibration

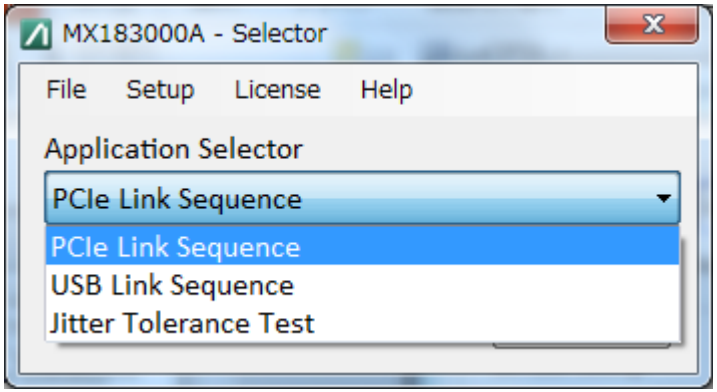


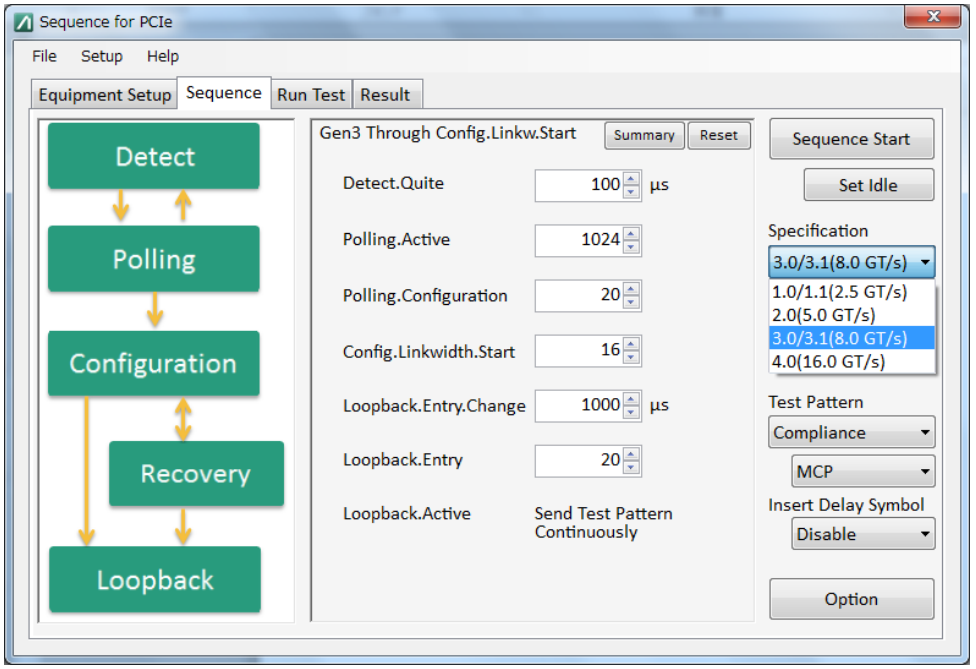
PCIe Gen4 base spec automated solution (GRL)

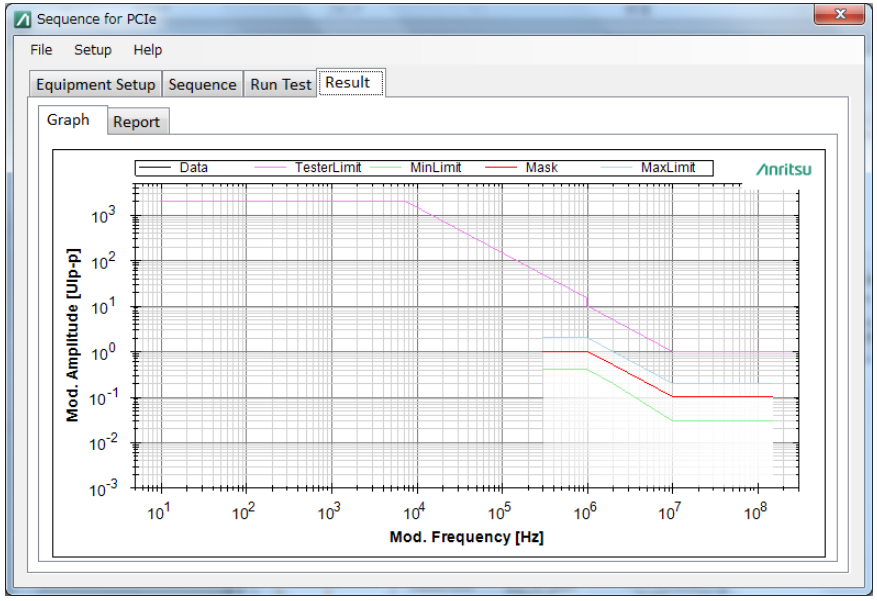


PCIe Gen1 to 4 loop back link generation (Anritsu)

MX183000A



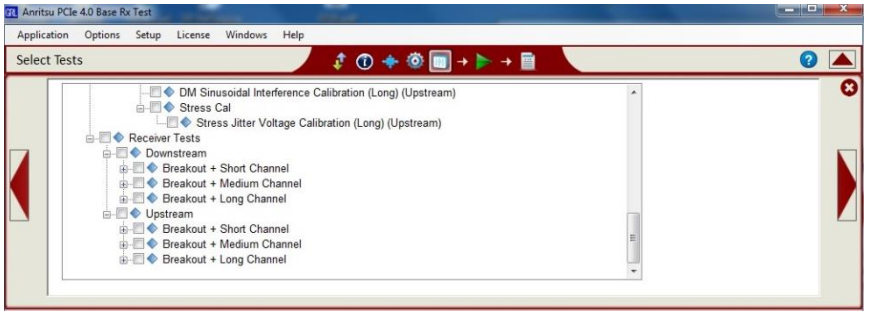




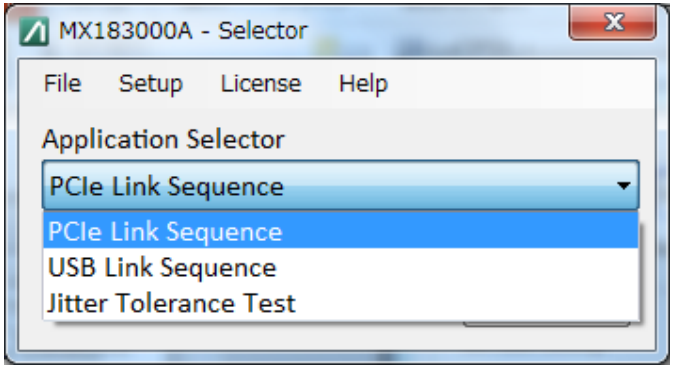
- Sets DUT in loop back mode
- PCIe Gen 1 to Gen4
- Jitter tolerance “margin” test

Anritsu PCIe Solution operation procedure

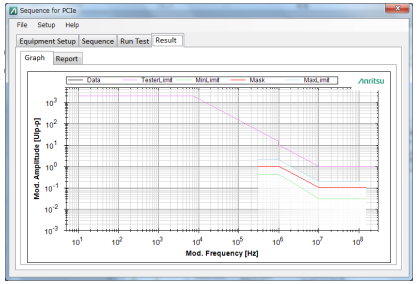
1. Calibrate waveform by GRL SW



2. Set DUT in loop back mode



3. Jitter tolerance test for two option
   - AAA) Anritsu margin test
   - BBB) GRL Go / No Go test



Anritsu / GRL PCIe Solution features

GRL-PCIE4-BASE-RXA Key Features

Automate PCIe 4.0 Rx Base Spec Test using Anritsu equipment

Perform Receiver Jitter Tolerance test at the push of a button

Reduce technical risk using an industry-accepted calibration methodology

Achieve consistent results with rapid test execution

MX183000A Key Features

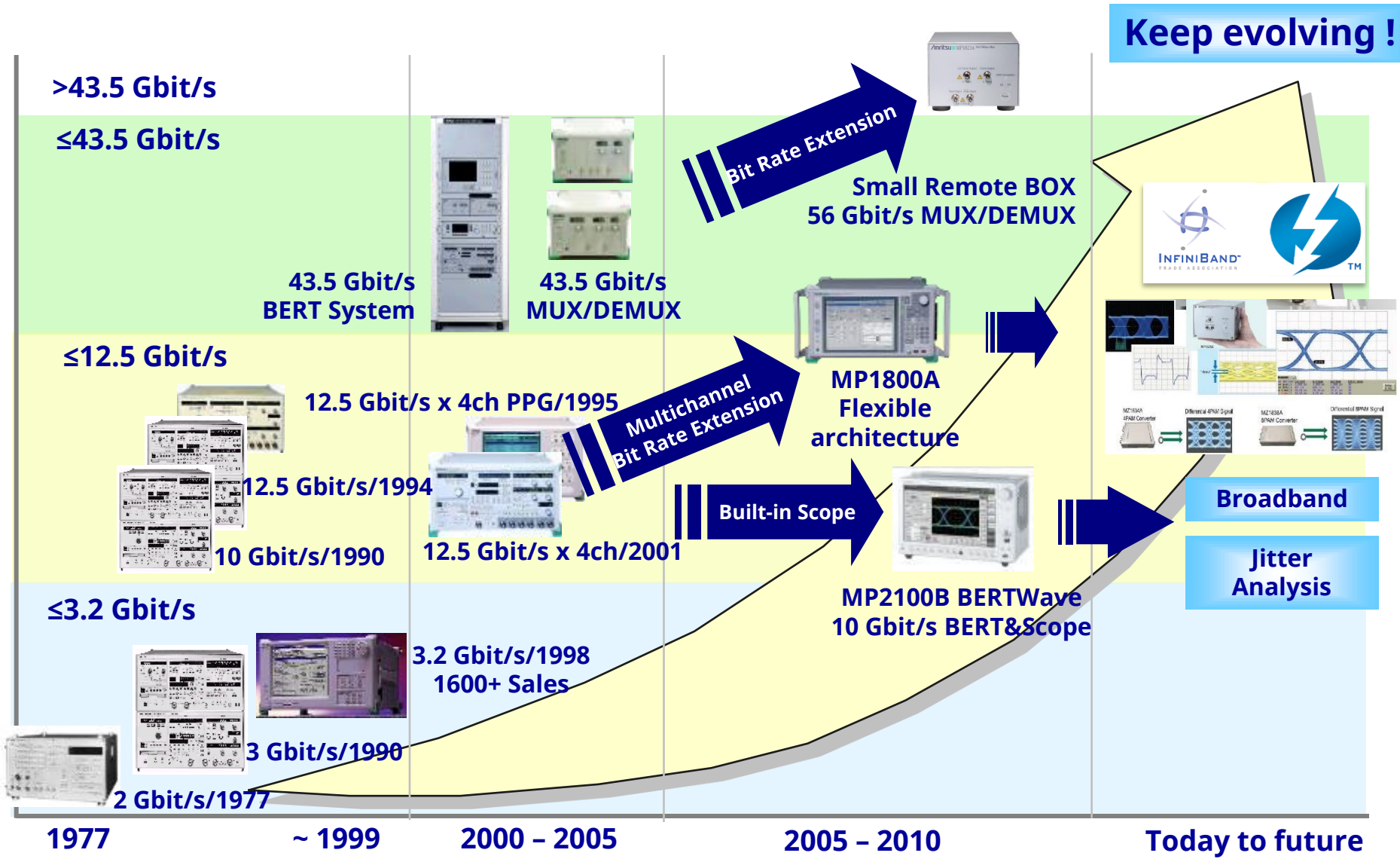
Establish loop back mode for PCIe Gen1 to Gen4
Jitter tolerance margin test
Supporting also USB3.1 Gen1 (5Gbps) & Gen2 (10Gbps)

Application Specifications

- Data Rates: 16 GT/s
- Supported Receiver Test: Common Clock Architecture without SSC
- This application is compatible with:
  - **Keysight 32 GHz** Oscilloscope (DSAX or newer series)
  - **Anritsu MP1800A** Signal Quality Analyzer
  - **Artek CLE-1000 A2** Variable ISI Channel

Appendix

History of Anritsu BERTS



Anritsu Product Lineup

R&D Cutting Edge

Design Verification Test

Manufacturing

Signal Quality Analyzer
MP1800A Series

Solution:

- 10/25/32/64 Gbit/s device tests

Features:

- Easy support for latest applications by adding functions matching customers' TTM due to flexible/scalable modular architecture
- Unique Jitter and Emphasis functions, high sensitivity, built-in Clock Recovery, and PAM signal generation for 32G applications

BERTWave
MP2100B Series

Solution:

- 10 Gbit/s BER tests, EYE Pattern measurements

Features:

- All-in-one solution supporting BERT and Scope
- BERT expansion up to 4 channels
- Fast remote control and high-speed Eye Mask tests
- Compact design (180 mm deep)

Anritsu

envision : ensure

公知 2016-8 MG No. MP1800_32G-E-L-1-(6.00)