58 G/64 Gbaud Multichannel PAM4 BERT
PAM4 PPG MU196020A
PAM4 ED MU196040B  NEW

Signal Quality Analyzer-R
MP1900A Series
Outline of MP1900A Series PAM4 BERT

- Supports bit error rate measurements optimized for high-speed 400 GbE and next-generation 800 GbE interfaces
- High-quality data output waveforms up to 64 Gbaud and high input sensitivity performance provide strong support for testing PAM4 device designs
- All-in-one Jitter Addition, Clock Recovery, Emphasis, NRZ/PAM3/PAM4 Pattern Editing, SER functions, etc.
- Easily configured, high-reproducibility PAM4 measurement solution

MP1900A PAM4 Target Applications
200/400/800 GbE, CEI-56G/112G, InfiniBand HDR, 64G Fibre Channel
MP1900A PAM4 BERT Features

- All-in-one, high-reproducibility, easily configured test solution
- High-quality waveforms for more accurate measurement
- Easy, low-cost, future-proof expandability supporting high bit rates and multichannels
PAM4 All-in-One BERT Solution

Easy-to-use and configure all-in-one solution with high reproducibility, helping cut test times

Typ. 36 mV at 53.125 G
High Input Sensitivity

ED w/ Built-in Clock
Recovery and Equalizer

SER/BER, Capture,
Logging functions

PAM4 ED
MU196040B

PAM4 PPG
MU196020A

No External Equipment, Compact
Module with Built-in PAM4
Functions

High-Quality 64G PAM4
Waveforms with Variable
Emphasis/Linearity Functions

DUT
High-Quality Waveform PAM4 PPG MU196020A

Best-in-class waveform quality with low Intrinsic Jitter (typ. 170 fs (rms) and fast Tr/Tf (typ. 8.5 ps) for more accurate evaluation of actual DUT performance

64.2 Gbaud

53.125 Gbaud

26.5625 Gbaud

Differential 1.4 Vp-p, PRBS13Q pattern, J1789A 40-cm cable + 70 GHz Scope
116 Gbit/s PAM4 Best Level High-Sensitivity Input Performance

High sensitivity input of 36 mV (typical at 53.125 Gbaud) simplifies previously difficult PAM4 error troubleshooting measurements.

**Error-Free** at 53.125 Gbaud
Best level PAM4 sensitivity

Typ. 36 mV EH/ Eye
Multichannel Support and Expandability (1/2)

One MP1900A PPG supports up to 4ch for 400 GbE (53 Gbaud x 4 Lanes), and faster evaluations, helping cut future support upgrade costs.

- **Channel Synchronization**

  One MP1900A unit supports synchronous output for up to 4ch; two units support up to 8ch.

  *Future support for 8ch

<table>
<thead>
<tr>
<th>Channel</th>
<th>a1</th>
<th>a2</th>
<th>a3</th>
<th>a4</th>
<th>a5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ch1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ch2</td>
<td></td>
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<tr>
<td>Ch3</td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Ch4</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

- **2ch Combination (NRZ)**

  Supports shift to “a1b1 a2b2 . . .” pattern

<table>
<thead>
<tr>
<th>Channel</th>
<th>a1</th>
<th>a2</th>
<th>a3</th>
<th>a4</th>
<th>a5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ch1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ch2</td>
<td>b1</td>
<td>b2</td>
<td>b3</td>
<td>b4</td>
<td>b5</td>
</tr>
</tbody>
</table>

- **4-Lane DUT (Driver + E/O) Measurement Example**
Multichannel Support and Expandability (2/2)

Expanded support for 800G using 8ch synchronization function (4ch x 53.125 Gbaud PAM4 x two MP1900A units)
Supports QSFP-DD transceiver FEC evaluation using 8-lane FEC Pattern Generation function

Synchronized 8-lane FEC Pattern

400G QSFP-DD, OSFP Optical Transceiver or
800G Next Generation Transceiver
Jitter Tolerance Measurement Function

Supports PAM4 Jitter Tolerance test using just one unit. A measurement system to help cut measurement time is configured easily by combining the Jitter/Noise Addition function, built-in Clock Recovery function, and Jitter Tolerance MX183000A-PL001 software.
When the DUT has a built-in bit error counter, combination with the MP1900A PPG makes it easy to configure a highly cost-effective Jitter Tolerance measurement environment.
Multilane FEC Evaluation

FEC can be evaluated by combining FEC pattern generation with error insertion, and reading the DUT bit error count.
PAM4 PPG/ED Specifications

PAM4 PPG MU196020A

- Baud-rate: 2.4 Gbaud to 32.1/58.2/64.2 Gbaud
- Output amplitude: 0.14 Vp-p to 1.6 Vp-p (Differential)
- Emphasis: 4Tap, ±20 dB (1 post/2 pre-cursor), ISI/Channel Emulator
- Intrinsic jitter(rms): 170 fs (typ., NRZ)
- Tr/Tf (20-80%): 8.5 ps (typ., NRZ)
- Multichannel synchronization
- FEC pattern generation

PAM4 ED MU196040B

- Baud-rate: 2.4 Gbaud to 32.1/58.2 Gbaud PAM4 and 64.2 Gbaud NRZ
- Input amplitude (max.): 1.0 Vp-p (NRZ, PAM4)
- Input sensitivity(Eye Height) : 23 mV (typ., 26.5625 Gbaud), 36 mV (typ., 53.125 Gbaud)
- Built-in Clock Recovery: 2.4 G to 29 Gbaud or 32.1 Gbaud/ 51 G to 58.2 Gbaud extension
- Analog bandwidth: >40 GHz (nominal)
- Built-in Equalizer: Low Frequency Equalizer(2 dB)+DFE(1.4 dB)
- SER measurement, logic error analysis using Diagnostics Mode, Capture, Logging function
PAM4 PPG Functions and Performance
PAM4/NRZ Data Output

Supports next-generation applications over 50 Gbaud, such as 400 GbE, CEI-112G, etc.

Typical Output Waveform (J1789A 40-cm Cable, 1400-mV Differential, PRBS15)
Easy PAM4 Level Control

Control Baud Rate, Level, Offset, Half Period Jitter, and Delay from one screen

- PAM4 Total Amplitude setting
- Independent PAM4 3Eye Amplitude control with voltage and % values
- Easy return to equal level using [Even] button

Level Control Reference Waveform
Linearity and Emphasis Controls

Supports TOSA device evaluations and stressed input tests using various channel insertion losses

MU196020A
PAM4 PPG

53G, Post1 Emphasis control

53G, Linearity control

53G, Pre1 Emphasis control
ISI, Channel Emulator

Shorter development period by eliminating need for multiple test PC boards with simple and high-reproducibility design tests of high-speed device channel loss dependency

- **Manual Setting:** Correct signal for target Eye Height/Width using 10Tap Emphasis function
- **Channel Emulator:** Emulate S2P and S4P loss insertion, and perform Emphasis compensation
- **ISI:** Emulate ISI using CEI-28G/25G Nyquist frequency loss setting

**Emulates Channel Loss**

or

**Generates Loss Calibration Signal**

(ISI option)

Typical ISI Function Waveforms

NRZ CEI-28G 14-dB Loss

PAM4 26.6G 4-dB Loss

PAM4 26.6G 6-dB Loss
PAM4 Test Patterns (1/2)

Supports PAM4 test patterns specified by 200 and 400 GbE standards

<table>
<thead>
<tr>
<th>Supported Test Patterns</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CEI</strong></td>
</tr>
<tr>
<td>QPRBS13-CEI, QPRBS31-CEI</td>
</tr>
<tr>
<td><strong>IEEE</strong></td>
</tr>
<tr>
<td>IEEE802.3bs/cd: PRBS13Q, PRBS31Q, SSPRQ, Square Wave</td>
</tr>
<tr>
<td>IEEE802.3bj: QPRBS13, JP03A, JP03B, Transmitter Linearity</td>
</tr>
<tr>
<td><strong>RS-FEC</strong></td>
</tr>
<tr>
<td>RS-FEC Scrambled Idle 100G 1 Lane (53.125 Gbaud, 100GBASE-DR)</td>
</tr>
<tr>
<td>RS-FEC Scrambled Idle 400G 4 Lanes (53.125 Gbaud, 400GBASE-DR4)</td>
</tr>
<tr>
<td>RS-FEC Scrambled Idle 400G 8 Lanes (26.5625 Gbaud, 400GBASE-FR8/LR8)</td>
</tr>
<tr>
<td><strong>InfiniBand</strong></td>
</tr>
<tr>
<td>PRBS13Q (InfiniBand), PRBS23Q, PRBS31Q(InfiniBand)</td>
</tr>
<tr>
<td><strong>Fibre Channel</strong></td>
</tr>
<tr>
<td>PRBS31Q (Fibre Channel)</td>
</tr>
<tr>
<td><strong>General Purpose</strong></td>
</tr>
<tr>
<td>PRBS7, 9, 10, 11, 13, 15, 20, 23, 31, Data (User defined) 4 to 256 Msymbol</td>
</tr>
</tbody>
</table>

Edit Data pattern using PAM4 symbol 0, 1, 2, and 3 values.
PAM4 Test Patterns (2/2)

- BER measurement for different pattern generation methods depending on DSPs
- Efficient detection of pattern generation circuit differences as well as logic errors, such as inverted logic and bit skew

![Diagram showing pattern generation methods and their components](image-url)

- Pattern Generation
- MSB and LSB Inverted Logic (before/after Gray Coding)
- Gray Coding
- 1/(1+D) Mod4 Pre-Coding
- Set bit skew between MSB and LSB
PAM4 Error Insertion Function

With PAM4, not only do errors occur at single level changes, there are also cases where double level changes occur due to MSB errors. Using the [Error Addition] tab to insert errors in each of these cases helps confirm communications and inspection of error results.

- **LSB Error Insertion**
  - Level 0 to 1: 00 → 01
  - Level 1 to 0: 01 → 00
  - Level 2 to 3: 10 → 11
  - Level 3 to 2: 11 → 10

- **MSB Error Insertion**
  - Level 0 to 2: 00 → 10
  - Level 1 to 3: 01 → 11
  - Level 2 to 0: 10 → 00
  - Level 3 to 1: 11 → 01
Cable Settings for Monitoring

Adjusts Emphasis to automatically correct loss of 80-cm cable connecting separate DUT

Using 40-cm cable @53G

- J1789A 40-cm cable best for evaluating this waveform
- Closed Eye opening with long cable (ex. 80-cm cable)
- Can automatically calibrate settings for effect of 80-cm cable

Using 80-cm cable @53G

Cable for data output setting: J1789A 0.4 m
PAM4 ED Functions and Performance
Outline of 116-Gbit/s PAM4 Error Detector for 400GbE/800GbE

- **High-performance BERT for 116-Gbit/s PAM4 error-free measurement**
  Simplify previously difficult PAM4 error troubleshooting
- **Industry-best high input sensitivity of 36 mV EH@53.125 Gbaud**
  Support more accurate evaluations up to 116-Gbit/s PAM4.
- **All-in-one 58-Gbaud PAM4 receiver test solution with built-in Clock Recovery and Equalizer functions**
  Support faster testing and debugging with easy measurement system configuration

- Wideband operation: 2.4 to 64.2 Gbaud for NRZ
  2.4 to 58.2 Gbaud for PAM4
- Support CEI-112G-VSR Stressed Receiver Input Test
- Built-in 58-Gbaud PAM4 Clock Recovery
- PAM4 symbol Capture function
- Multichannel measurement (up to 4ch/unit)

Target Applications: 100/200/400/800GbE, CEI-112G-VSR
All-in-One BERT w/ PAM4 Built-in Clock Recovery & Equalizer

Connections with external equipment and components are eliminated. PAM4 Jitter Tolerance measurements are simplified by the easy system configuration.

- Jitter
- ISI Control

PAM4 PPG MU196020A

DUT

PAM4 ED MU196040B w/built-in CR&EQ

- Built-in Clock Recovery to re-time DUT signal for 58-Gbaud PAM4 JTOL testing
- Equalizer function to open Eye of VSR stressed signal for measuring BER

Support BER measurement of closed-Eye signal with stress

Support PAM4 Jitter Tolerance test

Anritsu envision: ensure
CEI-112G-VSR Stressed Input Test Support

The true DUT low-error-rate Rx performance can be tested using the worst-case signal with added stress.

CEI-112G-VSR Worst-Case Rx input specification

<table>
<thead>
<tr>
<th>Item</th>
<th>Spec. (112G-VSR-PAM4)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baud Rate</td>
<td>36 to 58 Gbaud</td>
</tr>
<tr>
<td>Channel Loss</td>
<td>12 dB at 26.5625 GHz</td>
</tr>
<tr>
<td>EH6</td>
<td>&gt;37 mV</td>
</tr>
<tr>
<td>EW6</td>
<td>&gt;0.2 UI (&gt;3.76 ps)</td>
</tr>
<tr>
<td>Target BER</td>
<td>&lt;E-6</td>
</tr>
</tbody>
</table>

Worst-case performance signal

Higher sensitivity performance (E-8 or lower) than receiver model defined by CEI VSR standard (E-6)

PAM4 ED MU196040B
Built-in Equalizer

Combination of built-in Equalizer function and high input sensitivity performance supports higher accuracy measurements.

Error-Free at 53.125 Gbaud for inputting signals path through 3 dB loss (typ.).

DUT

MU196040B
Built-in Equalizer diagram

Low-frequency Equalizer

ISI Stressed eye signal

Decision feedback Equalizer

DFE

BER Measurement

Anritsu envision: ensure
PAM4 Symbol Capture Function

Capture function supports identification of PAM4 error symbols and cuts verification time.

Can specify error symbol position and level change of captured signal

Start capturing inputting symbols using Error detection, Match pattern, or External trigger.
Measurement Result Logging Function

Periodic saving of BER/SER, etc., measurement results can evaluate changes and stability of DUT time-dependent performance.

Sets measurement cycle and starts logging
Saves results to file
Measurement item selection
Times-periodically saved measurement results
Error Analysis Function (1/2)

Useful measurement of both symbol errors (MU196040B-041) and bit errors for specifying error causes by comparing both measurement results. Press [Details] for more detailed analysis by confirming results for 12 error types.

PAM4 bit-error measurement results
Separate error-rate measurements for MSB and LSB
Simultaneous measurement of 12 error types
The Diagnostics Mode is useful for troubleshooting logic errors, such as inverted logic and MSB/LSB bit skew, etc. When these types of logic errors prevent synchronization, the cause can be determined using the separate MSB and LSB error results and the bit skew result between MSB and LSB.
Appendix
Typical Configuration of 64 G PPG/58 G ED

<table>
<thead>
<tr>
<th>Model</th>
<th>Name</th>
<th>Option</th>
<th>Qty</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>MP1900A</td>
<td>Signal Quality Analyzer-R</td>
<td>-</td>
<td>1</td>
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</tr>
<tr>
<td>MU181000B</td>
<td>12.5GHz 4 port Synthesizer</td>
<td>-</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>MU181500B</td>
<td>Jitter Modulation Source</td>
<td>-</td>
<td>1</td>
<td>For jitter injection</td>
</tr>
<tr>
<td>MU196020A</td>
<td>PAM4 PPG</td>
<td>002, 011, 040, 042</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>MU196040B</td>
<td>PAM4 ED</td>
<td>002, 011, 021, 023, 041</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

Software for jitter tolerance test

<table>
<thead>
<tr>
<th>Model</th>
<th>Name</th>
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<tbody>
<tr>
<td>MX183000A-PL001</td>
<td>Jitter Tolerance Test</td>
</tr>
<tr>
<td>MX183000A-PL031</td>
<td>DUT Error Counts Import</td>
</tr>
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</table>

Optional parts

<table>
<thead>
<tr>
<th>Model</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1789A</td>
<td>Electrical Length Specified cable (0.4m, V connector)</td>
</tr>
<tr>
<td>J1790A</td>
<td>Electrical Length Specified cable (0.8m, V connector)</td>
</tr>
<tr>
<td>J1800A</td>
<td>ISI Board V</td>
</tr>
<tr>
<td>J1793A</td>
<td>Pick OFF Tee (V)</td>
</tr>
</tbody>
</table>
# 64 G PPG/58 G ED Module Option

<table>
<thead>
<tr>
<th>Model</th>
<th>Name</th>
<th>Model</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>MU196020A</td>
<td>PAM4 PPG</td>
<td>MU196040B</td>
<td>PAM4 ED</td>
</tr>
<tr>
<td>MU196020A-001</td>
<td>32G baud</td>
<td>MU196040B-001</td>
<td>32G baud</td>
</tr>
<tr>
<td>MU196020A-002</td>
<td>58G baud</td>
<td>MU196040B-002</td>
<td>58G baud (max 64.2Gbit/s NRZ/58.2Gbaud PAM4)</td>
</tr>
<tr>
<td>MU196020A-003</td>
<td>64G baud</td>
<td>MU196040B-011</td>
<td>Equalizer</td>
</tr>
<tr>
<td>MU196020A-011</td>
<td>4Tap Emphasis</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MU196020A-030</td>
<td>Data Delay</td>
<td>MU196040B-021</td>
<td>29G Clock Recovery (2.4 G to 29 Gbaud)</td>
</tr>
<tr>
<td>MU196020A-040</td>
<td>Adjustable ISI</td>
<td>MU196040B-022</td>
<td>32G Clock Recovery (2.4 G to 32.1 Gbaud)</td>
</tr>
<tr>
<td>MU196020A-042</td>
<td>FEC Pattern Generation</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MU196020A-050</td>
<td>Intel-Module Synchronization</td>
<td>MU196040B-023</td>
<td>58G Clock Recovery Extension (51 G to 58 Gbaud)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MU196040B-041</td>
<td>SER Measurement</td>
</tr>
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</table>
## PAM4 PPG MU196020A Specifications

<table>
<thead>
<tr>
<th>Item</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operation Rate (PAM4/NRZ)</td>
<td>2.4 Gbaud to 32.1/58.2/64.2 Gbaud (option selection)</td>
</tr>
<tr>
<td>No. of Channels</td>
<td>1</td>
</tr>
<tr>
<td>Output Amplitude</td>
<td>70 mVp-p to 800 mVp-p (Single-end)</td>
</tr>
<tr>
<td></td>
<td>140 mVp-p to 1600 mVp-p (Differential)</td>
</tr>
<tr>
<td>Offset</td>
<td>–2 V to +3.3 V</td>
</tr>
<tr>
<td>Emphasis</td>
<td>4 Tap, –20 to +20 dB</td>
</tr>
<tr>
<td>Channel Emulator</td>
<td>Generates waveform with insertion loss and simulates waveform with corrected insertion loss Set by loading S-Parameter file (S2P, S4P)</td>
</tr>
<tr>
<td>ISI</td>
<td>Simulates ISI generation waveform Set using loss (–8.00 to 8.00 dB) at CEI-specified Nyquist frequency Used in combination with channel board, such as J1800A/J1758A (optional accessories parts), or Noise Module MU195050A</td>
</tr>
<tr>
<td>Independently Variable PAM4 3 Eye</td>
<td>20% to 50% (PAM4 Amplitude 0/3 level = 100%)</td>
</tr>
<tr>
<td>PAM4 Pattern</td>
<td>SSPRQ, PRBS13Q, PRBS31Q, RS-FEC, etc.</td>
</tr>
<tr>
<td>PAM4 Pattern Error Addition</td>
<td>MSB Error, LSB Error, LSB&amp;MSB Error, RS-FEC Symbol Error</td>
</tr>
<tr>
<td>Tr/Tf (20% to 80%)</td>
<td>8.5 ps (typ., NRZ)</td>
</tr>
<tr>
<td>Random Jitter</td>
<td>170 fs rms (typ., NRZ)</td>
</tr>
<tr>
<td>I/O Connector</td>
<td>V (f)</td>
</tr>
<tr>
<td>Jitter Addition Function</td>
<td>SJ, RJ, BUJ, SSC (with MU181500B)</td>
</tr>
<tr>
<td>Noise Addition Function</td>
<td>CMI, DMI, White Noise (with MU195050A (32.1G max.) and J1792A)</td>
</tr>
</tbody>
</table>
### PAM4 ED MU196040B Specifications

<table>
<thead>
<tr>
<th>Item</th>
<th>Specification</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baud rate</td>
<td>2.4 to 32.1 Gbaud/64.2 Gbaud (NRZ)</td>
<td>Select upper limit as option</td>
</tr>
<tr>
<td></td>
<td>2.4 to 32.1 Gbaud/58.2 Gbaud (PAM4)</td>
<td></td>
</tr>
<tr>
<td>Input Signal Method</td>
<td>NRZ, PAM4</td>
<td></td>
</tr>
<tr>
<td>Number of Inputs</td>
<td>2 (Data, xData)</td>
<td></td>
</tr>
<tr>
<td>Input Amplitude</td>
<td>1.0 Vp-p (max.)</td>
<td></td>
</tr>
<tr>
<td>Input Sensitivity</td>
<td>36 mV (typ. at 53.125 G), 23 mV (typ. at 26.5625 G)</td>
<td>Eye Height of each PAM4 Eye</td>
</tr>
<tr>
<td>Stressed Margin</td>
<td>BER &lt; 1 E-8</td>
<td>When inputting minimum eye signal defined in CEI-112G-VSR</td>
</tr>
<tr>
<td>Analog Band</td>
<td>&gt;40 GHz (nominal)</td>
<td></td>
</tr>
<tr>
<td>Clock Recovery</td>
<td>2.4 to 29 Gbaud or 2.4 to 32.1 Gbaud</td>
<td>Option</td>
</tr>
<tr>
<td>Operation Range</td>
<td>51 to 58.2 Gbaud Extension</td>
<td></td>
</tr>
<tr>
<td>Equalizer</td>
<td>DFE (1.4 dB) + Low-frequency-Equalizer (2 dB)</td>
<td></td>
</tr>
<tr>
<td>BER/SER Measurement</td>
<td>Total BER, MSB/LSB BER, SER (option)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Logging, Capture (8 M bits/4 M PAM4 symbols)</td>
<td></td>
</tr>
<tr>
<td>Patterns</td>
<td>PRBS, Data (max. 268 Mbit (symbol)),</td>
<td></td>
</tr>
<tr>
<td></td>
<td>PAM4 Pattern (PRBS13Q, PRBS31Q, SSPRQ, QPRBS13-CEI, QPRBS31-CEI), Gray Code/PAM4 Pre-Code</td>
<td></td>
</tr>
<tr>
<td>Connector</td>
<td>V (f)</td>
<td></td>
</tr>
</tbody>
</table>
**PAM4 Test Patterns**

**PRBS13Q, PRBS31Q, SSPRQ:**
PAM4 patterns defined by IEEE802.3bs, 802.3cd 200 GbE, and 400 GbE standards

**QPRBS13-CEI:**
Pattern for Tx output measurement and Rx input calibration defined by CEI-56G PAM4 standard

**JP03A:**
“0303...” pattern string for evaluating transmitter RJ

**JP03B:**
Pattern (shown below) of 62 symbols composed of string of 15 contiguous “03” followed by 16 contiguous “30” for evaluating transmitter Even-Odd jitter

\[
030303030303030303030303030303303030303030303030303030303030303
\]

**Square:**
“3333333300000000” pattern string for OMA evaluation of optical interfaces (OMA: Optical Modulation Amplitude)

**Transmitter Linearity Test Pattern:**
Pattern of 160 symbols with following sequence of 10 PAM4 symbols repeated in 16UI lengths
\[\{0, 1, 2, 3, 0, 3, 0, 3, 2, 1\}\]

The newest specification for the Linearity Test uses a PRBS13Q pattern.

\[
R_{LM} = \min((3 \times ES1), (3 \times ES2), (2 - 3 \times ES1), (2 - 3 \times ES2))
\]

\[
V_{\text{mid}} = \frac{(V_0 + V_3)}{2}, \quad ES1 = \frac{(V_1 - V_{\text{mid}})}{(V_0 - V_{\text{mid}})}, \quad ES2 = \frac{(V_2 - V_{\text{mid}})}{(V_3 - V_{\text{mid}})}
\]

**Gray-xxxx:**
PAM4 signals use four levels to express 2-bit pairs, but sometimes a 2-bit change such as 01→10 may be detected incorrectly for one level. To prevent this, a Gray code (00→00, 01→01, 10→11, 11→10) is used as the pattern at the Tx side.