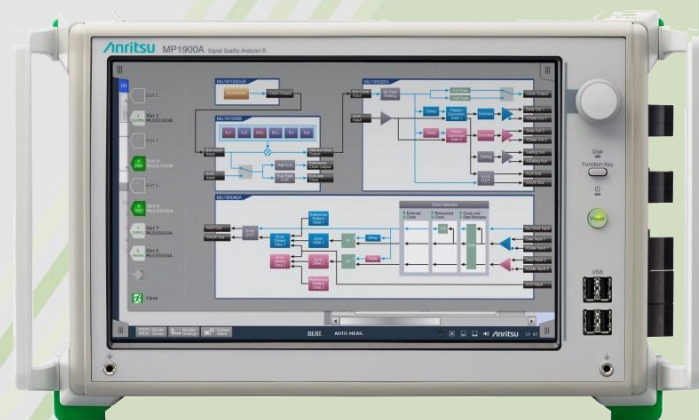




Signal Integrity Analysis Multi-channel High-Performance BERT

Signal Quality Analyzer-R
MP1900A Series



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SAS Test Solution

DisplayPort Test Solution

DDR5 Test Solution

Appendix



The growing spread of AI and machine learning is increasing the need for data centers, networks, and storage systems to process large amounts of data at high speed. Against this backdrop, PCI-SIG has drafted the base specification for PCIe 7. Like PCIe 6, PCIe 7 uses PAM4 (Pulse Amplitude Modulation 4) as its modulation scheme, but increases the transfer rate from 64 GT/s to 128 GT/s.

The Signal Quality Analyzer-R MP1900A Series is a high-performance, 8-slot modular BERT. It supports 32 Gbit/s multi-channel PPG/ED, 64 Gbaud PAM4 PPG/ED, and jitter/noise injection functions that can be expanded to suit specific measurement applications, making it ideal for signal integrity analysis of increasingly high-speed devices.

Combining the PAM4 PPG/ED MU196020C/MU196040B with the newly developed Re-Driver MU196060A in the all-in-one MP1900A simplifies the PCIe 5 (NRZ) Compliance Test worst-case configuration while supporting accurate Rx LEQ evaluation for the optimum return path using the powerful equalizer. In addition, this solution provides Link Training for PCIe 6 as well as an Rx evaluation solution for PCIe 7, supporting early validation against the PCIe 6 CEM and PCIe 7 Base specifications.

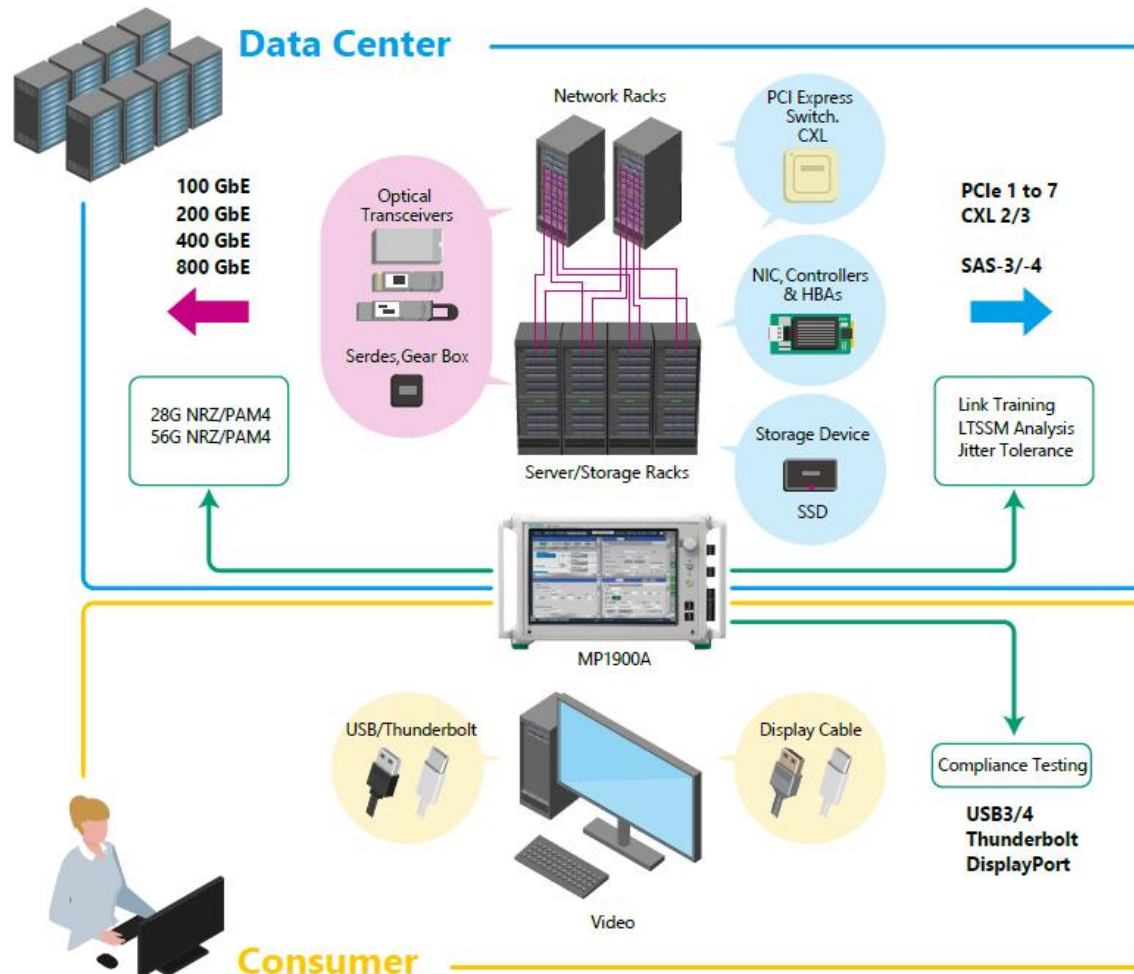
MP1900A Series Supported Applications

100 GbE/200 GbE/400 GbE/800 GbE, CEI-25G/28G/56G/112G, InfiniBand EDR/HDR, Fibre Channel, PCIe 1-7, CXL2/3, Thunderbolt 1/2/3/4, USB3.2/4 v1/4 v2, SAS-3/-4, DP1.4/2.0/2.1, DDR5, Optical module, SERDES, AOC, High-speed Interconnect

For the latest information, please refer to the "[Signal Quality Analyzer-R MP1900A series Selection Guide](#)"

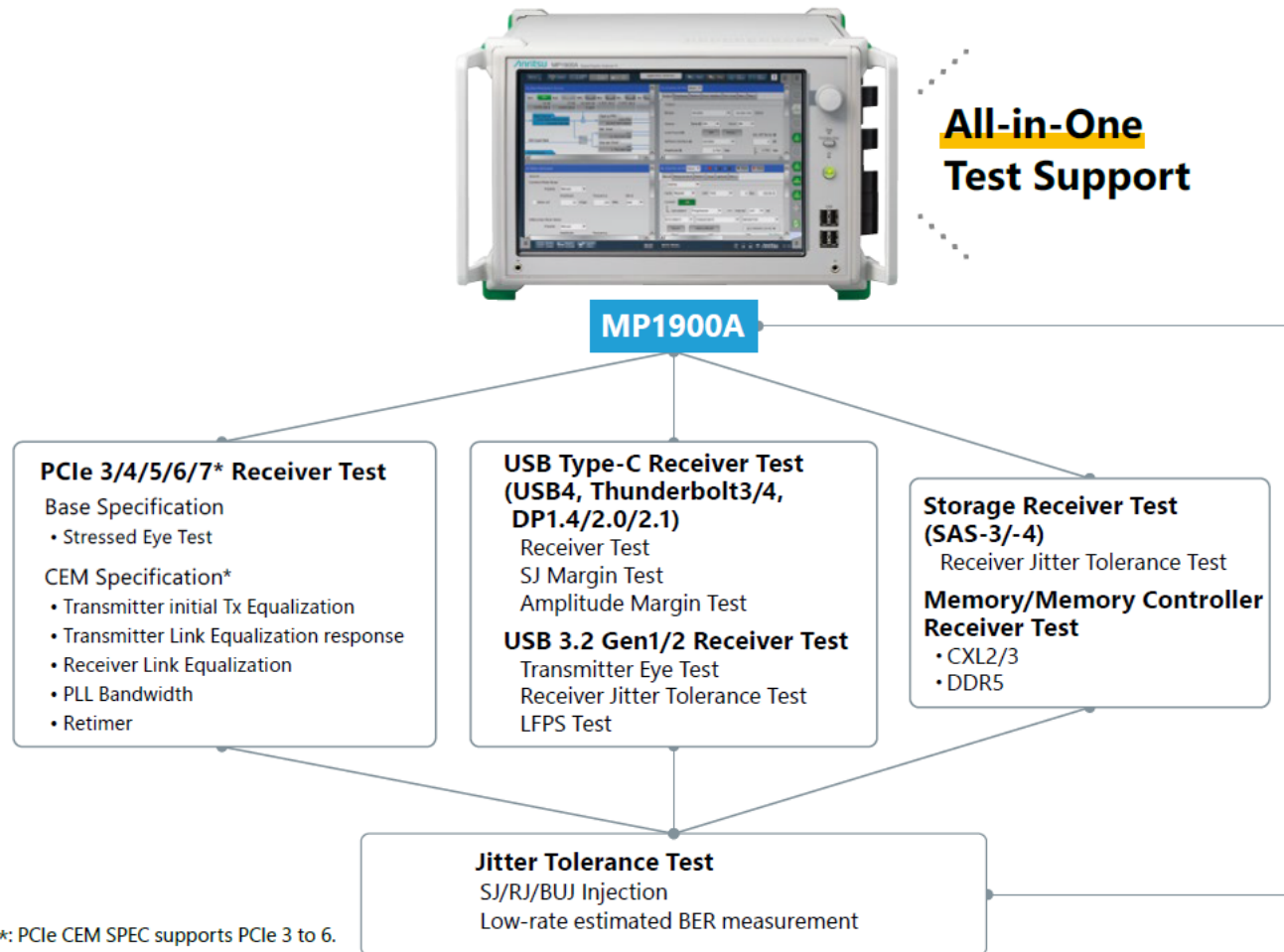
MP1900A Product Concept

The MP1900A series is a high-expandability, high-performance BERT supporting physical layer evaluations of high-speed interfaces. The all-in-one design covers early stage R&D evaluations ranging from next-generation 400/800 GbE network interfaces to PCI Express, USB and DP etc., bus interfaces.



Multi-IF Support

Expandable wideband operation from 2.4 to 64 Gbaud (128 Gbit/s) is supported. One unit enables Rx tests for PCIe Gen5 (32 GT/s), USB Type-C (USB4 (20 Gbit/s) , Thunderbolt3 (20 Gbit/s)), DisplayPort1.4 (8.1 Gbit/s), 2.1(20Gbit/s) and SAS-4 (22.5 Gbit/s).



Update Information

Demonstration video



[Unleash PCIe 6.0 USB Debugging and Validation](#)

[MP1900A PN Skew Evaluation Solution Demonstration Video](#)

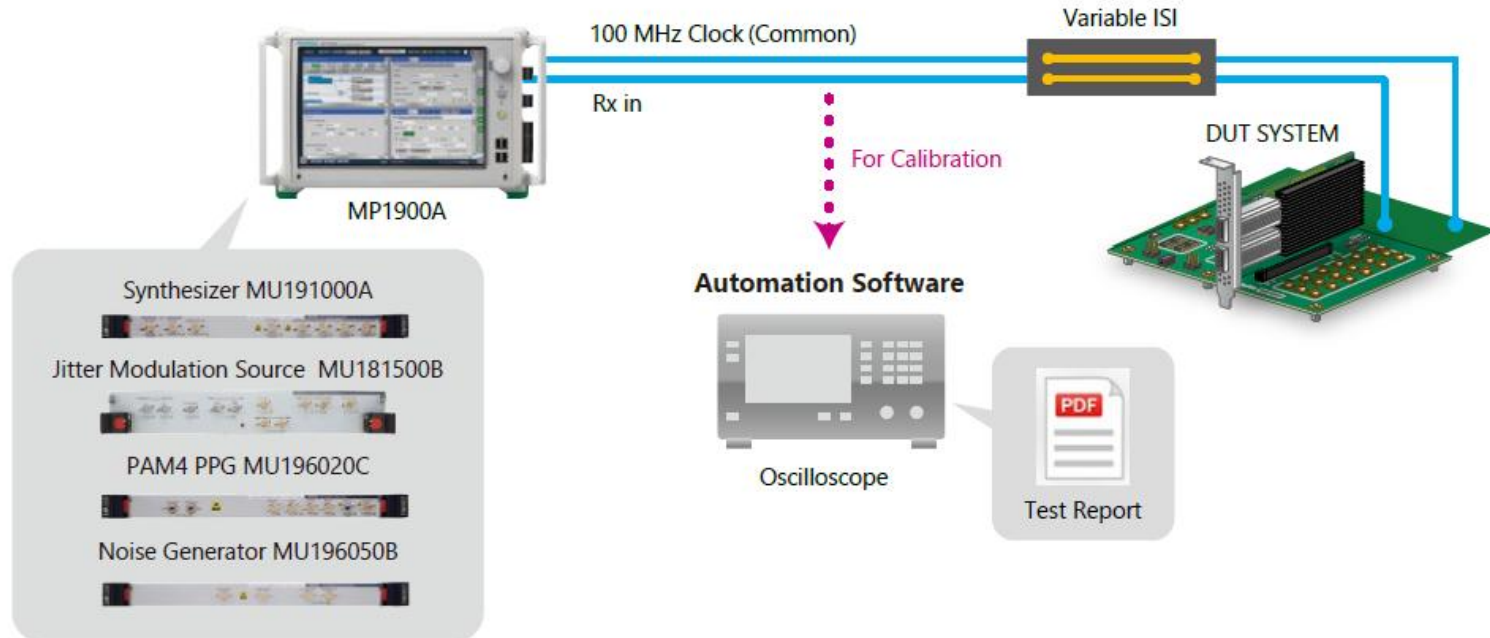
[MP1900A PCIe® 6.0 Rx and Tx LEQ Tests Demonstration Video](#)

Updated in Jan. 2026

- [PCIe7 Base Test Solution](#)
- [Sequence Editor Function For PCIe/CXL, USB3.2](#)
- Launch of [G0447A PCIe 6 External Re-Driver](#)
- [Test Configuration for PCIe Optical Re-timer](#)
- [USB/Thunderbolt Test Solution](#)
 - Updates accessories supporting USB4 v2 CTS 1.00 certification
- Added [DDR5 Test Solution](#)

- **Generates high-quality waveforms compliant with PCIe Gen7 requirements**
- **Jitter and noise injection testing**
Generates high-quality waveforms with SNDR of 35 dB, residual jitter of 108 fs, and rise/fall time (T_r/T_f) of 6.0 ps, supporting stable Rx testing.
- **Reduced evaluation time and improved efficiency through automation**
Enhances evaluation efficiency by providing automation software functions for stress signal calibration and jitter tolerance testing.

PCIe7 Base Rx Test



PCIe7 Base Test Equipment List

Model	Name	Option	Qty	Remark
MP1900A	Signal Quality Analyzer-R	-	1	
MU191000A	Synthesizer	-	1	PCIe1-7*
MU181500B	Jitter Modulation Source	-	1	PCIe1-7*
MU196020C	PAM4 PPG	003, 011	1	PCIe1-7*
MU196050B	Noise Generator	-	1	PCIe1-7*, J1793A x2 standard accessory

* PCIe CEM SPEC supports PCIe 3 to 6.

Choose the automation software matching your oscilloscope.

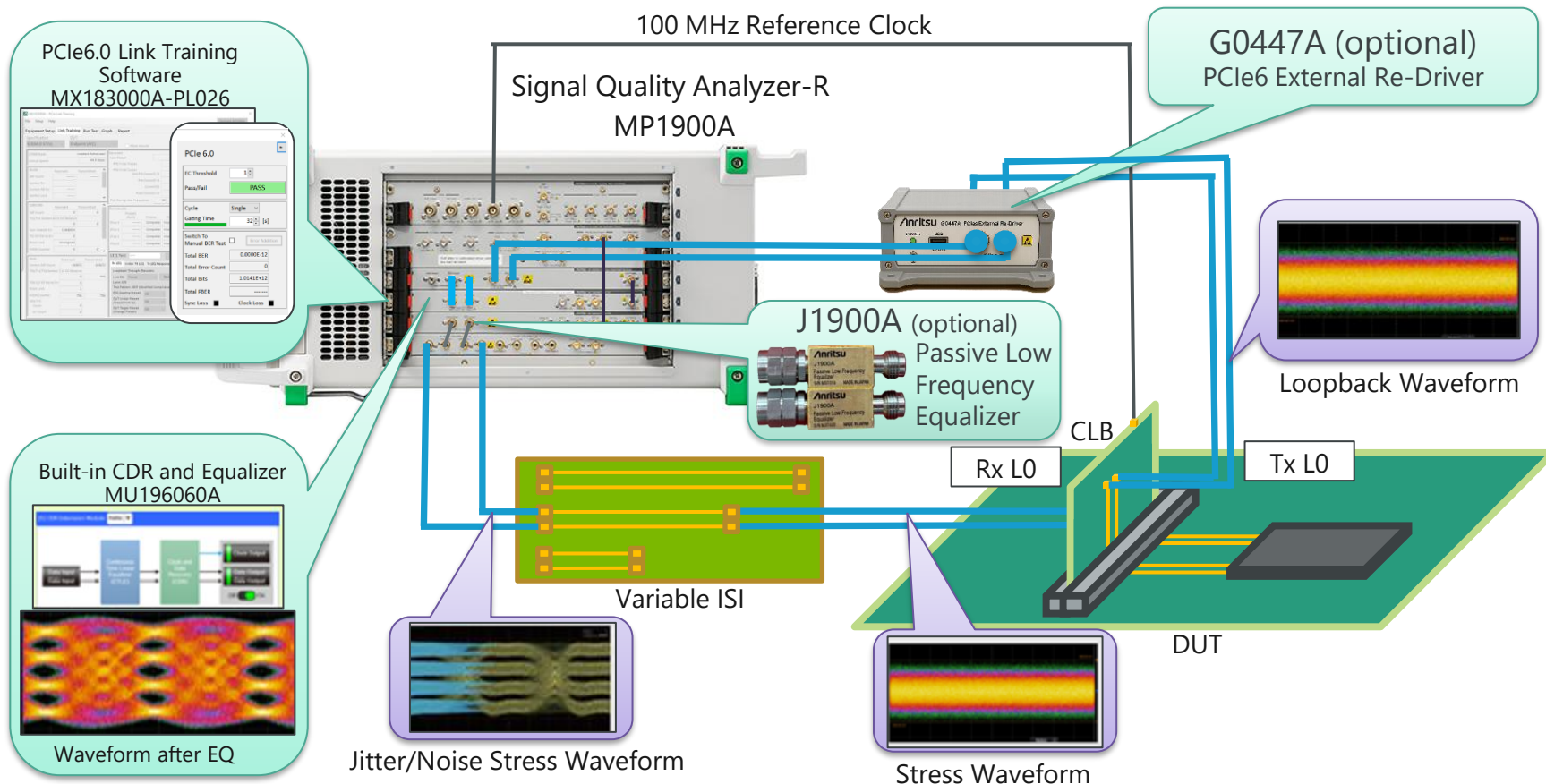
Model	Electrical Test	Remark
GRL-PCIE7-BASE-RXA	PCIE Gen7 Base Rx	For Tektronix or Keysight oscilloscopes Available from Granite River Labs

Contact your sales representative about automation software from Tektronix and Teledyne LeCroy.

For the latest information, please see the [Signal Quality Analyzer-R MP1900A Series Selection Guide](#).

MP1900A Series PCIe Receiver Test Solution

- Stable PCIe 6-link training and LTSSM event trigger functions.
- Analysis functions that are useful for debugging
 - LTSSM analysis
 - Switching between MSB/LSB and PAM4 symbol display and pattern analysis
 - BER/FBER, MSB/LSB Skew display function



For further details regarding the J1900A/G0447A, please contact Anritsu.

IP, AIC: The J1900A/G0447A is not required.

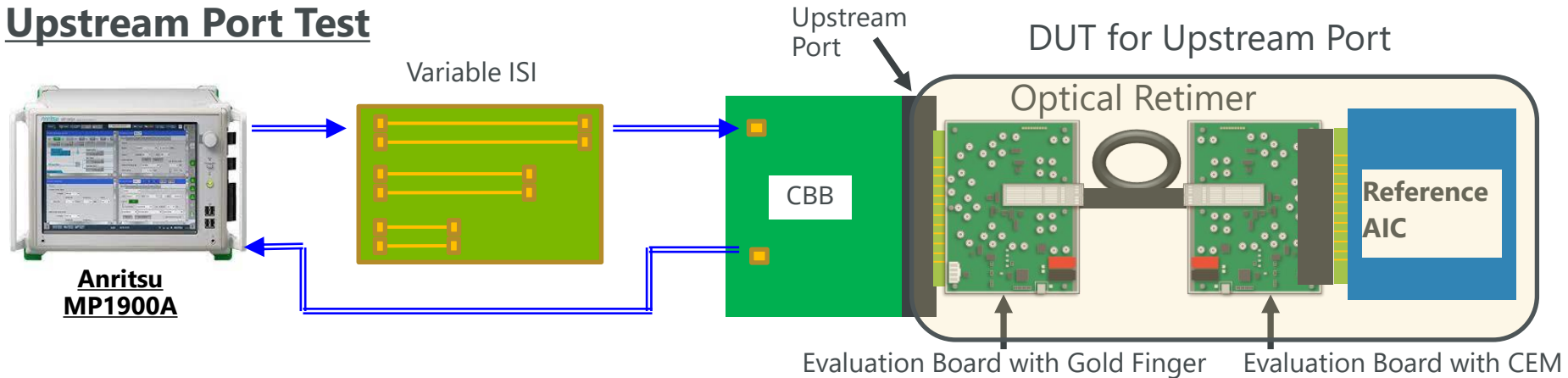
System: Back channel loss compensation under worst-case conditions is possible **using** the J1900A/G0447A.

Test Configuration for PCIe Optical Retimer

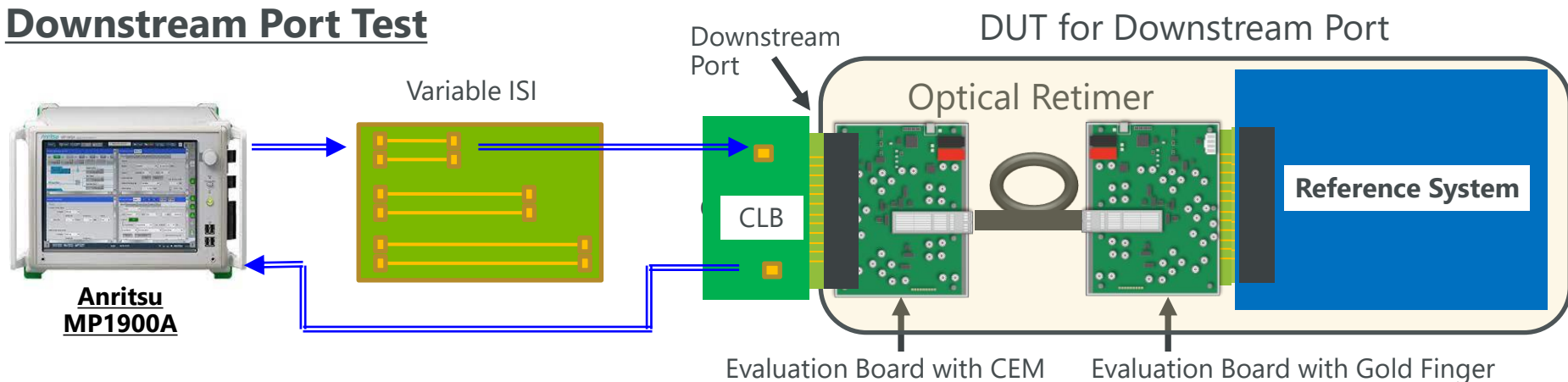
Although the details of the Optical Retimer compliance test have not been defined, it is considered as one of Retimer-based DUTs.

- Vendor must prepare their own system board and AIC.
- The Optical Retimer must be placed immediately before the reference system board or AIC.

Upstream Port Test



Downstream Port Test



MP1900A Series

Excellent expandability

- 8 slots (per one MP1900A main unit)
- Maximum transmission capacity up to 512 Gbit/s (supporting up to 8ch of 32 Gbit/s NRZ, 4ch of 64 Gbaud PAM4)
- All-in-one support for both high-speed network interfaces such as 400/800 GbE and bus interfaces such as PCIe

Full support for high-speed device signal integrity evaluations

- Bit rates of 2.4 Gbit/s to 32.1 Gbit/s (NRZ, SI PPG/ED series)
2.4 Gbaud to 64.2 Gbaud (128.4 Gbit/s) (PAM4, PAM4 PPG/ED series)
- Built-in Emphasis and Equalizer
- Low Intrinsic Jitter data output 115 fs rms (typ., SI PPG)
- High input sensitivity 15 mV (Eye Height) (typ., SI PPG)
- Built-in Clock Recovery
- Jitter (SJ/RJ/BUJ/SSC) and noise (CM/DM/White) tolerance measurements

All-in-one coverage of next-generation digital interface Rx tests

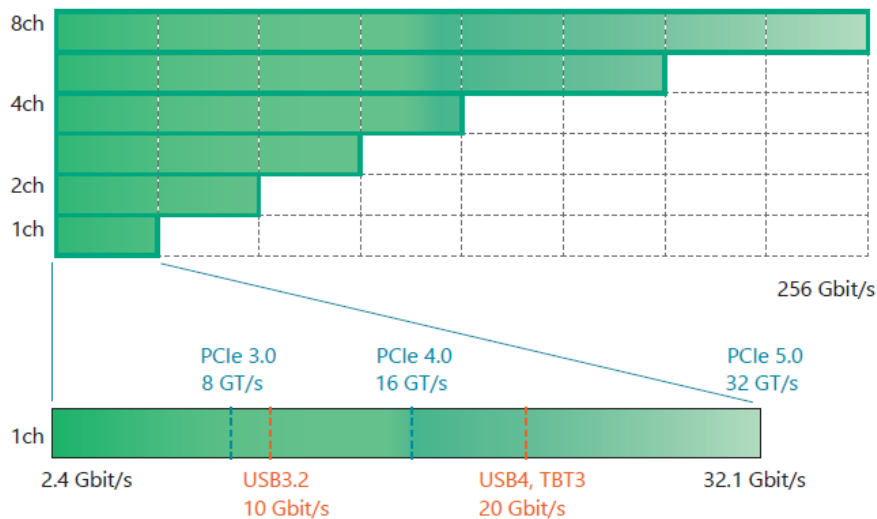
- Supports PCIe Gen1 to Gen6, SAS-3/-4, USB Type-C interface (USB3.2/USB4/Thunderbolt3), and DisplayPort1.4.
- Link Negotiation and LTSSM analysis functions
- Automated test-signal calibration and receiver tests

Supports Wideband & Multi-channel Measurement Requirements

The 8-slot modular type Signal Quality Analyzer-R MP1900A can be easily customized to support more measurement channels and new required functions and performance without wasting previous investments in equipment. With cost-effective upgrade support for next-generation interfaces, such as 400/800 GbE, the MP1900A will play a key role in bringing customers' products more quickly to market.

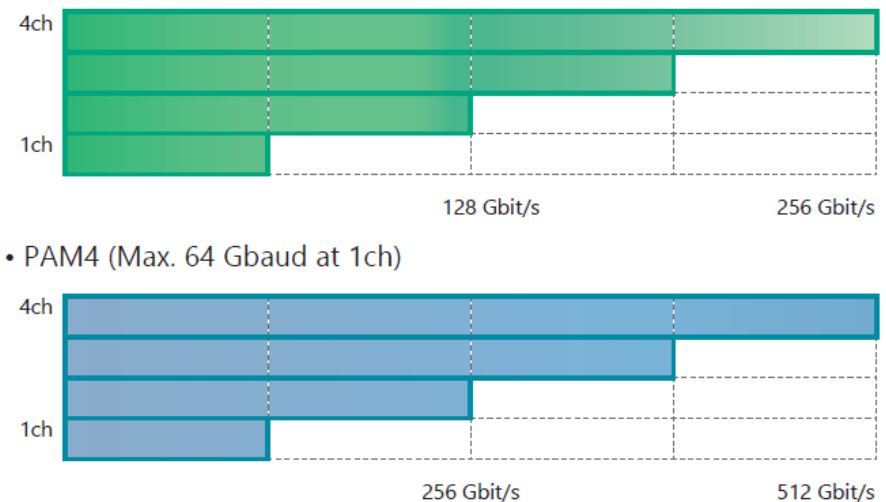
SI PPG/ED Module Expandability

- NRZ (Max. 32 Gbit/s at 1ch)



PAM4 PPG/ED Expandability*

- NRZ (Max. 64 Gbit/s at 1ch)



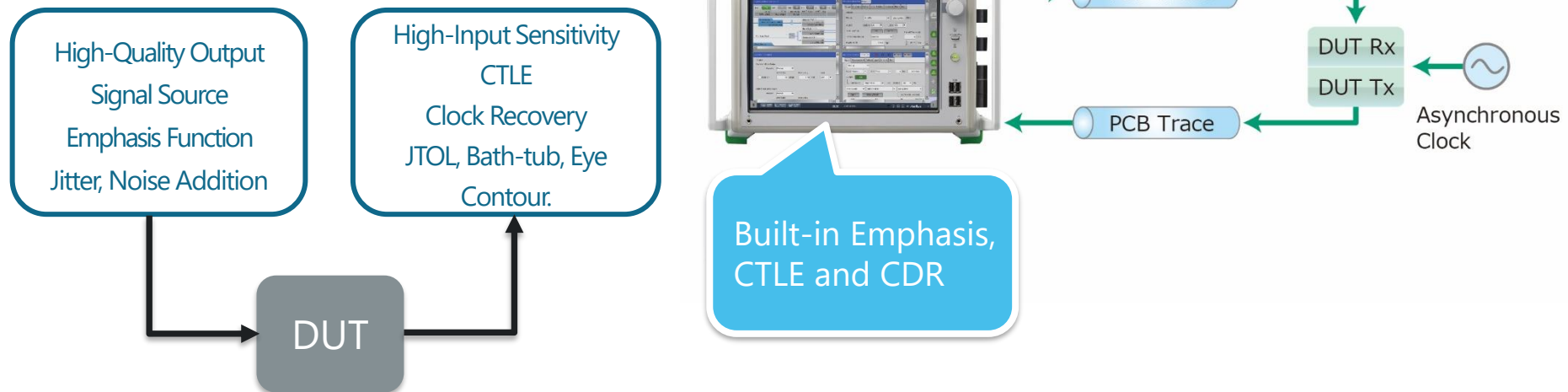
*: Refer to the 32G/64G NRZ/PAM4 Signal Integrity Test Solution Catalog (MP1900A_64G-E-A-1) for details of PAM4 PPG/ED.

Ideal for Signal Integrity Evaluations (1/2)

The 21G/32G bit/s SI PPG MU195020A has a built in 10Tap (max.) Emphasis option for simulating various devices and channels as well as for outputting corrected waveforms reproducing channel-path losses to help improve design evaluation efficiency.

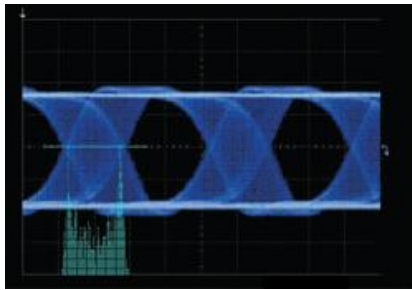
The Rx-side 21G/32G bit/s SI ED MU195040A has a built in multi-band CTLE (Continuous Time Linear Equalization) function supporting 28, 16, and 8 Gbit/s band input signals for performing BER measurements of Eyes closed by transmission path losses. Since this CTLE function is a hardware equalizer rather than software emulator, it supports evaluation of TRx BER performance under near-to-live conditions, such as BER evaluation of test signals, and comparison of DUT BER measurement results.

Signal Integrity Evaluations Required Performance and Functions

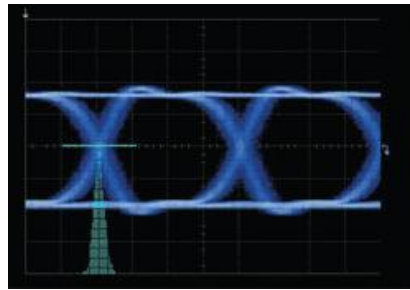


Ideal for Signal Integrity Evaluations (2/2)

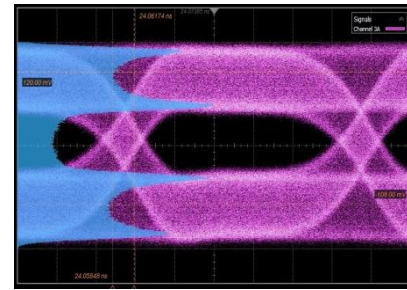
To perform high-speed receiver stressed input tolerance tests, the BER is measured under the worst conditions using a stressed signal with added jitter and voltage noise. Using the MP1900A series with the Jitter Modulation Source MU181500B, Noise Generator MU195040A with CDR function for adding various Jitter types and SSC and the Jitter Tolerance Test MX183000A-PL001 software, supports receiver tolerance tests in conformance with the various interface standards. The MP1900A series offers strong support for receiver stressed input tolerance tests by high-quality output signal before jitter and noise addition and high-linearity jitter and noise addition functions.



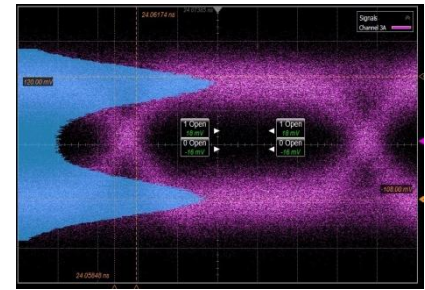
Sinusoidal Jitter(SJ)



Random Jitter(RJ)



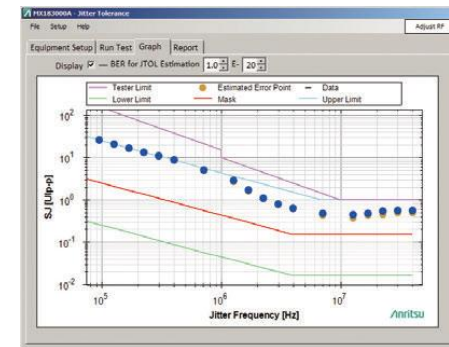
CM/DM Noise



White Noise

Jitter Tolerance Test Function (MX183000A-PL001)

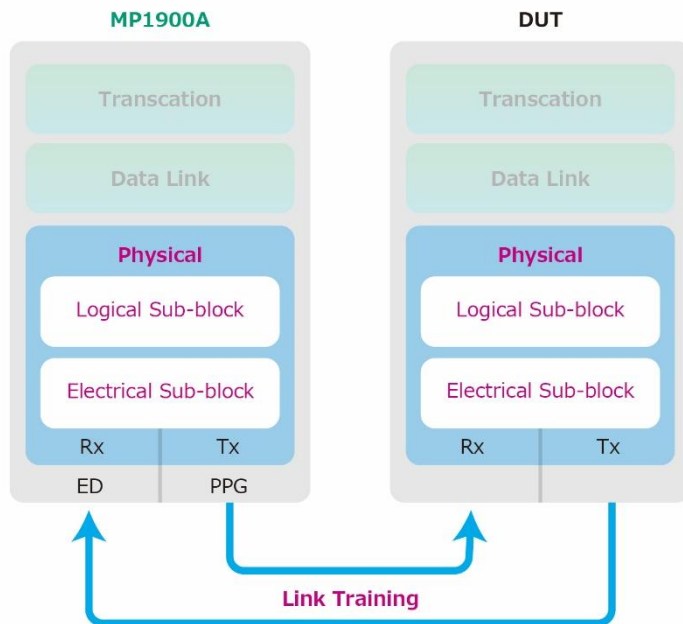
- High-versatility Jitter Tolerance measurements
- PHY Device Jitter Tolerance tests by impressing SJ/RJ/BUJ
- Standards-compliant Mask measurements
- Fast measurement times using low error rate estimation function, such as 1E-12 and 1E-15
- Tolerance measurements versus device characteristics using four Binary, Upward, Downward, Binary + Linear methods



Low Error Rate Estimation Jitter Tolerance Measurements

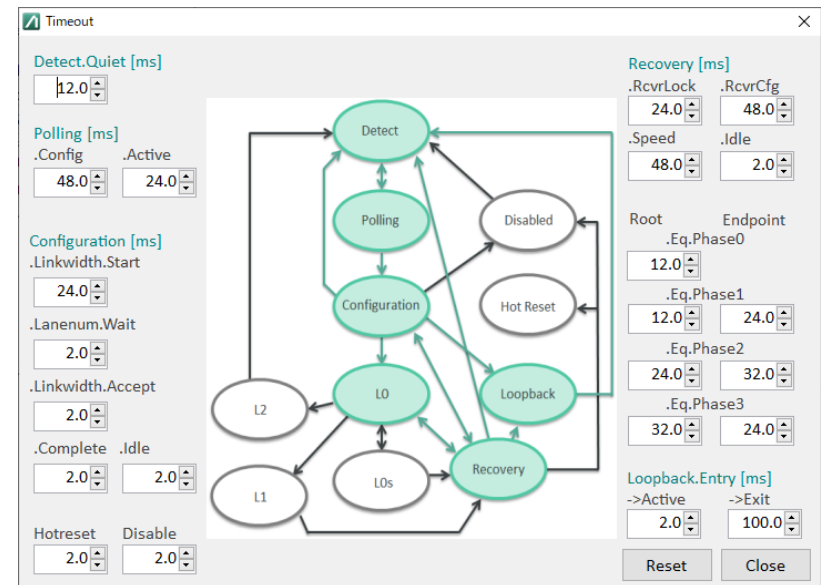
Built-in PCIe Link Training and LTSSM Analysis Functions

High-speed serial interfaces require good interconnectivity between devices and equipment, and it is important to identify whether a dropped Link is caused by physical or logical errors. The all-in-one MP1900A series supports Physical layer evaluations for PCIe Gen1 to Gen6 receivers, in addition to having Link Training for securing normal operation, also has functions for detecting and analyzing LTSSM (Link Training Status State Machine) fault transitions to improve detection efficiency.



Supports physical layer measurements of add-in cards and system boards

- Tx/Rx Link Equalization Response Test
- Rx Link Equalization Test
- Receiver Jitter Tolerance Test



PCIe Link Training State transitions

PCIe Link Training

(PCIe 1to4: MX183000A-PL021)

PCIe 5 Link Training

(MX183000A-PL021 and PL025)

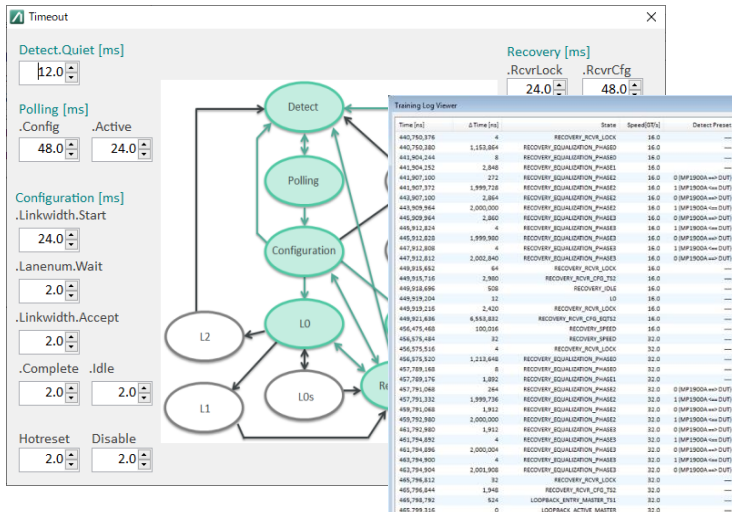
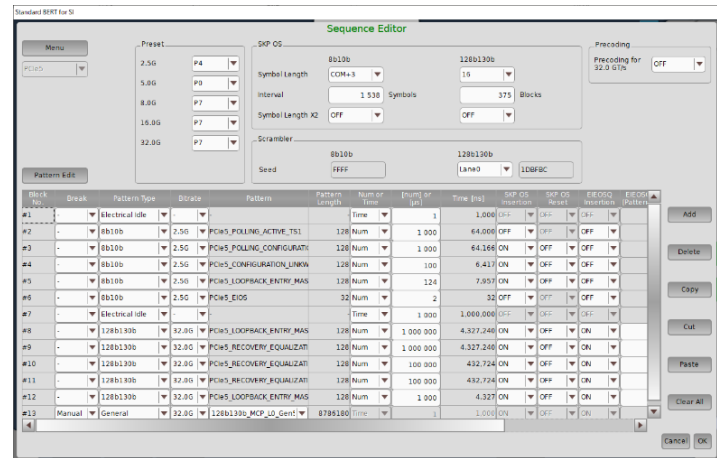
PCIe 6 Link Training

(MX183000A-PL021,PL025 and PL026)

The PCI-Express, USB 3.2, and CXL tests require evaluation by BER measurement when negotiation with the Link partner is completed. If this negotiation is not completed, although it is possible to use the LTSSM analysis function to troubleshoot the problem state, the built-in Sequence Editor function can troubleshoot the problem using detailed cause analysis. This function can be used to resolve negotiation problems quickly.

Identifying Link non-negotiation state using LTSSM function

Identifying problem parameters using status data occurrence times, sequence and encode data editing



Sequence Editor Function (MU195020A-050): PCIe 1/2/3/4, USB 3.2 Gen1/2

Sequence Editor Function PCIe 5 Extension (MU195020A-051): PCIe 5 Extension

Sequence Editor Function (MU196020A-050): PCIe 1/2/3/4/5/6)

Sequence Editor Function for Multi channel (MU196020A-051): For Multi channel

Sequence Editor Function (MU196020A-051): PCIe 1/2/3/4/5/6

Sequence Editor Function for Multi channel (MU196020A-052): For Multi channel

Sequence Editor Function PCIe 6 and CXL 3 Flits Extension (MU196020A-056): CXL2/3

MP1900A SI BERT

MP1900A SI PPG/ED Series Product Lineup

- 8-slot Platform
- 32G SI PPG/ED and Noise Generator Modules
- PCIe Link Training and LTSSM Analysis Functions
- Backward Compatibility with SQA Series MU181000B Synthesizer, Jitter Modulation Source MU181500B

Signal Quality Analyzer-R MP1900A



MX183000A-PL021 PCIe
MX183000A-PL025 PCIe Gen5 extension
MX183000A-PL022 USB
MX183000A-PL023 USB x2
Link Training (software)

21G/32G bit/s SI PPG MU195020A



21G/32G bit/s SI ED MU195040A



Noise Generator MU195050A



21G/32G bit/s SI PPG MU195020A Features

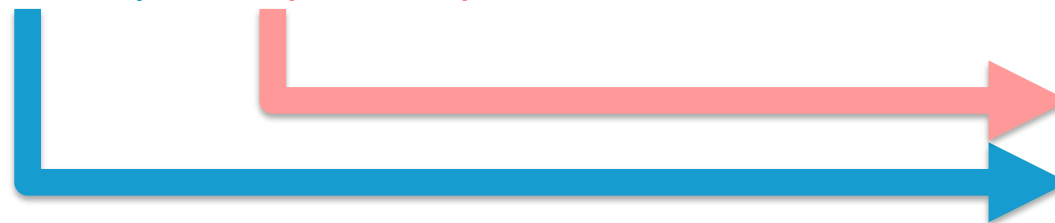
- Bit rate of 2.4 to 21 Gbit/s or 32.1 Gbit/s
- 1ch/2ch Selection
- 10Tap Emphasis built-in
- Data Output Amplitude 0.1 Vp-p to 1.3 Vp-p (Single-end)
0.2 Vp-p to 2.6 Vp-p (Differential)
- Low Intrinsic Jitter output of 115 fs rms (typ.)
- Tr/Tf (20%-80%) of 12 ps (typ.)
- Multi-channel synchronization function
- NRZ/PAM4 support (PAM4 uses 2ch Data out + G0375A remote head)
- PCIe / USB Link Training

21G/32G bit/s SI PPG MU195020A



Data1 (differential) Data2 (differential)

- 10Tap Emphasis
- High-Quality Output Waveforms
- Multi-channel Synchronization



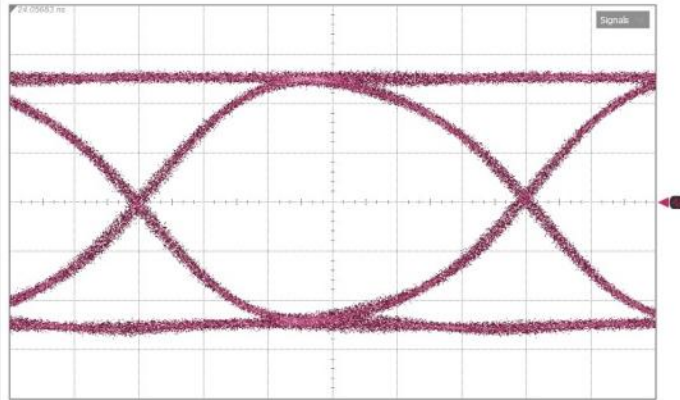
DUT

MU195020A PPG Data Output Waveforms

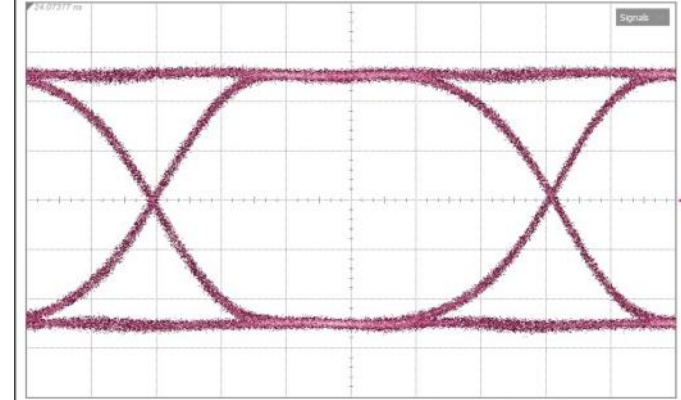
Low Intrinsic Jitter Data Output Waveforms for Signal Integrity Analysis

PRBS 2³¹-1, 1 Vp-p (Single end, 70 GHz observed with oscilloscope)

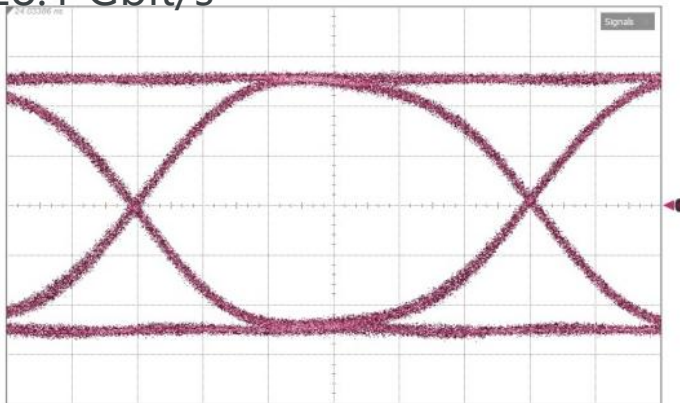
32.1 Gbit/s



21 Gbit/s



28.1 Gbit/s



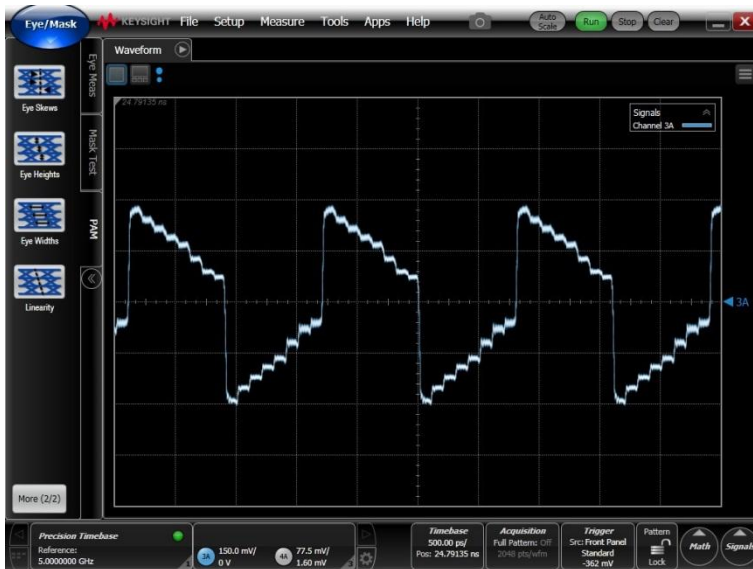
Low Intrinsic Jitter 115 fs (rms) @ 28.1 Gbit/s
("1010..." pattern)



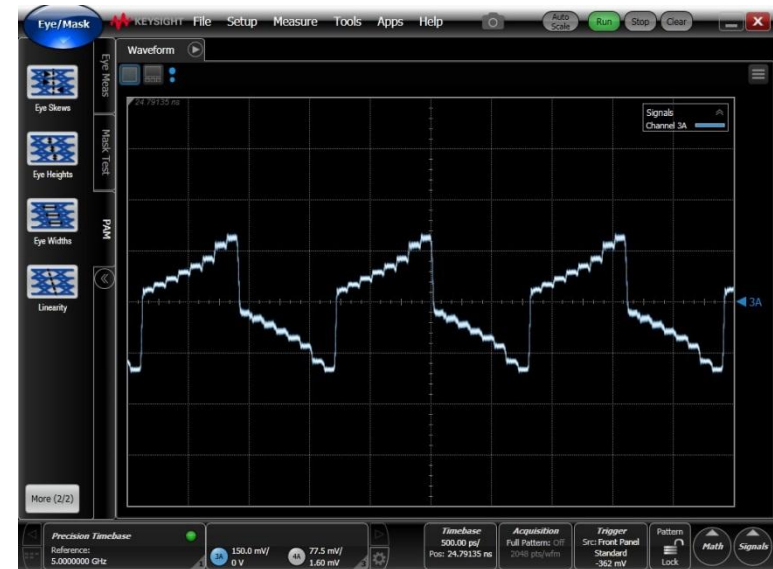
MU195020A PPG Data Output 10Tap Emphasis

Flexible Support for High-speed Device with Long-channel Design Evaluations

- 10Tap Emphasis
- Control up to 20 dB
- Pre-Emphasis output with peak output amplitude of 1.5 Vp-p



Waveform for correcting transmission path loss



Waveform emulating signal loss

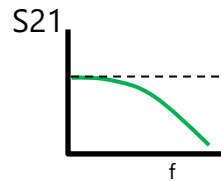
Voltage control at each 1 bit for 10-bit time period

Shorter Development Period by Eliminating Need for Multiple Test PC Boards Simple and High-Reproducibility Design Tests of High-Speed Device Channel Loss Dependency

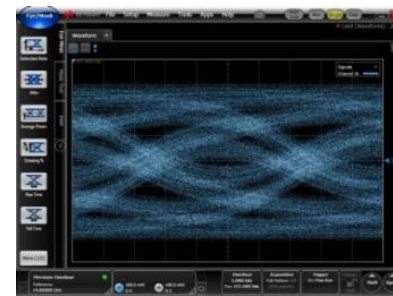
- Emulate channel loss by controlling Emphasis and generate loss-compensated signals
- Automatically calculate Emphasis setting using S-parameter



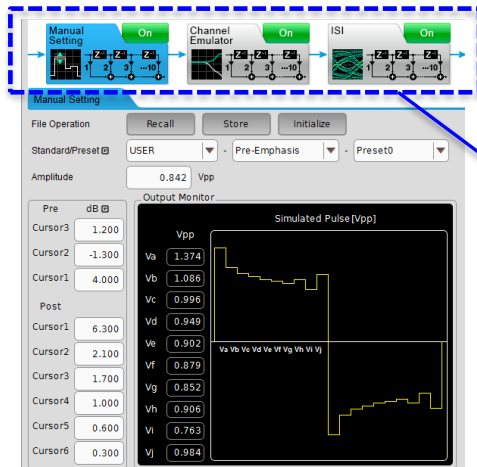
MP1900A SQA-R



Emulate channel loss
And generate loss-compensated
signals (Variable ISI option)



CEI-28G, 14 dB loss typical waveform
(ISI function)



• Manual Setting:

Correct signal for target Eye Height/Width using 10Tap Emphasis function

• Channel Emulator:

Emulate S2P and S4P data loss insertion, and perform Emphasis compensation

• ISI:

Emulate ISI using CEI-28G/25G Nyquist frequency loss setting

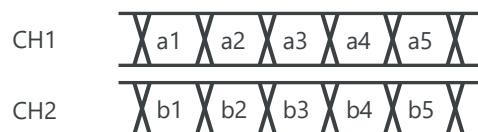
MU195020A PPG Multi-channel (1/2)

Enables multiplexing and higher bit rates, as well as crosstalk testing, through multi-channel data output, pattern synchronization, and skew control. Flexibly accommodates future high-bit-rate expansion and evaluation of multi-channel interfaces.

Number of Synchronized Channels	Supported Function	Applications	Equipment Configuration Example
2	2ch Combination	32G PAM4 generation 2:1 MUX evaluation	MU195020A 2ch PPG x1
4	64G x 2ch Combination	64G PAM4 generation 4:1 MUX evaluation	MU195020A 2ch PPG x2

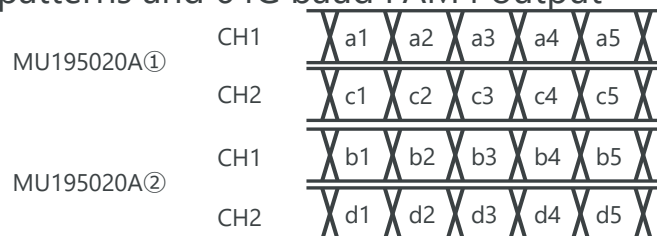
• 2ch Combination

Supports multiplexing into "a1b1
a2b2 . . ." patterns and PAM4 output



• 64G x 2ch Combination

Supports multiplexing from two 32G PPGs (4 channels) into "a1b1c1d1 a2b2c2d2 . . ." patterns and 64G baud PAM4 output



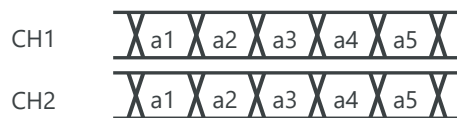
MU195020A PPG Multi-channel (2/2)

By using the Unit Sync function, multi-channel data output of up to 16 channels, pattern synchronization, and skew control are possible, enabling flexible support for evaluation of multi-channel interfaces.

Number of Synchronized Channels	Supported Function	Equipment Configuration Example	Number of MP1900A Units
8	Channel Synchronization	MU195020A 2ch PPG x4	1
16	Channel Synchronization Unit Sync	MU195020A 2ch PPG x8	2

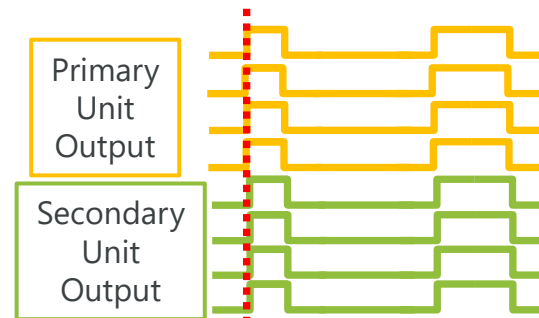
• Channel Synchronization

Supports parallel interface evaluation, crosstalk testing, and D/A converter evaluation, with up to 8 channels per MP1900A unit and synchronized output of up to two MP1900A units.



• Unit Sync

Using Unit Sync function enables alignment of data phase between units, allowing output of synchronized multi-lane data.



21G/32G bit/s SI ED MU195040A Features

- Bit rate of 2.4 to 21 Gbit/s or 32.1 Gbit/s
- 1ch/2ch selection
- Built-in multi-band CTLE function
 - Peak frequency: 14, 8, 4 GHz switchable
 - Gain control: 0 to -12 dB control
- Data input amplitude: 0.05 to 1.0 Vp-p (Single-end)
- Input sensitivity @ 28.1Gbit/s NRZ: 15 mV (Eye Height) (typ.); 22 mVp-p (Eye amplitude)
@ 28.1Gbit/s PAM4: 30 mV/Eye(Eye Height) (typ.); 150 mVp-p (Eye amplitude)
- Auto-measurements (Auto-search/Adjust, Eye Contour, Bathtub, Jitter Tolerance)
- Clock Recovery: 2.4 to 32.1 Gbit/s, SSC support
- PCI Express/USB Link Training

MU195040A 21G/32G bit/s SI ED



Data1 (differential)

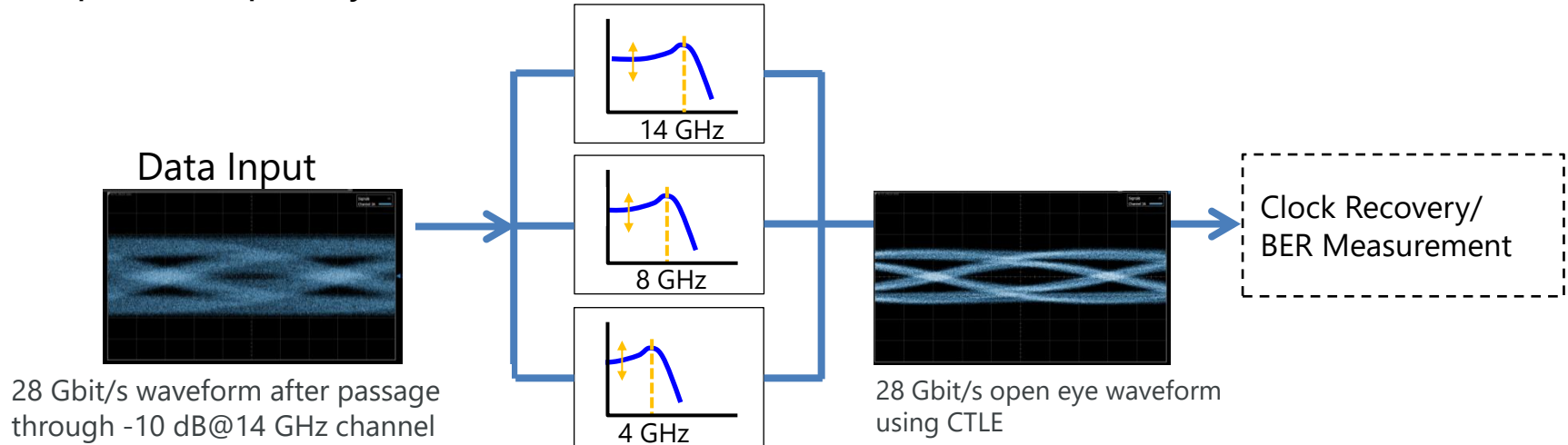
Data2 (differential)

- Multi-band CTLE
- High-sensitivity input
- CDR supporting SSC

DUT

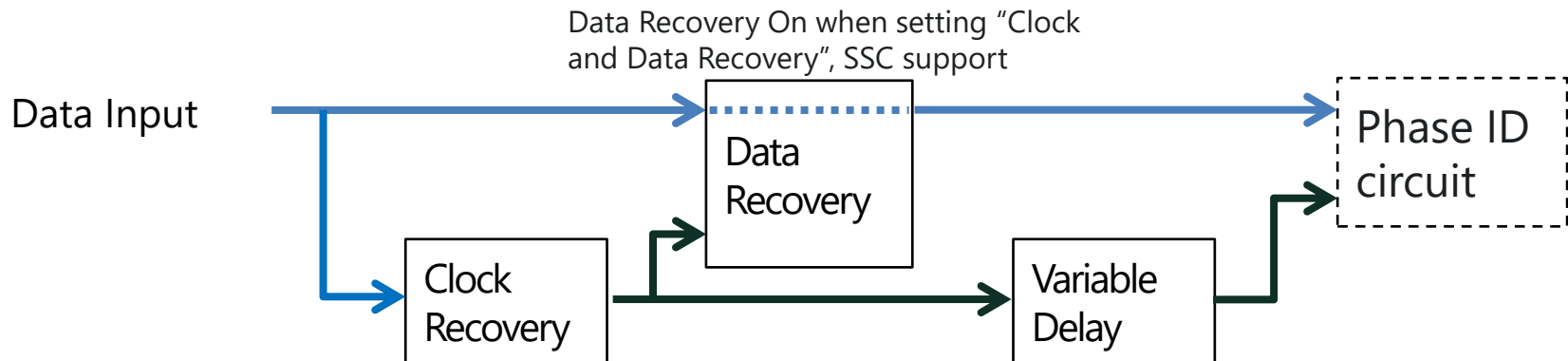
MU195040A ED Data Input CTLE/Clock Recovery Functions

Supports input receiver measurements for CEI-28G, PCIe Gen 3 to Gen 5 using 3-band CTLE (peak frequency of 14, 8 , and 4 GHz)



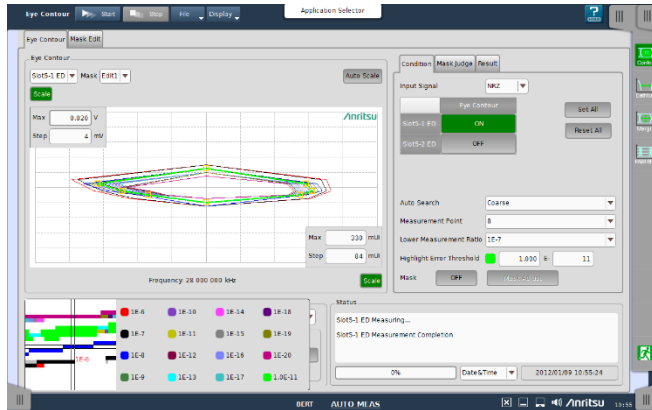
Supports SSC to implement Eye analysis for input signals with added Jitter

- 2.4 Gbit/s to 32.1 Gbit/s (extracts Clock from Data1 input signal)
- External Clock/Clock Recovery/Clock and Data Recovery_SSC support switching function

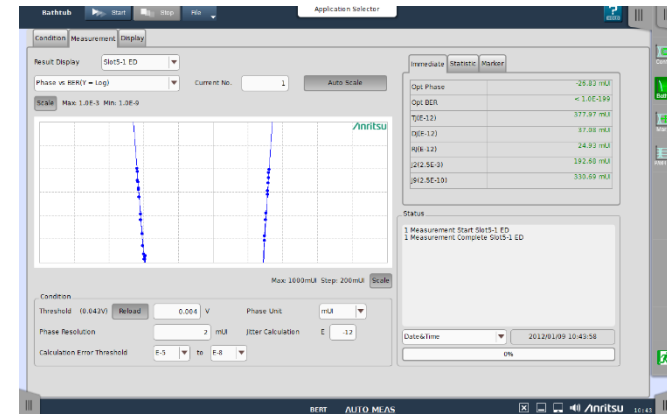


MU195040A ED Auto Measurement • Analysis Functions

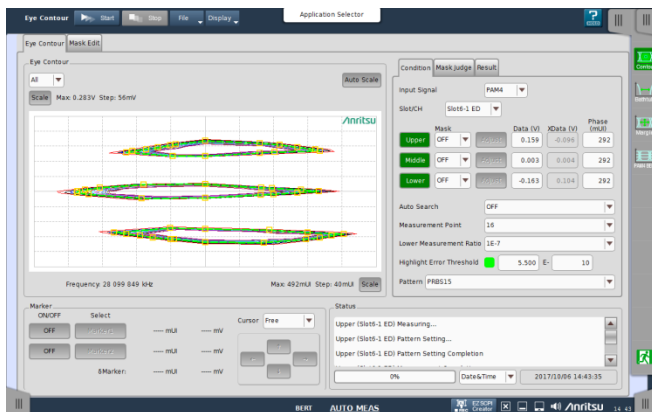
Higher-accuracy Eye analysis is supported using the auto-measurement and auto-analysis functions, such as Auto Search/Auto Adjust, Bathtub, Eye Contour, Eye Margin, and PAM BER measurement that make use of the measurement high-input-sensitivity performance.



Example of Eye Contour Measurement at Input of Small 50 mVp-p Signal



Bathtub Measurement Example



Example of Eye Contour Measurement at Input of PAM4 Signal

Noise Generator MU195050A Features

Supports Voltage Noise Tolerance tests specified by CEI and IEEE802.3 for backplane, PCIe, and Thunderbolt measurements

- Noise addition to Data signals up to bit rates of 32.1 Gbit/s
- 2ch output
- CMI/DMI/White noise support
 - Common mode noise frequency: 0.1 GHz to 6 GHz
 - Differential mode noise frequency: 2 GHz to 10 GHz
 - White noise band: 10 GHz; Crest Factor: >5
- Supports external noise input

MU195020A



MU195050A
Noise Generator

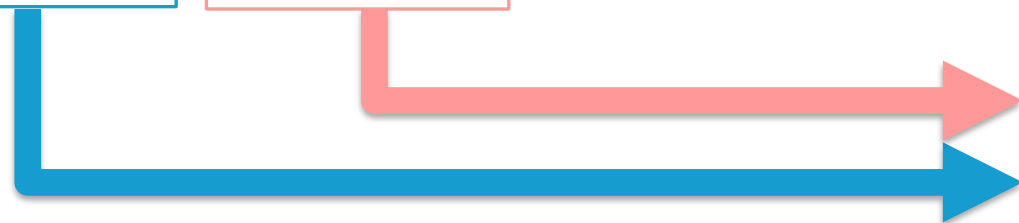


Data1 (differential)

Data2 (differential)

External input

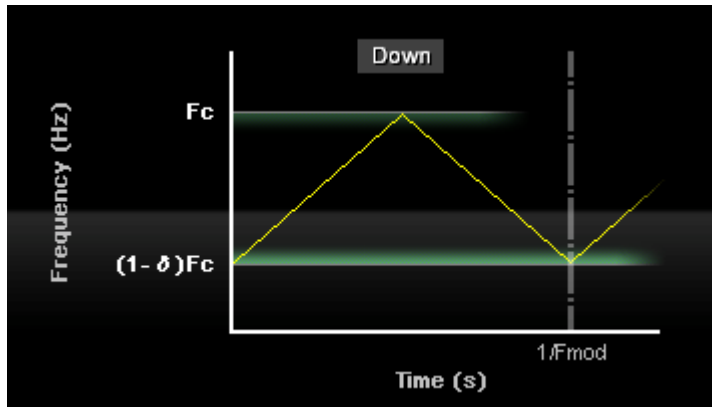
- Built-in CMI/DMI/White noise
- 2ch output



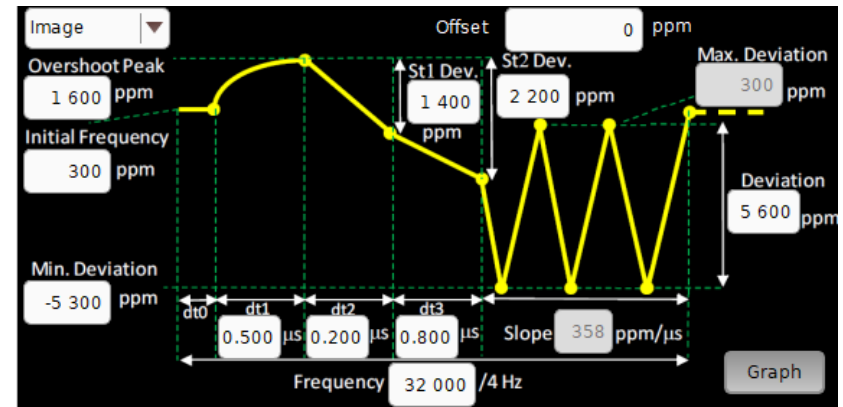
DUT

MU181500B Jitter SSC Profile Function

The new SSC Profile standard for USB 4, Display Port, etc., makes it easy to test SSC compliance of the DUT receiver clock recovery, etc.



Previous Triangular



USB 4 SSC Profile (image)

List

Initial Frequency

300

ppm

Offset

0

ppm

Frequency

32 000

Hz

Frame Divide Ratio

4

Frame Frequency

8 000

Hz

Deviation

5 600

ppm

Min. Deviation

-5 300

ppm

Max. Deviation

300

ppm

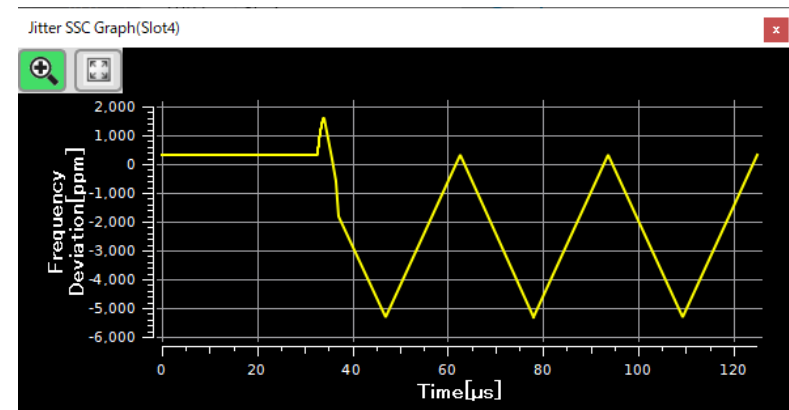
Window	Shape	ΔDeviation[ppm]	Time[μs]	Slope[ppm/μs]
dt1	Sinusoidal	1 300	1.500	---
dt2	Linear	-1 400	1.500	-933
dt3	Linear	-800	0.800	-1 000
dt4	Linear	-1 200	0.700	-1 714
Steady-State	Linear	5 600	87.890	358

Add

Delete

Graph

Variable Profile (List)



Variable Profile (Graph)

MP1900A PAM4 Application

Outline of MP1900A Series PAM4 BERT

- Supports bit error rate measurements optimized for high-speed 400 GbE and next-generation 800 GbE interfaces
- High-quality data output waveforms up to 64 Gbaud and high input sensitivity performance provide strong support for testing PAM4 device designs
- All-in-one Jitter Addition, Clock Recovery, Emphasis, NRZ/PAM3/PAM4 Pattern Editing, SER functions, etc.
- Easily configured, high-reproducibility PAM4 measurement solution

MP1900A PAM4 Target Applications

200/400/800 GbE, CEI-56G/112G, InfiniBand HDR, 64G Fibre Channel, PCIe1-6, USB4v2



MP1900A PAM4 BERT Features

- All-in-one, high-reproducibility, easily configured test solution
- High-quality waveforms for more accurate measurement
- Easy, low-cost, future-proof expandability supporting high bit rates and multichannels

PAM4 One Box Test Solution

Emphasis 4Tap, 20dB

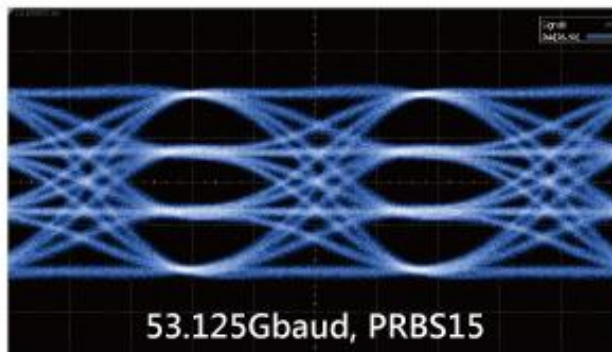
Built-in Clock Recovery



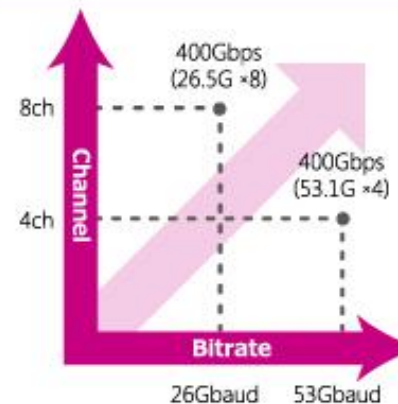
Jitter/Noise Addition

Jitter Tolerance Test

Highest Level Waveform Quality



Next-Generation Terabit



PAM4 All-in-One BERT Solution

Easy-to-use and configure all-in-one solution with high reproducibility, helping cut test times

**32G baud NRZ/PAM4 Re-Driver
MU196060A**

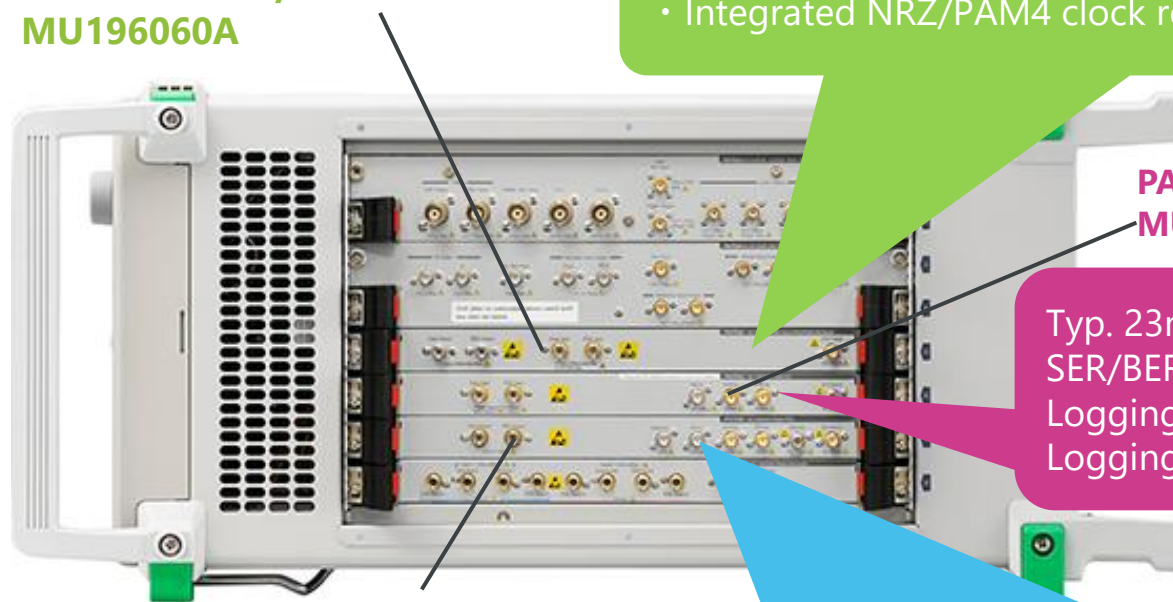
- Built-in CTLE equalizer
- Integrated NRZ/PAM4 clock recovery supporting PCIe4 to PCIe6

**PAM4 ED
MU196040B***

Typ. 23mV at 32.1G High Input Sensitivity
SER/BER, Capture,
Logging and analysis functions
Logging/Capture functions

**PAM4 PPG
MU196020C**

No External Equipment, Compact Module with Built-in PAM4 Functions
High-Quality PAM4 Waveforms(MAX 64G baud) with Variable
Emphasis/Linearity Functions



*For PCIe1-3, PAM4 ED must be changed to SI ED.

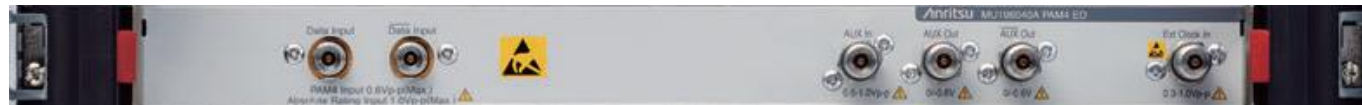
PAM4 PPG/ED Specifications

PAM4 PPG MU196020C



- Baud-rate: 2.4 Gbaud to 32.1 Gbaud /58.2 Gbaud /64.2 Gbaud * 1
- Output amplitude: 70 mVp-p~800 mVp-p、 1 mV step (Single-ended, PAM4)
- Emphasis: 4Tap
- Intrinsic jitter(rms): 108 fs
- Tr/Tf (20-80%): Typ. 6.0 ps (20-80%) at 32,64Gbaud (using J1789A)
Typ. 7.0 ps (20-80%) at 32,64Gbaud (using J1790A)
- Multichannel synchronization
- FEC pattern generation (Supports PCIe up to Gen6)

PAM4 ED MU196040B



- Baud-rate: 2.4 Gbaud to 32.1 Gbaud /58.2 Gbaud PAM4 * 1 * 2
- Input amplitude (max.): 1.0 Vp-p (NRZ, PAM4)
- Input sensitivity (Eye Height, PAM4) : 23 mV (typ., 26.5625 Gbaud), 36 mV (typ., 53.125 Gbaud)
- Built-in Clock Recovery: 2.4 Gbaud to 29 Gbaud /32.1 Gbaud/51 Gbaud to 58.2 Gbaud extension * 1
- Analog bandwidth: >40 GHz (nominal)
- Built-in Equalizer: Low Frequency Equalizer(2 dB)+DFE(1.4 dB)
- SER measurement, logic error analysis using Diagnostics Mode, Capture , Logging function

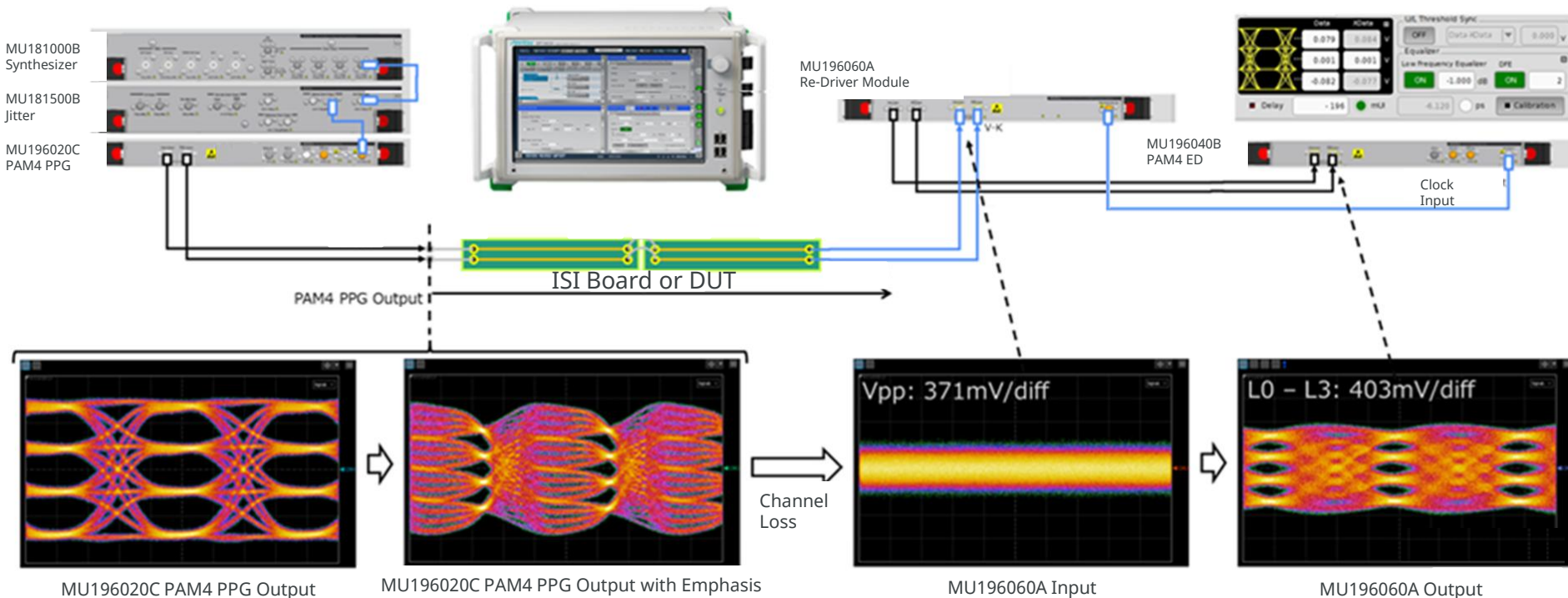
*1: The upper limit of the Baud-rate depends on the option configuration. *2: For NRZ signals, the maximum is 64.2 Gbits/s

NRZ/PAM4 Re-Driver Key Performance

32 Gbaud NRZ/PAM4 Re-Driver MU196060A



- Assured SSC tolerance using built-in CDR
- Supports both PAM4 and NRZ modulation methods
- Compensates for 30 dB loss at NRZ 32 Gbit/s for PCIe 5. (<1E-12)
- Compensates for 14 dB loss at PAM4 32 Gbaud for PCIe 6. (1E-9, Typ.)



Typical Configuration of 58 Gbaud PPG/ED

Model	Name	Option	Qty	Remark
MP1900A	Signal Quality Analyzer-R	-	1	
MU191000A	Synthesizer	-	1	
MU181500B	Jitter Modulation Source	-	1	For jitter injection
MU196020C	PAM4 PPG	002, 011, 040, 042	1	
MU196040B	PAM4 ED	002, 011, 021, 023, 041	1	

Software for jitter tolerance test

Model	Name
MX183000A-PL001	Jitter Tolerance Test
MX183000A-PL031	DUT Error Counts Import

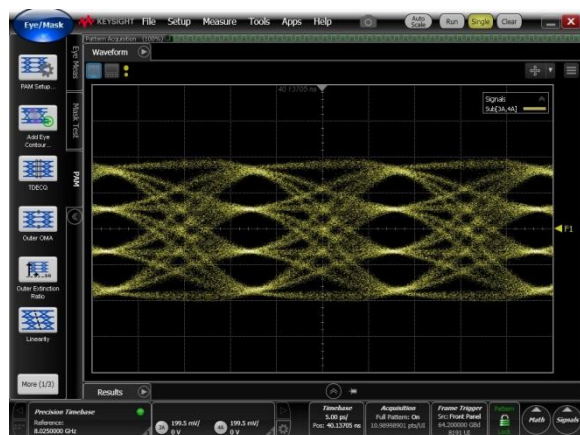
Optional parts

Model	Name
J1789A	Electrical Length Specified cable (0.4m, V connector)
J1790A	Electrical Length Specified cable (0.8m, V connector)
J1800A	ISI Board V
J1793A	Pick OFF Tee (V)

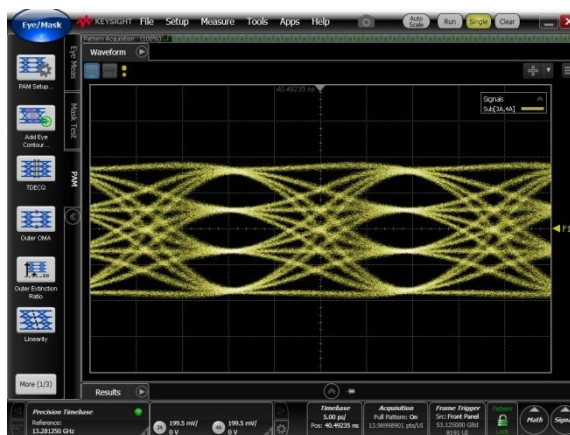
High-Quality Waveform PAM4 PPG MU196020C

Best-in-class waveform quality with low Intrinsic Jitter (typ. 170 fs (rms) and fast Tr/Tf (typ. 8.5 ps) for more accurate evaluation of actual DUT performance

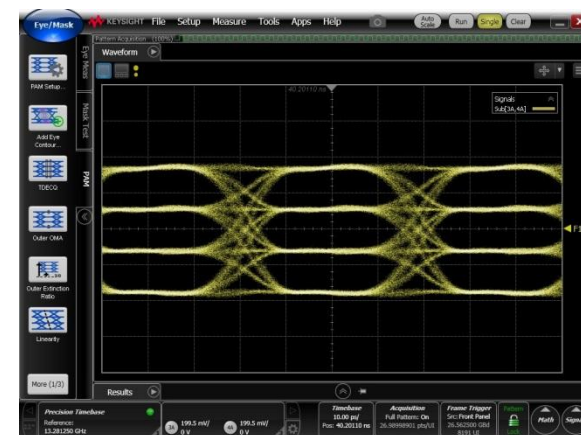
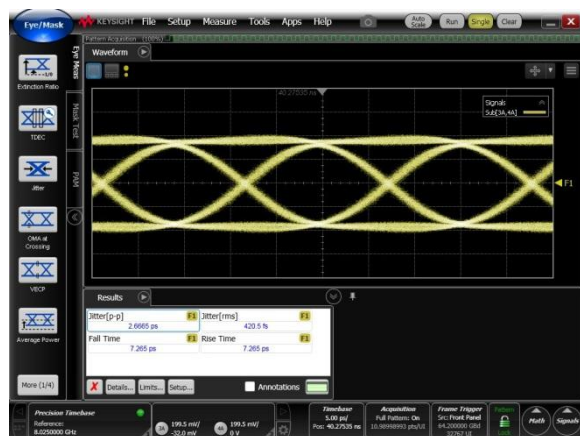
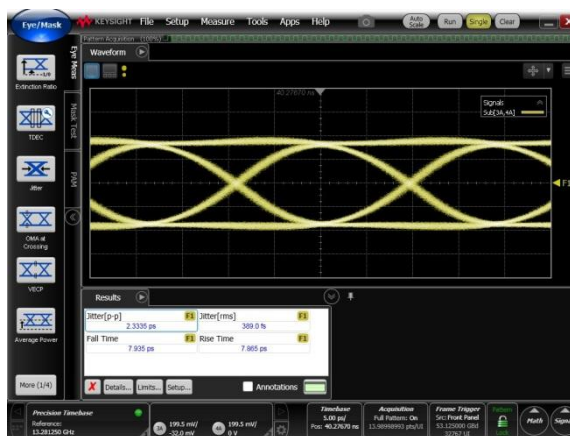
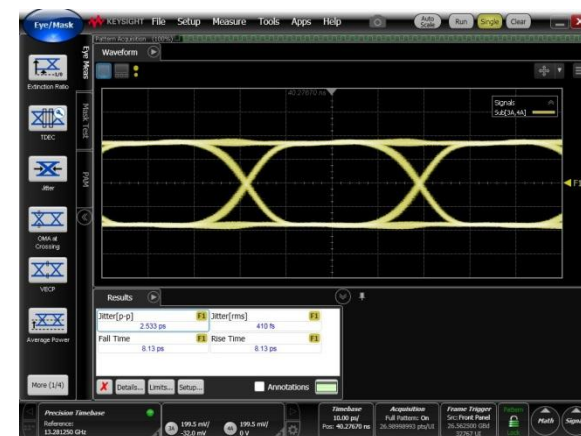
64.2 Gbaud



53.125 Gbaud



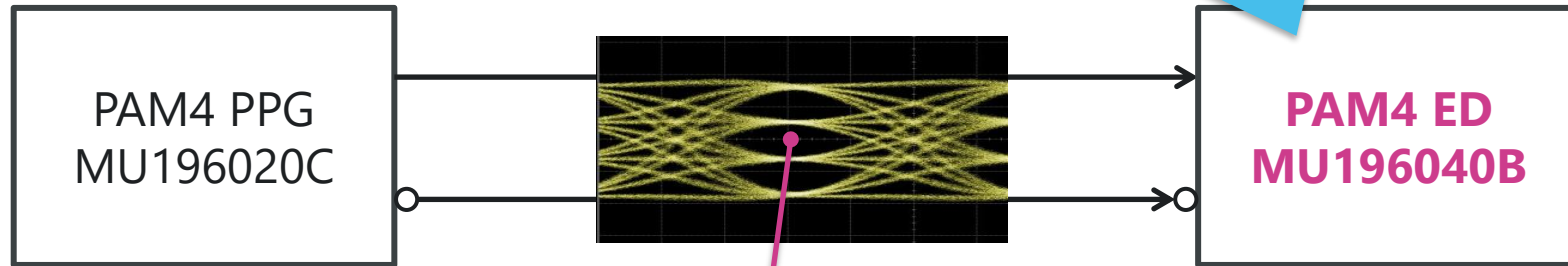
26.5625 Gbaud



Differential 1.4 Vp-p, PRBS13Q pattern, J1789A 40-cm cable + 70 GHz Scope

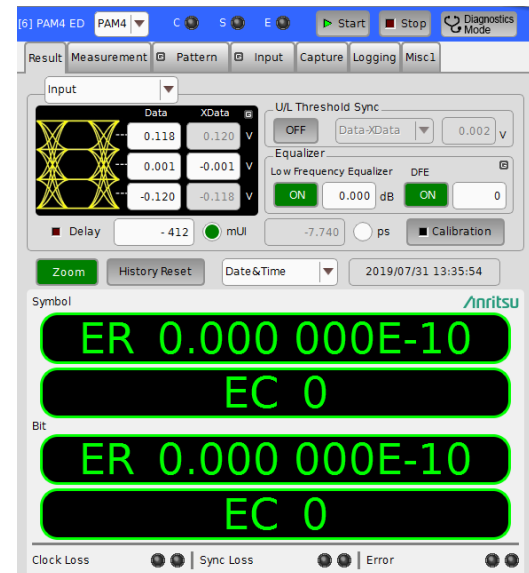
116 Gbit/s PAM4 Best Level High-Sensitivity Input Performance

High sensitivity input of 36 mV (typical at 53.125 Gbaud) simplifies previously difficult PAM4 error troubleshooting measurements.



Typ. 36 mV EH/ Eye

Error-Free at 53.125 Gbaud
Best level PAM4 sensitivity

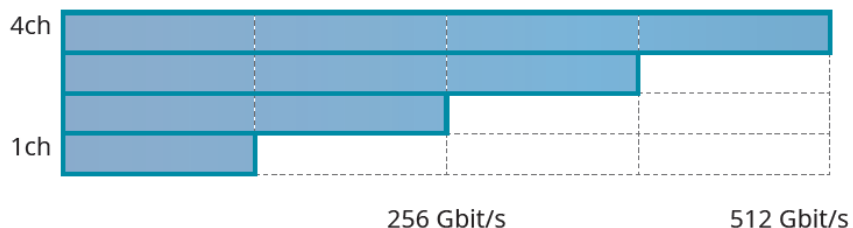


Multichannel Support and Expandability (1/2)

One MP1900A PPG supports up to 4ch for 400 GbE (53 Gbaud x 4 Lanes), and faster evaluations, helping cut future support upgrade costs.

PAM4 Solution

Max. 64 Gbaud at 1ch



• Channel Synchronization

One MP1900A unit supports synchronous output for up to 4ch; two units support up to 8ch.

*Future support for 8ch

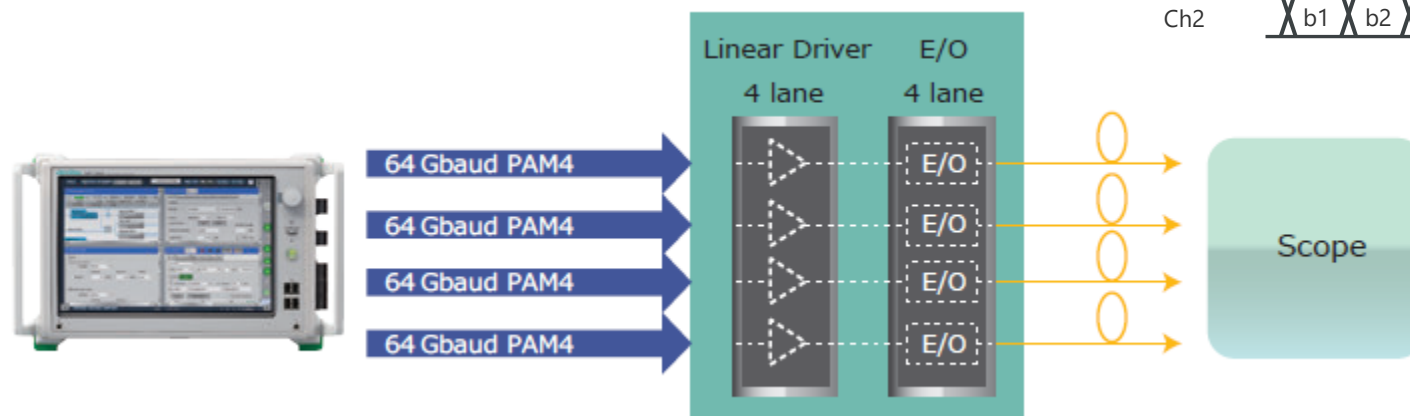
Ch1	X a1 X a2 X a3 X a4 X a5 X
Ch2	X a1 X a2 X a3 X a4 X a5 X
Ch3	X a1 X a2 X a3 X a4 X a5 X
Ch4	X a1 X a2 X a3 X a4 X a5 X

• 2ch Combination (NRZ)

Supports shift to "a1b1 a2b2 ..." pattern

Ch1	X a1 X a2 X a3 X a4 X a5 X
Ch2	X b1 X b2 X b3 X b4 X b5 X

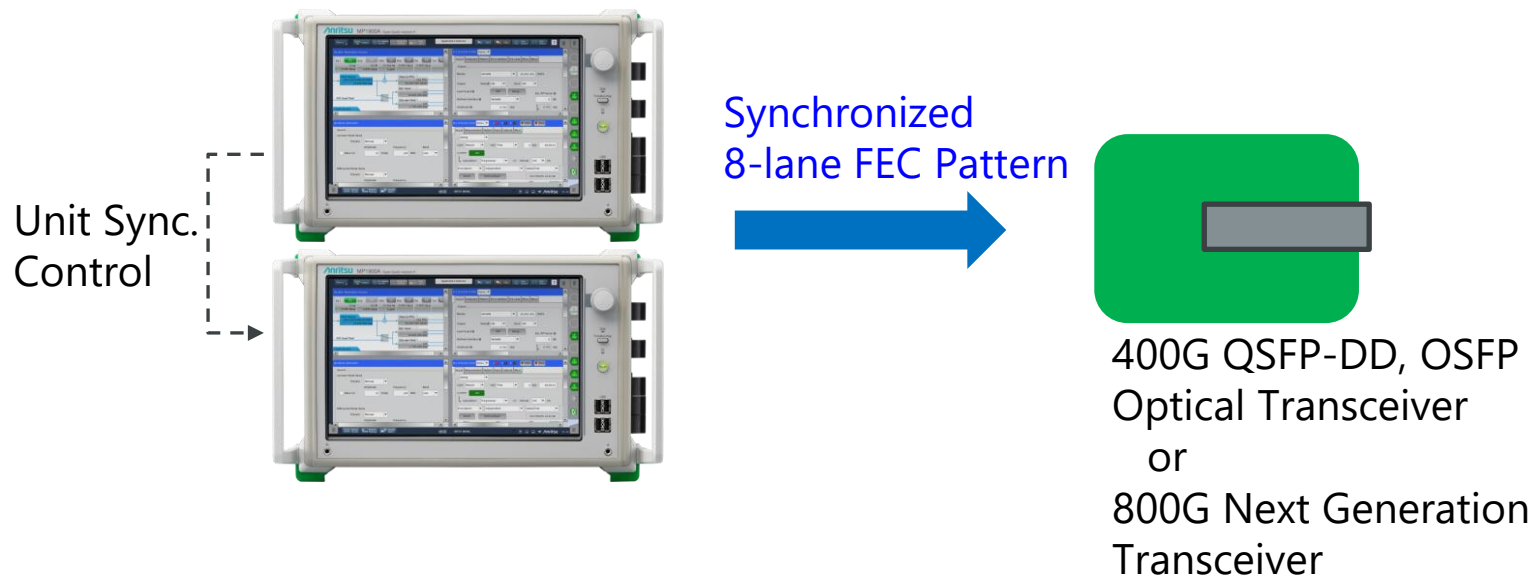
• 4-Lane DUT (Driver + E/O) Measurement Example



Multichannel Support and Expandability (2/2)

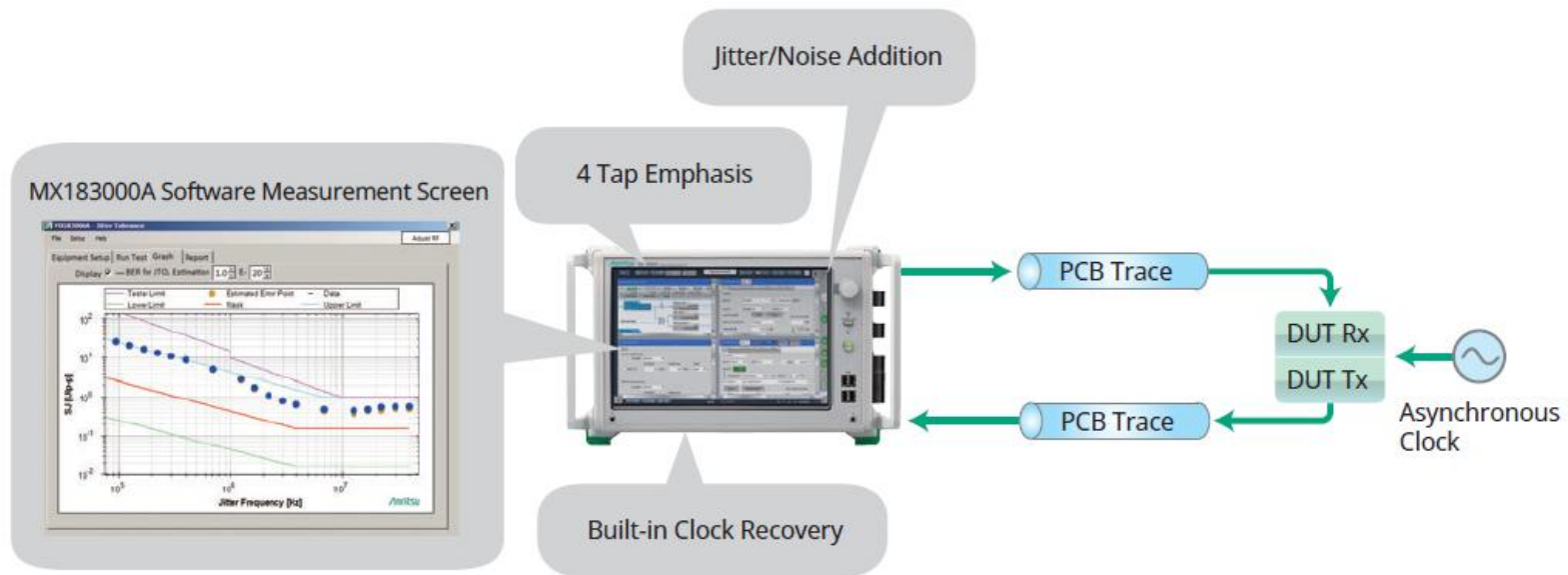
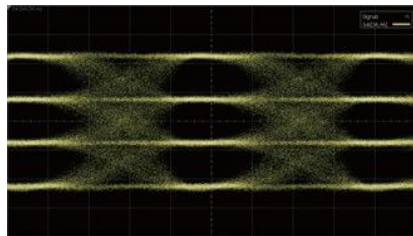
Expanded support for 800G using 8ch synchronization function
(4ch x 53.125 Gbaud PAM4 x two MP1900A units)

Supports QSFP-DD transceiver FEC evaluation using 8-lane FEC Pattern Generation function

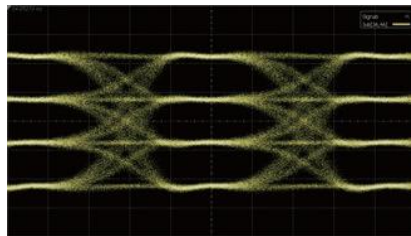


Jitter Tolerance Measurement Function

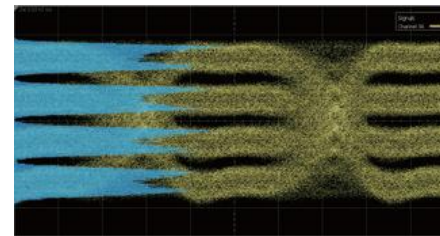
Supports PAM4 Jitter Tolerance test using just one unit. A measurement system to help cut measurement time is configured easily by combining the Jitter/Noise Addition function, built-in Clock Recovery function, and Jitter Tolerance MX183000A-PL001 software.



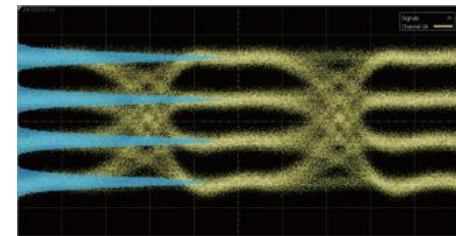
Sine-Wave Jitter (SJ)



Random Jitter (RJ)



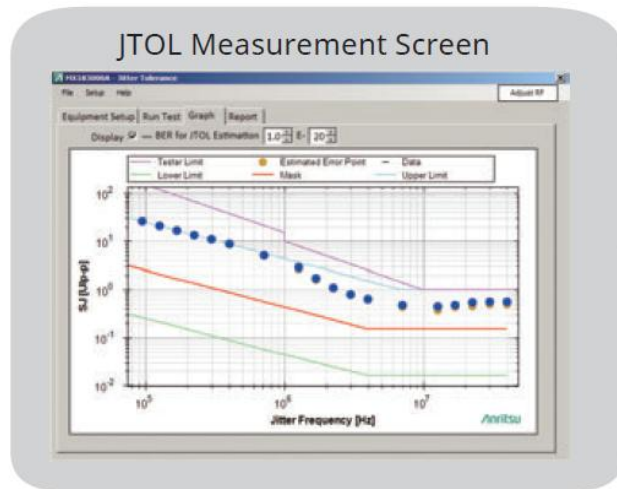
CM/DM Noise



White Noise

Jitter Tolerance Measurement using DUT BER Counter

When the DUT has a built-in bit error counter, combination with the MP1900A PPG makes it easy to configure a highly cost-effective Jitter Tolerance measurement environment.



Measure Jitter Tolerance using captured error count
(MX183000A-PL001 Jitter tolerance software)



PCB Trace

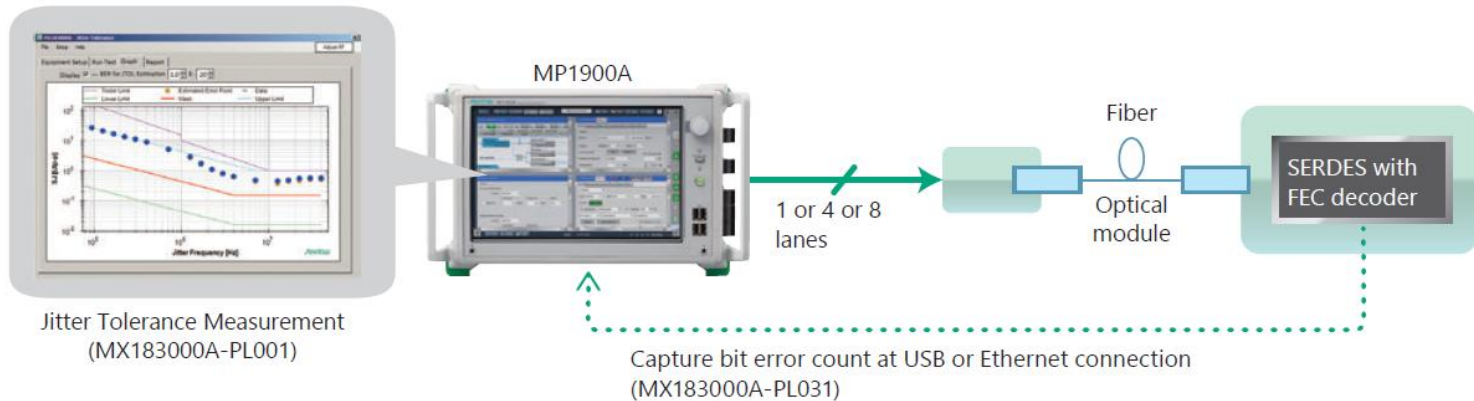


Capture error count via USB or Ethernet connection
(MX183000A-PL031 DUT Error Counts Import)

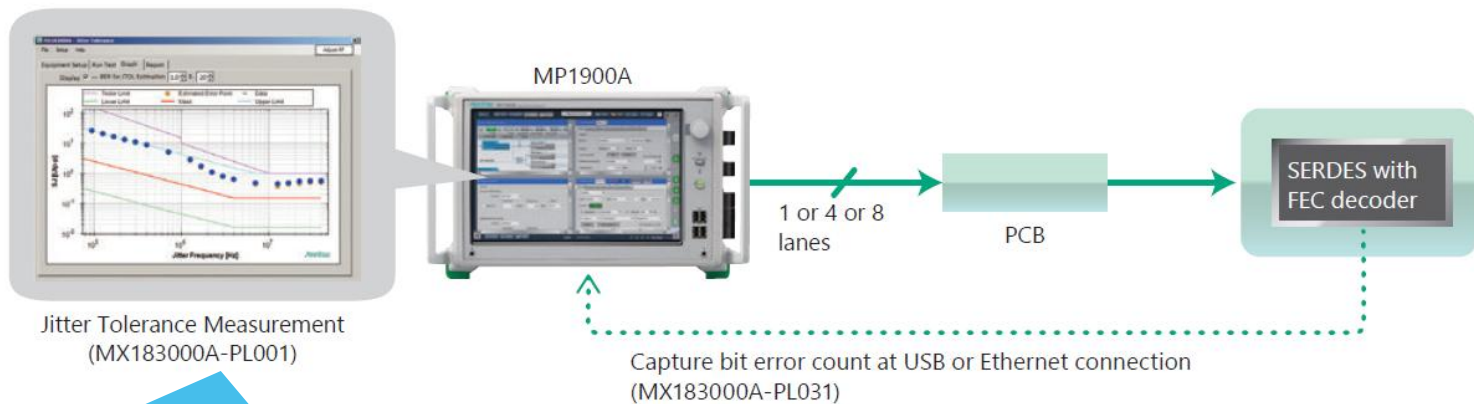
Multilane FEC Evaluation

FEC can be evaluated by combining FEC pattern generation with error insertion, and reading the DUT bit error count.

Evaluating Optical FEC Signal Transmission



Evaluating Electrical FEC Signal Transmission



Evaluate Jitter Tolerance, etc., using captured error count

MP1900A Mainframe

MP1900A Main Unit Features



MP1900A Front Panel



MP1900A Side Panel

- 8 Slots
- Install up to four 2ch PPG and ED modules
- Synchronize up to four MP1900A main units → Expansion to 2 Tbit/s
- Touch Screen
- GPIB x 1, and Ethernet x 2
- USB x 6, HDMI x 1, and D-SUB x 1
- Windows 10 IoT Enterprise



2 Tbit/s

Multi-channel Synchronized Output of Four MP1900A Main Units

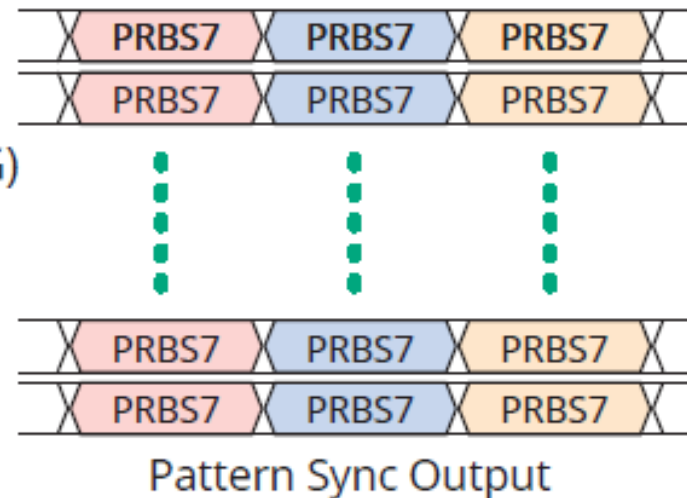
Future-proof Main Unit Expandability

- One Main Unit Supports 8ch (SIPPG) and 4ch (PAM4 PPG) Transmissions for Future High Bit Rates



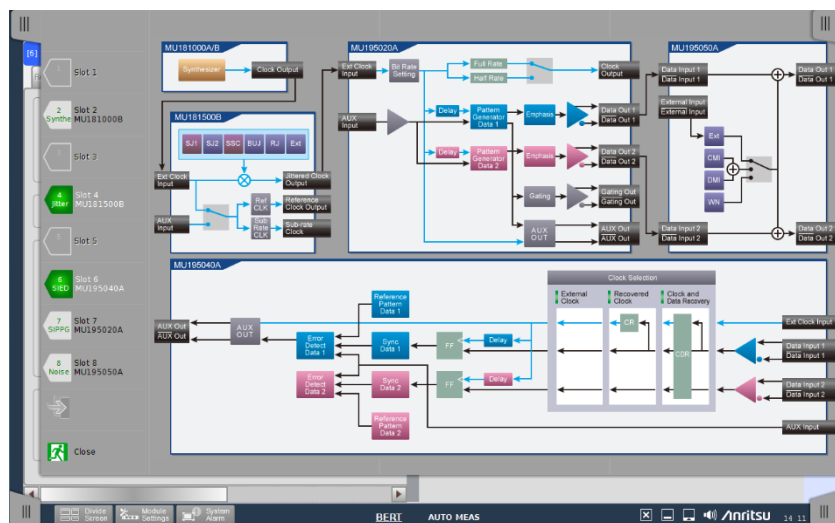
MP1900A

Differential
8ch (SIPPG)
4ch (PAM4PPG)

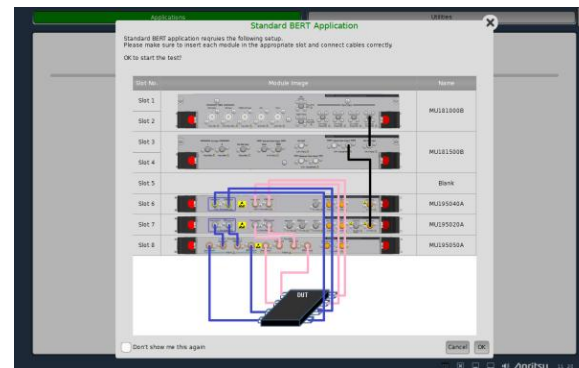


System View User Interface and Improved Operability using Multiple Windows

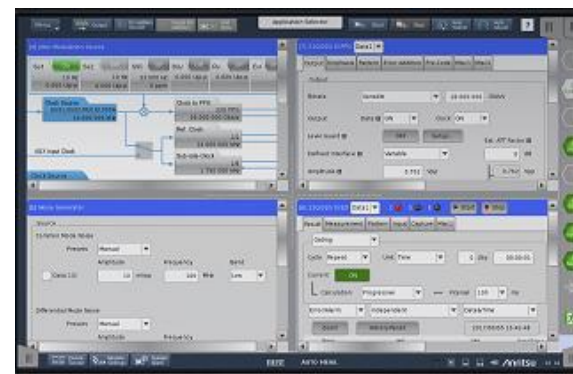
Operability is improved by the large 12.1-inch LCD touch panel and intuitive GUI. The newly developed System View user interface displays easy-to-understand system function blocks with help guidance for system settings and easy operation of each module.



System View User Interface

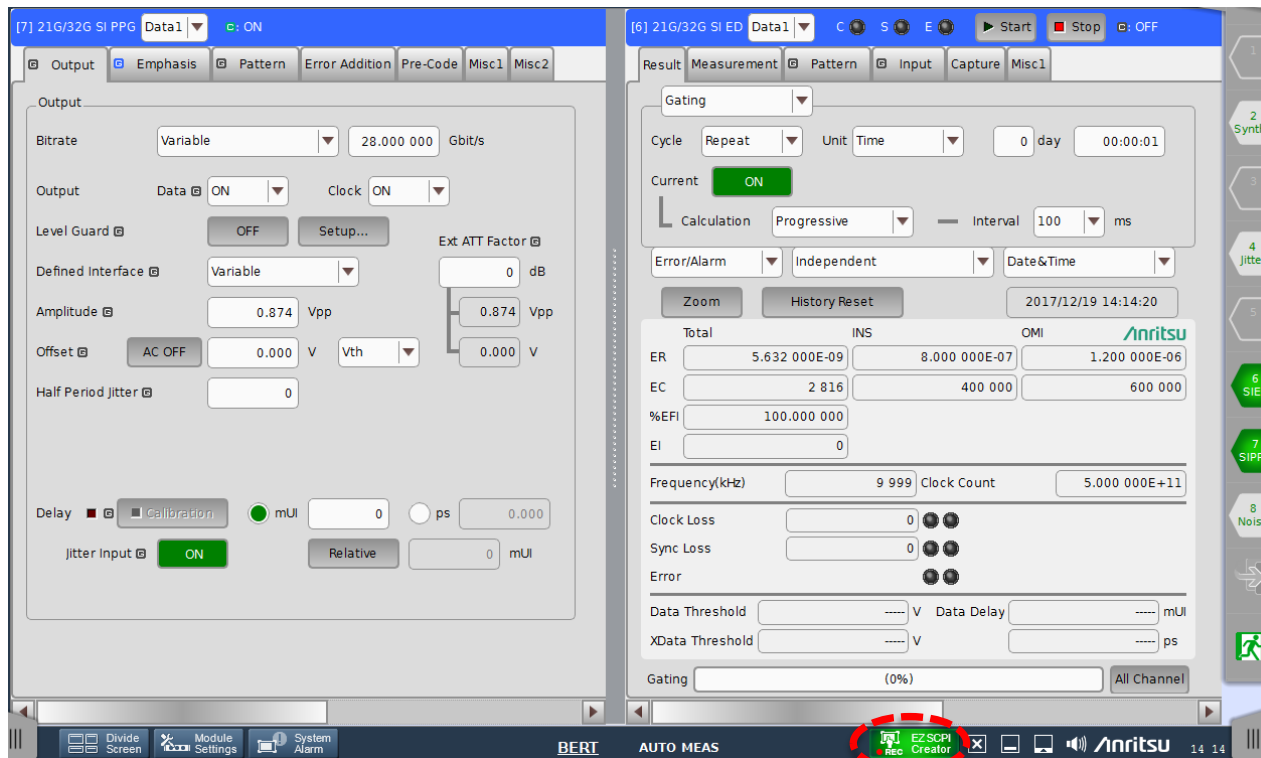


Setup Instructions



4ch Multi-channel Measurement Results on One Screen

Operation while EZ SCPI Creator is ON creates remote command strings automatically, making it easy to describe remote commands.



EZ SCPI Creator ON

For example, executing the following operations:

- Set PPG Amplitude
- Set PPG Pattern Type
- Set PPG PRBS Length
- Set Output On
- Start ED measurement



Automatically generates these operation remote commands

```
:UENtry:ID 1; :MODule:ID 7; :INTERface:ID 1; :OUTPut:DATA:AMPLitude DATA,0.574
:UENtry:ID 1; :MODule:ID 7; :INTERface:ID 1; :SOURce:PATtern:TYPE PRBS
:UENtry:ID 1; :MODule:ID 7; :INTERface:ID 1; :SOURce:PATtern:PRBS:LENG 31
:SOURce:OUTPut:ASET ON
:UENtry:ID 1; :MODule:ID 6; :INTERface:ID 1; :SENSe:MEASure:STAR
```

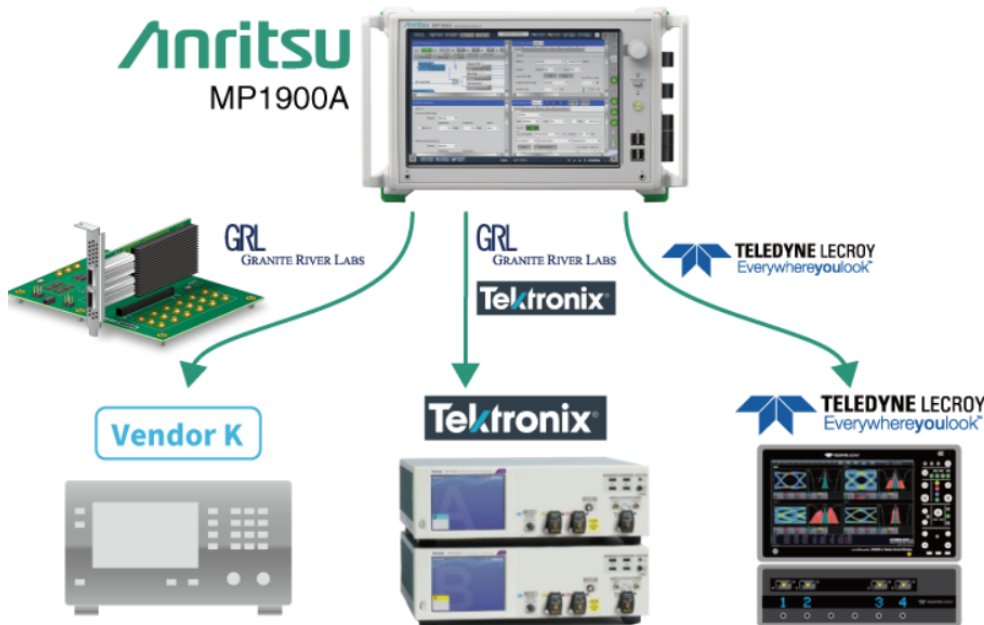
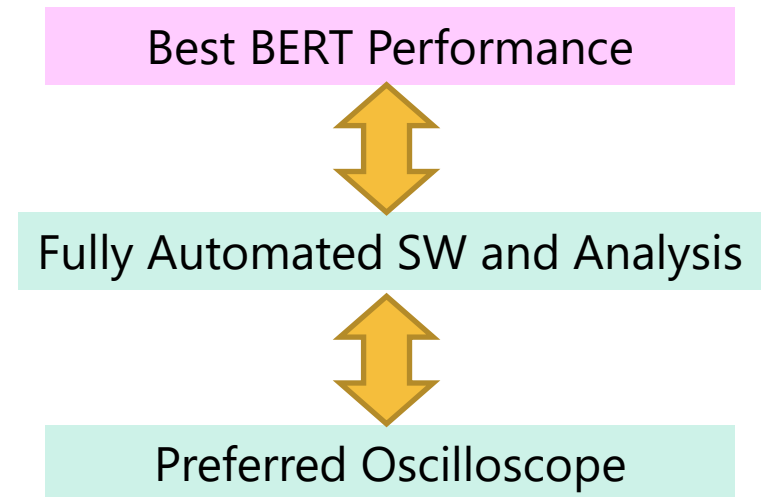
PCIe Test Solution

PCIe Tx LEQ/Rx Compliance Test

- Combination of best-performance BERT MP1900A and preferred oscilloscope -

Shorter test times and reduced investment cost

- Supports Combination with Teledyne LeCroy/Tektronix/Keysight Real-Time Oscilloscopes
- Automated Rx CEM and Base Tests: Calibration, Link EQ and Automated Tx Test
- Protocol Aware: Link Training/Equalization and LTSSM Analysis
- High-Expandability 32G Multichannel BERT for PCIe1 to 6



Measurement Item	Supported Software
Transmitter Test	Teledyne LeCroy, Tektronix, GRL*
Tx Response Time	MX183000A-PL021 PL025 (PCIe5) PL026 (PCIe6)
Stressed Signal Calibration	Teledyne LeCroy, Tektronix, GRL*
Transition to Loopback State	MX183000A-PL021 PL025 (PCIe5) PL026 (PCIe6)
Rx Link Equalization Test	MX183000A-PL021
Jitter Tolerance Test	MX183000A-PL001
PLL Loop Bandwidth Test	Teledyne LeCroy, Tektronix, GRL*

*Contact your sales representative about expected future support.

PCIe Link Training, LTSSM Analysis and Jitter Tolerance Measurements (1/5)

PCIe PHY IP Device Rx Test Sequence

Stress Signal Calibration

Transition to
Loopback Status

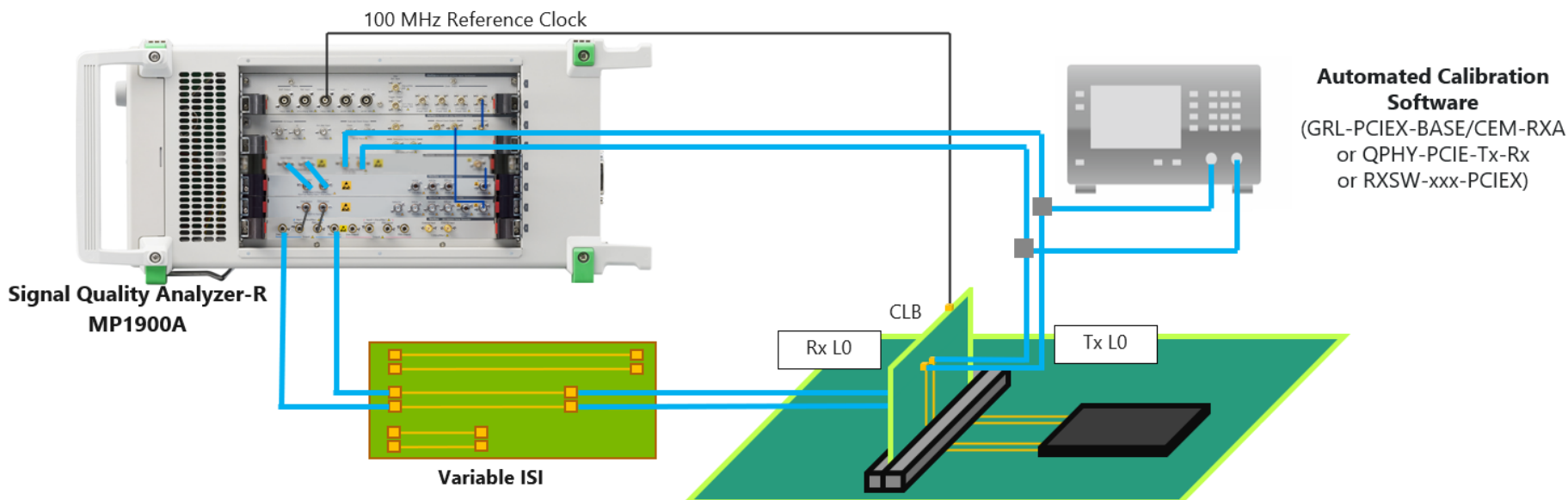
Stress Signal Input
Test

Applicable Software

Automation Software:
GRL-PCIEX-BASE/CEM-RXA
or QPHY-PCIE-Tx-Rx
or RXSW-xxx-PCIEX

Link Training Software:
MX183000A-PL021 (PCIe1 to 4)
MX183000A-PL025 (PCIe5 Extension) or
MX183000A-PL026 (PCIe6 Extension)

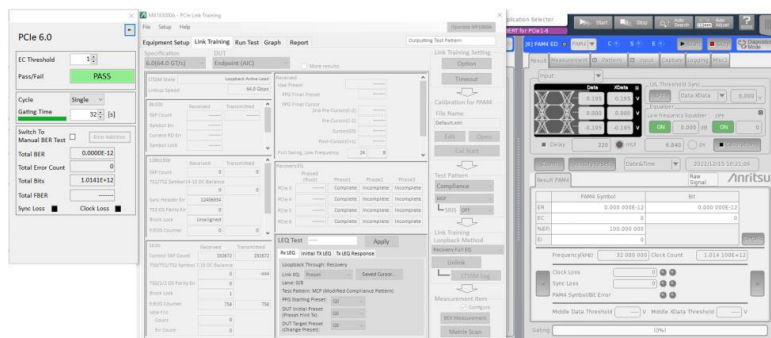
- Jitter Tolerance Margin Test:
MX183000A-PL001
- Jitter Sweep Test (Pass/Fail):



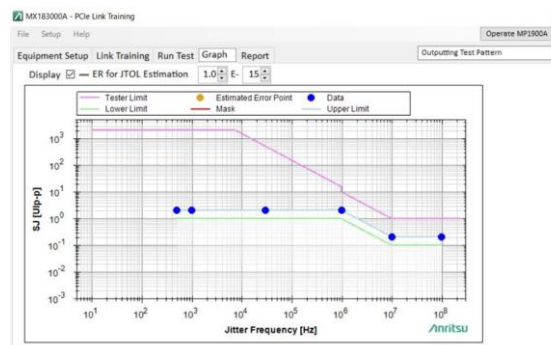
PCIe Link Training, LTSSM Analysis and Jitter Tolerance Measurements (2/5)

Combining the PCIe Link Training MX183000A-PL021 and Jitter Tolerance Test MX183000A-PL001 software supports tests from the Link with the DUT to the Jitter Tolerance test measurements required by PCIe receiver tests.

Displays Link Training Settings and Results



Automatic Measurement of Receiver Jitter Tolerance



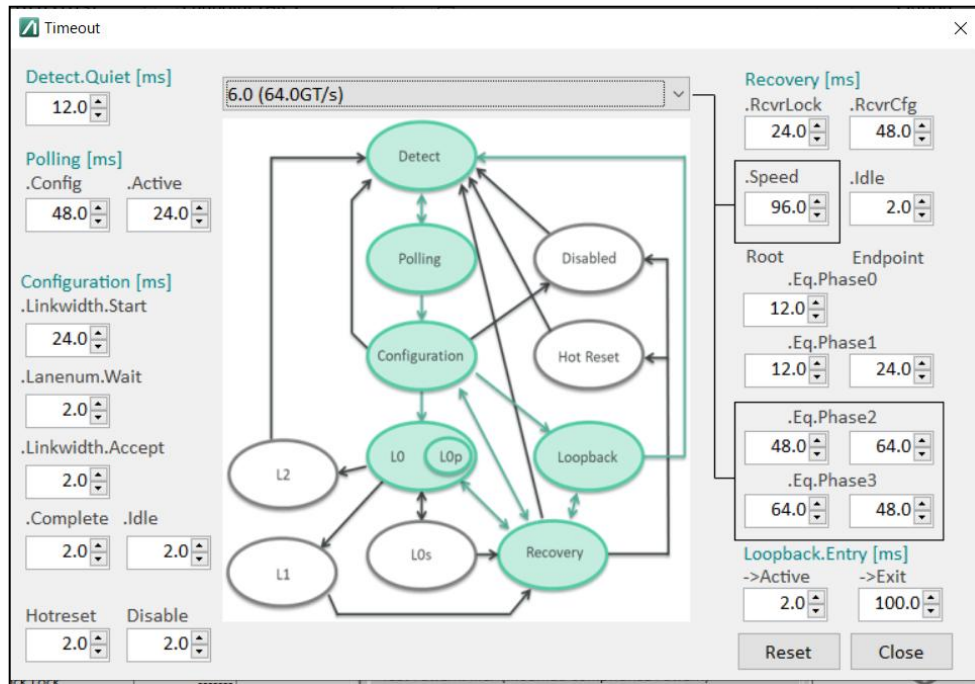
Item	MX183000A-PL021	PL025 extended	PL026 extended
Supported Standard	PCIe 1 (2.5 GT/s), PCIe 2 (5 GT/s), PCIe 3 (8 GT/s), PCIe 4 (16 GT/s)	PCIe 5 (32 GT/s)	PCIe 6 (64 GT/s)
Pattern	Compliance (MCP, CP), PRBS (7, 9, 10, 11, 15, 20, 23, 31)		
LTSSM State	Transition to Detect, Polling, Configuration, Recovery, Loopback		
Loopback Through	Configuration, Recovery	Config EQ 32G Config no EQ 32G Recovery EQ 32G Recovery Full EQ	Config EQ 64G Config no EQ 64G Recovery EQ 64G Recovery Full EQ
TS Setting Parameter	SKP Insertion, 8B/10B, 128B/130B, FTS, Link Number, Lane Number, Scrambling		-> +1b/1b

PCIe Link Training, LTSSM Analysis and Jitter Tolerance Measurements (3/5)

Shorter Development Period by LTSSM Analysis Functions for Troubleshooting Cause of Link Faults

Examine each state transition time and path from "Detect" to "Loopback".

Check results for each state transition using Training Log Viewer.

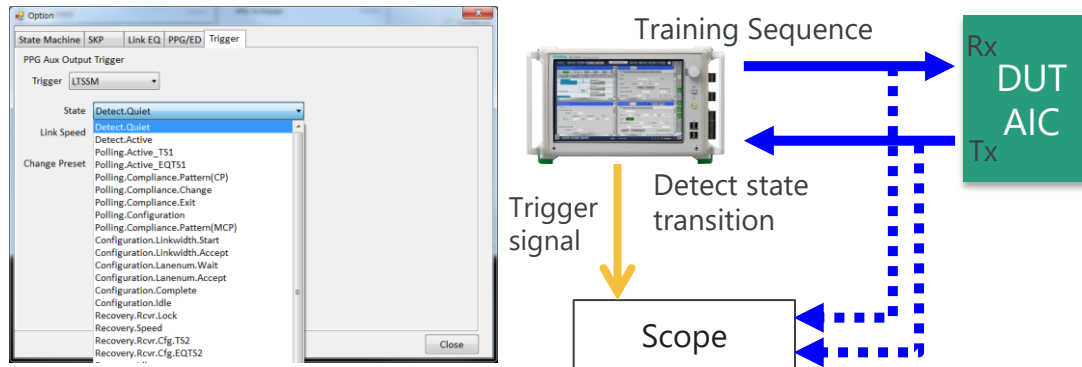


The screenshot displays the Training Log Viewer window, which contains a table of state transition data. The table has the following columns: Time [ns], Δ Time [ns], State, Speed[GT/s], and Detect Pres.

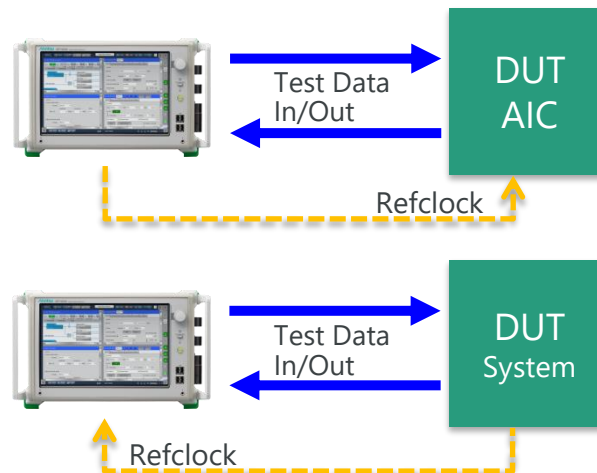
Time [ns]	Δ Time [ns]	State	Speed[GT/s]	Detect Pres
79,789,516	1,192	RECOVERY_IDLE (Fit Mode)	32.0	---
79,790,708	12	L0 (Fit Mode)	32.0	---
79,790,720	2,704	RECOVERY_RCVR_LOCK	32.0	---
79,793,424	1,004	RECOVERY_RCVR_CFG_EQTS2	32.0	---
79,794,428	9,034,092	RECOVERY_RCVR_CFG_EQTS2	32.0	---
88,828,520	100,016	RECOVERY_SPEED	32.0	---
88,928,536	32	RECOVERY_SPEED	64.0	---
88,928,568	4	RECOVERY_RCVR_LOCK	64.0	---
88,928,572	8,929,104	RECOVERY_EQUALIZATION_PHASE1_TSO...	64.0	---
97,857,676	1,380	RECOVERY_EQUALIZATION_PHASE1_TSO...	64.0	---
97,859,056	8	RECOVERY_EQUALIZATION_PHASE1_TSO...	64.0	---
97,859,064	1,396	RECOVERY_EQUALIZATION_PHASE2_TSO...	64.0	0 [MP1900A] > DUT
97,860,460	4	RECOVERY_EQUALIZATION_PHASE2_TS1...	64.0	1 [MP1900A] <= DUT
97,860,464	26,143,048	RECOVERY_EQUALIZATION_PHASE2_TS1...	64.0	0 [MP1900A] > DUT
124,003,512	2,000,008	RECOVERY_EQUALIZATION_PHASE3_TS1...	64.0	0 [MP1900A] > DUT
126,003,520	1,999,992	RECOVERY_EQUALIZATION_PHASE3_TS1...	64.0	1 [MP1900A] <= DUT
128,003,512	2,000,008	RECOVERY_EQUALIZATION_PHASE3_TS1...	64.0	0 [MP1900A] > DUT
130,003,520	1,999,992	RECOVERY_EQUALIZATION_PHASE3_TS1...	64.0	1 [MP1900A] <= DUT
132,003,512	1,392	RECOVERY_RCVR_LOCK	64.0	---
132,004,904	500	RECOVERY_RCVR_CFG_TS2	64.0	---
132,005,404	1,400	LOOPBACK_ENTRY_LEAD_TS1	64.0	---
132,006,804	0	LOOPBACK_ACTIVE_LEAD	64.0	---

PCIe Link Training, LTSSM Analysis and Jitter Tolerance Measurements (4/5)

Generate trigger at LTSSM transition timing to support examination using oscilloscope waveform.



Supports both common and separate Refclock test architectures and SRIS

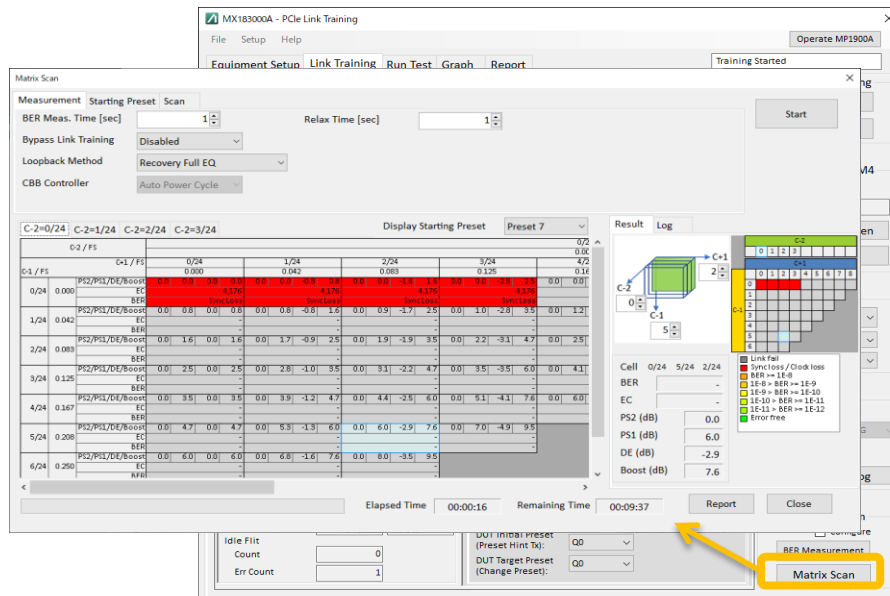


PCIe Link Training, LTSSM Analysis and Jitter Tolerance Measurements (5/5)

Matrix Scan Function

To ensure high quality communication with link partners on routes with high channel loss, it is necessary to select the optimum combination of Tx and Rx equalizers.

The Matrix scan function scans for the best Tx EQ setting at the receiver to find the best setting automatically at the receiver.



Graphical display of BER measurement results for each DUT Tx Preset setting

Checking DUT Receiver Equalizing Characteristics

The DUT receiver equalizing characteristics can be checked from the BER results after Loopback at BER measurement by changing the PPG output signal equalization by making any settings using either presets or the cursor.

PCIe 6.0

Preset Manual BER Measurement

EC Threshold 1

Pass/Fail

Cycle Single

Gating Time 32 [s]

Switch To Manual BER Test ☐ Error Addition

Total BER 3.6540E-06

Total Error Count 4176

Total Bits 1.0791E+09

Total FBER

Sync Loss ☐ Clock Loss ☐

Q7 : -2.9, 4.7, 0.0

Q0 : 0.0, 0.0, 0.0

Q1 : 0.0, 1.6, 0.0

Q2 : 0.0, 3.5, 0.0

Q3 : 0.0, 0.0, -1.6

Q4 : 0.0, 0.0, -3.5

Q5 : -1.3, 4.7, 0.0

Q6 : -1.6, 3.5, -3.5

Q7 : -2.9, 4.7, 0.0

Q8 : -3.5, 6.0, 0.0

Q9 : -4.4, 6.9, -1.6

Q10 : 0.0, 0.0, -9.5

Preset

Coefficient Calibrated Setting

C-2 0 0.0000 0.0000

C-1 0 0.0000 0.0000

C0 24 1.0000 1.0000

C+1 0 0.0000 0.0000

Calibrated Setting

PS2 0.0 0.0 dB

PS1 0.0 0.0 dB

DE 0.0 0.0 dB

Boost 0.0 dB

C-2=0/24 C-2=1/24 C-2=2/24 C-2=3/24

C-2	C+1	0/24	1/24	2/24	3/24	4/24	5/24	6/24	7/24	8/24
C-1	0.0000	0.0417	0.0833	0.1250	0.1667	0.2083	0.2500	0.2917	0.3333	
0/24	0.0000	0.000,0.0	0.000,0.8	0.000,1.6	0.000,2.5	0.000,3.5	0.000,4.7	0.000,6.0	0.000,7.6	0.000,9.5
1/24	0.0417	0.008,0.0	0.008,0.8	0.009,1.7	0.012,2.8	0.012,3.9	0.013,5.3	0.016,6.8	0.019,8.8	
2/24	0.0833	0.016,0.0	0.017,0.9	0.019,1.9	0.022,3.1	0.023,4.4	0.029,6.0	0.033,8.0		
3/24	0.1250	0.023,0.0	0.028,1.0	0.031,2.2	0.033,3.5	0.041,5.1	0.049,7.0			
4/24	0.1667	0.033,0.0	0.039,1.2	0.044,2.5	0.051,4.1	0.060,6.0				
5/24	0.2083	0.047,0.0	0.053,1.3	0.060,2.9	0.070,4.9					
6/24	0.2500	0.060,0.0	0.068,1.6	0.080,3.5						

Cursor

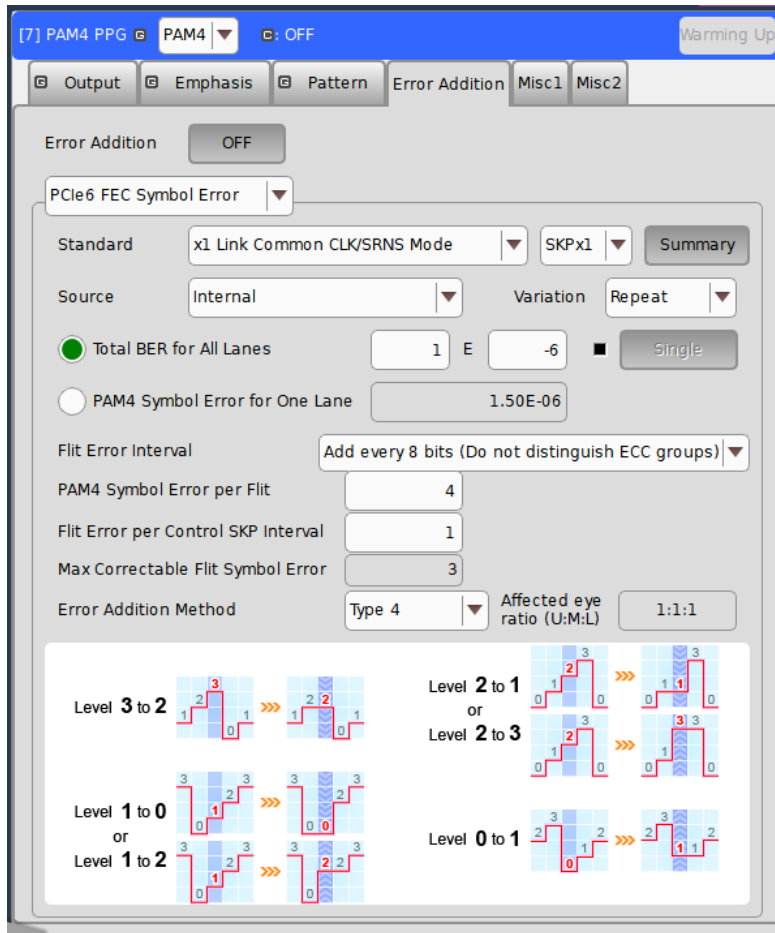
The data rate for PCIe standards has consistently doubled with each generation. While PCIe5 and earlier used the NRZ modulation method, PCIe6 adopted the PAM4 modulation method and introduced PCIe's own FEC (forward error correction) technology to ensure error correction and throughput.

Since the types of correctable errors differ, it is important to distinguish between FEC-correctable errors and non-FEC-correctable errors.

The MP1900A has the following PCIe FEC verification features

- 1. PPG FEC Error Addition function(PAM4 PPG)**
- 2. FEC Error Distribution function (PAM4 ED)**
- 3. FEC Capture function (PAM4 ED)**

Verification of FEC Ability



Key Features

PPG Error Addition function to add various types of error to FLIT (Flow Control Unit) data, helping verify the DUT FEC capability under stress conditions.

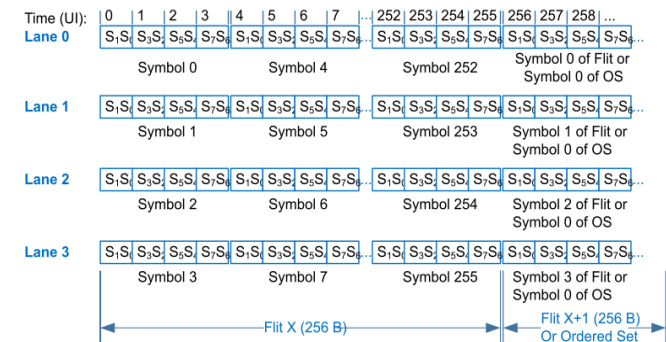


Table 4-12 Flit interleaving in a x4 Link

Description		Lane			
		0	1	2	3
512 UI	TLP Bytes [0...235]	0	1	2	3
		4	5	6	7
		8	9	10	11
		...	...	...	...
		224	225	226	227
		228	229	230	231
		232	233	234	235
		DLP 0	DLP 1	DLP 2	DLP 3
		DLP 4	DLP 5	CRC 0	CRC 1
		CRC 2	CRC 3	CRC 4	CRC 5
512 UI	DLP, CRC, ECC Bytes	CRC 6	CRC 7	ECC1 [0]	ECC2 [0]
		ECC0 [0]	ECC1 [1]	ECC2 [1]	ECC0 [1]

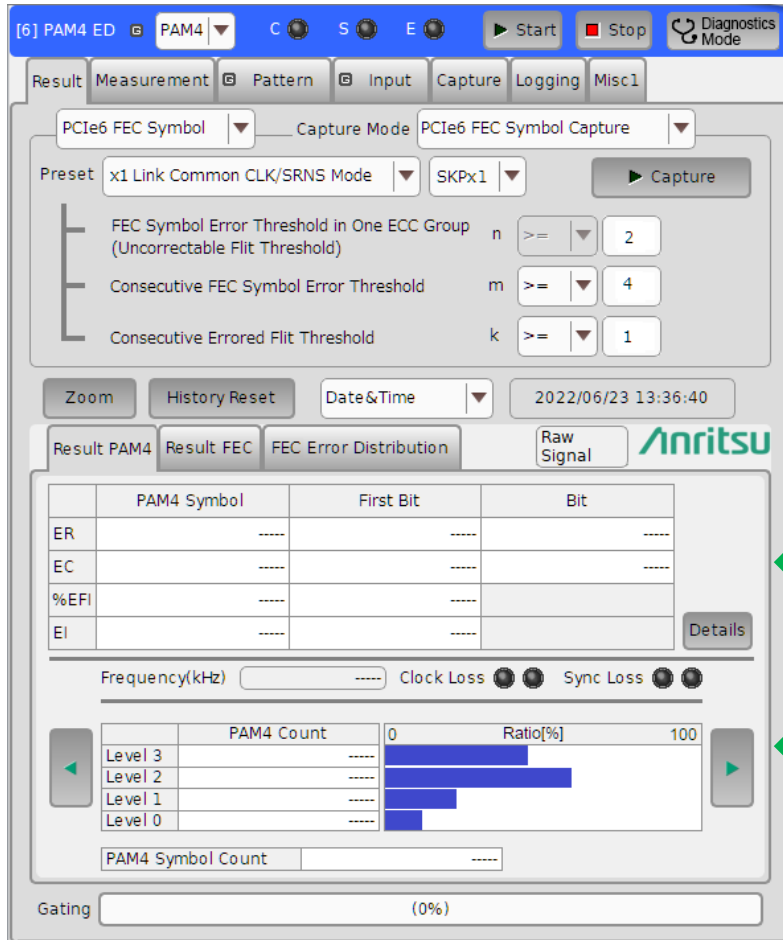
symbol placement in a x4 Link with 1b/1b encoding

PCle FEC is 3-way interleaved ECC Each ECC group can be corrected by one symbol ECC code is the last 6 symbols of the flit

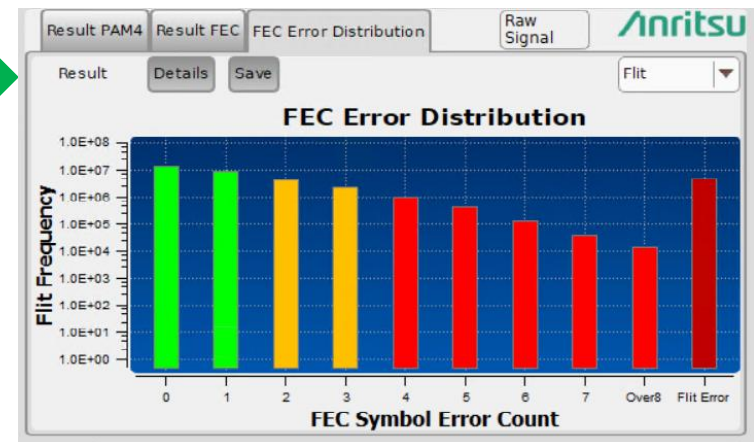
Real-time BER and FEC Error Distribution

Key Features

- FEC Error Distribution function for measurement and real-time display of correctable and uncorrectable errors. This allows accurate evaluation of the correction capability by FEC even at receiver tests with FBER (First Bit Error Rate) 1E-6 threshold.
- PAM4 Symbol Error Rate/Count
- First Bit Error Rate/Count
- Bit Error Rate/Count
- Uncorrectable .Flit Error Rate/Count
- FEC Symbol Error Rate/Count
- FEC Error Distribution

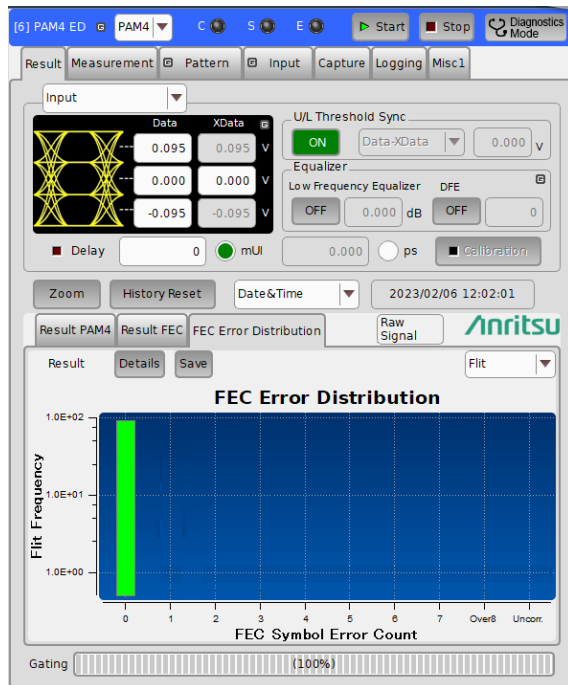
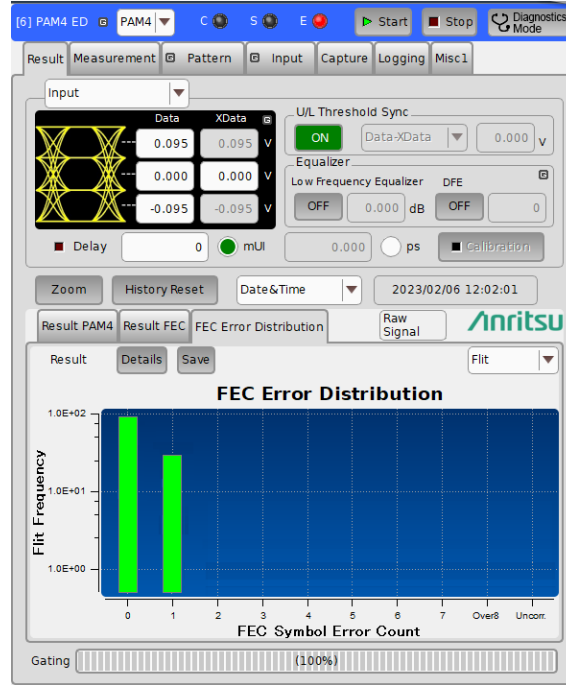


	Flit	FEC Symbol	Bit
ER	1.513 700E-01	3.997 900E-03	5.001 900E-04
EC	4 718 920	3.190 600E+07	3.199 600E+07
%EFI	0.000 000	0.000 000	
EI	10	10	

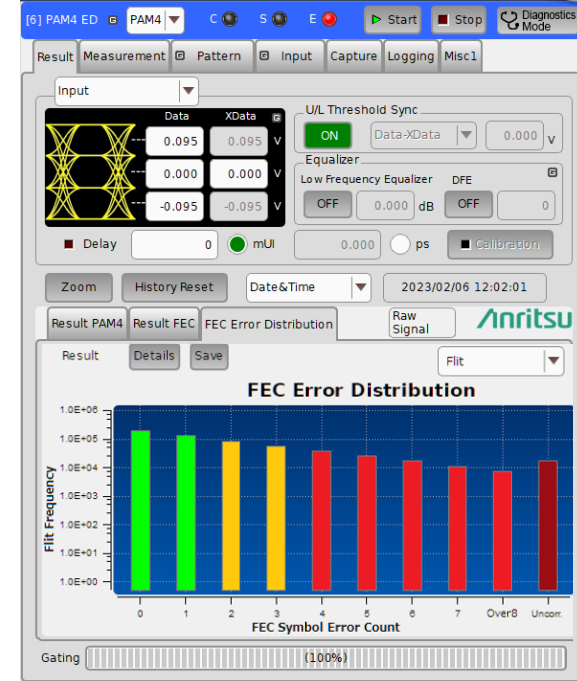


Stress vs FLIT FEC Error Distribution Example

Error Free



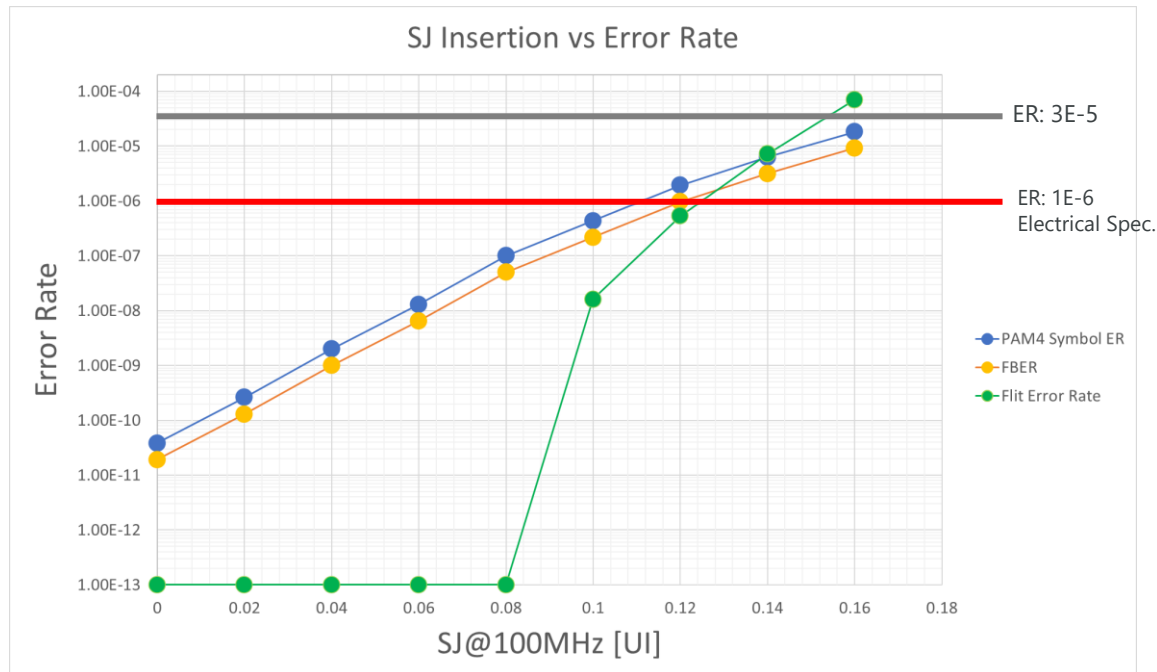
FLIT FEC Errors



Stress Injection

Verification Example Using FEC Analysis

This graph is an example of validating the FEC vs BER theoretical behavior using the MP1900A. The electrical specification parameters along with the FBER (First Bit Error Rate) of $<10^{-6}$ described in Electrical Sub-Block must be met to ensure the probability of a FLIT error after FEC is less than 3×10^{-5} . The validation result proves the theory that FLIT BER is 3×10^{-5} or less when FBER is 10^{-6} or less. As described, the MP1900A proves this behavior through actual measurements.



Measurement Condition

Loss Value: 12 inch of PCIe 5 Base CBB Rev4

SSC, RJ, DMI, CMI: OFF

SJ: 0 to 0.16UI (Swept)

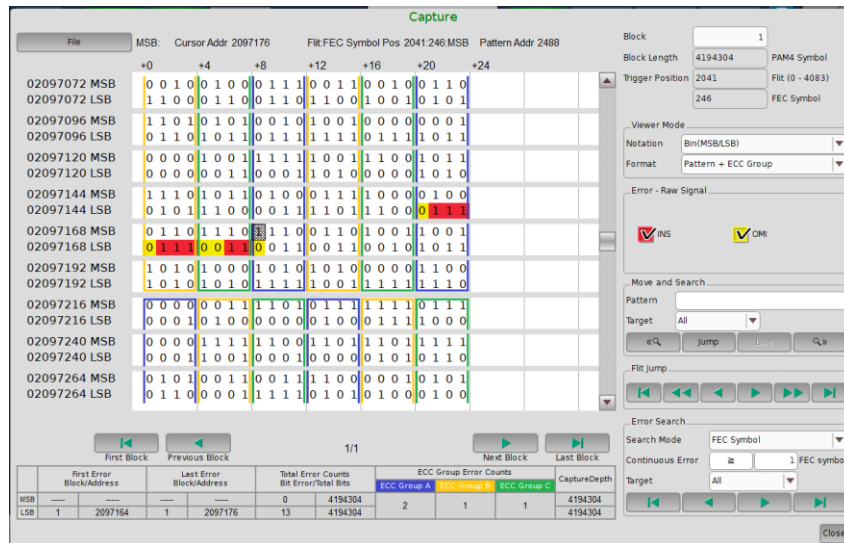
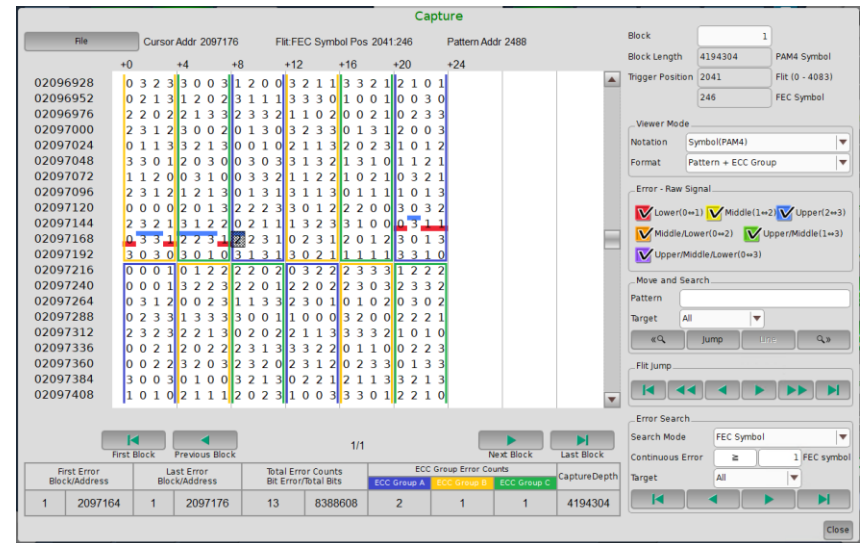
Tx Amplitude: 800 mVp-p @ before CBB Fixture

Tx EQ/DUT EQ: Best BER setting

Test Pattern: NOP FLIT x1

FEC Capture Function

FEC Capture function to capture Burst and other errors causing FLIT loss, supporting analysis of infrequent system failures and identification of cause, which can be time-consuming otherwise.



1. Various Displays

- MSB/LSB and PAM4 Symbol display switching and pattern analysis
- Color-coded Error type and Group identification
- Bit and Error count summaries

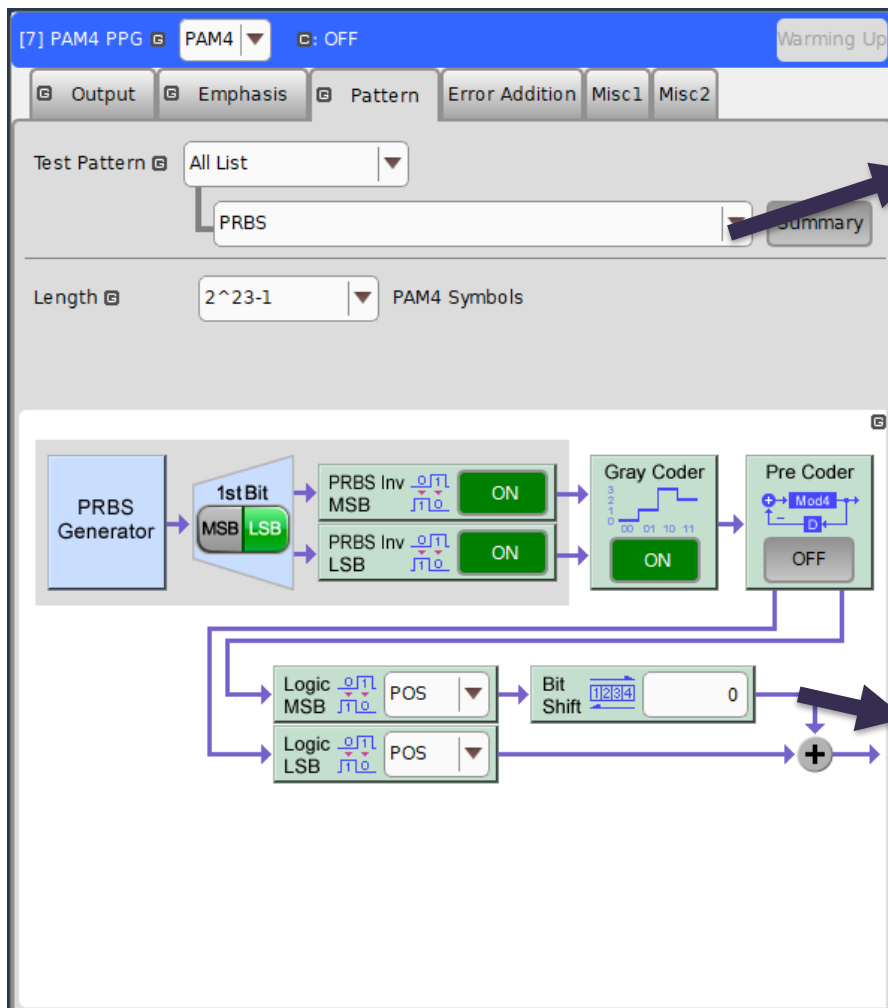
2. Pattern/Filter Searches

- Captured data search for specified pattern strings and consecutive Error counts
- Jump to FLIT head or FLIT block head positions

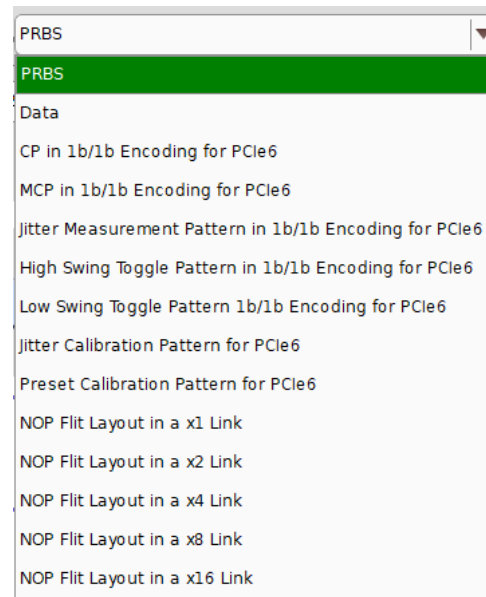
3. Other Useful Functions

- Capture start trigger using pattern sync or Error occurrence condition
- Save and load captured data pattern

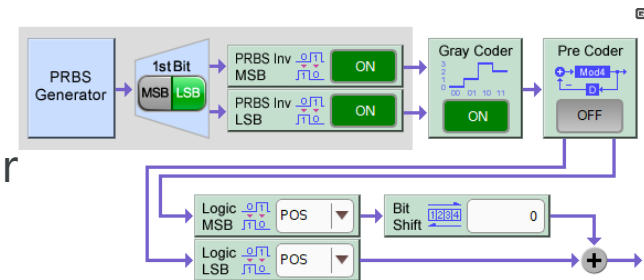
Intuitive Pattern Setting



Preset
Patterns



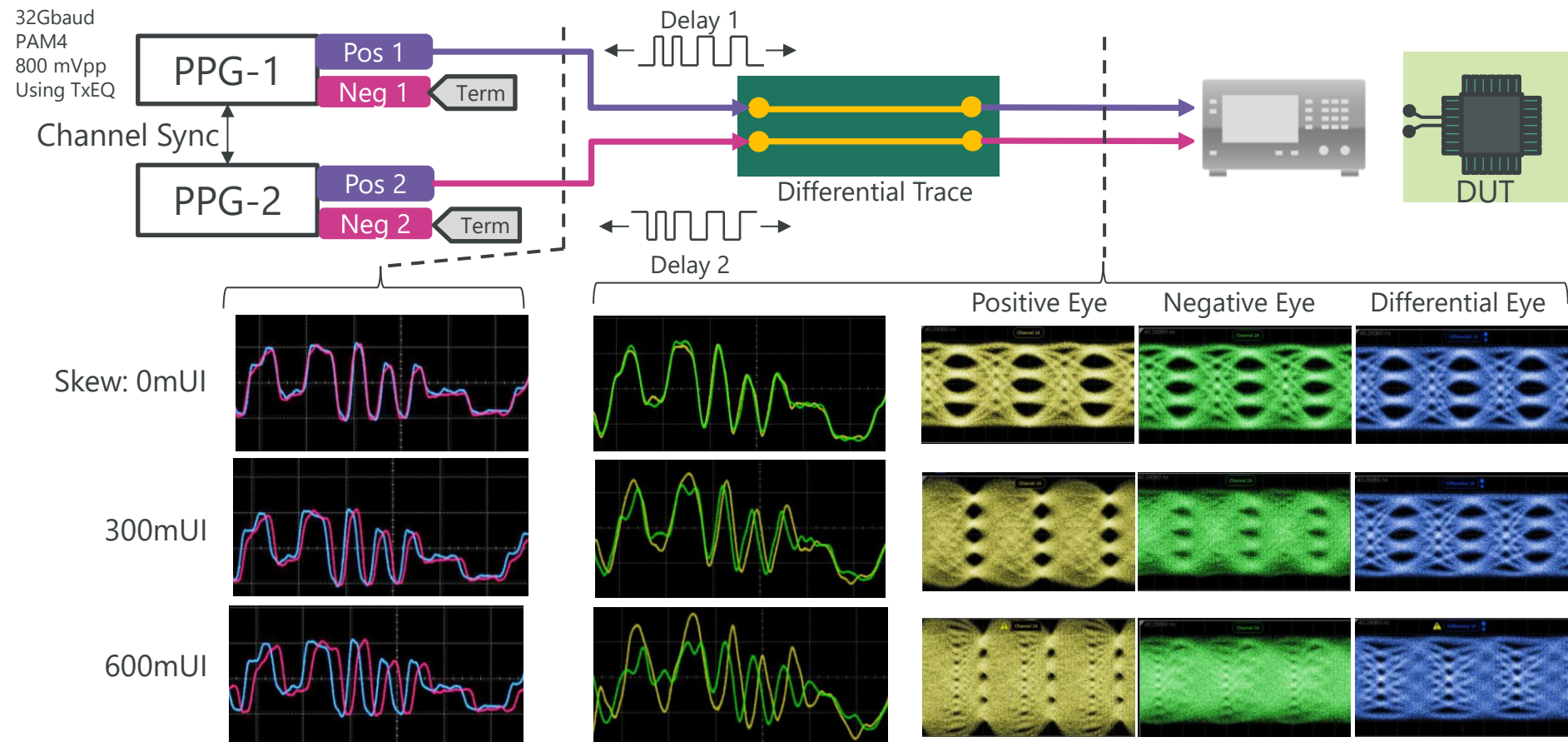
- First bit
- Polarity
- Gray Code
- Pre Code
- MSB/LSB
- Bit Shift



Skew Evaluation Solution

The MP1900A can adjust differential skew using its multi-channel synchronization function.

The coupled Positive/Negative lines in a differential line degrade Skew of both the Differential waveform and waveforms on each single line. Since this is asymmetric distortion, it cannot be compensated by the receiver (Rx) De-skew and this distortion can worsen the system BER. The MP1900A can perform this verification using the actual equipment, contributing to the detection and resolution of problems.



*Differential skew function requires two MU196020C (Opt-50) units.

PCIe Receiver Test Recommended Configuration

Model	Name	Option	Qty	Remark
MP1900A	Signal Quality Analyzer-R	-	1	
MU191000A	Synthesizer	-	1	
MU181500B	Jitter Modulation Source	-	1	
MU196020A	PAM4 PPG	001, 011, 060* ² , 043, (002)* ¹	1	*1: Required for 58 Gbaud Ethernet measurement *2: Contact Anritsu about option retrofit.
MU196040B	PAM4 ED	001, 011, 041, 043 (002, 022, 023)* ¹	1	
MU195040A* ³	SI ED	001, 010 or 020, 011 or 021, 022	1	For PCIe 1-3 test
MU195050A* ³ /MU196050B	Noise Generator	-	1	
MU196060A* ³	32G baud NRZ/PAM4 Re-Driver	001	1	
MU195050A	Noise Generator	-	1	
MX183000A-PL001	Jitter Tolerance Test	-	1	
MX183000A-PL021	PCIe Link Training	-	1	PCIe 1-4
MX183000A-PL025	PCIe 5 Link Training	-	1	Addition requires PL021
MX183000A-PL026	PCIe 6 Link Training	-	1	Addition requires PL021 and PL025

*1: Required for 58 Gbaud Ethernet measurement

*2: Contact Anritsu about option retrofit.

*3: When used MU195050A with MU195040A, Vf-Km Adaptor is required. Vf-Km Adaptor or Vm-Kf Adaptor is required depending on the connector shape of the DUT.

Refer to the Selection Guide for details.

PCIe Receiver Test Recommended Equipment List (2/3)

Model	Name	Option	Qty	Mandatory/ Optional	Remark
J1815A	MP1900A PCIe Measurement Component Set	-	1	Optional	For PCIe1 to PCIe6
Z2025A	PCIe CBB Controller	-	1	Optional	<ul style="list-style-type: none"> • For Add-in-card tests, • It is possible to reset the DUT and automatically turn on the power supply from the automation software. This improves verification efficiency and is effective for verification in remote environments. • Supports GRL and Tektronix automation software
Z2029A	PCIe 100 MHz Reference Clock Buffer	-	1	Mandatory For AIC	For Add-in-card tests For PCIe1 to PCIe6
J1900A	Passive Low Frequency Equalizer	-	2	Optional	Contact our business section about J1900A/G0447A.
G0447A	PCIe6 External Re-Driver		1	Optional	

For the latest information, please see to the "[Signal Quality Analyzer-R MP1900A series Selection Guide](#)"

PCIe Receiver Test Recommended Equipment List (3/3)

Choose the automation software matching your oscilloscope.

Model	Electrical Test	Scope Vender	Automation soft vender
QPHY-PCIE* ¹ -TX-RX	PCIe 3/4/5/6 Tx, Rx	Teledyne LeCroy	Teledyne LeCroy
GRL-PXE* ¹ -CEM-RXA GRL-PXE* ¹ -BASE-RXA GRL-PXE* ² -RXA	PCIe 3/4/5/6 BASE PCIe 3/4/5/6 CEM	Tektronix Keysight	Granite River Labs
TekRxTest	PCIe 3/4/5/6 Tx, Rx	Tektronix	Tektronix

*¹ 3/4/5/6 . *² 5/6

For the latest information, please see to the "[Signal Quality Analyzer-R MP1900A series Selection Guide](#)"

■ PCIe 5 (MU196060A Re-driver and MU195040A SI-ED)

Item	Specifications	Remarks
Target Applications	PCIe 1-5	Requires PAM4 PPG or SI PPG and SI ED.
Loss Compensation	30 dB at 16 GHz, BER <1E-12	When using MU196060A. NRZ, MCP, SSC 33 kHz 5300 ppm Down spread
SKP OS Filtering	Supported	
Matrix Scan		
Jitter Tolerance		

■ PCIe 6 (MU196060A Re-driver and MU196040B PAM4 ED)

Item	Specifications	Remarks
Target Applications	PCIe 4-6	Requires PAM4 PPG, PAM4 ED and MU196060A. PCIe 1-3 supports Link Training only. Use SI ED not PAM4 ED for BER measurement, Matrix scan and JTOL at PCIe 1-3.
Loss Compensation	0 dB at 16 GHz, BER <1E-8, 1E-12(Typ.) 14 dB at 16 GHz, BER <1E-6, 1E-9(Typ.)	PAM4, MCP, SSC 33 kHz 5300 ppm Down spread
SKP OS Filtering	Supported (PCIe 4-6)	
Matrix Scan		
Jitter Tolerance		
PCIe 6 FEC	Supported	

USB/Thunderbolt Test Solution

- Supports SI PPG 2.4 to 32.1 Gbit/s and PAM4 PPG 2.4 to 64.2 Gbaud bands.
- Combining the customer's own oscilloscope with the MP1900A and automation software supports complex tests while cutting the work burden.
- The SI PPG and PAM4 PPG both output high-quality waveforms. The SI PPG has a Tr/Tf of 12 ps and intrinsic jitter of 115 fs rms. The PAM4 PPG has a Tr/Tf of 8.5 ps and intrinsic jitter of 170 fs rms, while the SI ED has a high input sensitivity of 15 mV EH.
- The high-performance multi-channel BERT supports high-reproducibility receiver tests.
- The PAM4 PPG supports USB4 v2 tests
- Adding the 2ch option supports USB 3.2 x 2 tests.

Support Configuration for USB and Thunderbolt

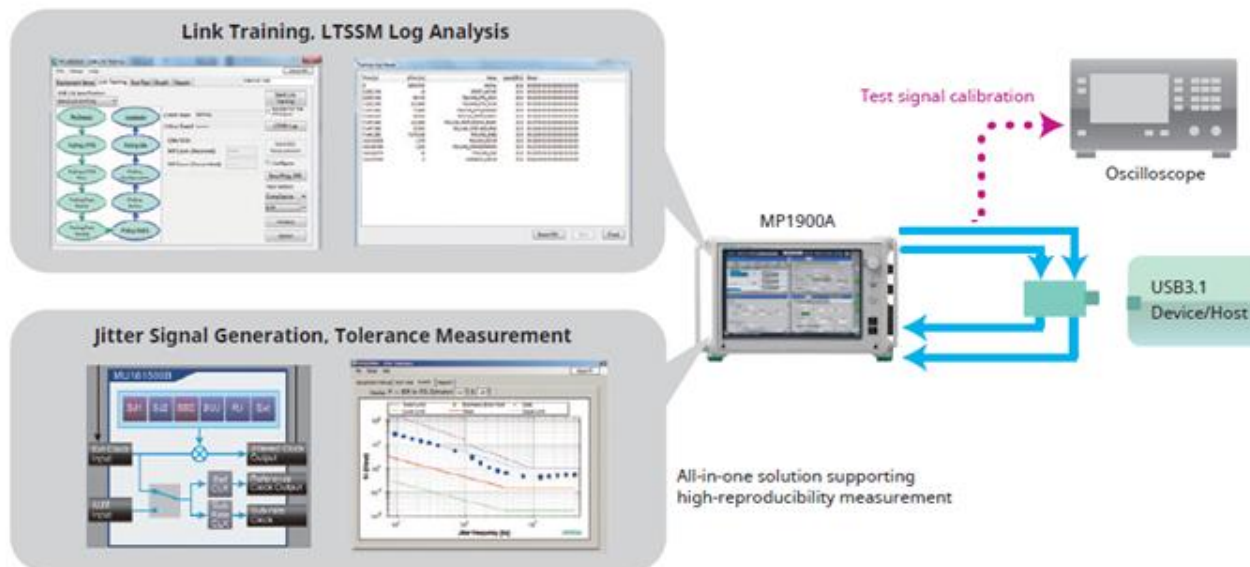
	SI PPG	PAM4 PPG	SI ED
USB 3.2	✓	-	✓
USB 3.2x2	✓*1	-	✓*1
USB4 v1/Thunderbolt3/4	✓*2	✓*2	-
USB4 v2	✓*3	✓	-

*1 Requires 2ch option; *2 Select any one PPG; *3 Used as aggressors

MP1900A Series USB3.2 Receiver Test Solution

- All-in-one USB 3.2 Protocol Aware Rx test solution
Supports USB 3.2 x 2 with 2ch PPG/ED
- Wideband BERT 2.4 Gbit/s to 32.1 Gbit/s supporting USB4 v1 and Thunderbolt3/4
- High-quality waveforms with low Intrinsic Jitter, high-reproducibility measurement using high-sensitivity ED
- Link Training and LTSSM analysis function
- Transmit and receive LFPS and LBPM signals
- Supports LFPS Rx test
- Insert and identify SKP Ordered Set
- Jitter Addition (SJ, RJ, BUJ, SSC) and Tolerance measurement

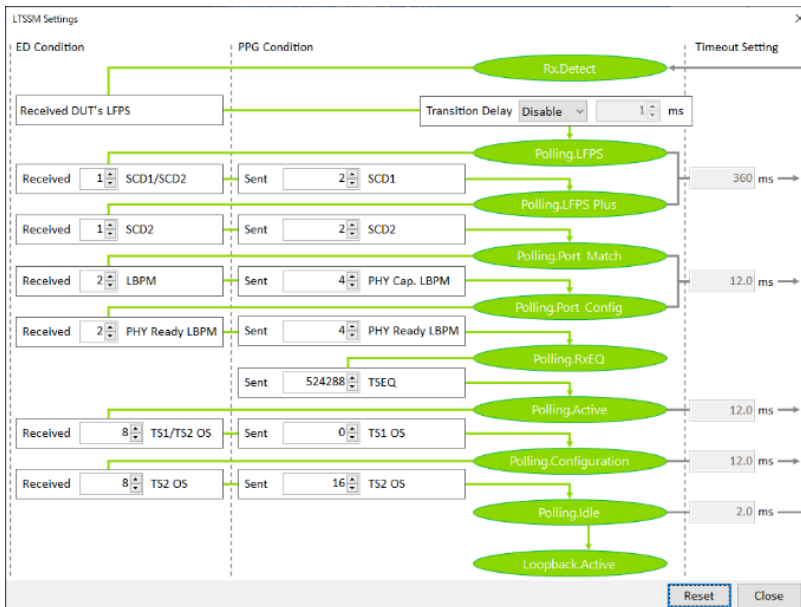
USB Receiver Test Solution



USB3.2 Link Training, LTSSM Analysis and Jitter Tolerance

Shorter Development Period by LTSSM Analysis Function for Troubleshooting Cause of Link Faults

Controls state transition from "Detect" to "Loopback" required by Rx test



For confirming results of each state transition with Training Log Viewer

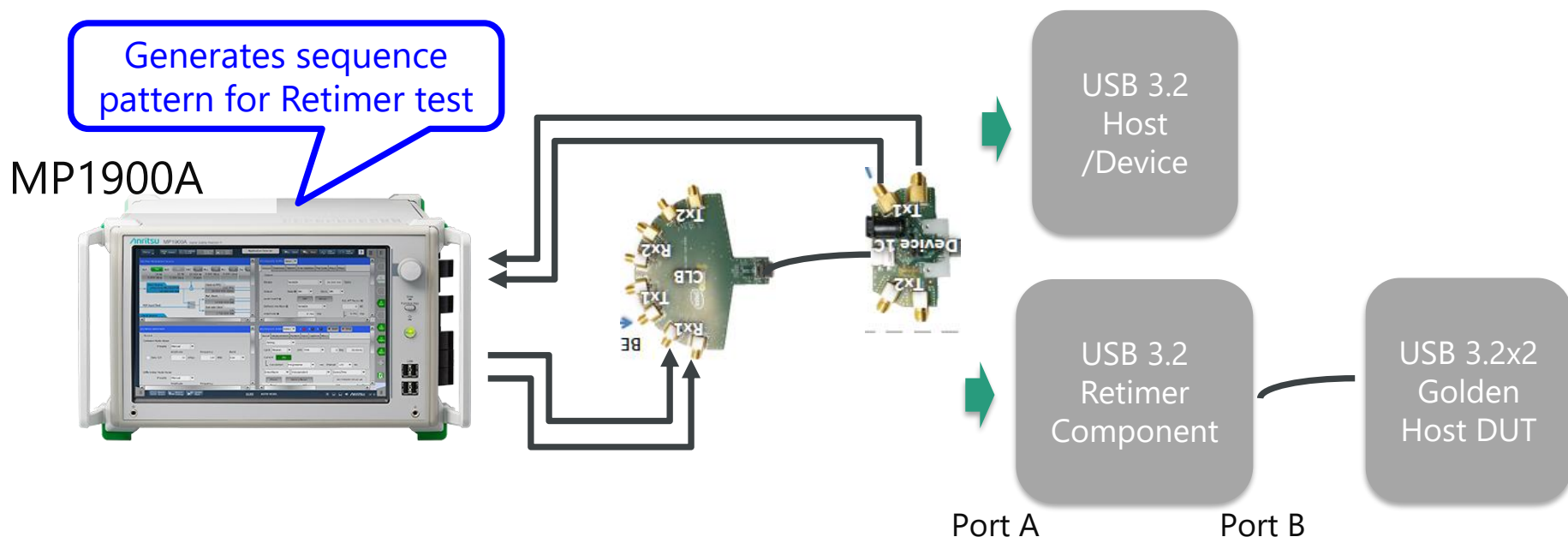
The Training Log Viewer displays a table of state transitions and timing data. The table has five columns: Time [ns], Δ Time [ns], State, Speed[Gt/s], and Detail.

Time [ns]	Δ Time [ns]	State	Speed[Gt/s]	Detail
0	6,945,704	INITIAL	10.0	00 00 00 00 00 00 00 00 00 00
6,945,704	24	DETECT_ACTIVE	10.0	00 02 00 00 00 00 00 00 00 00
6,945,728	69,440	POLLING_LFPS_SCD1	10.0	00 12 00 00 00 00 00 00 00 00
7,015,168	121,864	POLLING_LFPS_PLUS	10.0	00 14 00 00 00 00 00 00 00 00
7,137,032	71,808	POLLING_LFPS_ENDSCD	10.0	00 15 00 00 00 00 00 00 00 00
7,208,840	89,048	POLLING_PORT_MATCH	10.0	00 16 00 00 00 00 00 00 00 00
7,297,888	110,080	POLLING_PORT_CONFIG_READY	10.0	00 17 00 00 00 00 00 00 00 00
7,407,968	26,392	POLLING_PORT_ENDLBPM	10.0	00 18 00 00 00 00 00 00 00 00
7,434,360	7,178,248	POLLING_RXEQ	10.0	00 1A 00 00 00 00 00 00 00 00
14,612,608	2,176	POLLING_ACTIVE	10.0	00 1B 00 00 00 00 00 00 00 00
14,614,784	2,192	POLLING_CONFIGURATION	10.0	00 1C 00 00 00 00 00 00 00 00
14,616,976	24	POLLING_IDLE	10.0	00 1D 00 00 00 00 00 00 00 00
14,617,000	0	LOOPBACK_ACTIVE	10.0	00 64 00 00 00 00 00 00 00 00

Buttons at the bottom: Export CSV, Stop, Close.

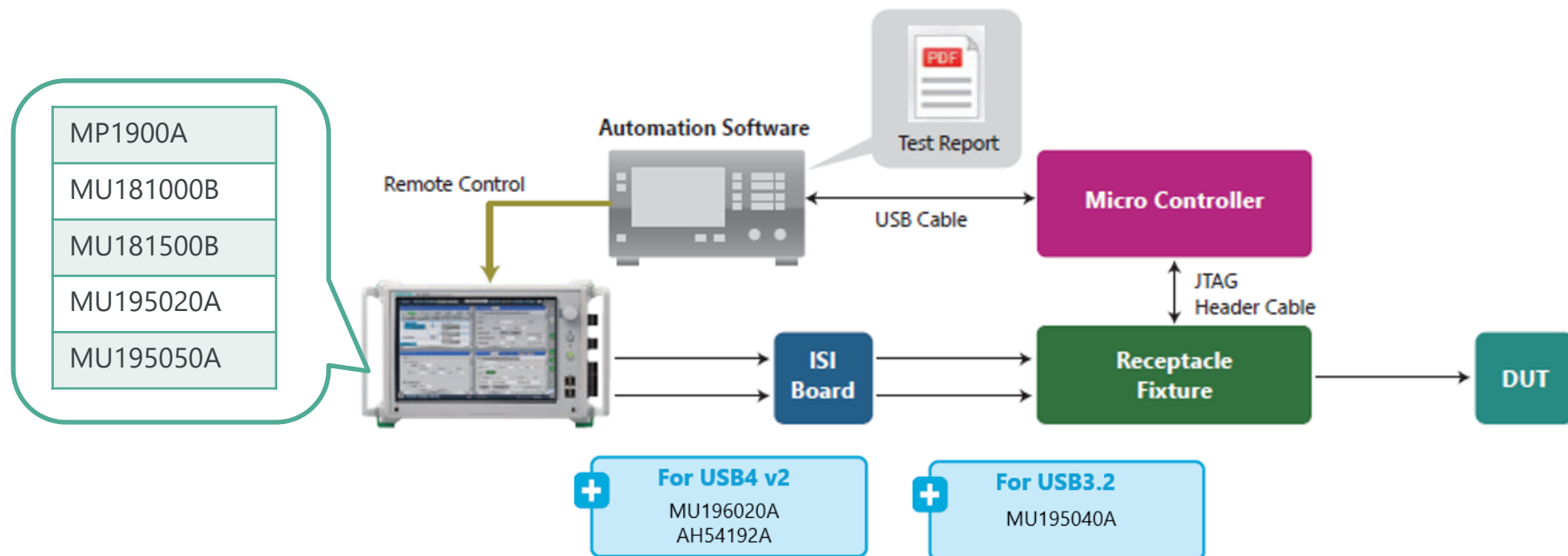
USB 3.2 Retimer Rx Test Support

- Supports Rx test for each USB 3.2 Retimer DUT type (BLR/SRIS, Embedded/Component, Active Cable)
- Adding Golden DUT (stable device) to conventional Host/Device test configuration supports USB 3.2 Retimer test.
- Can edit Retimer test sequence (requires option) to match DUT features.



USB4 v1/v2 , Thunderbolt 3/4 Receiver Test Solution

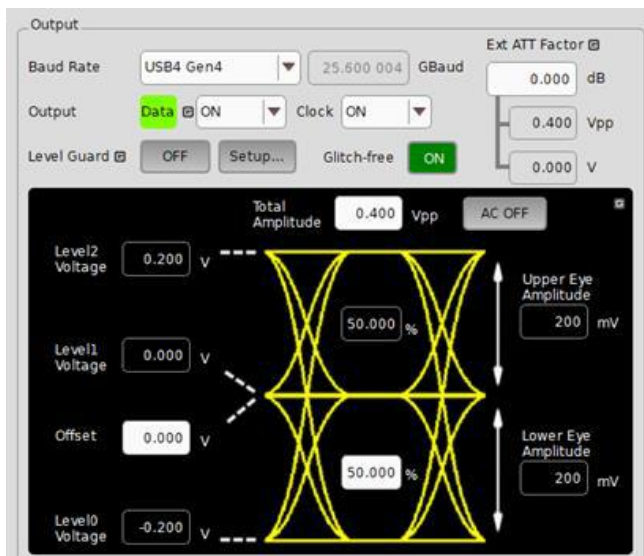
- The same configuration supports both wideband BERT 2.4 Gbit/s to 32.1 Gbit/s and Thunderbolt 3 and 4 tests. Adding the SI ED to this configuration supports USB 3.2 tests, and adding the PAM4 PPG and Amplifier (AH54192A) supports USB4 v2 tests.
- High-reproducibility tests due to low intrinsic jitter and high-quality waveforms.
- Both control of DUT BER counter and transition to Loopback mode from control PC via Micro Controller.
- Jitter (SJ, RJ, Total Jitter), SSC, ACCM, Eye Height and Eye Width calibrated using Automation Software.
- USB4 v2 hardware certification was obtained in 2025.



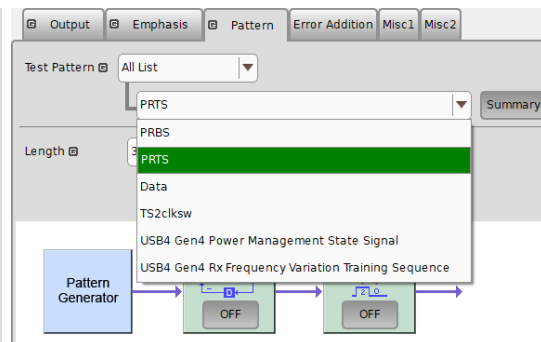
USB4 v2 Receiver Test

- USB4 Version 2.0 Compliance Test Pattern Generation
Supports PRTS, TS2cksw patterns and more.
- 25.6 Gbaud PAM3 Signal Generation Upgradable to 64.2G PAM4.
- All-in-one USB 3.2, USB4 v1, Thunderbolt 3/4, USB4 v2 Rx Tests.
- Automated Calibration and Rx Test
Supports key makers' oscilloscopes* and cuts complex test procedures and work burden.

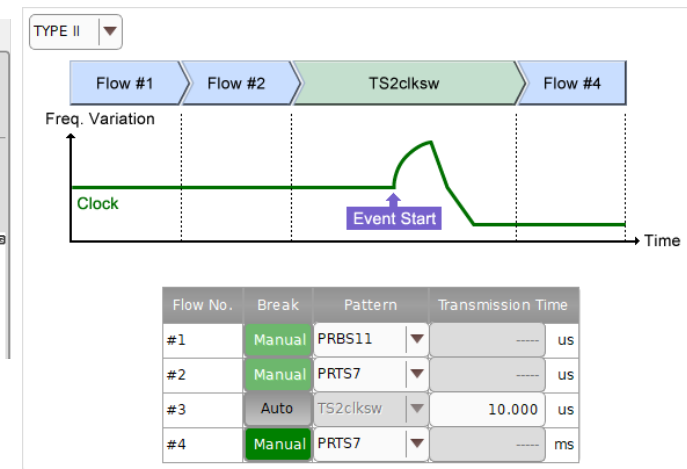
*Ask about supported oscilloscopes.



PAM3 Signal, Amplitude, Linearity Setting Screen



USB4v2 Test Pattern Support



Rx Frequency Variation Training Sequence Setting

USB Type-C Receiver Test Recommended Equipment List (1/4)

Model	Name	Option	USB3.2	USB3.2x2	USB4v1	USB4v2
MP1900A	Signal Quality Analyzer-R	-	1	1	1	1
MU191000A	Synthesizer	-	1	1	1	1
MU181500B	Jitter Modulation Source	-	1	1	1	1
MU195020A	21G/32G bit/s SI PPG	010, 011	1		1	1*1
		020, 021, 031		1		
		050	1*2	1*2		
MU195040A	21G/32G bit/s SI ED	010, 011, 022	1			
		020, 021, 022		1		
MU196020C	PAM4 PPG	001, 011, 045*3			1	1
MU195050A	Noise Generator	-	1	1	1	1
MX183000A-PL001	Jitter Tolerance Test	-	1	1		
MX183000A-PL022	USB Link Training	-	1	1		
MX183000A-PL023	USB 3.2 x 2 Link Training	-		1		

*1 For Aggressor signal generation; Opt-011 not required

*2 For generating Retimer test sequence pattern

*3 For USB4 v2 only

USB Type-C Receiver Test Recommended Equipment List (2/4)

Model	Name	USB3.2	USB3.2x2	USB4 v1
J1551A	Coaxial Skew Matched Cable (0.8 m)	2*4	4*4	2*4
K261	DC Block			2
AH54192A	Differential linear amplifier			
-	ISI Channel			1
USB31CET	USB3.1 Type-C Test Fixture	1	1	
-	USB4 v1/TBT3 Test Fixture			1
	USB4 v1/TBT3 Micro controller			1
-	K-SMP Adapter			4

*4 Can substitute J1821A

For the latest information, please see to the “[Signal Quality Analyzer-R MP1900A series Selection Guide](#)”

USB Type-C Receiver Test Recommended Equipment List (3/4)

For USB4 v2^{*5}

Model	Name	Qty	Where to Buy
AH54192A	Differential linear amplifier	1	Anritsu
J1943A	MP1900A USB4 v2 Measurement Component Set ^{*6}	1	Anritsu (Summer 2026 launch) ^{**7}
-	ISI Channel	1	Wilder Technologies or Wild River Technology
-	USB4 v2 Fixture	1	Wilder Technologies or Luxshare-ICT
-	USB4 v2 Micro Controller	1	Wilder Technologies or Granite River Labs

J1943A MP1900A USB4 v2 Measurement Component Set^{*6} (details)

Model	Name	Qty	Remarks
K261	DC Block	2	
J1821A	Coaxial Skew Matched Cable Pair (0.8m, K Connector)	4	Pair cable
J1949A	Coaxial Skew Matched Cable Pair (0.6m, K Connector)	1	Pair cable Launches soon (currently January 2026) ^{*7}
J1789A	Electrical Length Specified Coaxial Cable(0.4m, V connector)	2	
J1820A	Electrical Length Specified Coaxial Cable(0.4m, K connector)	4	
J1888A	Fixed Attenuator (6 dB, V Connector)	2	41VA-6 can also be used
J1792A	Skew matched pair semirigid cable (V-K)	1	Pair cable
J1808A	Fixed Adapter(K(f)-K(f))	2	
J1748A	Power Splitter	2	For Aggressor signal splitting
J1632A	Terminator (SMA)	2	

^{*5} CTS1.00 certification configuration; changes to quantities indicated in red (updated 2026.01)

^{*6} CTS1.00 certification configuration

^{*7} Enquire about details

For the latest information, please see to the
["Signal Quality Analyzer-R MP1900A series Selection Guide"](#)

USB Type-C Receiver Test Recommended Equipment List (4/4)

Choose the automation software matching your oscilloscope.

Model	Electrical Test	Remark
QPHY-USB4-TX-RX	USB4/TBT3 Tx, Rx	Teledyne LeCroy scope Purchase from Teledyne LeCroy
QPHY-USB3.1-Tx-Rx	USB 3.2 Tx, Rx	
GRL-USB4V2-RXA	USB4 v2 TX,RX	Keysight/Tektronix scope Purchase from Granite River Labs
GRL-USB4-RXA	USB4/TBT3,4 RX	
GRL-USB32-RXA	USB 3.2/USB 3.2 x2 Rx	

Sequence Editor Function For PCIe/CXL, USB3.2

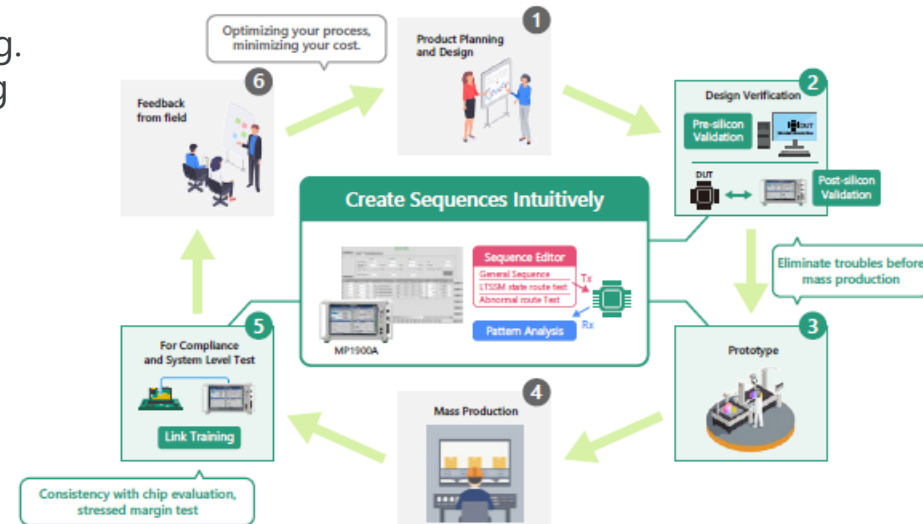
Sequence Editor Function

Addressing High-Speed Bitrate Issues

Increasing bit-rate speeds make differentiating between physical layer errors and protocol errors more complex, which increases the burden of verification and debugging. Sequence Editor helps speed-up debugging by analyzing and isolating these errors efficiently.

Resolving issues in multi-channel environments beyond compliance testing

By supporting not only 1 Lane but also 2- and 4-Lane configurations, Sequence Editor can reproduce both Compliance Test environments as well actual market usage environments. This enables identification and resolution of potential issues in advance by reproducing load conditions according to real-world usage environments, thereby mitigating troubles after product launch.



Unleash PCIe 6.0 USB Debugging and Validation

Model name	Name
MU196020A-051	Sequence Editor Function
MU196020A-052	Sequence Editor Function for Multi-Channel (MU196020A-051 is required for all modules)
MU196020A-056	Sequence Editor Function PCIe 6 and CXL 3 Flits Extension
MU196040B-051	PCIe Sequence Editor Pattern Analysis

Model name	Name
MU195020A-050	Sequence Editor Function
MU195020A-051	Sequence Editor Function PCIe 5 Extension (MU195020A-050 is required.)

Sequence Editor Function

Transmission Pattern Customization and Advanced Debugging Support

Users can use the Sequence Editor function freely to create and edit transmission patterns for PCIe 1-6, CXL2/3 and USB 3.2.

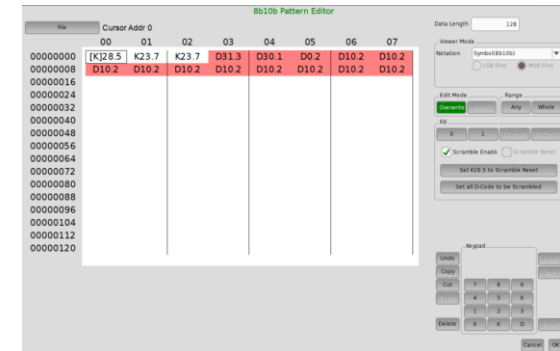
Users can reproduce actual Link Training behavior by using LTSSM logs and can debug Link Training easily by changing the conditions of states that are not operating normally. Data received from the DUT can be displayed easily using the HSSB Data Analysis function (SI ED only).

Intuitive and Excellent Usability

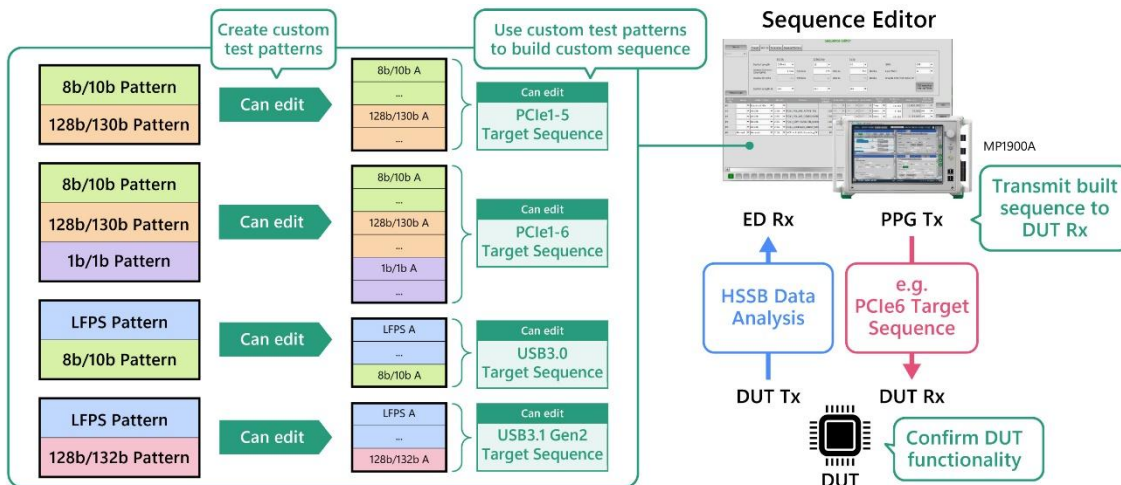
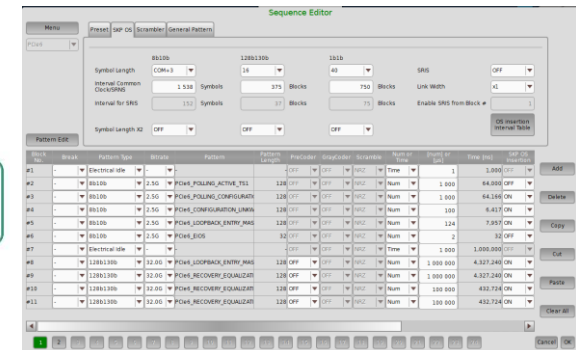
Sequence Editor features a dedicated user interface for PCIe 1 to 6, CXL2/3 and USB 3.2, enabling intuitive sequence creation.

Both symbol-level editing for 8b/10b, 128b/130b, 1b/1b, and NULL Flits as well as scrambler settings for arbitrary symbols are easily configured.

The ability to customize ordered set information and transmission counts and sequences makes simplifies creation of test cases, significantly contributing to higher test quality and reproduction of bugs.



8b/10b Pattern Editor Screen (Scrambled)



Sequence Editor Screen (PCIe6)

Sequence Editor Function

Sample Use Case

- Custom patterns and sequences support transitioning the DUT to non-default routes for comprehensive LTSSM testing.

Example: The default route during Link Training is PCIe5 Config No Equalization Loopback.

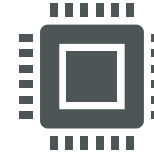
Example: This tests functionality when the DUT transitions to the Disabled state during configuration.



PPG Tx



DUT Rx



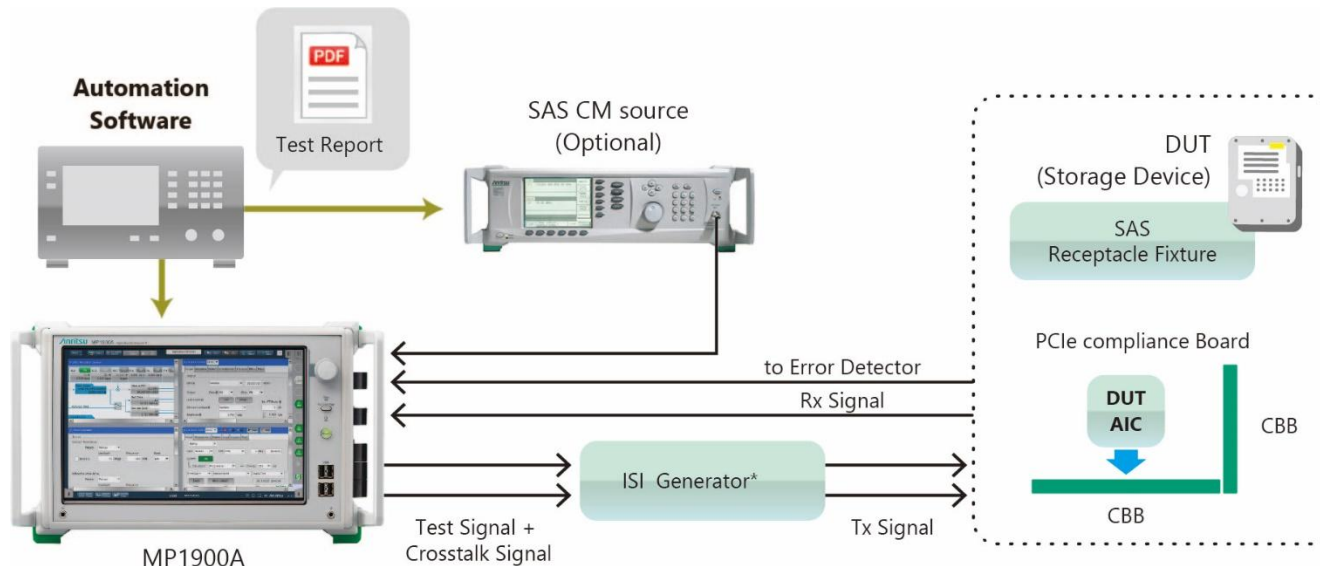
Default Route (PCIe6 Config NoEq Loopback)		
Link Speed	Pattern	Remarks
-	Electrical Idle	Detect
2.5G	8b/10b TS1	Polling.Active
2.5G	8b/10b TS2	Polling.Configuration
2.5G	8b/10b TS1	Configuration.Linkwidth.Start (Disable Link bit = 0)
2.5G	8b/10b TS1	Loopback.Entry
2.5G	8b/10b EIOS	Entry to Speed Change
-	Electrical Idle	Speed Change
32.0G	128b/130b TS1	Loopback.Entry
2.5G	128b/130b EIOS	Entry to Speed Change
-	Electrical Idle	Speed Change
64.0G	1b/1b TS1	Loopback.Entry
64.0G	1b/1b MCP	Loopback.Active

Non-default Route for Testing (Disabled)		
Link Speed	Pattern	Remarks
-	Electrical Idle	Detect
2.5G	8b/10b TS1	Polling.Active
2.5G	8b/10b TS2	Polling.Configuration
2.5G	8b/10b TS1	Configuration.Linkwidth.Start (Disable Link bit = 1)
2.5G	8b/10b TS1	Disabled
-	Electrical Idle	Disabled

Must send Disable Link bit = 1 to DUT

SAS Test Solution

- Same configuration supports receiver tests of SAS and PCIe.
Wideband operation from 2.4 Gbit/s to 21 Gbit/s with expansion to 32.1 Gbit/s
Supports SAS-4 (22.5 Gbit/s) and Gen5 (32G) measurements without changing configuration
- Combination with automation software supports oscilloscope from main makers
Simplifies complex test procedures and reduces work burden by using own oscilloscope.
- High-performance multichannel BERT with high-quality output waveforms (12-ps Tr/Tf, 115-fs rms Intrinsic Jitter) and high-input sensitivity (15 mV EH)
Supports higher-reproducibility receiver tests



* Should use specified ISI generator by PCIe or SAS

SAS Receiver Test Recommended Equipment List (1/2)

Model	Name	Option	Qty	Remark
MP1900A	Signal Quality Analyzer-R	-	1	
MU191000A	Synthesizer		1	
MU181500B	Jitter Modulation Source	-	1	
MU195020A	21G/32G bit/s SI PPG	001*, 010, 011, 040	1	*Add Opt-001 for expansion to SAS-4
MU195050A	Noise Generator	-	1	
MU195040A	21G/32G bit/s SI ED	001*, 010, 011, 022	1	*Add Opt-001 for expansion to SAS-4
J1758A	Variable ISI Channel	-	1	
-	Mated Adapter Fixture Pair	-	1	
K261	DC block	-	2	
MG3692C	2GHz to 20GHz Signal Generator	-	1	for CM tests
K241C	RF Splitter	-	1	

Requires cables to connect with other equipment

For the latest information, please see to the "[Signal Quality Analyzer-R MP1900A series Selection Guide](#)"

SAS Receiver Test Recommended Equipment List (2/2)

Choose the automation software matching your oscilloscope.

Model	Measurement item	Remark
GRL-SAS3-RXA	SAS3 Receiver Calibration and Test	Tektronix or Keysight scope Purchase from Granite River Labs
GRL-SAS4-RXA	SAS4 Receiver Calibration and Test	
GRL-SAS34-RXA	SAS4 and SAS3 Receiver Calibration and Test	

DisplayPort Test Solution

DisplayPort Receiver Test Solution

- Wideband operation from 2.4 Gbit/s^{*1} to 21 Gbit/s with expansion to 32.1 Gbit/s without hardware upgrade

Flexible support for DisplayPort2.0 (20 Gbit/s) and future faster speeds

(*1: Can only generate special RBR (1.62 Gbit/s) pattern)

- All-in one Dual-Channel PPG

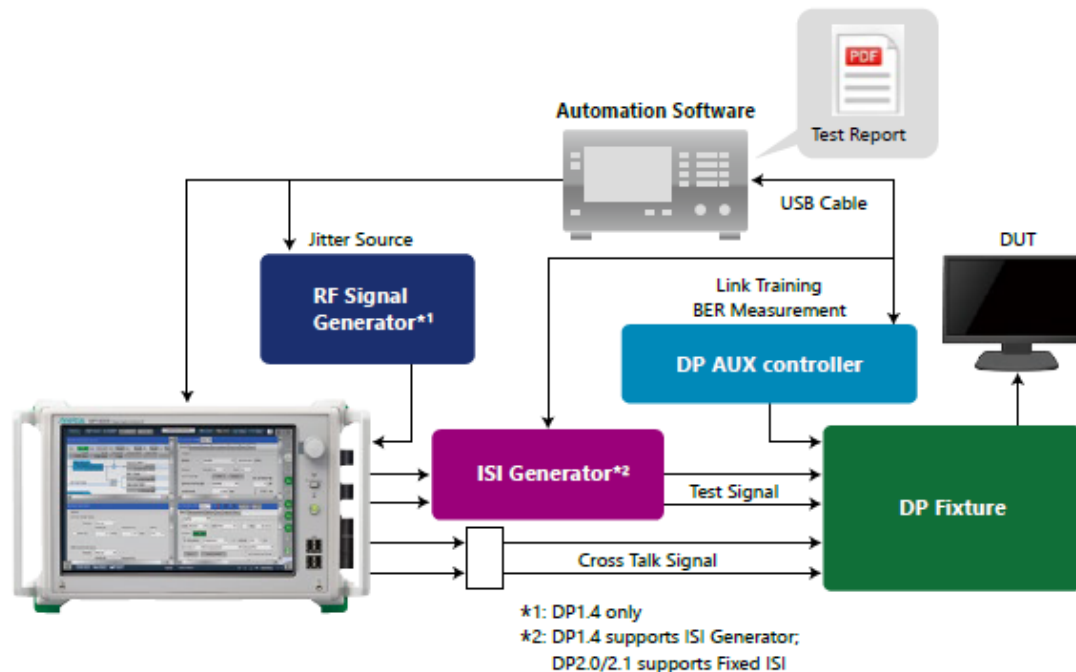
True crosstalk effects can be analyzed by controlling inter-channel skew.

- Combination with automation software supports oscilloscope from main makers

Simplifies complex test procedures and reduces work burden by using own oscilloscope

- High-quality output waveforms (12-ps Tr/Tf, 115-fs rms Intrinsic Jitter) PPG

Supports higher-reproducibility receiver tests.



DisplayPort Receiver Test Recommended Equipment List (1/4)

Model	Name	Option	DP1.2 Qty	DP2.0/2.1 Qty	Remark
MP1900A	Signal Quality Analyzer-R	-	1	1	
MU191000A	Synthesizer	-	1	1	
MU181500B	Jitter Modulation Source	-	1	1	
MU195020A	21G/32G bit/s SI PPG	020, 021,031	1	1	
MU195050A	Noise Generator	-	1	1	

For the latest information, please see to the "[Signal Quality Analyzer-R MP1900A series Selection Guide](#)"

DisplayPort Receiver Test Recommended Equipment List (2/4)

For DisplayPort 1.4

Item	Model Number	Description	Q'ty	Where to Buy
Basic Accessory	K261	Ultra Wide Band DC Block, 10 kHz - 40 GHz	2	Anritsu
	AN44182A	1:4 Power divider	2	Anritsu
	DSG815	297 MHz Jitter Source	1	RIGOL
	41KB-6	6 dB attenuator (For 297 MHz SJ)	1	Anritsu
	CLE1000-A2	Artek ISI-A2	1	aceunitech
	DPT-200 controller set	DPT-200, USB-A to USB-B cable, Power adaptor ,DisplayPort RefSource AUX Controller(OPTION)	1	UNIGRAF
	HL9450-60	Transition Time Converter (<1 GHz) 60 ps	2	HYPERLABS
	HL9450-150	Transition Time Converter (<1 GHz) 150 ps	2	HYPERLABS
	J1821A	Coaxial skew match cable(0.8 m, K connector)	8	Anritsu
	J1625A	COAXIAL CABLE 1M(SMA connector)	1	Anritsu
	J1398A	N-SMA ADAPTOR	1	Anritsu
	J1632A	TERMINATOR	6	Anritsu
For Fullsize DP Accessory	DP-TPA-P	DisplayPort Plug Adapter(For DP1.4)	1	Wilder Technology
	DP R	DisplayPort Receptacle Adapter(For DP1.4)	1	Wilder Technology
	DP-TPA-A	Display Port Aux Control Adapter	1	Wilder Technology
	DP Cable	DP cable for AUX control No length specified.	1	Don't Care
For Type-C Accessory	DPC Plug	Display Port Type-C Plug Adapter	1	Wilder Technology
	DPC Receptacle	Display Port Type-C Receptacle Adapter	1	Wilder Technology
	DPC Control board	Display Port Type-C Control Board	1	Wilder Technology
	DP-TypeC Cable	DP cable for AUX control	1	Don't Care

For the latest information, please see to the "[Signal Quality Analyzer-R MP1900A series Selection Guide](#)"

DisplayPort Receiver Test Recommended Equipment List (3/4)

For DP2.0/2.1

Item	Model Number	Description	Q'ty	Where to Buy
Basic Accessory	K261	Ultra Wide Band DC Block, 10 kHz - 40 GHz	2	Anritsu
	AN44182A	1:4 Power divider	2	Anritsu
	ISI-USB4	WildRiver ISI board	1	WildRiverTechnology
	DPT-200 controller set	DPT-200, USB-A to USB-B cable, Power adaptor DisplayPort RefSource AUX Controller(OPTION)	1	UNIGRAF
	J1551A	Coaxial skew match cable(0.8 m, K connector)	8	Anritsu
	J1632A	TERMINATOR	6	Anritsu
For Fullsize DP Accessory	ENH-DP-TPA-P	Enhanced DisplayPort Plug DP2.1a test adapter	1	Wilder Technology
	ENH-DP-TPA-R	Enhanced DisplayPort Receptacle DP2.1a test adapter	2	Wilder Technology
	DP-TPA-A	Display Port Aux Control Adapter	1	Wilder Technology
	DP2.1 Cable 0.8 m	For 20 Gbit/s ISI	1	Don't Care
	DP2.1 Cable 2 m	For 10 Gbit/s ISI	1	Don't Care
	DP Cable	DP cable for AUX control No length specified.	1	Don't Care
For Type-C Accessory	DPC Plug	Display Port Type-C Plug Adapter	1	Wilder Technology
	DPC Receptacle	Display Port Type-C Receptacle Adapter	2	Wilder Technology
	DPC Control board	Display Port Type-C Control Board	1	Wilder Technology
	USB-C cable 0.8 m	For 20 Gbit/s ISI	1	Don't Care
	USB-C cable 2 m	For 10 Gbit/s ISI	1	Don't Care
	DP-TypeC Cable	DP cable for AUX control	1	Don't Care

For the latest information, please see to the "[Signal Quality Analyzer-R MP1900A series Selection Guide](#)"

DisplayPort Receiver Test Recommended Equipment List (4/4)

Model	Measurement item	Remark
GRL-DP14-SINKAN	DisplayPort1.4 SINK	Tektronix or Keysight scope Purchase from Granite River Labs
GRL-DP21-SINK-AN	DisplayPort2.1 SINK	Tektronix or Keysight scope Purchase from Granite River Labs
QPHY-DisplayPort 2.1/1.4	DisplayPort1.4 and 2.1 SINK	Teledyne LeCroy scope Purchase from Teledyne LeCroy

For the latest information, please see to the "[Signal Quality Analyzer-R MP1900A series Selection Guide](#)"

DDR5 Test Solution

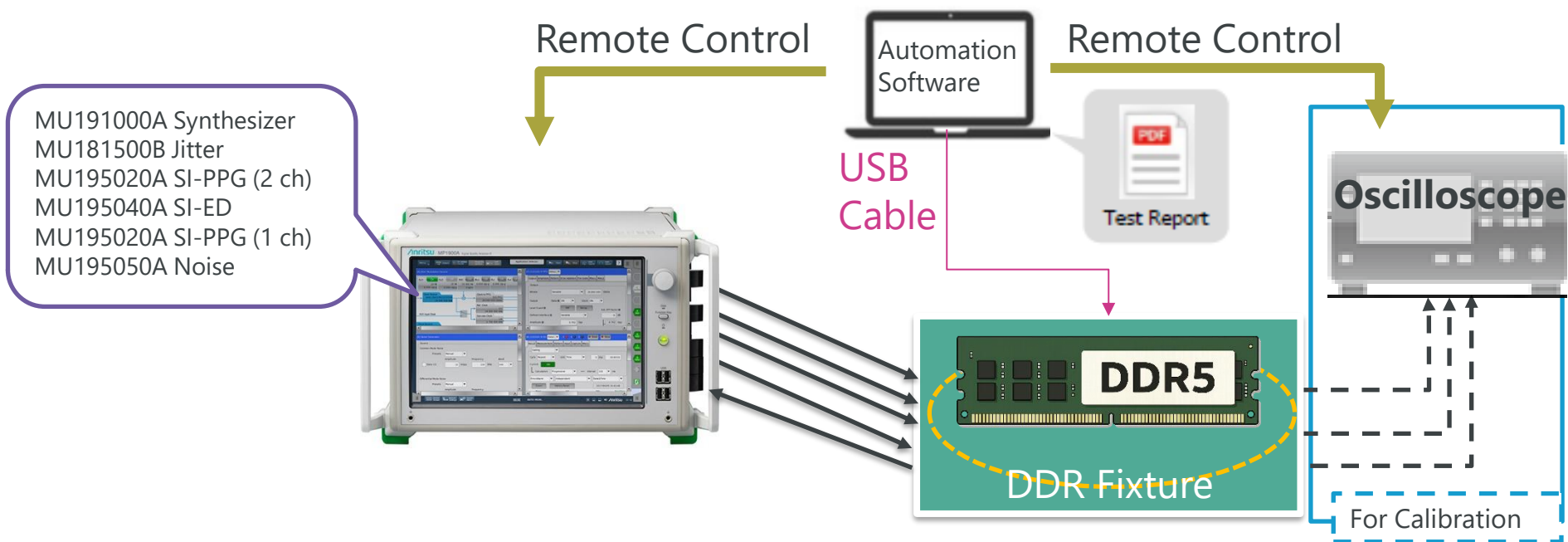
(Double Data Rate 5)

DDR5 is the fifth generation of Double Data Rate Synchronous Dynamic Random Access Memory (DDR5 SDRAM). It was introduced in 2021 by JEDEC, the industry standardization organization. DDR5 has expanded transmission speeds up to 8.4 Gbit/s, and new features such as DFE (Decision Feedback Equalization) have been adopted to improve high-speed signal reliability. New receiver tests have been established to ensure signal integrity of high-speed signals.

The Signal Quality Analyzer-R MP1900A has the functions and performance to support DDR5 receiver testing and supports sensitivity tests and stressed-Eye tests following the standards.

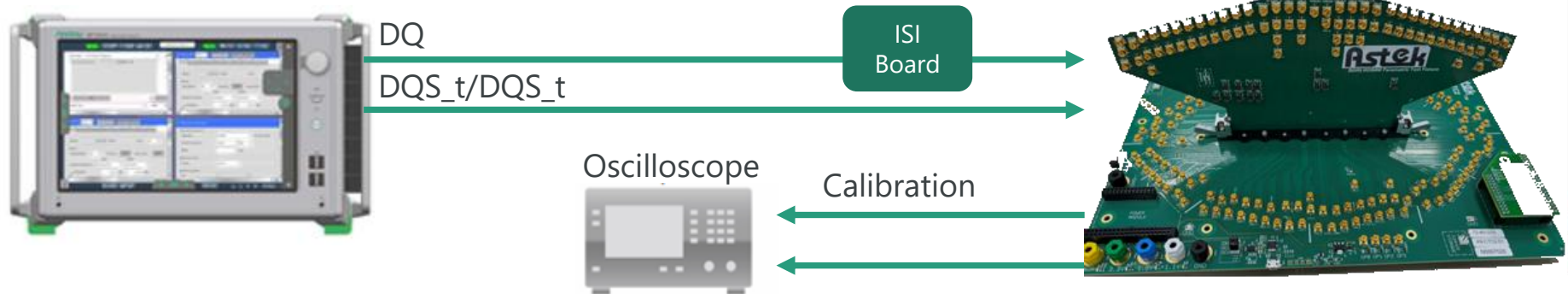
DDR5 Rx Test Solution

- Supports JEDEC JESD79-5C calibration and measurement Conformance Tests (Rx DQS Jitter Sensitivity, Rx DQS Voltage Sensitivity, Rx DQ Voltage Sensitivity, Rx Stressed Eye)
- Cuts Conformance Test times by integration with Tektronix Clarius Compliance DDR5 DRAM Receiver Test Solution
- Outputs synchronized signals from multiple PPGs by using MP1900A PPG multi-channel function and can control synchronized DQS and DQ as burst signals to simulate operations as close-to-real real market conditions and improve verification quality.
([Click for PPG multichannel explanation.](#))

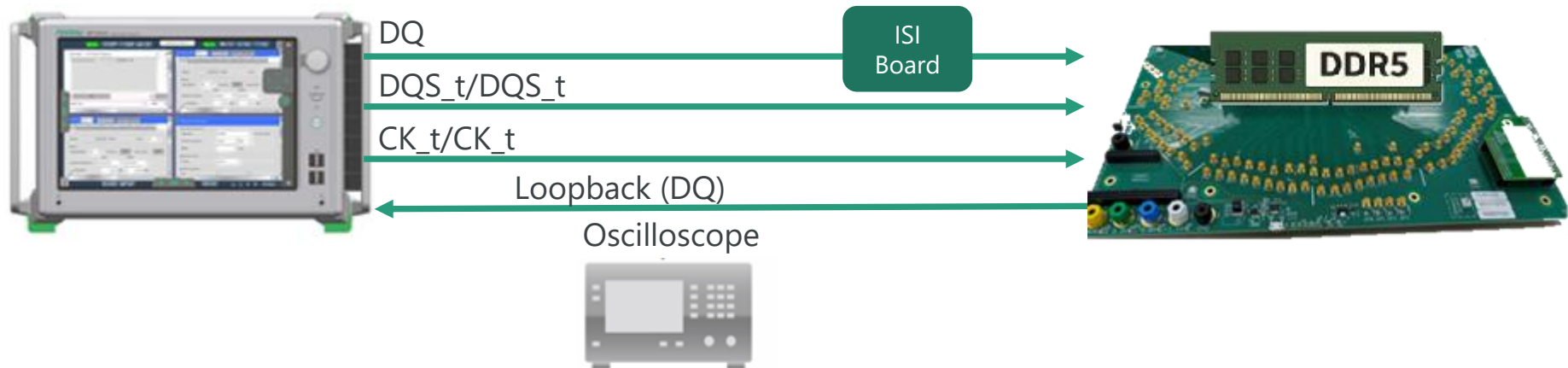


DDR5 Receiver Test Solution

Calibration Amplitude, RJ, SJ



Receiver Test Voltage Sensitivity, Jitter Sensitivity, Stressed Eye

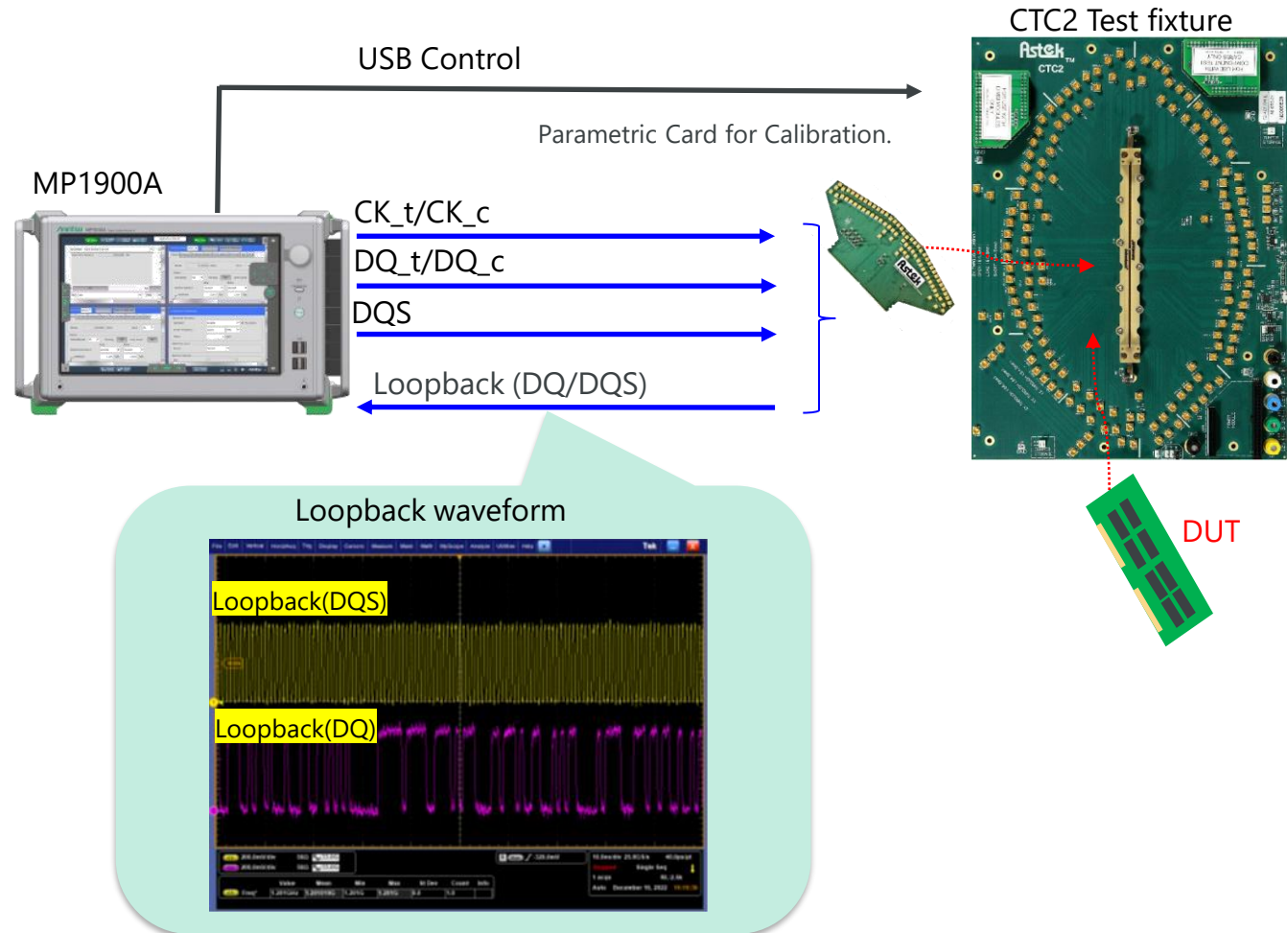


DDR5 Receiver Test Solution

The following items can be measured by loading the required script from the MP1900A to the DUT for the RDIMM memory loopback settings.

- Voltage sensitivity
- Jitter sensitivity
- Stressed Eye test

Modules for MP1900A
MU191000A Synthesizer
MU181500B Jitter
MU195020A SI-PPG(2ch)
MU195040A SI-ED
MU195020A SI-PPG(1ch)
MU195050A Noise Generator



Recommended DDR5 Rx Test Solution Equipment List (1/2)

Module Configuration

Model	Name	Option	Qty	Remark
MP1900A	Signal Quality Analyzer-R	-	1	
MU191000A	Synthesizer	-	1	
MU181500B	Jitter Modulation Source	-	1	
MU195020A	21G/32G bit/s SI PPG	010, 011, 030, 040	1	Can change 010->020, 011->021, 030->031
MU195020A	21G/32G bit/s SI PPG	020, 021, 031	1	
MU195040A	21G/32G bit/s SI ED	010, 011	1	
MU195050A	Noise Generator	-	1	

DDR5 Rx Test requires 3ch SI PPG output. Choose from the following combinations.

MU195020A-020 (2ch PPG) x2
or
MU195020A-020 (2ch PPG) + MU195020A-010 (1ch PPG)



or



Refer to the Signal Quality Analyzer-R MP1900A series Selection Guide for the latest information.

Recommended DDR5 Rx Test Solution Equipment List (2/2)

Accessories

Model	Name	Qty	Remark
41KC-6	Precision Fixed Attenuator (6 dB)	3	
J1551A	Coaxial Skew Matched Cable (0.8 m, K-connector)	3 Pairs	
J1439A	Coaxial Cable (0.8 m, K-connector)	2	
J1624A	COAXIAL CABLE 0.3 m (SMA connector)	(4)	Use MU181000B standard accessory cables (4 pcs).
J1746A	Skew Matched Pair Semirigid Cable (K-connector, Data Input 1)	(1 Pair)	Use MU195050A standard accessory.
	SMP to SMA Adapter Cable	7	
	Power Supply (dual output, +12 V,+3.3 V)	1	
A9-AUTO-01	Reset Automation Kit	1	Contact ASTEK. https://www.astekcorp.com/
A9-CTC2-01	DDR5 CTC2 Test Fixture	1	
A9-DIMM5	DDR5 Parametric Test Card	1	

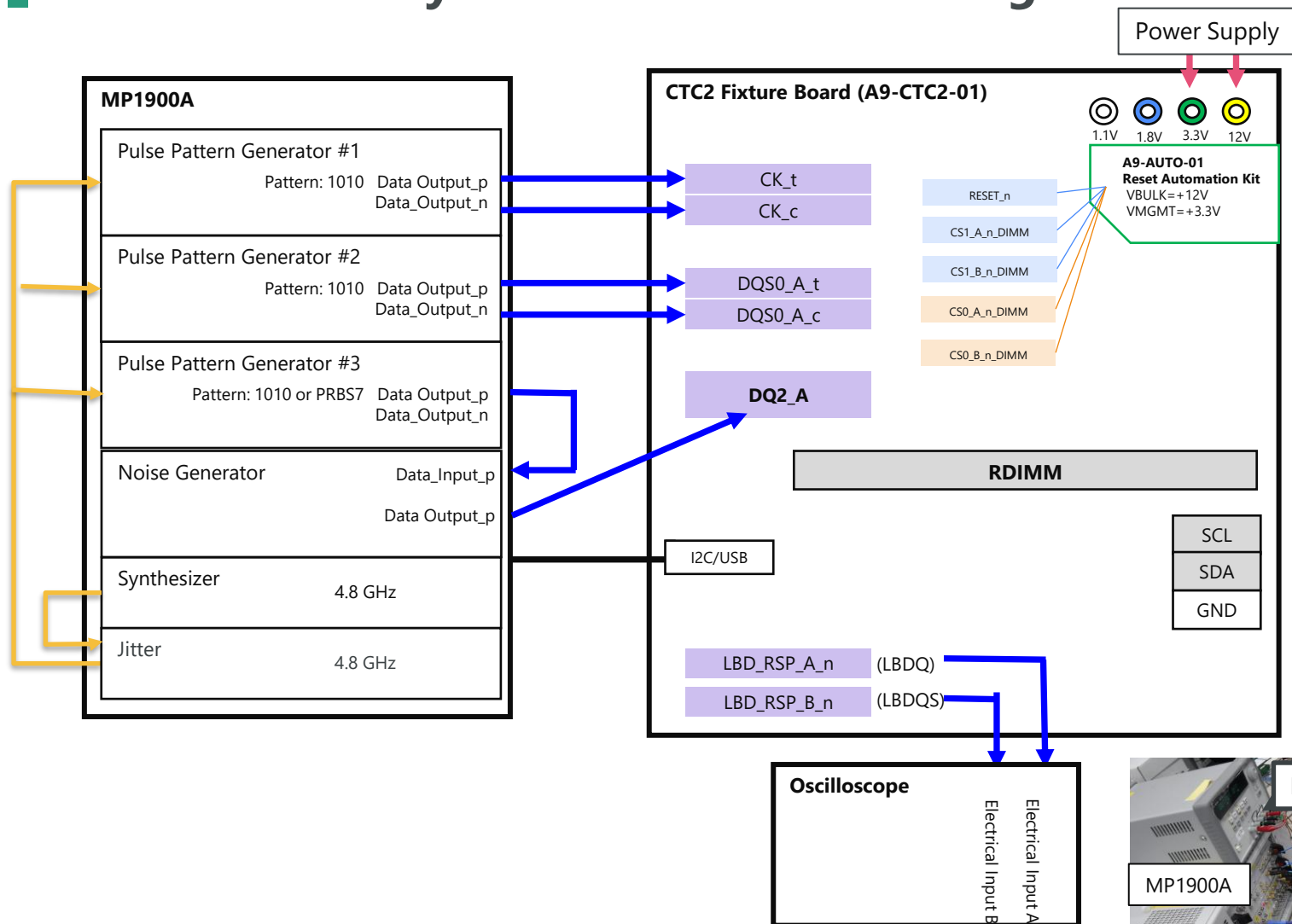
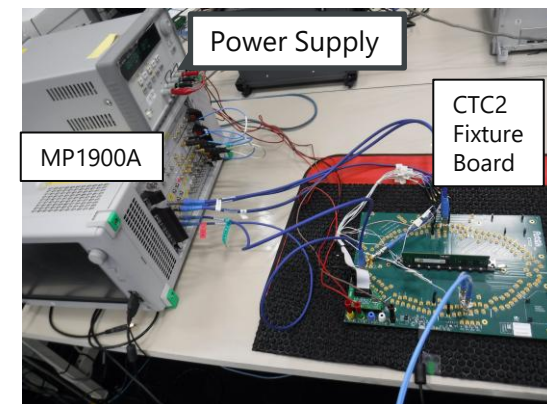
Scope

Model	Remark
DPO72304series, MSO72304 series(Tektronix)	For Automation

Automation Software

Name	Qty	Remark
Clarius Automation Framework	1	Contact Tektronix.
Clarius Compliance DDR5 DRAM Receiver Test Solution	1	

RDIMM Memory Rx Test Connection Diagram





A9-AUTO-01
Automation Kit

- 16 SMP cables
- Reset, Chip Select, and Command/Address signals on the CTC2 to automatically perform reset sequencing of a DIMM



A9-CTC2-01
CTC2 Test Fixture

- All high-speed signals are brought out to SMP connectors
- Traces are length matched to within 1 ps
- Low speed signals are brought out to 50 mil headers
- VIN Bulk and VIN Management are brought out to 50 mil headers



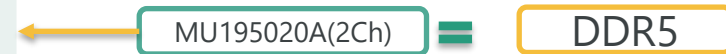
A9-DIMM5DDR5
Parametric Test Card

- All high-speed signals brought out to SMP connector
- All signals matched to within 1ps
- Supports DIMM testing
- 12V and 3.3V for DIMM mode

Expanding from PCIe 5 to DDR5 Configuration

Adding the MU195020A 21G/32G bit/s SI PPG creates a DDR5 solution for customers who already have a PCIe5 environment.

SLOT	Model Name	Product Name / Description
	MP1900A	SIGNAL QUALITY ANALYZER-R
1	MU191000A	Synthesizer
2-3	MU181500B	Jitter Modulation Source
4-5	Blank or MU196060A	Blank or Re-Driver
6	MU195040A	21G/32G bit/s SI ED
7	MU195020A	21G/32G bit/s SI PPG (1ch)
8	MU195050A	Noise Generator



Appendix



Ordering Information Specifications

Refer to [MP1900A Data Sheet](#)

