High-Speed Serial-Bus Interface Solution
PCIe 5 Support
Signal Quality Analyzer-R
MP1900A Series
PCIe, USB, Thunderbolt Market Trend

Discussion started as 32Gbaud PAM4
Key Features

- **Signal Quality**
  - Low Jitter/Clean Eye
  - 10TAP Emphasis for Tx
  - High Sensitivity
  - 12 dB Variable CTLE for Rx
  - Jitter/Noise Source in One Package

- **Scalability**
  - 32 Gbit/s NRZ up to 16ch
  - 112 Gbit/s PAM4 (56 Gbaud) up to 4ch

- **Analyzability**
  - Ready for PCIe-G5 bit rate (32G NRZ)
  - PCIe-G5 Link Training (Negotiation)
  - PCIe-G5 LTSSM Analysis
  - FEC Pattern Generation

- **Usability**
  - All-in-One: PC Controller, Noise Source, Emphasis, CTLE, CDR, etc.
  - New GUI/Touch Screen
### MP1900A Series Products

- High-Expandability Software Solutions Supporting Multiple Interfaces
- Device Rx Test Calibration and Test Automation

<table>
<thead>
<tr>
<th>Model</th>
<th>Name</th>
<th>Option</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>MP1900A</td>
<td>Signal Quality Analyzer-R</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MU181000B</td>
<td>12.5GHz 4port Synthesizer</td>
<td>02</td>
<td></td>
</tr>
<tr>
<td>MU181500B</td>
<td>Jitter Modulation Source</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MU195020A</td>
<td>21G/32G bit/s SI PPG</td>
<td>01, 10, 11, 40 or 01, 20, 21, 41</td>
<td>1ch or 2ch</td>
</tr>
<tr>
<td>MU195040A</td>
<td>21G/32G bit/s SI ED</td>
<td>01, 10, 11, 22</td>
<td>1ch</td>
</tr>
<tr>
<td>MU195050A</td>
<td>Noise Generator</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MX183000A-PL001</td>
<td>Jitter Tolerance Test Software</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MX183000A-PL021</td>
<td>PCIe Link Training Software</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MX183000A-PL025</td>
<td>PCIe Gen5 Link Training Software</td>
<td></td>
<td>New release</td>
</tr>
</tbody>
</table>

**Automation software for Keysight/Tektronix Scope**

<table>
<thead>
<tr>
<th>Model</th>
<th>Name</th>
<th>Option</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>GRL-PCIE4-BASE-RXA</td>
<td>PCIe Gen4 Base Automation Software</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GRL-PCIE4-CEM-RXA</td>
<td>PCIe Gen4 CEM Automation Software</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GRL-PCIE5-BASE-RXA</td>
<td>PCIe Gen5 Base Automation Software</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GRL-PCIE5-CEM-RXA</td>
<td>PCIe Gen5 CEM Automation Software</td>
<td></td>
<td>New release</td>
</tr>
</tbody>
</table>

**Automation software for Teledyne Lecroy Scope**

<table>
<thead>
<tr>
<th>Model</th>
<th>Name</th>
<th>Option</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>QPHY-PCIE-Tx-Rx</td>
<td>PCIE Gen3/4/5 Automation Software</td>
<td></td>
<td>*</td>
</tr>
</tbody>
</table>

*1: Enquire about support for Gen5 CEM
**PCIe Tx LEQ/Rx Compliance Test**

- Combination of best-performance BERT MP1900A and preferred oscilloscope -

**Shorter test times and reduced investment cost**

- Supports Combination with Lecroy/Tektronix(Keysight Real-Time Oscilloscopes
- Automated Rx CEM and Base Tests: Calibration, Link EQ and Automated Tx Test
- Protocol Aware: Link Training/Equalization and LTSSM Analysis
- High-Expandability 32G Multichannel BERT for PCIe1 to 5
PCIe Gen5 Test Solution
PCI Express Gen5 Rx Test Features

Key Features

- Automated Measurement and Calibration using Automation Software
  GRL-PCIE5-BASE/CEM-RXA/QPHY-PCIE-Tx-Rx
- True Crosstalk Test using Dual-Channel PPG
- Logical Sub Block Evaluation using MX183000A

Supported Standards

<table>
<thead>
<tr>
<th>Supported Standard</th>
<th>DUT</th>
<th>Calibration</th>
<th>Link Training</th>
<th>Jitter Tolerance Test</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCI Express Base Spec</td>
<td>1.x/2.0/3.x/4.0/5.0</td>
<td>Host/End Point SERDES</td>
<td>3.x/4.0/5.0: Supported</td>
<td></td>
</tr>
<tr>
<td>PCI Express CEM Spec</td>
<td>3.x/4.0/5.0</td>
<td>System/Device Card</td>
<td>3.x/4.0: Supported 5.0: Supported</td>
<td>Supported</td>
</tr>
</tbody>
</table>

Jitter Tolerance Test Function (Opt-PL001)

- Impress SJ/RJ to Test PHY Device Jitter Tolerance
- Device Margin Test using Estimated Low- Rate BER Measurement
- Measurement Result Report Creation in HTML and CSV Format
Features of Anritsu PCIe Solution (1/2)

Key Automation Software Features
GRL-PCIE5-BASE/CEM-RXA/QPHY-PCIE-Tx-Rx
- PCIe 5.0 Rx Base/CEM Spec Based Fully Automated Waveform Calibration
- Easy Rx Stress Tolerance Test
- Auto-calibration Controls Test Condition Dispersion (Scatter/Randomness)
- High-speed Waveform Calibration with Consistent Test Results

Key MX183000A Features
- PCIe Gen1 to Gen5 Loopback Mode
- Jitter Tolerance Margin Test

Application Specifications
- Data Rate: 32 GT/s
- Common/SRIS/SRNS Clock Architecture
- Required Instruments:
  - Keysight 50 GHz Oscilloscope (DSAX or newer series) or Tektronix 50 GHz (DPS or newer series)
  - Anritsu Signal Quality Analyzer-R MP1900A
  - Gen5 Base Fixture or Gen4 ISI board
Bit Error Analysis

- Set Loopback Preset to Manual and change the preset from P0 to P10 to determine the optimum preset/Cursor at the DUT.

- To find the DUT optimum setting, change CTLE Gain to 0 to –12 dB.

- The optimum Tx EQ value can be found automatically using the matrix Scan function.
Generating Stress Signal for Rx Test & Measuring BER Using MP1900A

- Stress Signal Generation
  - Jitter Addition Function: SJ/RJ/SSC
  - Noise Addition Function: Common Mode/Differential Mode
  - Emphasis Control
  - Crosstalk Signal Generation: Multichannel 4ch max./MP1900A

- BER Measurement
  - Jitter Tolerance Measurement
  - High-sensitivity Input Function: 15 mV (typ.) Eye Height Input
  - CDR Function: 2.4 to 32.1 Gbit/s Wideband
  - Built-in CTLE: 0 to –12 dB/0.1 dB
Gen5 Crosstalk Test

• Dual channel PPG enables true crosstalk testing
PCI Express Gen5 Rx Test Outline

- PCI Express PHY IP Device Rx Test Sequence

  Stress Signal Calibration
  Transition to Loopback Status
  Stress Signal Input Test

  Automation Software:
  GRL-PCIE5-BASE/CEM-RXA
  or QPHY-PCIE-Tx-Rx

  Link Training Software:
  MX183000A-PL021 (Gen1 to 4)
  MX183000A-PL025 (Gen5)

  - Jitter Tolerance Margin Test:
    MX183000A-PL001
    or
  - Jitter Sweep Test (Pass/Fail):
    GRL-PCIE5-BASE/CEM-RXA or QPHY-PCIE-Tx-Rx

Applicable Software

PCI express Measurement Summary
PCI Express Gen5 Calibration Points (1/3)

Stress Signal Calibration

Transition to Loopback Status

Stress Signal Input Test

---

**Table 8.9 Stressed Jitter Eye Parameters**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>2.5 GT/s</th>
<th>5.0 GT/s</th>
<th>8.0 GT/s</th>
<th>16.0 GT/s</th>
<th>32.0 GT/s</th>
<th>Units</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>VLS-LAUNCH</td>
<td>Generator launch voltage</td>
<td>800 to 1200</td>
<td>800 to 1200</td>
<td>800 to 1200</td>
<td>720 to 800</td>
<td>720 to 800</td>
<td>mV PP</td>
<td>Note 1</td>
</tr>
<tr>
<td>TXIUI</td>
<td>Unit Interval</td>
<td>400</td>
<td>200</td>
<td>125</td>
<td>62.5</td>
<td>31.25</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>TXI-EyE</td>
<td>Eye width</td>
<td>≤ 0.4</td>
<td>≤ 0.32</td>
<td>≤ 0.30</td>
<td>≤ 0.30</td>
<td>≤ 0.30</td>
<td>UI</td>
<td>Note 3, 4, 8, 10</td>
</tr>
<tr>
<td>TXI-EyH</td>
<td>Eye height</td>
<td>≤ 175</td>
<td>≤ 100</td>
<td>≤ 25</td>
<td>≤ 15</td>
<td>≤ 15</td>
<td>mV PP</td>
<td>Note 2, 4, 8, 9</td>
</tr>
<tr>
<td>TXI-SJ</td>
<td>Swept Sj</td>
<td>N/A</td>
<td>75 ps (max)</td>
<td>See Section 8.4.2.2.1</td>
<td>See Section 8.4.2.2.1</td>
<td>See Section 8.4.2.2.1</td>
<td>ps</td>
<td>Note 5</td>
</tr>
<tr>
<td>TXI-RI</td>
<td>Random Jitter</td>
<td>N/A</td>
<td>3.4</td>
<td>(max) 3.0</td>
<td>1.0</td>
<td>0.5</td>
<td>ps RMS</td>
<td>Note 6, 7</td>
</tr>
<tr>
<td>VLS-DIFF</td>
<td>Differential noise</td>
<td>N/A</td>
<td>N/A</td>
<td>14</td>
<td>14</td>
<td>10</td>
<td>mV PP</td>
<td>Note 7, 12 Adjust to set EHS. Frequency = 2.1 GHz.</td>
</tr>
<tr>
<td>VLS-CM</td>
<td>Common mode noise</td>
<td>150</td>
<td>150</td>
<td>150</td>
<td>150</td>
<td>150</td>
<td>mV PP</td>
<td>Note 8</td>
</tr>
</tbody>
</table>
PCI Express Gen5 Calibration Points (2/3)

Stress Signal Calibration

Transition to Loopback Status

Stress Signal Input Test

Figure 8-22 Rx Testboard Topology for 16.0 and 32.0 GT/s

MP1900A
PCI Express Gen5 Calibration Points (3/3)

Stress Signal Calibration

Automation Software GRL-PCIE5-BASE/CEM-RXA/QPHY-PCIE-Tx-Rx Features

- Stress Signal Calibration
- Transition to Loopback Status
- Stress Signal Input Test

Examples of Calibration Setting and Measurement Screens

One-touch Calibration of Stress Input Signal and Testing using Automation software

- Supports PCIe-Gen5 Rev1.0 Devices
- Executes Calibration of High-reproducibility Test Signal and Rx Test
PCI Express Gen5 Link Training (1/7)

- Link Training using MX183000A-PL025
  - PPG Pattern Control using MX183000A
  - Screen Functions for Easy Setting of Measurement Conditions and Test Execution
  - Controls PCI Express Device Status and Supports Logical Sub Block Evaluation
  - 8B/10B, 128B/130B, Scramble SKIP Insertion

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**Item** | **MX183000A-PL025 Specification**
--- | ---
Supported Standard | Gen5 (32 GT/s)
Test Pattern | Compliance (MCP, CP), PRBS (7, 9, 10, 11, 15, 20, 23, 31)
LTSSM State | Transition to Detect, Polling, Configuration, Recovery, Loopback
Loopback Through | Configuration, Recovery
TS Set Pattern | SKP Insertion/Filtering, 8B/10B, 128B/130B, FTS, Link Number, Lane Number, Scrambling
PCI Express Gen5 Link Training (2/7)

- Added and Changed Several Parameters Affecting Link Training

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Enhanced Link Behavior Control</td>
<td>Added TS parameter for LEQ to PCIe 5.0</td>
</tr>
<tr>
<td>Precoding</td>
<td>Receiver can request precoding from transmitter to operate at data rates of 32.0 GT/s or higher</td>
</tr>
</tbody>
</table>
| SKP OS/EIEOS/EIEOSQ              | SKP OS Identifier changed from AAh to 99h  
32G EIEOS has same frequency compared to 16G  
Two consecutive EIEOS for data rates of 32.0 GT/s |
| MCP 5.0                          | EIEOS changed to EIEOSQ                                                       |
PCI Express Gen5 Link Training (3/7)

- Enhanced Link Behavior Control

  Defined option to perform Recovery Equalization when selecting loopback through configuration route

Only for 32 GT/s (New)  
8, 16, and 32 GT/s (Legacy)
PCI Express Gen5 Link Training (4/7)

- Enhanced Link Behavior Control
  Defined new routes for Link Equalization

<table>
<thead>
<tr>
<th>Case</th>
<th>8.0 GT/s EQ</th>
<th>16.0 GT/s EQ</th>
<th>32.0 GT/s EQ</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>✔</td>
<td>-</td>
<td>-</td>
<td>PCIe 3</td>
</tr>
<tr>
<td>B</td>
<td>✔</td>
<td>✔</td>
<td>-</td>
<td>PCIe 4</td>
</tr>
<tr>
<td>C</td>
<td>-</td>
<td>-</td>
<td>✔</td>
<td>PCIe 5 Equalization bypass to highest rate support</td>
</tr>
<tr>
<td>D</td>
<td>✔</td>
<td>✔</td>
<td>✔</td>
<td>PCIe 5 Full Equalization required</td>
</tr>
<tr>
<td>E</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>PCIe 5 No Equalization needed</td>
</tr>
</tbody>
</table>
Precoding

At 32.0 GT/s, an optional precoding mechanism is provided, which receivers can enable optionally, to reduce the risk of DFE-related error bursts in high transition data patterns causing silent data corruption.

The receiver can request precoding from its transmitter for operation at data rates of 32.0 GT/s or higher.

Precoding can be applied independently to either Tx or Rx.
PCI Express Gen5 Link Training (6/7)

MX183000A Already Supports:

✔ Enhanced Link Behavior Control
✔ Precoding
✔ SKP OS/EIEOS
✔ MCP 5.0
PCI Express Gen5 Link Training (7/7)

- Strong MX183000A Support for Customer Debugging

LTSSM Log Viewer

LTSSM Trigger
### PCI Express Gen5 Rx JTOL Test (1/5)

- **Stress Signal Input Test (Jitter Tolerance Margin Test Using MX183000A-PL001)**
- Jitter Control and Tolerance Measurement using MX183000A
  - Impresses SJ and Tests PHY Device Jitter Tolerance
  - Tests Device Margin using Low BER Estimation
  - Outputs Measurement Results in HTML and CSV Formats

<table>
<thead>
<tr>
<th>Item</th>
<th>MX183000A-PL001 Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Jitter Setting Range</td>
<td>Complies with MU181500B Jitter Modulation Source</td>
</tr>
<tr>
<td>Direction Search</td>
<td>Binary, Downward Linear, Downward Log, Upward Linear, Upward Log,</td>
</tr>
<tr>
<td></td>
<td>Binary + Linear</td>
</tr>
<tr>
<td>Detection</td>
<td>Error Rate, Error Count, Estimate</td>
</tr>
<tr>
<td>Error Threshold</td>
<td>1.0E-3 to 1.0E-14</td>
</tr>
<tr>
<td>Highlight Error Rate</td>
<td>9.9E-9 to 1.0E-20 (at estimate)</td>
</tr>
<tr>
<td>Report Function</td>
<td>Reports results in HTML and CSV formats</td>
</tr>
</tbody>
</table>
PCI Express Gen5 Rx JTOL Test (2/5)

- Measurement System Uncertainty
  - Challenging calibration targets
  - Severe DUT Rx margins cause factors preventing error-free measurement
  - Eliminate BER measurement system uncertainties
PCI Express Gen5 Rx JTOL Test (3/5)

- All-in-One MP1900A with built-in CDR
  - Recovers Clock from Data using SSC to eliminate errors caused by Data/Clock line length differences

- MP1900A w/ High Signal Quality and High Repeatability
  - Jitter time and temperature dependency: <±2% (2 days, ±5°)
  - Low Intrinsic Jitter: 115 fs rms
PCI Express Gen5 Rx JTOL Test (4/5)

- Crosstalk Impact on Signal Quality

Crosstalk can impact signal quality at high data rates. PCIe 5 allocates a port to transmit MCP from other a non-test lane of the DUT (Training Sequence Symbol Number 5, Bit 5). This method cannot generate a quantitative Aggressor Signal.
PCI Express Gen5 Rx JTOL Test (5/5)

- MP1900A Generates Aggressor Signal using Multichannel Generator
  - All-in-one BERT with multichannel signal generator
  - Supports DUT requests to send MCP

Data Tx (Differential), Aggressor for Crosstalk
800 to 1200 mV adjustable

Data Rx (Differential)

Data Tx (Differential), Victim

ISI Calibration Channel

BER Measurement

Test Board

PHY IC

Anritsu
envison: ensure
PCI Express Gen5 Test Report

1) Run Tests (Pass/Fail at test points)

2) Generate Report