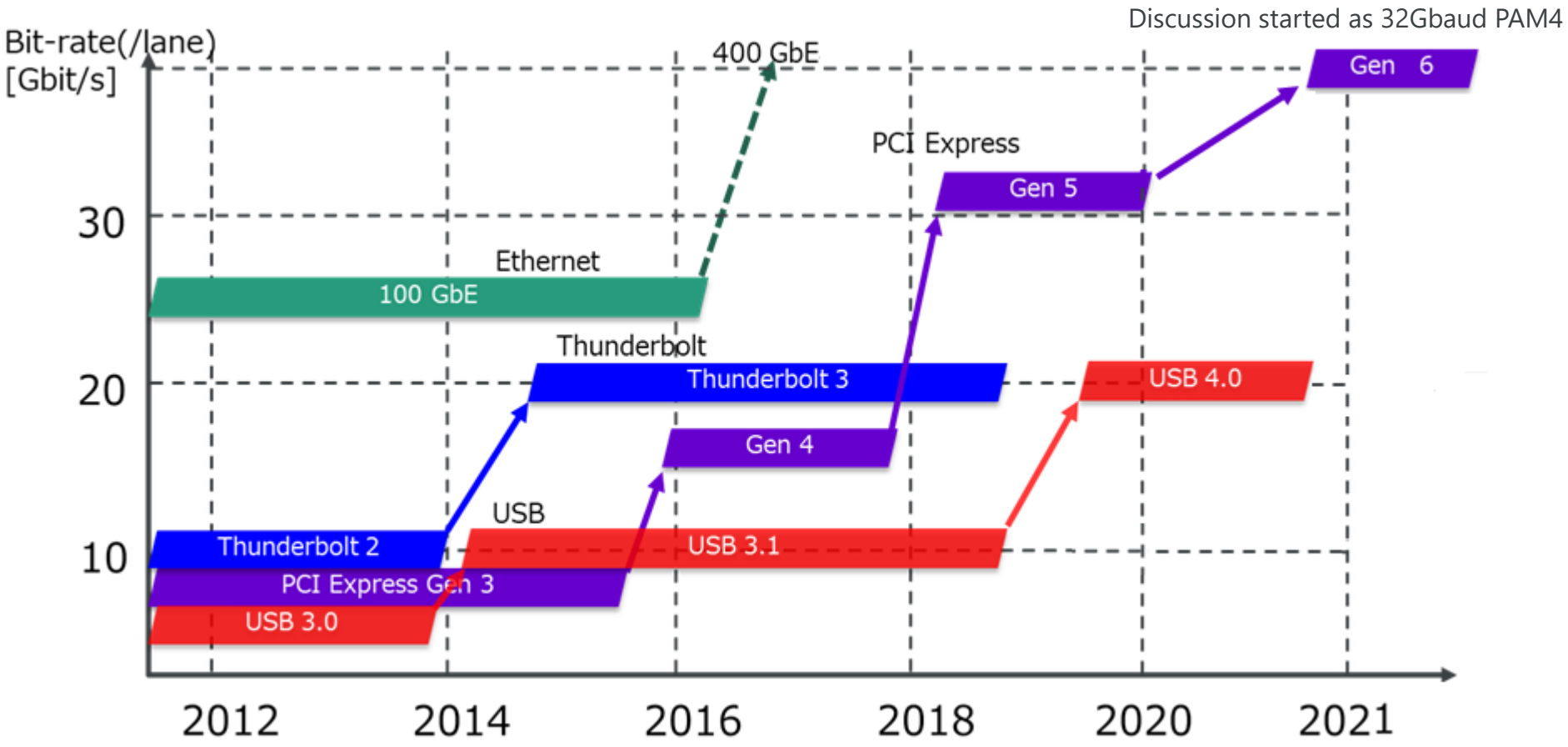
Anritsu envision:ensure

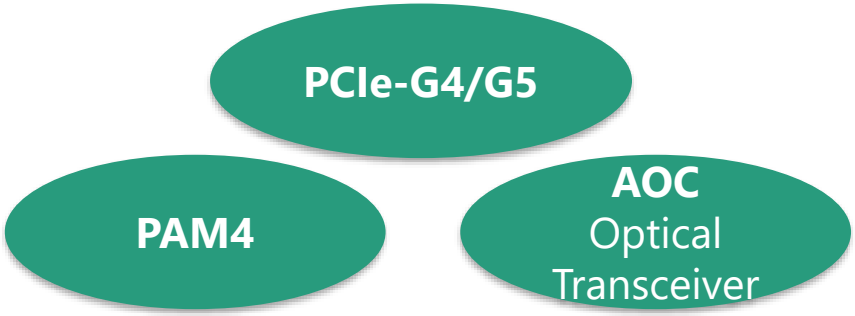
High-Speed Serial-Bus Interface Solution PCIe 5 Support

Signal Quality Analyzer-R MP1900A Series

PCIe, USB, Thunderbolt Market Trend



Key Features



All-in-one support from Network IF to BUS IF

SQA-R **MP1900A**

- **Signal Quality**
  - Low Jitter/Clean Eye
  - 10TAP Emphasis for Tx
  - High Sensitivity
  - 12 dB Variable CTLE for Rx
  - Jitter/Noise Source in One Package
- **Scalability**
  - 32 Gbit/s NRZ up to 16ch
  - 112 Gbit/s PAM4 (56 Gbaud) up to 4ch
- **Analyzability**
  - Ready for PCIe-G5 bit rate (32G NRZ)
  - PCIe-G5 Link Training (Negotiation)
  - PCIe-G5 LTSSM Analysis
  - FEC Pattern Generation
- **Usability**
  - All-in-One: PC Controller, Noise Source, Emphasis, CTLE, CDR, etc.
  - New GUI/Touch Screen

MP1900A Series Products

- High-Expandability Software Solutions Supporting Multiple Interfaces
- Device Rx Test Calibration and Test Automation

Model	Name	Option	Remarks
MP1900A	Signal Quality Analyzer-R		
MU181000B	12.5GHz 4port Synthesizer	02	
MU181500B	Jitter Modulation Source		
MU195020A	21G/32G bit/s SI PPG	01, 10, 11, 40 or 01, 20, 21, 41	1ch or 2ch
MU195040A	21G/32G bit/s SI ED	01, 10, 11, 22	1ch
MU195050A	Noise Generator		
MX183000A-PL001	Jitter Tolerance Test Software		
MX183000A-PL021	PCIe Link Training Software		
MX183000A-PL025	PCIe Gen5 Link Training Software		New release
Automation software for Keysight/Tektronix Scope			
GRL-PCIE4-BASE-RXA	PCIE Gen4 Base Automation Software		
GRL-PCIE4-CEM-RXA	PCIE Gen4 CEM Automation Software		
GRL-PCIE5-BASE-RXA	PCIE Gen5 Base Automation Software		
GRL-PCIE5-CEM-RXA	PCIE Gen5 CEM Automation Software		New release
Automation software for Teledyne Lecroy Scope			
QPHY-PCIE-Tx-Rx	PCIE Gen3/4/5 Automation Software		*

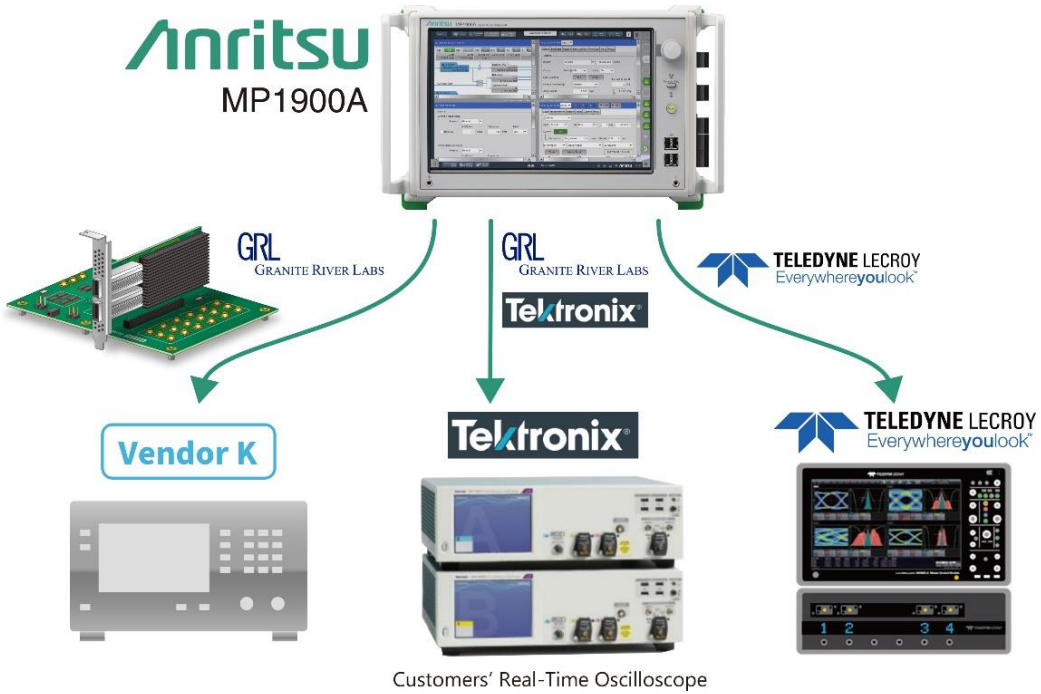
*1: Enquire about support for Gen5 CEM

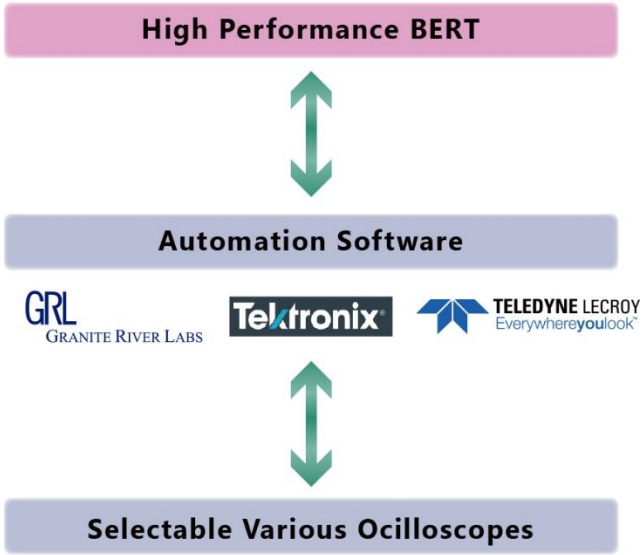
PCIe Tx LEQ/Rx Compliance Test

- Combination of best-performance BERT MP1900A and preferred oscilloscope -

Shorter test times and reduced investment cost

- Supports Combination with Lecroy/Tektronix/Keysight Real-Time Oscilloscopes
- Automated Rx CEM and Base Tests: Calibration, Link EQ and Automated Tx Test
- Protocol Aware: Link Training/Equalization and LTSSM Analysis
- High-Expandability 32G Multichannel BERT for PCIe1 to 5





PCIe Gen5 Test Solution

PCI Express Gen5 Rx Test Features

✓ Key Features

- Automated Measurement and Calibration using Automation Software
  GRL-PCIE5-BASE/CEM-RXA/QPHY-PCIE-Tx-Rx
- True Crosstalk Test using Dual-Channel PPG
- Logical Sub Block Evaluation using MX183000A

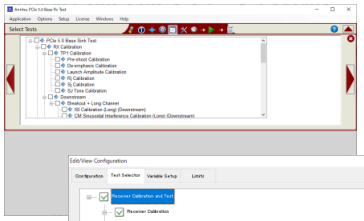
Supported Standards

Supported Standard		DUT	Calibration	Link Training	Jitter Tolerance Test
PCI Express Base Spec	1.x/2.0/3.x/4.0/ 5.0	Host/End Point SERDES	3.x/4.0/5.0: Supported	1.0 to 4.0: Supported 5.0: Supported	Supported
PCI Express CEM Spec	3.x/4.0/5.0	System/Device Card	3.x/4.0: Supported 5.0: Supported		

Jitter Tolerance Test Function (Opt-PL001)

- ✓ Impress SJ/RJ to Test PHY Device Jitter Tolerance
- ✓ Device Margin Test using Estimated Low- Rate BER Measurement
- ✓ Measurement Result Report Creation in HTML and CSV Format

Features of Anritsu PCIe Solution(1/2)



Key Automation Software Features

GRL-PCIE5-BASE/CEM-RXA/QPHY-PCIE-Tx-Rx

PCIe 5.0 Rx Base/CEM Spec Based Fully Automated Waveform Calibration

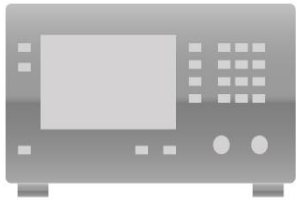
Easy Rx Stress Tolerance Test

Auto-calibration Controls Test Condition Dispersion (Scatter/Randomness)

High-speed Waveform Calibration with Consistent Test Results

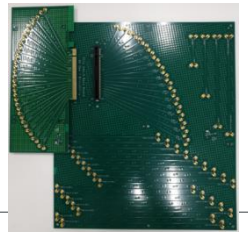
Key MX183000A Features

PCIe Gen1 to Gen5 Loopback Mode
Jitter Tolerance Margin Test



Application Specifications

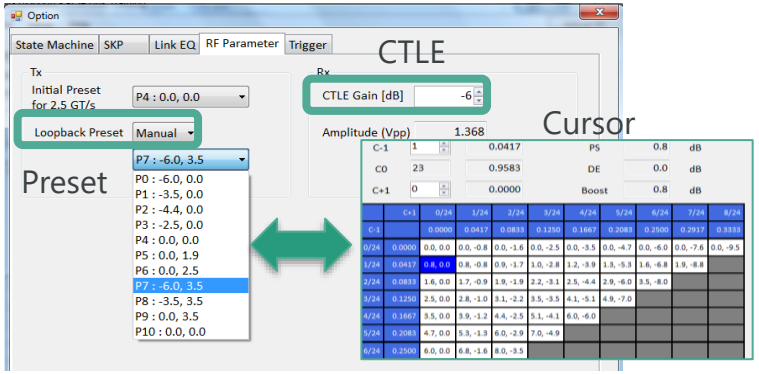
- Data Rate: 32 GT/s
- Common/SRIS/SRNS Clock Architecture
- Required Instruments:
  - Keysight 50 GHz Oscilloscope (DSAX or newer series) or Tektronix 50 GHz (DPS or newer series)
  - Anritsu Signal Quality Analyzer-R MP1900A
  - Gen5 Base Fixture or Gen4 ISI board



Features of Anritsu PCIe Solution(2/2)

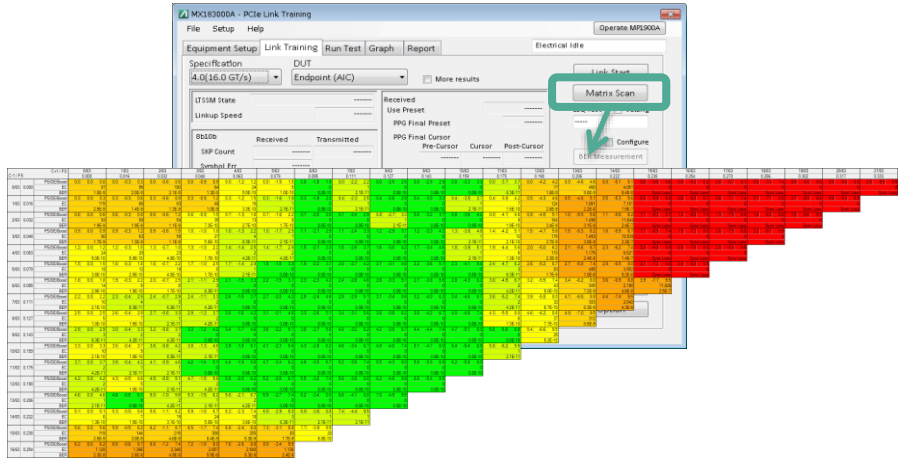
Bit Error Analysis

- Set Loopback Preset to Manual and change the preset from P0 to P10 to determine the optimum preset/Cursor at the DUT.



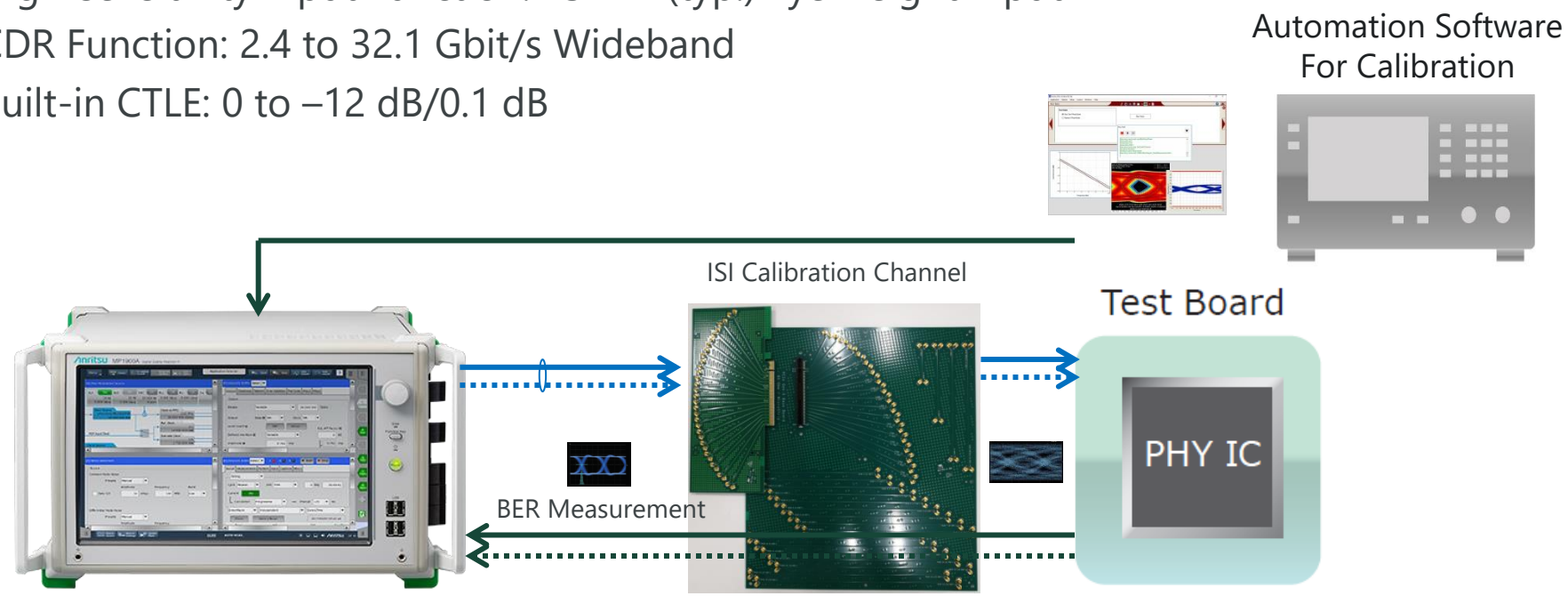
- To find the DUT optimum setting, change CTLE Gain to 0 to –12 dB.

- The optimum Tx EQ value can be found automatically using the matrix Scan function.



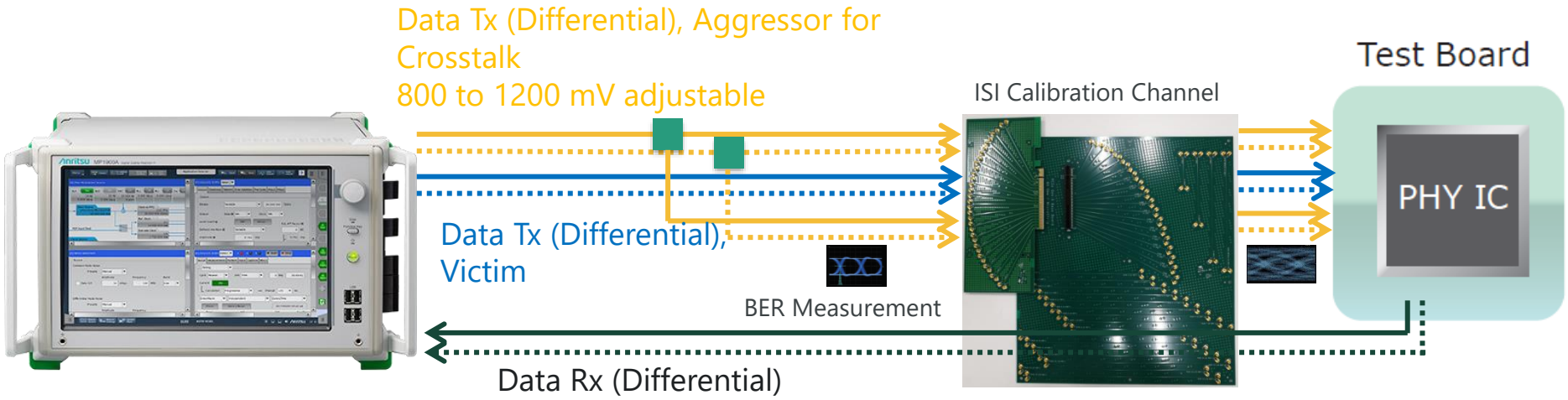
Generating Stress Signal for Rx Test & Measuring BER Using MP1900A

- Stress Signal Generation
  - Jitter Addition Function: SJ/RJ/SSC
  - Noise Addition Function: Common Mode/Differential Mode
  - Emphasis Control
  - Crosstalk Signal Generation: Multichannel 4ch max./MP1900A
- BER Measurement
  - Jitter Tolerance Measurement
  - High-sensitivity Input Function: 15 mV (typ.) Eye Height Input
  - CDR Function: 2.4 to 32.1 Gbit/s Wideband
  - Built-in CTLE: 0 to –12 dB/0.1 dB



Gen5 Crosstalk Test

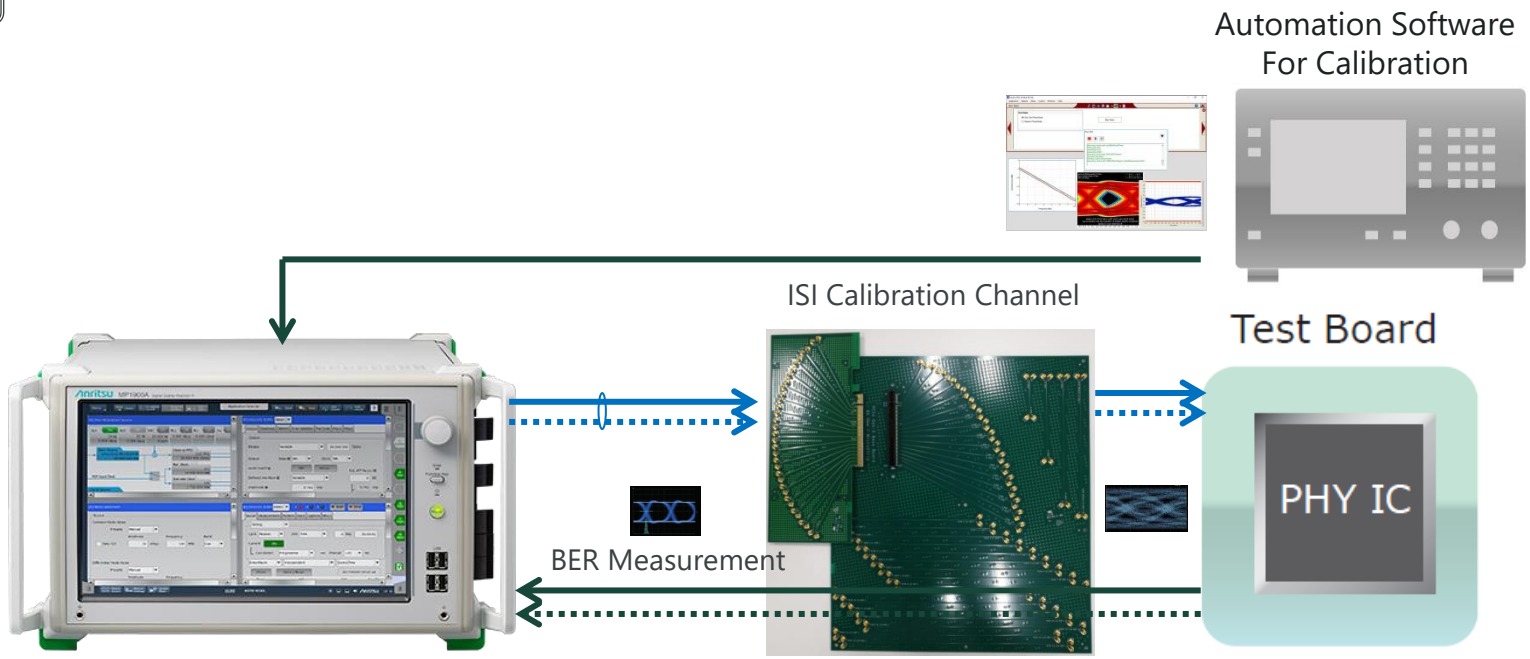
- Dual channel PPG enables true crosstalk testing



PCI Express Gen5 Rx Test Outline

➢ PCI Express PHY IP Device Rx Test Sequence

Stress Signal Calibration	Transition to Loopback Status	Stress Signal Input Test
Applicable Software		
Automation Software: GRL-PCIE5-BASE/CEM-RXA or QPHY-PCIE-Tx-Rx	Link Training Software: MX183000A-PL021 (Gen1 to 4) MX183000A-PL025 (Gen5)	・Jitter Tolerance Margin Test: MX183000A-PL001 or ・Jitter Sweep Test (Pass/Fail): GRL-PCIE5-BASE/CEM-RXA or QPHY-PCIE-Tx-Rx



PCI express Measurement Summary

PCI Express Gen5 Calibration Points (1/3)

Stress Signal Calibration → Transition to Loopback Status → Stress Signal Input Test

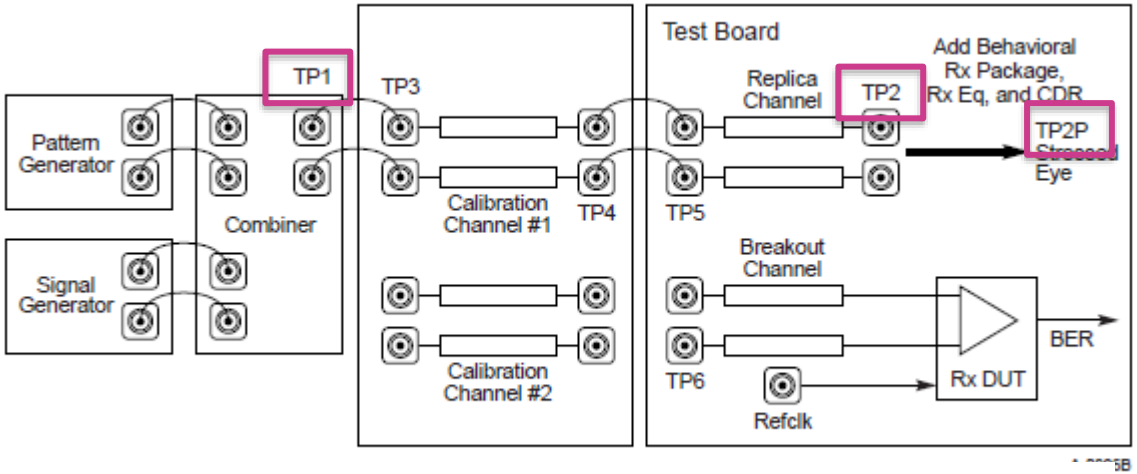


Table 8-9 Stressed Jitter Eye Parameters

Symbol	Parameter	2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	32.0 GT/s	Units	Details
$V_{RX-LAUNCH}$	Generator launch voltage	800 to 1200	800 to 1200	800 to 1200	720 to 800	720 to 800	mV PP	Note 1
T_{RX-UI}	Unit Interval	400	200	125	62.5	31.25	ps	
T_{RX-ST}	Eye width	≤ 0.4	≤ 0.32	≤ 0.30	≤ 0.30	≤ 0.30	UI	Note 3, 4, 8, 10
V_{RX-ST}	Eye height	≤ 175	≤ 100	≤ 25	≤ 15	≤ 15	mV PP	Note 2, 4, 8, 9
$T_{RX-ST-SJ}$	Swept Sj	N/A	75 ps (max) See Note 11	See Section 8.4.2.2.1	See Section 8.4.2.2.1	See Section 8.4.2.2.1	ps	Note 5
$T_{RX-ST-RJ}$	Random Jitter	N/A	3.4	(max) 3.0	1.0	0.5	ps RMS	Note 6, 7
$V_{RX-DIFF-INT}$	Differential noise	N/A	N/A	14	14	10	mV PP	Note 7, 12 Adjust to set EH. Frequency = 2.1 GHz .
$V_{RX-CM-INT}$	Common mode noise	150	150	150	150	150	mV PP	Note 8

PCI Express Gen5 Calibration Points (2/3)

Stress Signal Calibration → Transition to Loopback Status → Stress Signal Input Test

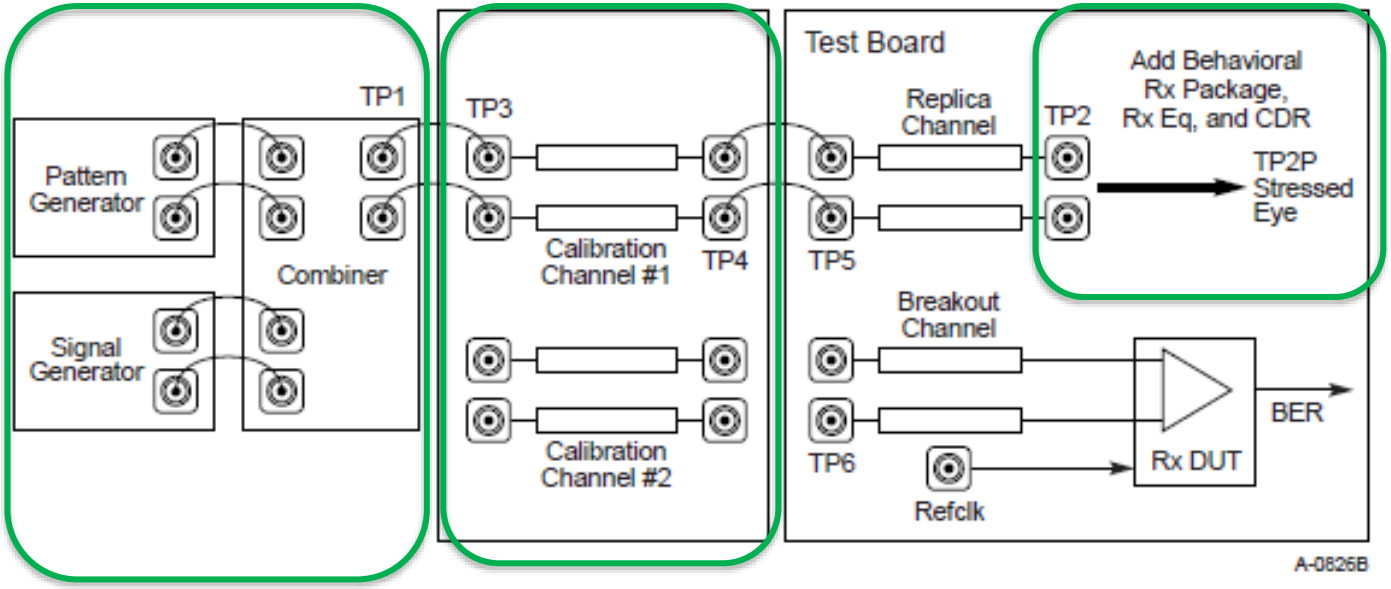
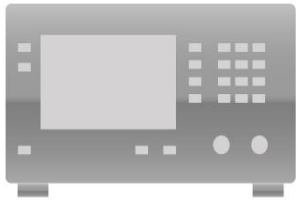


Figure 8-22 Rx Testboard Topology for 16.0 and 32.0 GT/s

MP1900A

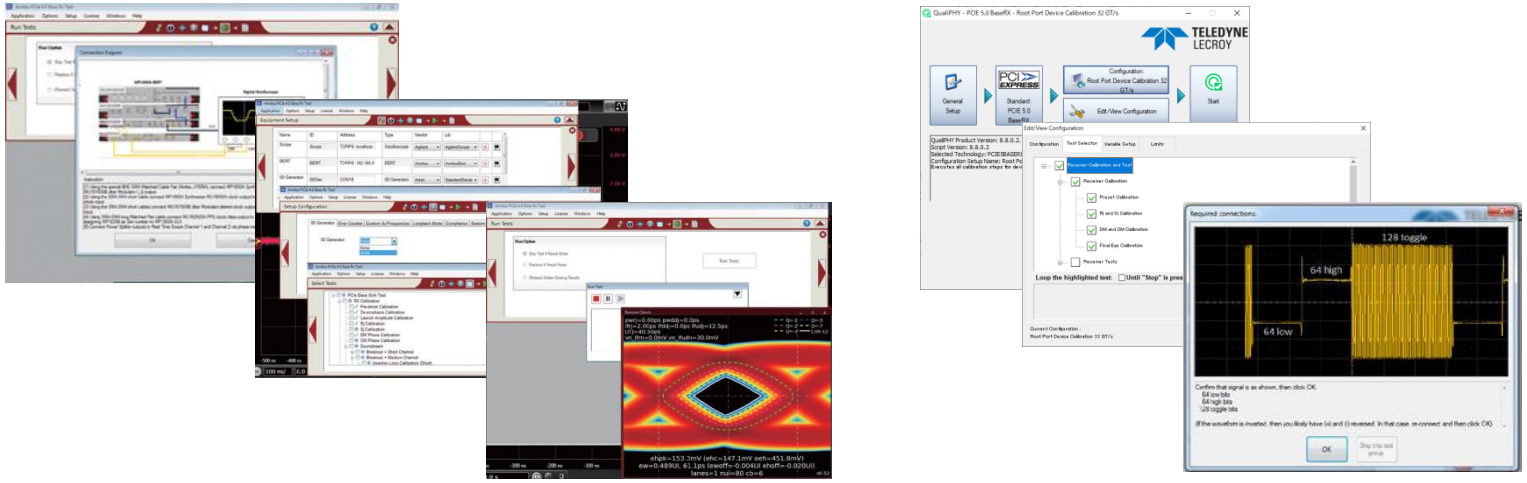


PCI Express Gen5 Calibration Points (3/3)

Stress Signal Calibration → Transition to Loopback Status → Stress Signal Input Test

- Stress Signal Calibration

Automation Software GRL-PCIE5-BASE/CEM-RXA/QPHY-PCIE-Tx-Rx Features



Examples of Calibration Setting and Measurement Screens

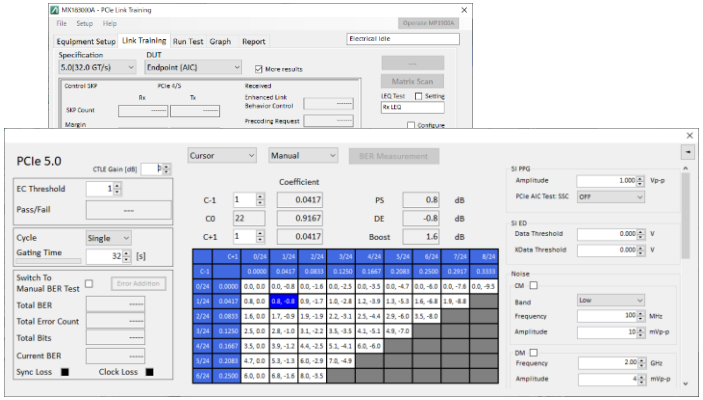
One-touch Calibration of Stress Input Signal and Testing using Automation software

- ✓ Supports PCIe-Gen5 Rev1.0 Devices
- ✓ Executes Calibration of High-reproducibility Test Signal and Rx Test

PCI Express Gen5 Link Training(1/7)

Stress Signal Calibration → **Transition to Loopback Status** → Stress Signal Input Test

- Link Training using MX183000A-PL025



PCI Express Link Training Screen

PPG Pattern Control using MX183000A

- ✓ Screen Functions for Easy Setting of Measurement Conditions and Test Execution
- ✓ Controls PCI Express Device Status and Supports Logical Sub Block Evaluation
- ✓ 8B/10B, 128B/130B, Scramble SKIP Insertion

Item	MX183000A-PL025 Specification
Supported Standard	Gen5 (32 GT/s)
Test Pattern	Compliance (MCP, CP), PRBS (7, 9, 10, 11, 15, 20, 23, 31)
LTSSM State	Transition to Detect, Polling, Configuration, Recovery, Loopback
Loopback Through	Configuration, Recovery
TS Set Pattern	SKP Insertion/Filtering, 8B/10B, 128B/130B, FTS, Link Number, Lane Number, Scrambling

PCI Express Gen5 Link Training(2/7)

- Added and Changed Several Parameters Affecting Link Training

Requirement	Description
Enhanced Link Behavior Control	Added TS parameter for LEQ to PCIe 5.0
Precoding	Receiver can request precoding from transmitter to operate at data rates of 32.0 GT/s or higher
SKP OS/EIEOS/EIEOSQ	SKP OS Identifier changed from AAh to 99h 32G EIEOS has same frequency compared to 16G Two consecutive EIEOS for data rates of 32.0 GT/s
MCP 5.0	EIEOS changed to EIEOSQ

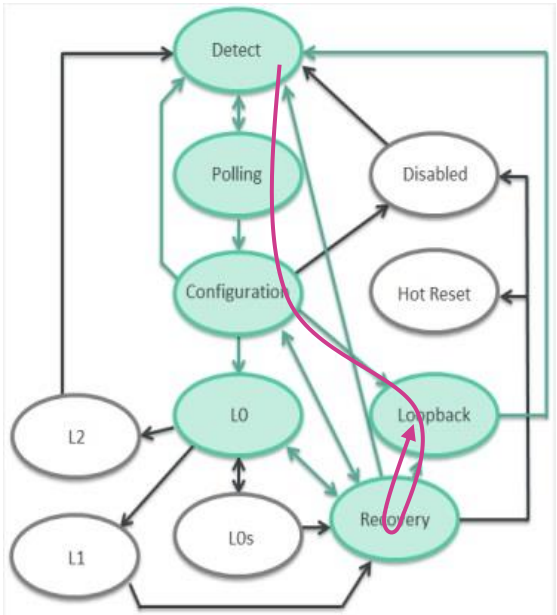
PCI Express Gen5 Link Training(3/7)

Stress Signal Calibration → **Transition to Loopback Status** → Stress Signal Input Test

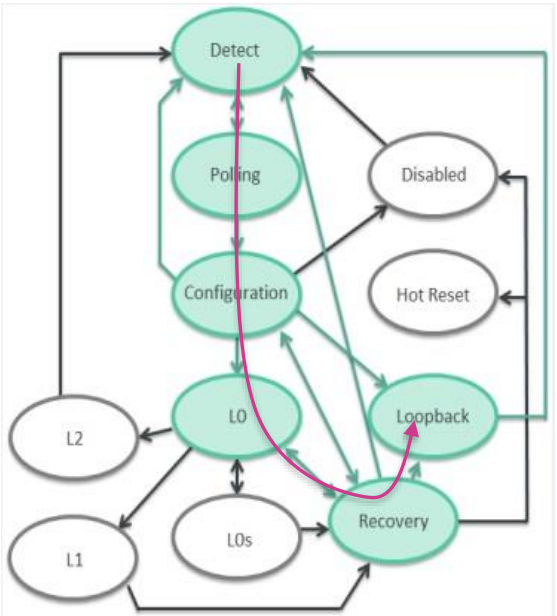
- Enhanced Link Behavior Control

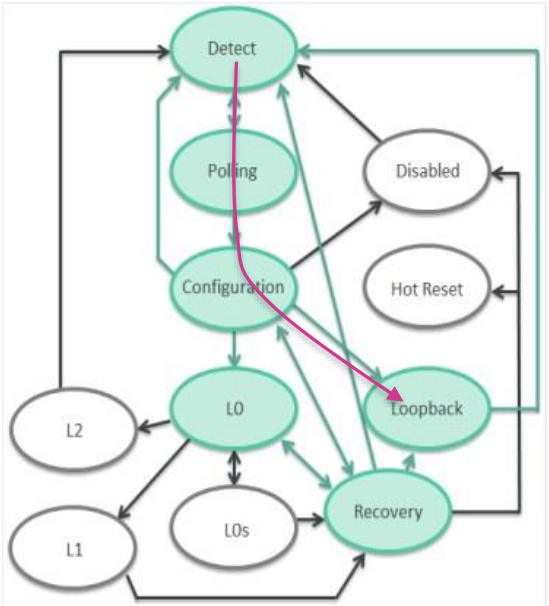
  Defined option to perform Recovery Equalization when selecting loopback through configuration route

Only for 32 GT/s (New)



8, 16, and 32 GT/s (Legacy)





PCI Express Gen5 Link Training(4/7)

- Enhanced Link Behavior Control

  Defined new routes for Link Equalization

Case	8.0 GT/s EQ	16.0 GT/s EQ	32.0 GT/s EQ	Description
A	✔	-	-	PCIe 3
B	✔	✔	-	PCIe 4
C	-	-	✔	PCIe 5 Equalization bypass to highest rate support
D	✔	✔	✔	PCIe 5 Full Equalization required
E	-	-	-	PCIe 5 No Equalization needed

PCI Express Gen5 Link Training(5/7)

Stress Signal Calibration → Transition to Loopback Status → Stress Signal Input Test

- Precoding

At 32.0 GT/s, an optional precoding mechanism is provided, which receivers can enable optionally, to reduce the risk of DFE-related error bursts in high transition data patterns causing silent data corruption.

The receiver can request precoding from its transmitter for operation at data rates of 32.0 GT/s or higher.

Precoding can be applied independently to either Tx or Rx.

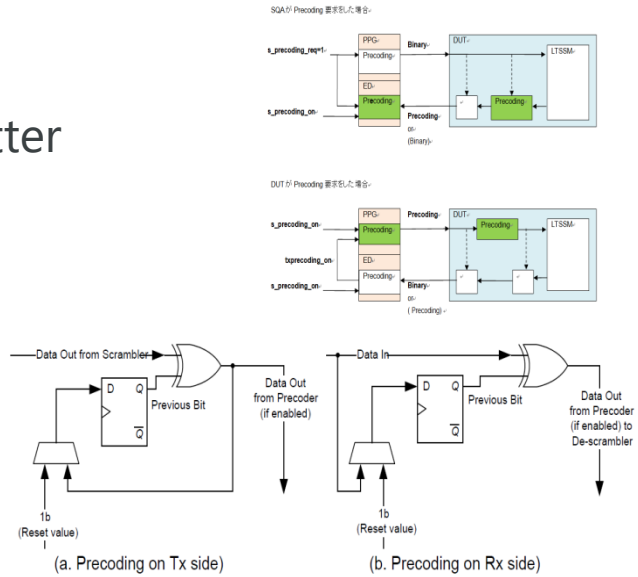
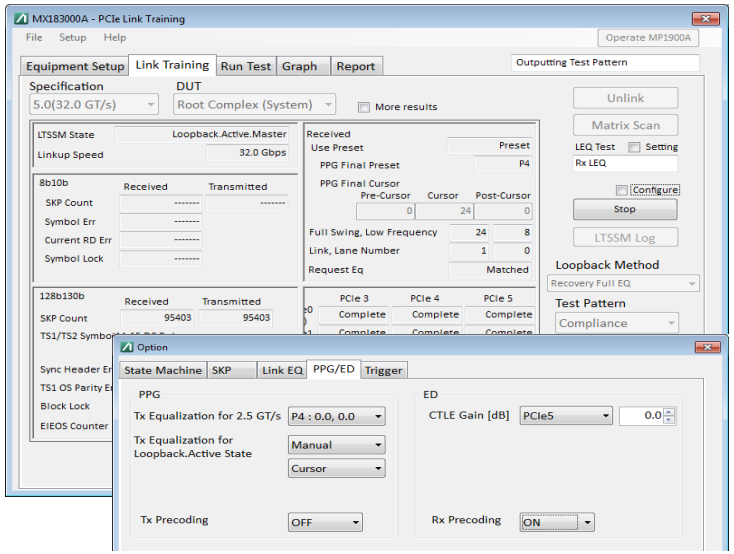


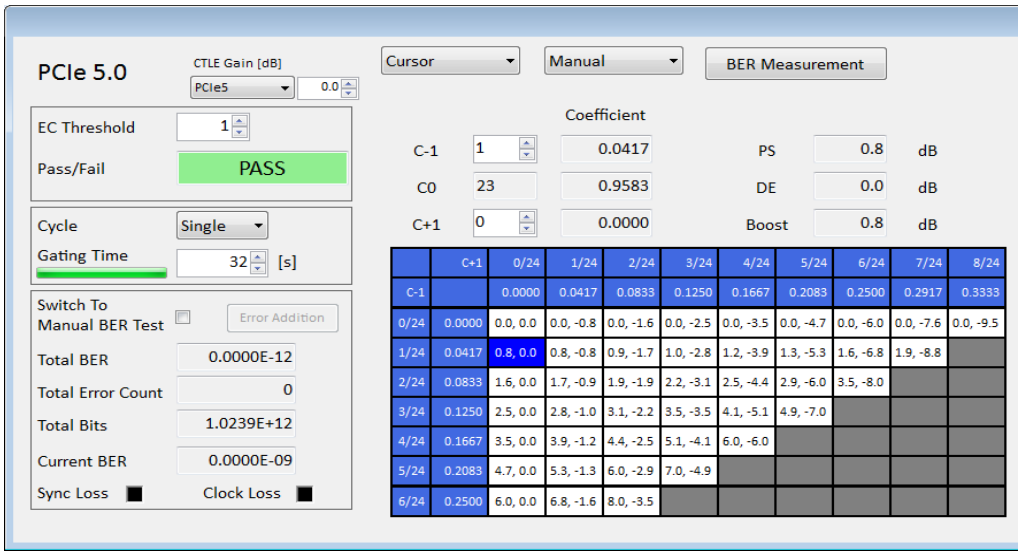
Figure 4-20 Precoding working the scrambler/ de-scrambler

PCI Express Gen5 Link Training(6/7)

Stress Signal Calibration → **Transition to Loopback Status** → Stress Signal Input Test

- MX183000A Already Supports:
  - ✓ Enhanced Link Behavior Control
  - ✓ Precoding
  - ✓ SKP OS/EIEOS
  - ✓ MCP 5.0





PCI Express Gen5 Link Training(7/7)

Stress Signal Calibration → Transition to Loopback Status → Stress Signal Input Test

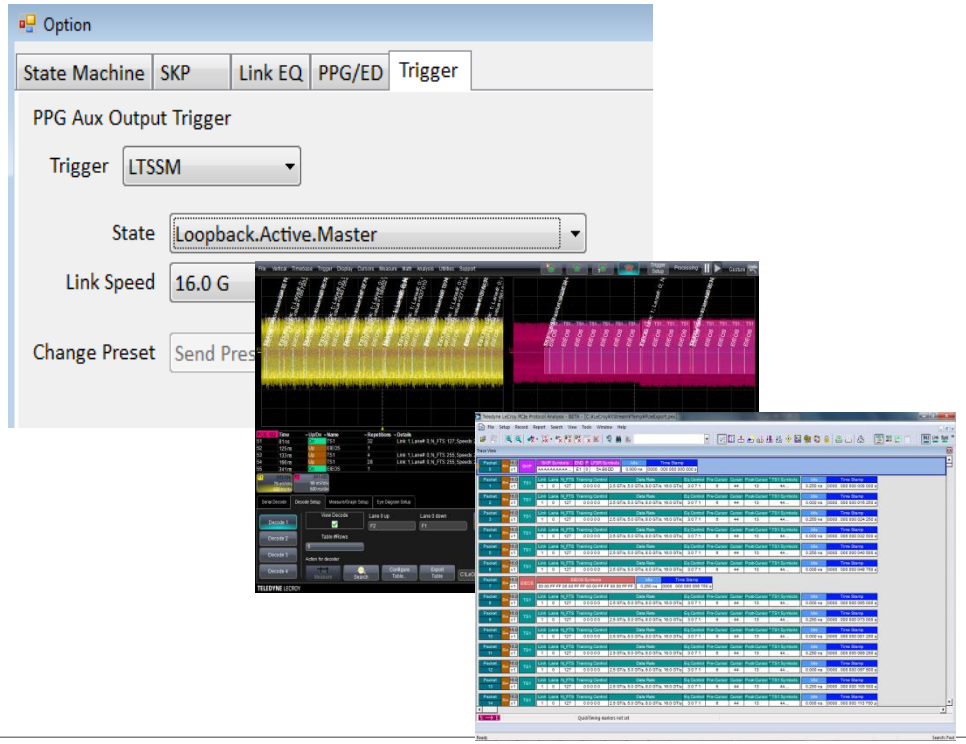
- Strong MX183000A Support for Customer Debugging

LTSSM Log Viewer

Training Log Viewer

Time [ns]	ΔTime [ns]	State	Speed[GT/s]	Detect Preset	Error Count	Use Preset	Preset	Pre-cursor	Cursor	Post-cursor	FS	LF
440,750,376	4	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
440,750,380	1,153,864	RECOVERY_EQUALIZATION_PHASE0	16.0	---	---	---	---	---	---	---	24	8
441,904,244	8	RECOVERY_EQUALIZATION_PHASE0	16.0	---	---	---	---	---	---	---	24	8
441,904,252	2,848	RECOVERY_EQUALIZATION_PHASE1	16.0	---	---	---	---	---	---	---	---	---
441,907,100	272	RECOVERY_EQUALIZATION_PHASE2	16.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P6	3	21	0	---	---
441,907,372	1,999,728	RECOVERY_EQUALIZATION_PHASE2	16.0	1 (MP1900A <== DUT)	0	1 (Preset)	P6	3	21	0	---	---
443,907,100	2,864	RECOVERY_EQUALIZATION_PHASE2	16.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P4	0	24	0	---	---
443,909,964	2,000,000	RECOVERY_EQUALIZATION_PHASE2	16.0	1 (MP1900A <== DUT)	0	1 (Preset)	P4	0	24	0	---	---
445,909,964	2,860	RECOVERY_EQUALIZATION_PHASE3	16.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P5	2	22	0	---	---
445,912,824	4	RECOVERY_EQUALIZATION_PHASE3	16.0	1 (MP1900A <== DUT)	0	1 (Preset)	P5	2	22	0	---	---
445,912,828	1,999,980	RECOVERY_EQUALIZATION_PHASE3	16.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P5	2	22	0	---	---
447,912,808	4	RECOVERY_EQUALIZATION_PHASE3	16.0	1 (MP1900A <== DUT)	0	1 (Preset)	P4	0	24	0	---	---
447,912,812	2,002,840	RECOVERY_EQUALIZATION_PHASE3	16.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P4	0	24	0	---	---
449,915,652	64	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
449,915,716	2,980	RECOVERY_RCVR_CFG_TS2	16.0	---	---	---	---	---	---	---	---	---
449,918,696	508	RECOVERY_IDLE	16.0	---	---	---	---	---	---	---	---	---
449,919,204	12	L0	16.0	---	---	---	---	---	---	---	---	---
449,919,216	2,420	RECOVERY_RCVR_LOCK	16.0	---	---	---	---	---	---	---	---	---
449,921,636	6,553,832	RECOVERY_RCVR_CFG_EQTS2	16.0	---	---	---	---	---	---	---	---	---
456,475,468	100,016	RECOVERY_SPEED	16.0	---	---	---	---	---	---	---	---	---
456,575,484	32	RECOVERY_SPEED	32.0	---	---	---	---	---	---	---	---	---
456,575,516	4	RECOVERY_RCVR_LOCK	32.0	---	---	---	---	---	---	---	---	---
456,575,520	1,213,648	RECOVERY_EQUALIZATION_PHASE0	32.0	---	---	---	---	---	---	---	24	8
457,789,168	8	RECOVERY_EQUALIZATION_PHASE0	32.0	---	---	---	---	---	---	---	24	8
457,789,176	1,892	RECOVERY_EQUALIZATION_PHASE1	32.0	---	---	---	---	---	---	---	---	---
457,791,068	264	RECOVERY_EQUALIZATION_PHASE2	32.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P6	3	21	0	---	---
457,791,332	1,999,736	RECOVERY_EQUALIZATION_PHASE2	32.0	1 (MP1900A <== DUT)	0	1 (Preset)	P6	3	21	0	---	---
459,791,068	1,912	RECOVERY_EQUALIZATION_PHASE2	32.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P4	0	24	0	---	---
459,792,980	2,000,000	RECOVERY_EQUALIZATION_PHASE2	32.0	1 (MP1900A <== DUT)	0	1 (Preset)	P4	0	24	0	---	---
461,792,980	1,912	RECOVERY_EQUALIZATION_PHASE3	32.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P5	2	22	0	---	---
461,794,892	4	RECOVERY_EQUALIZATION_PHASE3	32.0	1 (MP1900A <== DUT)	0	1 (Preset)	P5	2	22	0	---	---
461,794,896	2,000,004	RECOVERY_EQUALIZATION_PHASE3	32.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P5	0	24	0	---	---
463,794,900	4	RECOVERY_EQUALIZATION_PHASE3	32.0	1 (MP1900A <== DUT)	0	1 (Preset)	P4	0	24	0	---	---
463,794,904	2,001,908	RECOVERY_EQUALIZATION_PHASE3	32.0	0 (MP1900A ==> DUT)	0	1 (Preset)	P4	0	24	0	---	---
465,796,812	32	RECOVERY_RCVR_LOCK	32.0	---	---	---	---	---	---	---	---	---
465,796,844	1,948	RECOVERY_RCVR_CFG_TS2	32.0	---	---	---	---	---	---	---	---	---
465,798,792	524	LOOPBACK_ENTRY_MASTER_TS1	32.0	---	---	---	---	---	---	---	---	---
465,799,316	0	LOOPBACK_ACTIVE_MASTER	32.0	---	---	---	---	---	---	---	---	---

LTSSM Trigger



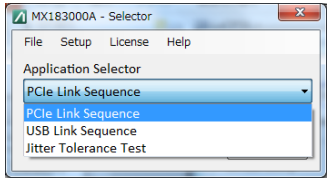
PCI Express Gen5 Rx JTOL Test (1/5)

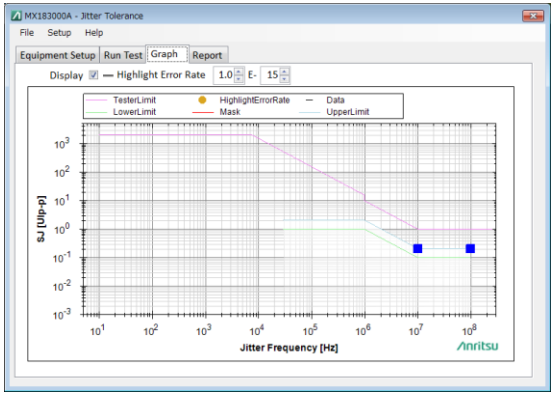
Stress Signal Calibration → Transition to Loopback Status → **Stress Signal Input Test**

➢ Stress Signal Input Test (Jitter Tolerance Margin Test Using MX183000A-PL001

Jitter Control and Tolerance Measurement using MX183000A

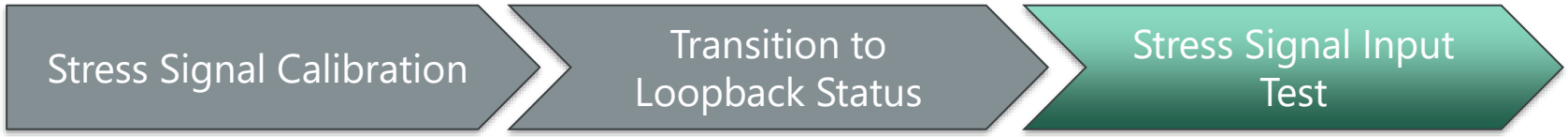
- ✓ Impresses SJ and Tests PHY Device Jitter Tolerance
- ✓ Tests Device Margin using Low BER Estimation
- ✓ Outputs Measurement Results in HTML and CSV Formats





Item	MX183000A-PL001 Specifications
Jitter Setting Range	Complies with MU181500B Jitter Modulation Source
Direction Search	Binary, Downward Linear, Downward Log, Upward Linear, Upward Log, Binary + Linear
Detection	Error Rate, Error Count, Estimate
Error Threshold	1.0E-3 to 1.0E-14
Highlight Error Rate	9.9E-9 to 1.0E-20 (at estimate)
Report Function	Reports results in HTML and CSV formats

PCI Express Gen5 Rx JTOL Test (2/5)



- Measurement System Uncertainty

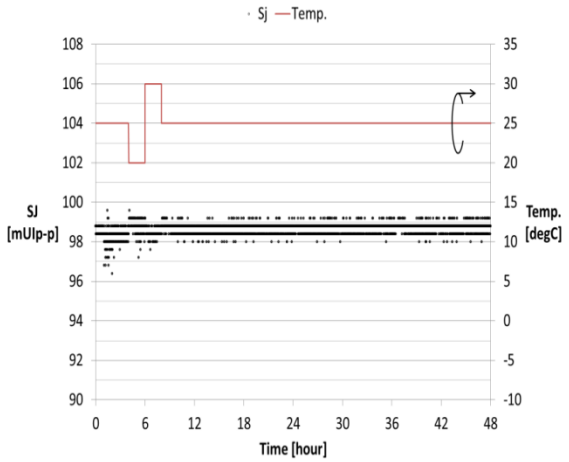
  - Challenging calibration targets
  - Severe DUT Rx margins cause factors preventing error-free measurement
  - Eliminate BER measurement system uncertainties

PCI Express Gen5 Rx JTOL Test (3/5)

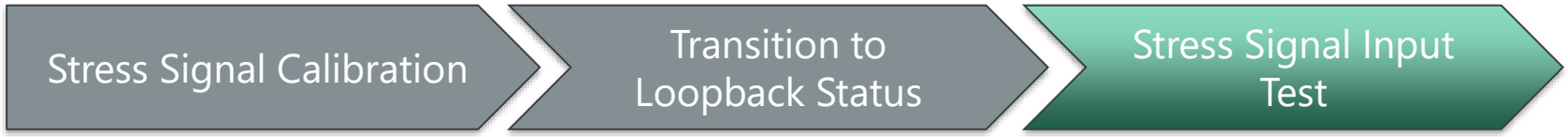
Stress Signal Calibration → Transition to Loopback Status → Stress Signal Input Test

- All-in-One MP1900A with built-in CDR
  - Recovers Clock from Data using SSC to eliminate errors caused by Data/Clock line length differences

- MP1900A w/ High Signal Quality and High Repeatability
  - Jitter time and temperature dependency: <±2% (2 days, ±5°)
  - Low Intrinsic Jitter: 115 fs rms



PCI Express Gen5 Rx JTOL Test (4/5)



- Crosstalk Impact on Signal Quality

Crosstalk can impact signal quality at high data rates.

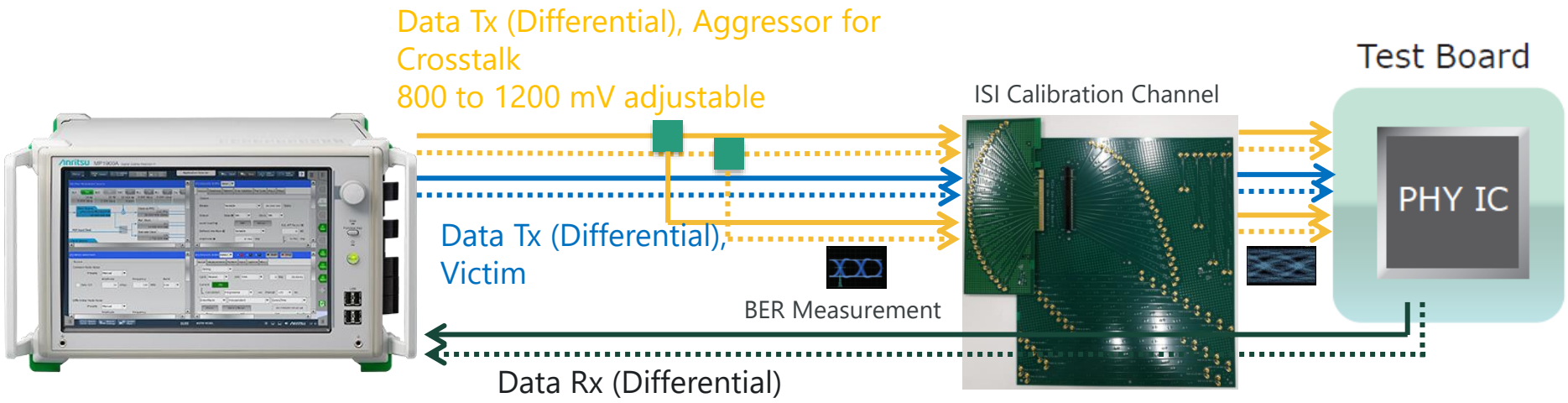
PCIe 5 allocates a port to transmit MCP from other a non-test lane of the DUT (Training Sequence Symbol Number 5, Bit 5).

This method cannot generate a quantitative Aggressor Signal.

PCI Express Gen5 Rx JTOL Test (5/5)

Stress Signal Calibration → Transition to Loopback Status → Stress Signal Input Test

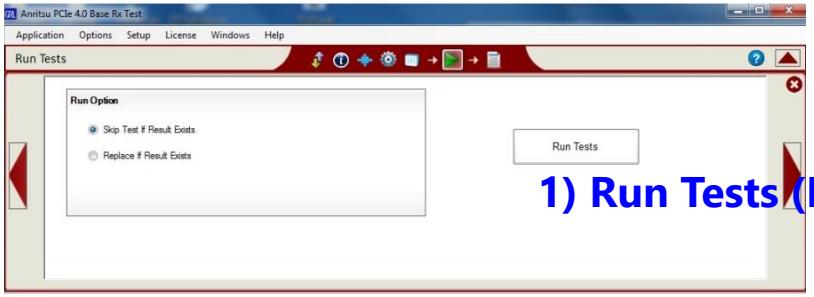
- MP1900A Generates Aggressor Signal using Multichannel Generator
  - All-in-one BERT with multichannel signal generator
  - Supports DUT requests to send MCP



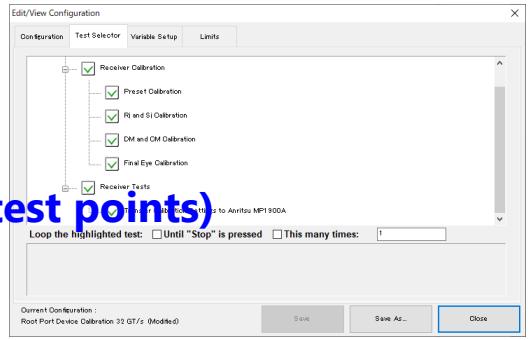
PCI Express Gen5 Test Report

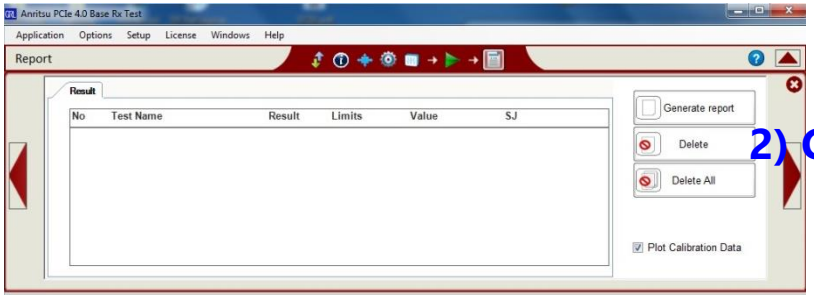
Stress Signal Calibration → Transition to Loopback Status → Stress Signal Input Test

- Stress Signal Input Test

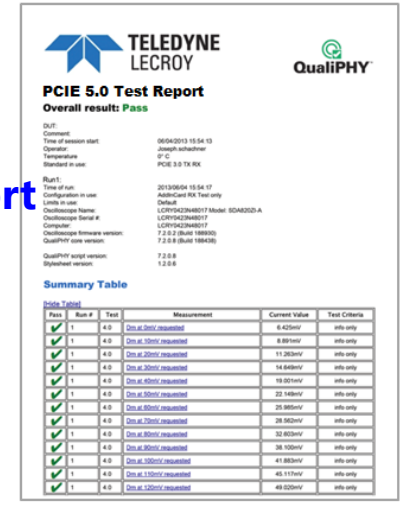


1) Run Tests (Pass/Fail at test points)





2) Generate Report



Anritsu

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