Technical Note

Anritsu envision : ensure

Effect of Transmission Line Length on BER Testing

- How to Handle High-Speed Digital Signals -

Signal Quality Analyzer-R MP1900A
Signal Quality Analyzer MP1800A

1. Market Trends and Trends in Measurement Demand

Development is now progressing on 100 GbE, 400 Gbps, and 1 Tbps communications systems due to the need for increases in the speed and capacity of networks, servers and storage. Consequently, 30+ Gbps interfaces are being developed for internal systems communication.

When handling signals faster than 30 Gbps, more care is required than conventional signals. Anritsu has previously compiled technical notes for measuring instruments when observing these types of high-speed signal waveforms.*[1]

This document describes notes for handling the lengths of cables carrying clock and data signals, with focus on testing the jitter tolerance of high-speed signals, as well as the handling of differential signals that are becoming mainstream in high-speed transmissions.

2. Preparing for Testing

Correct measurement requires correct use of measuring instruments. At the same time, it also requires correct understanding of the instruments' limitations. Measurements beyond these limitations often measure the characteristics of the instrument, rather than those of the device under test (DUT). For example, when measuring a waveform using a sampling scope, if the waveform includes a frequency component outside the sampling scope's frequency band, the true characteristics of the input waveform will not be displayed; instead, the characteristics of the sampling scope will be displayed.*[1]

Similarly for jitter tolerance measurements, if jitter exceeding the tolerance of any instrument in the measurement setup is applied during measurement, the jitter tolerance of that instrument rather than that of the DUT will show in the results. If the measuring instrument has a D-flip-flop, FIFO, or other retiming circuit, or PLL circuit like clock recovery, this can be a bottleneck for jitter tolerance. When testing jitter tolerance, it is essential to know the actual performance boundaries of the measuring instruments.

Even if all the measuring instruments in the measurement system have sufficient jitter tolerance, the measurement result may be worse than the true DUT characteristics, depending on the set up. Recent increases in data-signal speeds require strict assessment of the impact of jitter in order to ensure transmission quality. Due to the adverse impact of the noise environment (e.g., from power supplies, thermal, and PLL), jitter applied during testing is becoming more complex and faster, and the total jitter amount is trending upward. Under these circumstances, jitter tolerance testing must consider the impact of items that did not pose great problems in the past, such as differences in the lengths of the routes of the clock and data signals in the test system.

The next section describes precautions when handling the lengths of clock and data routes.

3. Differences in Lengths of Clock and Data Routes

This section describes the lengths of clock and data signal routes using a measurement system where the pulse pattern generator (PPG) data signal is connected to an error detector (ED) via the DUT and clock recovery unit (CRU) as an example.

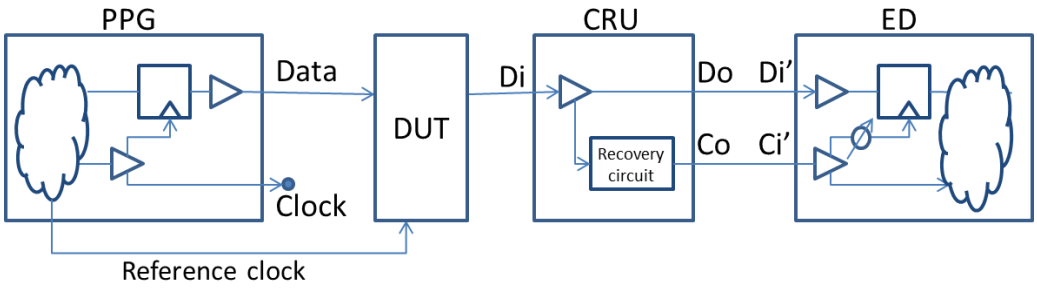

Figure 3.1: Jitter Tolerance Measurement System

The data signal output the DUT is connected to the CRU. The CRU splits the data signal into two routes: one passing through the CRU for output again unchanged, and another connected to a circuit that recovers the clock. The CRU outputs the data signal, and the clock recovered from the data signal. Here, the timing of the clock and data output from the CRU are compared. Since the data signal is simply split by the CRU, it passes along a shorter route. Meanwhile, the clock signal is recovered based on the data signal, and there is some delay in the clock-recovery circuit itself. Consequently, it passes along a longer route than the data signal.

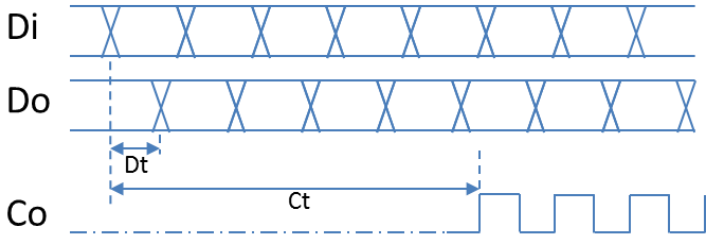

Figure 3.2: CRU I/O Timing

Figure 3.2 does not show the time from when the burst data is input until the clock is recovered. Rather, it shows the timing of a specific data crossover point and the phase-aligned clock edge, where *Di* is the CRU input data, *Do* is the CRU output data, and *Co* is the output of the clock recovered by the CRU.

Although it is impossible to determine that the data crossover point and clock-edge timing phases are aligned using the actual CRU, if the phases are aligned, logically we can conclude that times *Dt* and *Ct* in Fig. 3.2 will not change even at slower bit rates. In the figure, *Dt* is the propagation delay from when data is input to the CRU until it is output, and *Ct* is the propagation delay from when data is input to the CRU until the recovered clock is output. Although we cannot determine the edge dip where *Dt* and *Ct* are constant by observing the *Co* and *Do* waveforms at a single bit rate, we can identify the data and clock edges where *Ct* and *Dt* are constant by observing the waveform with multiple bit rates. The state where the relationship between *Ct* and *Dt* is constant regardless of the bit rate is called "absolute phase alignment."

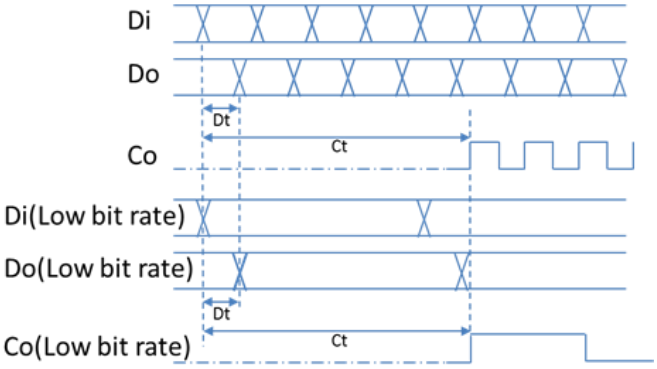

Figure 3.3: CRU I/O Timing (Low Bit Rate)

Within the test system, we must also know the difference in the lengths of the routes taken by the clock and data signals in the ED. To measure the data signal accurately, the instrument must be designed so that the distance to the first D-flip-flop is the shortest. The clock signal route tends to be longer than the data signal route, because divided clocks are generated using circuits in the back end of the ED. As shown in Fig. 3.4, this results in a longer *Ct-dff* time than *Dt-dff*.

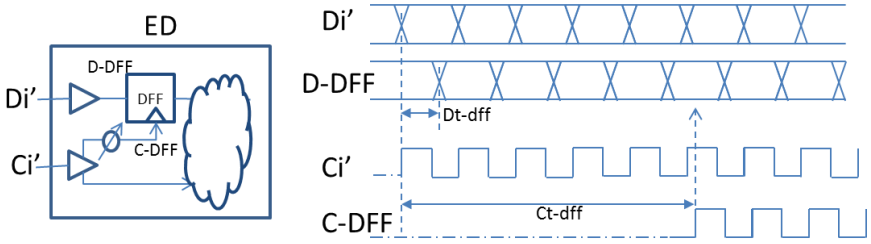

Figure 3.4: Routes and Timing in ED

Furthermore, if a unit with a D-flip-flop, such as a pre-emphasis unit, is connected midway in the test system, the lengths of the data and clock signal routes between the PPG and Emphasis must be ascertained in the same way.

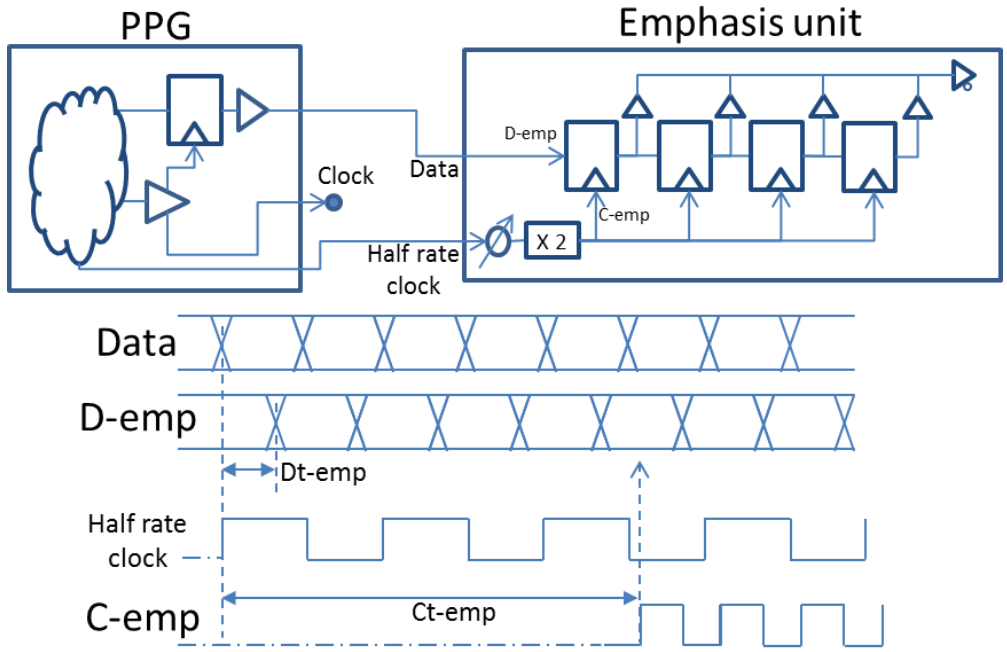

Figure 3.5: Connections and Timing between PPG and Emphasis

For example, in the case of the Anritsu MP1825B Emphasis, the PPG outputs a half-rate clock that the Emphasis unit multiplies to a full-rate clock. In this case, the clock propagation delay (*C-emp*) is longer than the data propagation delay (*D-demp*) between the PPG and Emphasis unit due to the delay in the circuit used to multiply the half-rate clock.

Under these circumstances, to align the phases of the clocks and data between these devices, the lengths of the cables connecting devices like the CRU and ED, and the PPG and Emphasis, must be adjusted taking into account the differences in lengths of the signal routes inside the devices. Since the clock route between the CRU and ED is longer by (Ct – Dt) + (Ct-dff – Dt-dff), the data cable must be lengthened by the amount of the time difference (Figs. 3.2 and 3.4). Similarly, the clock and data between PPG and Emphasis can be aligned by lengthening the data route by (Ct-emp – Dt-emp) (Fig. 3.5).

If the jitter impact is low, absolute alignment of the clock and data signals in the ED is unnecessary. If the relationship between the clock and data in the first D-flip-flop of the ED meets the conditions for hold time and setup time, a valid measurement can be obtained. Error detectors have auto search and other features to adjust the relationship between the data and clock automatically, so it is normally unnecessary to pay attention to the relationship between the clock and data within measuring instruments.

Similarly, if the impact of jitter is low, the user does not need to adjust the phase relationship of the Anritsu Emphasis Unit, because it adjusts the clock and data phase internally automatically.

Next, what about when the jitter impact is high? As explained above, we do not need to worry about absolute phase alignment when the jitter impact is low, but if the jitter impact is high, the measurement system must consider absolute phase.

The following example describes the impact of jitter by comparing the amount of change at the data crossover point when applying 10-Hz, 10UI, sine-wave jitter to a 10-Gbps data signal, versus applying 10-MHz, 10UI sine-wave jitter to the same signal.

On a 50-Ω transmission line, an electrical signal normally travels at a speed of 4.75 ns per meter. This means that when measuring the data signal with an oscilloscope, changing the cable length by 10 cm would shift the waveform position by 475 ps.

Each cycle of a 10-Gbps data signal is 100-ps long, so applying jitter of 10UI causes the data crossover point to make the round trip in 1000 ps. In this case, the data crossover point would travel a distance equivalent to 1000 ps x 2, and by converting using the above electrical speed of 4.75 ns per meter, this is equivalent to about 42 cm.

Next, consider the jitter modulation rate. A jitter modulation rate of 10 Hz means movement of 42 cm at a rate of 10 Hz (i.e. every 100 ms). Similarly, a modulation rate of 10 MHz means moving a distance of 42 cm every 100 ns. In other words, at the same jitter, a greater distance is moved at a faster modulation rate.

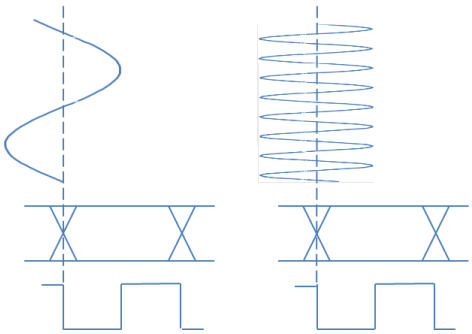

Figure 3.6: Example of Different Modulation Rates at 1UI Jitter

Now, consider the case when the lengths of the clock and data routes are different (i.e. they are not absolutely phase aligned).

For example, if the clock cable is 1 m and the data cable is 50 cm, there is a 50-cm difference in the lengths of the routes. In other words, the data will be received 2.375 ns after it is sent, and the clock will be received 4.75 ns after it is sent. Normally, the receiver will adjust the phase with consideration for this time lag to optimize the relationship between the clock and data. Namely, the phase will have been designed so that the clock rising edge is near the center of two data crossover points to ensure adequate setup and hold times.

Now, consider the changes when jitter is applied to synchronized data and clock signals sent simultaneously, focusing only on the change in the relationship between the clock rising edge and the data cross point caused by the jitter. Even in the presence of jitter, errors do not occur if the clock and data change at the same time, and the optimum phase relationship is maintained. However, errors will occur at the receiving side if either the clock or data route includes a circuit like a PLL that limits the bandwidth of the jitter components and the jitter modulation frequency is outside the circuit bandwidth. Errors occur because the amount of jitter in the clock and data is different, and the phase relationship between the clock and data will exceed the setup and hold time limits of the receiving circuit. To describe the mechanism causing absolute phase errors, this explanation assumes there are no bandwidth-limiting circuits in the measurement system.

The change in the clock and data phase relationship caused by jitter is transmitted at the same speed as the electrical signal itself. Consequently, if the clock and data edges start moving at the same time and there is a 50-cm difference in route lengths, the change on the data side will reach the receiver in 2.375 ns compared to 4.75 ns on the clock side. If the phase difference between the clock and data on the receiving end becomes so large during this 2.375 ns that the setup and hold times cannot be assured, the information is not transmitted correctly, causing errors.

Applying 10-Hz, 10UI, sine-wave jitter causes the clock and data to move with a round trip of 100UI in 1 second. The impact on the clock and data phase relationship during this 2.375-ns interval should be minor, because the movement is only 475 nUI (10 UI/10 Hz x 2 (round trip) x 2.375 ns). Meanwhile, applying 10-MHz, 10UI, sine-wave jitter has a very large impact on the clock and data phase relationship, because by the same calculation, the movement is 475 mUI (10 UI/10M Hz x 2 (round trip) x 2.375 ns).

This impact is greater at larger jitter modulation rates, jitter modulation amounts, and differences between clock and data route lengths. The impact is increased by bit rate, because it is more difficult to ensure the receiver phase margin at faster bit rates. Recent increases in data-transmission speeds have resulted in stricter jitter tolerance requirements. Consequently, while awareness of the clock and data absolute phase was unnecessary previously, now it must be taken into account when building a measurement system.

The manufacturer of your instrument can specify the difference between its clock and data phases.

4. Attentions for Measuring Differentials

Differential high-speed signals are becoming common. This section describes how to handle such signals. Differential signals have several advantages. For example, Data and xData can each act as the others' signal threshold voltage, reducing the impact of common-mode noise applied to both Data and xData, simultaneously. Additionally, twice the voltage margin is obtained compared to using a single-ended device. However, differential signals faster than 20 Gbps require very careful handling, because the voltage and phase margins are worse under some conditions than when using a single-ended device.

The following describes handling of a 28-Gbps signal as a differential signal. Such signals are in active development currently.

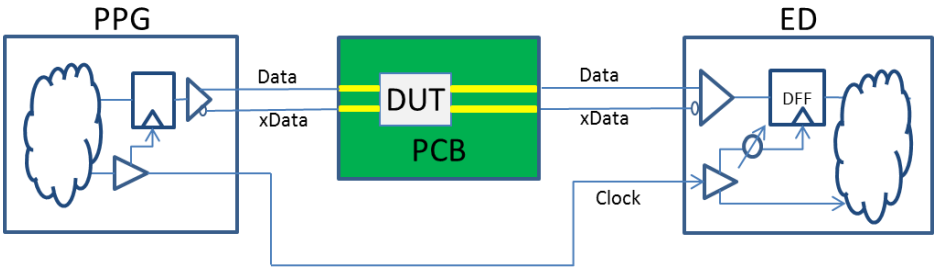

Figure 4.1: Differential Measurement System

In a system like the one above, with the DUT on the PCB connected to an ED via a cable, the differential signal output from the DUT passes through the PCB and cable and is connected to the ED. When handling a differential signal, all differential routes on the DUT must be the same length.

Although we can reduce error between the differentials via the routes on the PCB, what about the route using the cable between the PCB and measuring instrument? This requires an extremely accurate phase-matched cable. The cycle for a 28-Gbps signal is about 35.7 ps. As described in the previous section, electrical signals on a 50-Ω transmission line travel at 4.75 ns per meter, so a 28-Gbps signal with a 35.7 ps cycle has an electrical length of about 7.5 mm. In other words, a 7.5-mm difference in cable lengths is equivalent to a 1-bit skew. Of course, under these conditions, the system cannot operate correctly as a differential signal because if the cable lengths were just 2 to 3 mm different, the skew would be about 40%.

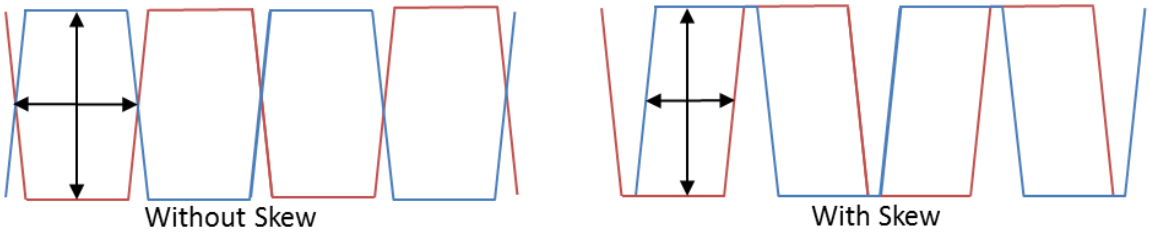

Figure 4.2: Skew and Differential Signals

With the constant-time high- and low-level signal shown in Figure 4.2, there is a risk that the phase margin will be narrower than the voltage margin. However, the actual signal is affected by ISI due to limitations on the bandwidth of the transmission line and other factors. As a result, there is no guarantee that the signal changes fully between high and low level.

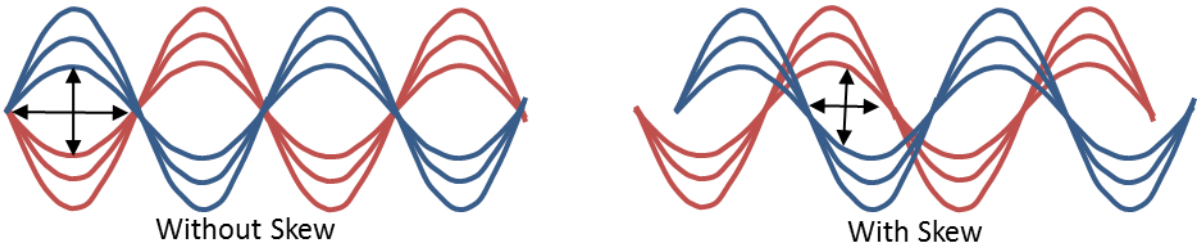

Figure 4.3: Differential Signal Impacted by ISI and Skew

Figure 4.3 shows that when there is skew between differential signals, the voltage margin of a single-ended device is not doubled although differential signals are used. The margin decreases even further if distortion or other noise is added to the signals, yielding worse results when handling them as differential signals than when using a single-ended device.

Furthermore, the electrical length of almost all cables changes by about 2 to 3 ps when the cable is bent or stretched. Although there is rarely need to worry about this, bending the cable when using a single-ended device or low bit rate can change the electrical length by close to 10% of a cycle when using a fast signal (e.g. 28 Gbps).

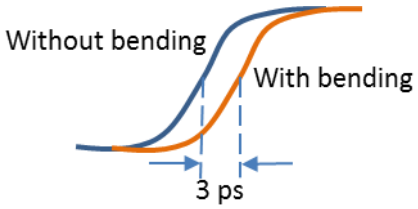

Figure 4.4: Changes in Electrical Length Due to Cable Bending

How should differential signals be used under these types of conditions? One solution is to attach a delay device with a small variable range of about 50 to 100 ps at each end of the phase-matched cables and adjust the electrical lengths to be equal. Bends in cables between devices must be minimized as well.

Even so, it may still be unfeasible to completely eliminate minor errors due to cable bends. In such cases, another solution is to measure with a single-ended device, rather than with differential signals.

The next section describes how to check cable length.

5. How to Measure Differences in Cable Lengths

This section describes two ways to determine whether cables have different lengths. The first is by checking a pulse-signal waveform using a sampling scope; the second is by using a TDR.

5.1 Checking with Pulse Waveform

Even using two phase-matched cables and a sampling scope with multiple inputs, we cannot measure whether the cable lengths are the same by simply connecting both cables at the same time and measuring two inputs, because there is internal skew between the scope inputs. Although nearly all scopes have a feature to adjust internal skew, here we describe a method for measuring simply one input at a time.

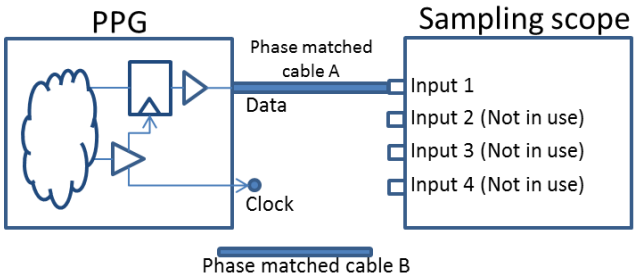

Figure 5.1: Measurement System Using PPG and Sampling Scope

Set the bit rate to be measured at the signal source (e.g. PPG) to 1/10 or lower, the pattern length to 1,024 bits with 16 bits of 1 and all other bits of 0. Connect the first cable (A) to be measured to the PPG output and the scope input.

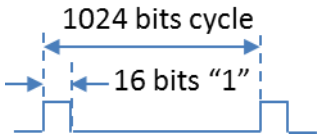

Figure 5.2: Pattern Configuration

Observe the output from the PPG on the scope to see one crossover point from 0 to 1, and save this waveform on the scope. Next, disconnect cable A and connect the second cable (B) to the same scope input. If the cables are very similar in length, differences between the stored first cable A waveform and the second cable B currently displayed can be seen.

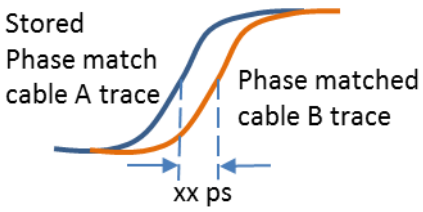

Figure 5.3: Difference between Stored and Displayed Waveforms

Although more accurate measurement is possible by increasing resolution in the time direction, if there is a large length difference between the cables, the edge for comparison may not be displayed after changing the cables. In this case, obtain accurate measurement by setting a coarse resolution in the time direction, and gradually increasing the resolution while observing the edge positions of the two cable waveforms.

5.2 Checking with TDR

This method uses a TDR to measure the cable length using the scope only, rather than checking the pulse waveform using a PPG and scope.

Connect one end of the cable to the TDR cable end, and leave the other end of the cable unconnected. The waveform at the measurement start is displayed as shown in the figure below.

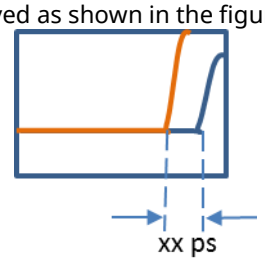

Figure 5.4: TDR Cable Measurement Display

For an unterminated 50-Ω cable, the vertical part on the display is where the impedance becomes infinite. Increase the resolution in the time direction to zoom-in on the point where the infinite impedance appears and save the measurement result. Connect the second cable and make the same measurement. Here, remember, that—rather than indicating the difference in cable lengths directly—the difference on the time axis is double the difference in the cable lengths, because the TDR sends a pulse from the scope side and measures the time until the reflection returns, meaning it displays the pulse round trip.

6. Conclusion

The use of high-speed signals is becoming commonplace. This document describes how to deal with lengths of transmission lines in order to measure such signals accurately from two perspectives: measuring jitter tolerance, and measuring differential signals. This discussion is general in nature; the situation for even faster bit rates still remains to be addressed.

Anritsu will continue updating the measurement literature as your partner in assuring accurate measurement.

7. References

*1: Selecting Tools at Measurement of High-Speed Digital Signals (MP1800A_MP2100A_JE1100)

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Specifications are subject to change without notice.

● **United States**
Anritsu Company
1155 East Collins Blvd., Suite 100, Richardson,
TX 75081, U.S.A.
Toll Free: 1-800-267-4878
Phone: +1-972-644-1777
Fax: +1-972-671-1877

● **Canada**
Anritsu Electronics Ltd.
700 Silver Seven Road, Suite 120, Kanata,
Ontario K2V 1C3, Canada
Phone: +1-613-591-2003
Fax: +1-613-591-1006

● **Brazil**
Anritsu Eletronica Ltda.
Praça Amadeu Amaral, 27 - 1 Andar
01327-010 - Bela Vista - Sao Paulo - SP
Brazil
Phone: +55-11-3283-2511
Fax: +55-11-3288-6940

● **Mexico**
Anritsu Company, S.A. de C.V.
Av. Ejército Nacional No. 579 Piso 9, Col. Granada
11520 México, D.F., México
Phone: +52-55-1101-2370
Fax: +52-55-5254-3147

● **United Kingdom**
Anritsu EMEA Ltd.
200 Capability Green, Luton, Bedfordshire, LU1 3LU, U.K.
Phone: +44-1582-433200
Fax: +44-1582-731303

● **France**
Anritsu S.A.
12 avenue du Québec, Bâtiment Iris 1- Silic 612,
91140 VILLEBON SUR YVETTE, France
Phone: +33-1-60-92-15-50
Fax: +33-1-64-46-10-65

● **Germany**
Anritsu GmbH
Nemetschek Haus, Konrad-Zuse-Platz 1
81829 München, Germany
Phone: +49-89-442308-0
Fax: +49-89-442308-55

● **Italy**
Anritsu S.r.l.
Via Elio Vittorini 129, 00144 Roma, Italy
Phone: +39-6-509-9711
Fax: +39-6-502-2425

● **Sweden**
Anritsu AB
Kistagången 20B, 164 40 KISTA, Sweden
Phone: +46-8-534-707-00
Fax: +46-8-534-707-30

● **Finland**
Anritsu AB
Teknobulevardi 3-5, FI-01530 VANTAA, Finland
Phone: +358-20-741-8100
Fax: +358-20-741-8111

● **Denmark**
Anritsu A/S
Torveporten 2, 2500 Valby, Denmark
Phone: +45-7211-2200
Fax: +45-7211-2210

● **Russia**
Anritsu EMEA Ltd.
Representation Office in Russia
Tverskaya str. 16/2, bld. 1, 7th floor.
Moscow, 125009, Russia
Phone: +7-495-363-1694
Fax: +7-495-935-8962

● **Spain**
Anritsu EMEA Ltd.
Representation Office in Spain
Edificio Cuzco IV, Po. de la Castellana, 141, Pta. 5
28046, Madrid, Spain
Phone: +34-915-726-761
Fax: +34-915-726-621

● **United Arab Emirates**
Anritsu EMEA Ltd.
Dubai Liaison Office
902, Aurora Tower,
P O Box: 500311- Dubai Internet City
Dubai, United Arab Emirates
Phone: +971-4-3758479
Fax: +971-4-4249036

● **India**
Anritsu India Private Limited
2nd & 3rd Floor, #837/1, Binnamangla 1st Stage,
Indiranagar, 100ft Road, Bangalore - 560038, India
Phone: +91-80-4058-1300
Fax: +91-80-4058-1301

● **Singapore**
Anritsu Pte. Ltd.
11 Chang Charn Road, #04-01, Shriro House
Singapore 159640
Phone: +65-6282-2400
Fax: +65-6282-2533

● **P.R. China (Shanghai)**
Anritsu (China) Co., Ltd.
Room 2701-2705, Tower A,
New Caohejing International Business Center
No. 391 Gui Ping Road Shanghai, 200233, P.R. China
Phone: +86-21-6237-0898
Fax: +86-21-6237-0899

● **P.R. China (Hong Kong)**
Anritsu Company Ltd.
Unit 1006-7, 10/F., Greenfield Tower, Concordia Plaza,
No. 1 Science Museum Road, Tsim Sha Tsui East,
Kowloon, Hong Kong, P.R. China
Phone: +852-2301-4980
Fax: +852-2301-3545

● **Japan**
Anritsu Corporation
8-5, Tamura-cho, Atsugi-shi, Kanagawa, 243-0016 Japan
Phone: +81-46-296-6509
Fax: +81-46-225-8352

● **Korea**
Anritsu Corporation, Ltd.
5FL, 235 Pangyoyeok-ro, Bundang-gu, Seongnam-si,
Gyeonggi-do, 13494 Korea
Phone: +82-31-696-7750
Fax: +82-31-696-7751

● **Australia**
Anritsu Pty. Ltd.
Unit 20, 21-35 Ricketts Road,
Mount Waverley, Victoria 3149, Australia
Phone: +61-3-9558-8177
Fax: +61-3-9558-8255

● **Taiwan**
Anritsu Company Inc.
7F, No. 316, Sec. 1, NeiHu Rd., Taipei 114, Taiwan
Phone: +886-2-8751-1816
Fax: +886-2-8751-1817

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