Anritsu

Application Note

High Speed Measurements on Modulated Signals

ML2480A Series Power Meters and MA2491A Power Sensor

An examination of high speed Power Meter architectures and measurements on the latest wireless communication systems

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High Speed Measurements on Modulated Signals

By

Guy Purchon
Product Marketing Manager, Anritsu Limited European Measurement Division, Rutherford Close, Stevenage, Herts. Guy.purchon@eu.anritsu.com

Introduction

This paper deals with the design and construction and measurement principles of a new high speed dual display channel power meter, the ML2480A series from Anritsu.

Wideband modulated signals have historically been used in radar and microwave telecommunication systems. Developments in recent years have seen the application of high modulation rates to a number of new systems reaching commercial deployment, amongst these are Wideband CDMA and Wireless LAN.

A key characteristic of these signals is a high degree of AM in the power envelope. Designers and manufacturers need to be able to measure and verify the peak and average power of the transmission power envelope. This paper outlines the design of a new power meter, which is able to accurately measure the real time variation in the power envelope.

Power Measurements

Accurate power measurement has relied on two main sensor techniques.

1. The thermal element which always reads true RMS power, but which has a slow response time
2. The zero bias Schottky diode.

Historically the zero bias Schottky diode has been used as a high sensitivity square law detector operating from power levels of –70dBm to –20dBm. The introduction of linearity correction techniques first pioneered in scalar analysers increased the dynamic range of the sensor to +20dBm. At first these techniques were limited to CW signals, but the availability of cheaper Digital Signal Processors led to the creation of sampling power meters such as the ML2437A capable of measuring GSM signals using real time linearity correction. Recent advances in signal processing technology have enabled the development of high speed wide bandwidth sampling power meters.

High Speed Signals

Peak measurements tend to have slightly different meanings depending on the market application.

Radar
For radar pulses, the ‘peak power’ is usually taken to mean the average power in the pulse.

Wireless
For Wireless LAN and WCDMA, the peak is the actual maximum excursion of the signal, and it is the ratio between the peak and the average power that is measured.

A power meter must be able to capture sufficient data to accurately measure the peak and calculate the average of the signal. The bandwidth of the system must be wide enough to ensure the peak of the signal is not degraded by bandwidth limitations.

Bandwidth or Rise Time?

The first task of the design is to decide upon the bandwidth of the signal to be measured. WCDMA has a chip rate of 3.84Mc/s so a signal bandwidth of >5MHz would be adequate for this scenario. WLAN and Radar signals have potentially much higher bandwidths. WLAN 802.11a/g supports 64QAM on the highest data rate of 54Mp/s and requires a much wider bandwidth of 20MHz to accurately capture the signal. Radar signals are often specified in terms of their rise time rather than bandwidth.

Typically the parameter 'bandwidth' can be used to describe small or large signal behaviour, however many of these signals slew over a fairly large dynamic range, so a rise time specification is also required. This drives the requirements for the design of the signal amplifiers, as the amplifiers have to slew over several volts for the measurement of the signal.

The new power meter and sensor combination has a large signal bandwidth of 20MHz and a rise time of 18ns.

Sensor design

A new sensor was developed to meet the specification. The diode sensor has two main modes of operation. Below approximately –30dBm, the diode is operating below its 'knee' on the i/v graph and is acting as a square law detector which will measure the RMS power of any input signal. Above –30dBm the diode is operating above the knee and the diode is behaving as an envelope detector. The diode's impedance is lower and the response time is much faster than in the square law region. All of the modulated measurements use the envelope detection region of the diode sensor. The sensor also incorporates a fet switch, a 'chopper' which allows the diode to operate as a RMS, square law detector down to –60dBm.

The bandwidth of the sensor is controlled by two main factors.

- The impedance of the diode at the operating conditions

- The filter capacitor on the substrate used for smoothing the rectified output.

The diode response time can be altered by changing the loading resistance. This also alters the sensitivity so a trade off is made between these two parameters.

The capacitor is normally chosen so that a smooth DC output is available at the lowest frequency of use. In this particular case, the sensor was designed to have a full bandwidth of 20MHz. Sensors are calibrated to a traceable reference of 50MHz and an extra switchable 5MHz low pass filter is used for calibration.

Amplifier Design.

The amplifier has to combine good DC performance, stability and drift, high slew rate and bandwidth.

The amplifiers are made from commercially available designs.

High slew rate wide bandwidth amplifiers are commercially available, but the offset and drift tends to be poor compared with instrumentation standards, similarly instrumentation amplifiers with good drift and zero characteristics tend to have low slew rates. A composite amplifier design was produced to combine the best characteristics of both amplifiers.

The incoming signal from the sensor is split at the input into two components for amplification. The dc and low frequency component of the signal is amplified by a low drift DC amplifier, and the high frequency component is amplified by a high slew rate amplifier. The signals are then recombined and sampled by a 64Ms/s A/D converter. Three ranges are used to cover the dynamic range for modulated measurements, to give sufficient overlap for high crest factor signals such as CDMA.

Sampling Rates.
There are two basic sampling schemes that can be used to sample signals and which have been used in power meter designs.

Under-sampling.

Many power meters sample at well below the Nyquist rate of the input signal. A typical wide bandwidth power meter may sample at 1-2Ms/s and rely on the repetitive nature of the input waveform and dithering of the sampling signal to build up a picture of the waveform, or to collate enough information on the input signal. The advantage of this approach is that it eases some of the design constraints on the signal processing hardware. The considerable disadvantage is that the waveform is an amalgam from many successive samples, preventing an accurate glimpse of a real signal picture from being formed.
For example, a 1Ms/s power meter is trying to measure a radar pulse of 500ns width. The power meter can only take 1 sample per pulse and so will require about 30 pulses to build up a picture of the pulse. For a WCDMA signal, the trace displayed will be a stitched together amalgam of different samples taken from the continuously varying waveform. They will not show the actual power level variation of the WCDMA signal.

Over-sampling.

The alternative is to pick a sampling frequency well above the Nyquist rate of just above 2 times the input frequency. The A/D converter chosen for this application samples at 64Ms/s, over three times the input bandwidth.

This has the disadvantage of putting extra burden on the data acquisition but has the considerable advantage of being able to depict the actual changes taking place in the signal. To use the two examples mentioned previously, the radar signal could be captured and measured in a single shot, so that a greater degree of consistency in the measurement conditions has been achieved. For the WCDMA designer, an over-sampling power meter gives the opportunity to look at the actual power envelope variations.

Signal Processing

The Anritsu ML2480A is capable of having two display channels making measurements. Each display channel can be set up for different measurement conditions, so the signal processing has been designed to capture two sets of measurements alternately.

The power meter also supports two sensor inputs. Each sensor input has its own signal amplifier and A/D converter so that simultaneous sampling on both inputs produces a true high speed ratio measurement.

The signal processing is split into 2 stages. The raw data from the A/D converter is captured automatically under control of an FPGA and placed in a trace buffer. The DSP then reads this data and calculates the linearity correction for each sample. Each sample is corrected before averaging. The A/D converter runs at 64Ms/s. Each display channel has been allocated a trace buffer size of 256K. The trace buffer is implemented as a circular buffer which enables the power meter to display pre-trigger data if required. When a trigger event occurs this puts a flag on the position in the trace buffer which can then be used to calculate the pre-trigger time specified by the user before the trigger event occurred.

The user can select whether to have 200 or 400 display points, so in the worst case, a full buffer of 256K readings needs to be compressed down to display 200 ordinates. It is essential that the salient points of the signal are correctly passed over so that the display values of average and peak power are correct for the data acquired over the full capture time.

WCDMA

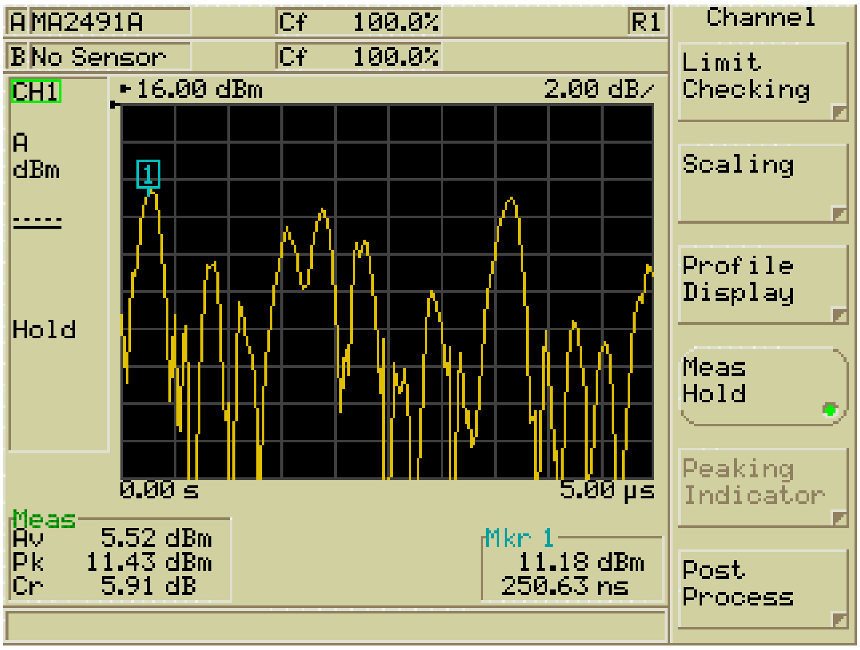

Figure 1.
Power Envelope of a WCDMA transmission

Figure 1shows a 5µs segment of a 3G WCDMA transmission. The readout box on the lower left hand side of the display shows the average power, the peak power and the crest factor measured over the 5µs. The power varies rapidly in amplitude. In this particular example, there is no compression of the signal data required, the display is showing the complete variation of the input signal.

Typically a WCDMA measurement would be made over a longer capture time than 5µs and so the information needs to be compressed into the display ordinates without sacrificing the accuracy of the average power and peak power.

To see how this is done, lets take as an example a 1ms burst of WCDMA with 200 display points set on the power meter. Under these conditions each display point encompasses 5µs worth of data, such as captured and displayed above. For each of the 5µs sections of data, three values are passed over for each display ordinate; the maximum value, the minimum value and the average value.

The average value is normally used to plot the variation in time on the graph, so that the display shows the variation in the average power of the WCDMA signal over time. The calculated average value on the display box is using all 200 of the average powers passed over. The peak value has been found from the 200 maximum values passed over from the DSP, so that the peak value and crest factor can always be correctly calculated.

The user can choose to display the variation of the maximum power of the signal instead of the variation in the average. The average value will still remain calculated correctly in the display box. The example above shows the results plotted in graphical form, but the user can also select just to display the average, peak and crest results as a numerical output without the graph.

RADAR

Radar provides a different challenge. Here the function of the peak power measurement is to measure the average power in the pulse within precisely defined limits. Two additional measurement tools are required for this measurement.

1. Gates that can be used to select a precise section of the waveform for the calculation of the average power

2. A signal trigger that can be used to trigger the measurement and used as a time reference for the display and gate.

The application of a measurement gate is key to radar pulse measurements. The gates are implemented within the DSP software and can used to delineate the power readings that fall within their boundaries. The timing of the gate is set from the trigger point.

Within the gate the max, min and average powers are calculated and passed to the gate display box. Up to 4 gates with independent timings from the trigger event can be set to measure a sequence of pulses.

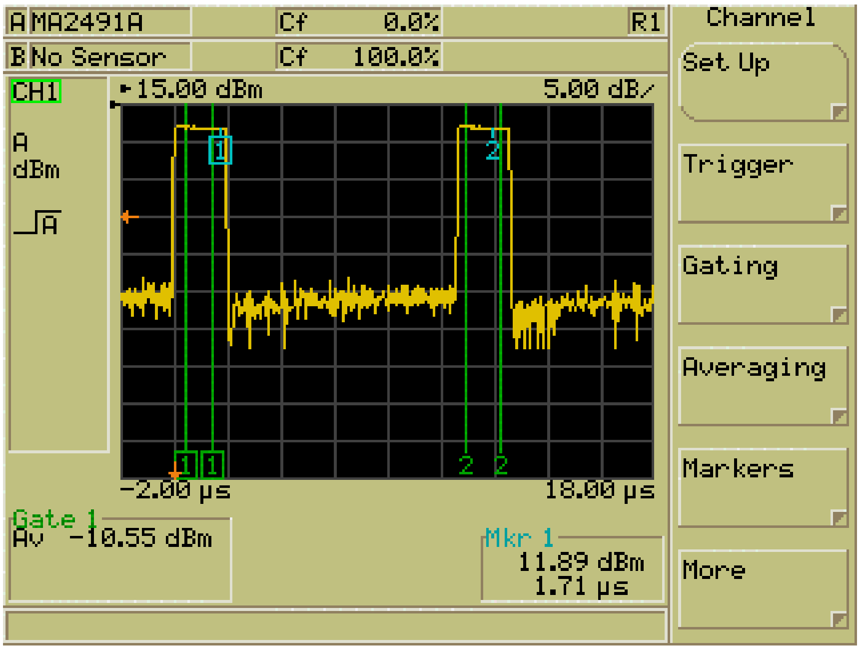

Figure 2: A pair of pulses

A key aspect to the performance is the repeatability and latency of the trigger. The data acquisition runs continuously in a circular buffer. The trigger event is used to tag the data in the buffer so that the latency is no more than +/- 1 clock cycle of the A/D converter, i.e. about 16ns.

Many of the principles used in the Radar pulse measurement are also applicable to GSM signals.

WLAN

WLAN combines the pulsed profile of the radar signal with the rapid variation of the CDMA power envelope. OFDM WLAN can support up to 64 carriers each with 64QAM modulation. There are two sections of the signal where the power can be measured.

These are the training sequence which lasts for 16µs at the start of the signal, and the data payload. The training sequence can be used to characterise the power control loop in the WLAN transmitter.

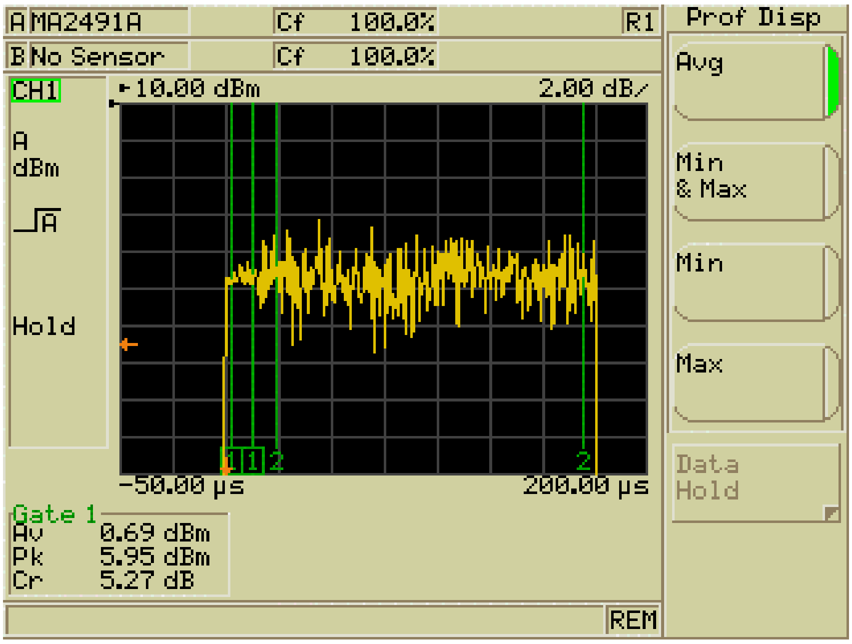

Figure 3. 802.11a Burst with 2 gates applied

Figure 3 shows the measurement of an 802.11a signal. 2 gates have been set up, Gate 1 to capture the training sequence at the start of the pulse and Gate 2 to measure the power during the data payload. It can be seen that the training sequence is relatively flat compared with the data payload.

In fact examining the power envelope of 802.11a with 64QAM shows that the variation of power during the payload is more extreme than WCDMA (see figure 4). The correct design of WLAN power amplifiers depends upon being able to accurately characterise the payload envelope, with 20MHz bandwidth, there is no need to manually correct the peak reading as required by lower bandwidth power meters.

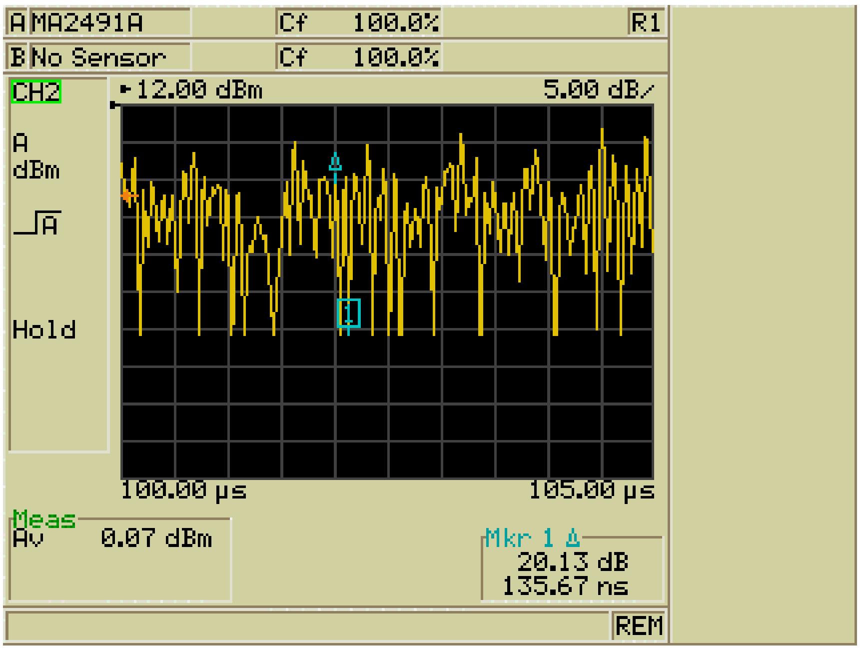

Figure 4. A view of 5µs of the data payload in a 802.11a,OFDM, 64QAM, 54Mb/s signal

Conclusion
This paper has described how the new Anritsu high speed power meter operates and shows how the techniques employed in the design can be used to measure a variety of high speed signals such as WCDMA, WLAN and Radar. The over-sampling architecture offers the user to track actual changes in the power envelope rather than relying on an amalgam of samples built up over successive traces.

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