APPLICATION NOTE

Circulating Loop Measurements

MP1763C/MP1764C

Pulse Pattern Generator/Error Detector

MEASUREMENT GROUP
ANRITSU CORPORATION

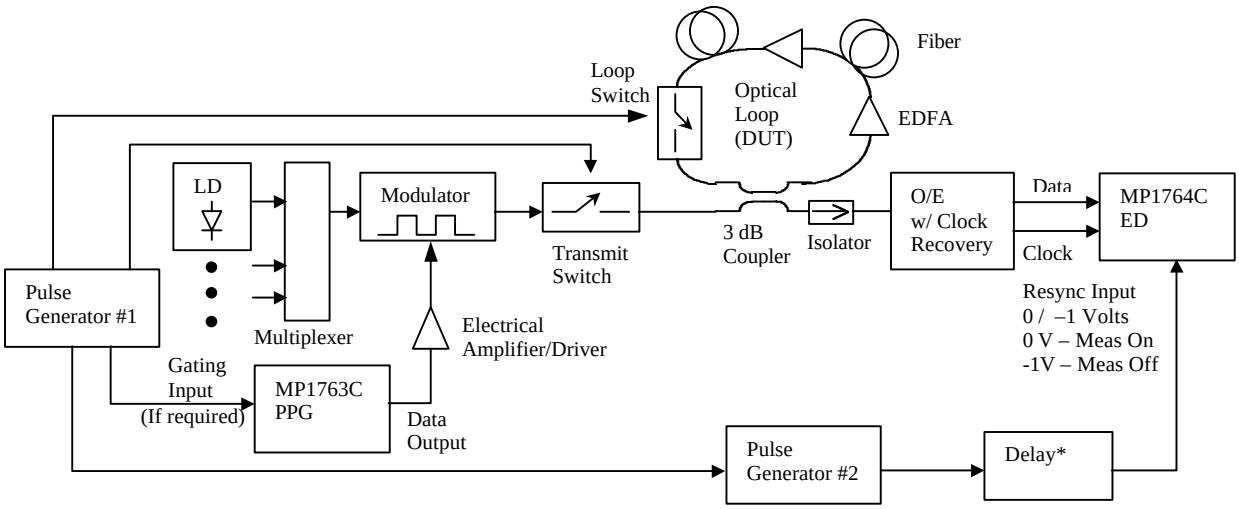
Using the MP1763C and MP1764C for Circulating Loop Measurements

The popularity of burst (pulse) data measurements utilizing high speed Bit Error Rate Testers (BERTS) has increased in recent years with engineers who are designing Gigabit telecommunication systems. Circulating Loop test setups, which compactly simulate long-haul fiber transmission systems, require BERTS that transmit and receive burst data streams.

The Anritsu MP1763C 12.5 Gigabit Pulse Pattern Generator (PPG) and MP1764C 12.5 Gigabit Error Detector (ED) are well suited for the demanding requirements of burst data measurements. This note describes how the MP1763/64 12.5 Gigabit BERT system is used in Circulating Loop experiments.

Circulating Loop Testing

Circulating Loop (also called Optical Loop) testing has been performed since the late 1970's [1]. Initially the Optical Loop tests were used to characterize pulse propagation in early MM and SM fiber systems. A recent renewed interest in Circulating Loop testing has been fueled by R&D of OC-192/STM-64 rate (9.95328 Gb/s) transmission systems, dispersion compensating systems Soliton transmission systems, EDFA based systems, and WDM systems. Optical Loop configurations allow designers to simulate long haul optical transmission system with just a fraction of the overall system hardware (fiber, optical amplifiers, filters, etc.). The designer benefits from reduced setup size, complexity, and cost. For example, an entire transpacific 10,000 km system can be simulated in a lab using an Optical Loop setup consisting of only 400 km of fiber and 8 optical amplifiers. By looping through the Optical Loop 25 times the behavior of the full system can be evaluated. Circulating Loop experiments yield valuable information on the full system BER, eye diagram shape, dispersion, Signal-to-Noise ratio, and interchannel interaction of a WDM system. A typical Circulating Loop test configuration is given in Figure 1.



*A separate Delay circuit is not required if Pulse Generator #2 has a "Trigger Delay" feature.

Figure 1: Circulating Loop Setup

Description of Circulating Loop Setup

A simplified description of the operation of a Circulating Loop setup follows.

The Pulse Pattern Generator (PPG)/modulator generates an optical gigabit data stream. Closing the Transmit Switch loads the data stream into the optical loop (via the 3 dB coupler). After the loop fills with data (the Loop Time), the Transmit Switch opens and the Loop Switch closes. The loaded bit stream then recirculates around the loop. Each time around the loop the data passes through the coupler. The coupler directs a portion of the data to the O/E where the Error Detector (ED) monitors the BER of the bit stream. A delay circuit sets the distance range monitored by the ED. For clarification, a representative example is given below.

A Circulating Loop is used to simulate an OC-192/STM-64 (9.95328 Gb/s) 10,000 km system. The Loop consists of a DUT containing 8 EDFA's separated by 50 km of fiber (total loop length = 400 km). The Loop Time, which is related to Loop Length by: Loop Time = Loop Length/Velocity of Light in Fiber, is 2 ms (400 km ÷ 2E5 km/s). The Loop Gain is adjusted to unity. The data must loop 25 times to simulate 10,000 km. The total elapsed time for 25 loops is 50 ms. The duty cycle of the data burst is 4% (2ms/50ms). Figure 2 shows the timing diagram for this example. To monitor the data quality at 6000 km the Delay circuit is set for 30 ms (Loop 15).

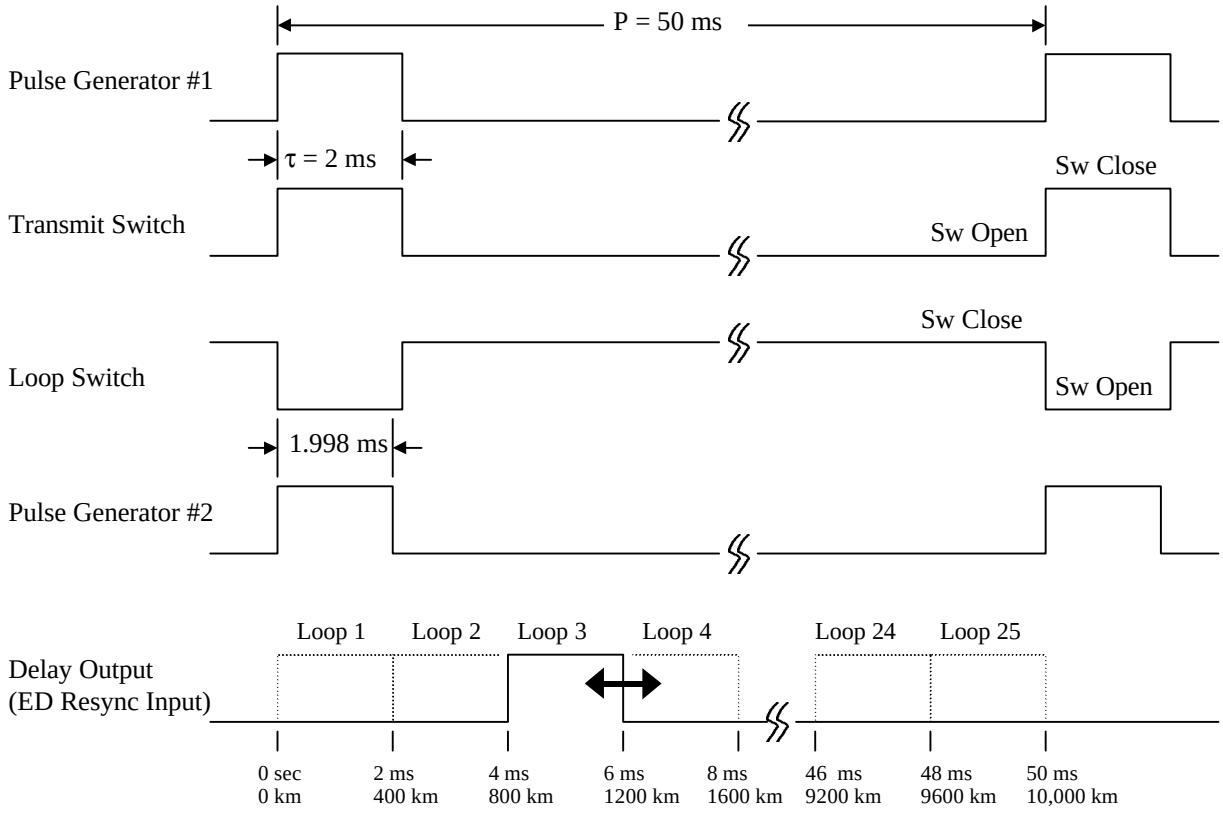


Figure 2: Example Circulating Loop Timing Diagram

Circulating Loop Components

Optical Loop: The Optical Loop consists of a representative portion of the overall transmission system. Typically, the DUT contains spans of fiber separated by optical amplifiers/isolators/filters. The minimum length of the loop (minimum loop time) is constrained by the sync time of the Error Detector. A sync time of approximately 1 us is typical for a 10 Gb/s rate. The maximum length of the loop is limited only by the user's resources. Generally, due to cost and part availability constraints, the user will opt for a loop setup which minimizes part count and fiber lengths while still representing of the overall transmission system.

The gain of the DUT loop is adjusted to equal 1. This allows the data to recirculate without loss.

Pulse Generator #1: Provides synchronizing signals to the Loop Switch, Transmit Switch, PPG, and Pulse Generator #2. The pulse width of PG #1, τ, is derived from the Loop Time. The period, P, is dependent on the maximum simulated distance.

Pulse Generator #2: This Pulse Generator is slaved to Pulse Generator #1. The pulse width setting of this unit is slightly less than τ to account for trailing edge switching transients. The trailing edge transient time is related to the fall time of the Transmit Switch. It is recommended that the PW of Pulse Generator #2 be 2 us less than τ.

Pulse Generator #2 can act as a delay circuit if equipped with an "External Trigger Delay" feature. Adjust the Trigger Delay to monitor the appropriate Loop interval on the Error Detector.

Transmit Switch/Loop Switch: These switches must have low insertion loss, low polarization dependency, high extinction ratio, and small rise/fall times to minimize transients. The repetition rate of the switch is a function of the loop time. Typical repetition rates are in the kHz range.

O/E with Clock Recovery: This circuit converts the Optical Loop output signal to electrical DATA and CLOCK signals suitable for input into the Error Detector. The voltage levels into the Error Detector should be in the range 0.25 to 2.0 Vp-p (this is guaranteed input range; ED typically work properly for input levels down to 50 mVp-p).

Pulse Pattern Generator: The PPG provides the gigabit bit pattern that drives the optical modulator. The PPG data output must produce a high quality eye diagram, i.e. fast rise/fall times, low distortion, low jitter, and high Q factor[2] (minimal noise on the eye "rails"). The Anritsu MP1763C has a tr/tf of less than 30 ps, less than 10% distortion, less than 20 ps p-p of crossover jitter, and a Q factor of >40dB.

It may be necessary to pulse the PPG when the extinction ratio of the Transmit Switch is not adequate. The MP1763C can be pulsed by connecting it's GATING INPUT to the output of Pulse Generator #1. The voltage levels specified for the GATING INPUT are 0/-1(almost same with SCFL level). 0 volts corresponds to data on.

Error Detector: The ED must be able to synchronize quickly on incoming burst data. An Error Detector cannot make valid error measurements until synchronization is achieved. Circulating Loop tests are not possible if the sync time approaches or exceeds the duration of the burst data. The Anritsu MP1764C has very fast synchronization times for both standard PRBS patterns and user defined patterns (DATA). To achieve fast sync times for DATA the MP1764C has a unique

mode called Quick Sync[3]. When Quick Sync is activated the ED stores the first N bits it receives from the DUT (where N is the user specified pattern length). These N bits become the reference pattern and are compared with the following N bits that are input into the Error Detector. This technique results in synchronization times on the order of 1 us. The following equations give the sync time for the MP1764C.

PRBS Sync Time = 4096/f + 0.4us

Quick Sync Time = 4 x N/f

where:

f is the data rate in bits/sec
N is the DATA pattern length

Typical values for synchronization times are given in Table 1.

Bit Rate	PRBS Sync Time	Quick Sync Time*
622 Mb/s	7.0 us	6.4 us
2.5 Gb/s	2.0 us	1.6 us
10 Gb/s	0.8 us	0.4 us

*assumes a DATA pattern length of 1024 bits

Table 1: Synchronization Times for MP1764C Error Detector

The MP1764C does not require a continuous "local" clock signal during burst measurements-only the burst clock recovered by the O/E is necessary.

LD, Multiplexer, Modulator, and Electrical Amplifier: The LD is typically a DFB operating in the 1310 nm or 1550 nm window. Multiple 1550 nm band DFB sources can be used in conjunction with a multiplexer to simulate WDM channels. Each DFB is modulated either directly or externally with a Lithium Niobate or EO modulator. An external electrical amplifier/driver is then required when the maximum PPG output of 2V p-p is not sufficient to drive the modulator. Anritsu offers a complete line of Wideband Amplifiers and High Speed Drivers that boost the PPG output with minimal distortion (see the Anritsu High Speed Devices Catalog). One recommended Anritsu Driver is the A7HC2107.

MP1763C/MP1764C Setup for Circulating Loop Measurements

The MP1763C is configured as follows:

- The desired bit rate is set by adjusting the clock rate of the Internal Clock (Option 01) or external synthesizer.
- The test pattern is set to PRBS or DATA (a user defined pattern). If DATA is selected, input the user pattern via front panel manual input, GPIB interface, or floppy disk. Manual front panel input of the pattern is feasible for pattern lengths less than approx. 1000 bits. For longer patterns a GPIB or floppy disk transfer is recommended. The MX176401A application software facilitates the programming and transfer of long DATA patterns. Alternately, the MP1763/64 File Conversion Software allows the user to store and transfer a DATA pattern using a floppy disk.

- The amplitude of the data output is adjustable in the range 0.25 to 2.0 Vp-p. A DC offset is also selectable.
- If the user wishes to pulse the PPG data output, Pulse Generator #1 is connected to the GATING INPUT on the rear panel. The GATING INPUT uses 0/-1 Volt Logic, where a 0 level is Data On and –1 is Data Off . This input has a 50 ohm SMA connector.

The MP1764C is configured as follows:
- Burst Mode is activated by setting rear panel Function 1 switch #5 to "1" (On). An LED labeled "BURST MODE" on the lower right portion of the front panel will illuminate.
- The output of the DELAY circuit is connected to the RESYNC INPUT on the rear panel. The RESYNC INPUT uses 0/-1 Volt Logic, where a 0 level is Measurement On and –1 is Measurement Off. This input has a 50 ohm SMA connector.
- Set the test pattern to PRBS or DATA. For PRBS patterns, select the same pattern that is chosen on the PPG, i.e. 2^{15} –1, 2^{23} –1, etc. For DATA patterns select QUICK under SYNC MODE. Enter the length of the DATA pattern.
-Select the desired timed measurement mode: REPEAT, SINGLE, or UNTIMED. Select START. REPEAT and AUTO SYNC on is recommended.
- Adjust the Threshold and Delay Time values manually to locate the "center of the eye". Note: the AUTO SEARCH function does not work properly with burst data.
- Verify that the input data into the MP1764A is greater than 50 mV p-p (minimum sensitivity)

Helpful Tips

- Verify the test setup by connecting the MP1763C directly to the MP1764C (bypass the Optical Loop and set Delay for 0 sec). Confirm the MP1764C is operating error free before inserting the Loop. If errors are present decrease the PW of Pulse Generator #2.
- The MP1763C Clock and Trigger outputs are continuous when the GATING INPUT is used. Only the DATA output is turned on/off. The MP1764C outputs a trigger signal only when a clock signal is input. If the clock is a burst signal, the Trigger output is only active during the clock ON portion of the burst period.
- AUTO SEARCH, EYE MARGIN, and ERROR ANALYSIS do not function in Burst Mode. BLOCK WINDOW and BIT WINDOW operate in Burst Mode.
- The Stretched and Direct Error Outputs are available in Burst Mode
- Burst Switch "ON" disables the Sync Loss and Clock Loss alarms. If desired, the Burst Switch can be left ON when measuring continuous (non-burst) data. Conditions that normally produce a Sync Loss or Clock Loss alarm will instead generate a large numbers of errors.

[1]For a additional information on Circulating Loop Experiments refer to:
Bergano, N. S, C. R. Davidson, Circulating Loop Experiments for the Study of Long-Haul Transmission Systems Using Erbium-Doped Fiber Amplifiers, Journal of Lightwave Technology, Vol. 13, No. 5, May 1995

[2] For further discussion on Q factor (Quality Factor) refer to:
Bergano, N. S., F. W. Kerfoot, and C. R. Davidson, Margin Measurements in Optical Amplifier Systems, IEEE Photonics Technology Letters, Vol. 5, No 3, March 1993.

[3] For more information on Quick Sync refer to:
Anritsu MP1764C 12.5 GHz Error Detector Synchronization Modes, Technical Note No. 075 G, Nov 1995.

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Specifications are subject to change without notice.

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