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Anritsu

MX368034A

PDC PACKET Software

(For MG3681A Digital Modulation Signal Generator)



For receiver testing of PDC packet system

Outputs signals for RCR STD-27 standard PDC packet system receiver tests

The MX368034A PDC packet software is installed in the MU368030A Universal Modulation Unit, when the MU368030A is housed in the MG3681A Digital Modulation Signal Generator. It can output RCA STD-27 standard PDC user packet channel (UPCH).

Simple operation and signal pattern change

Signals for receiver tests of UPCH communication base station and mobile station specified by RCR STD-27 can be outputted by selecting waveform data stored in a large capacity PC memory card, without setting complicated parameters.

Downlink 3 data rate UPCH patterns and Uplink 1 UPCH pattern can be changed.

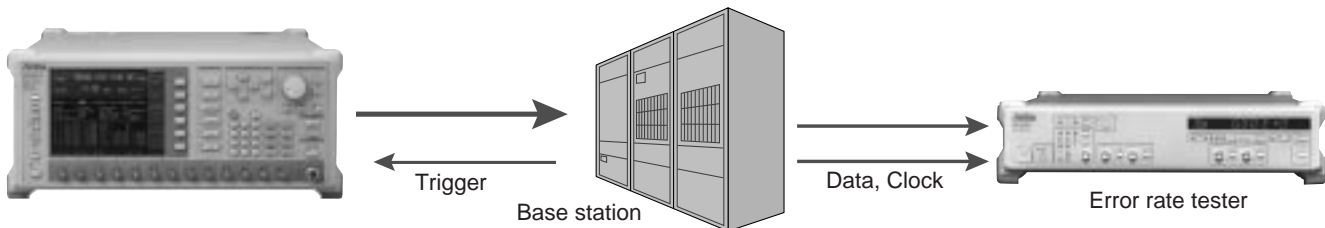


Signal pattern selection

Base station test

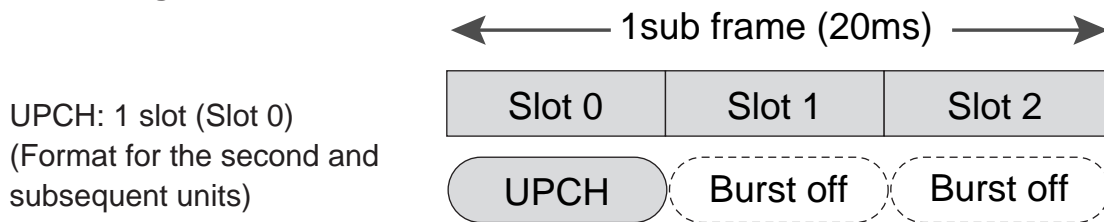
UPCH communication receiver tests (BER: Bit Error Rate) can be performed by selecting a Uplink UPCH pattern required for testing the base station (BS).

Receiver test



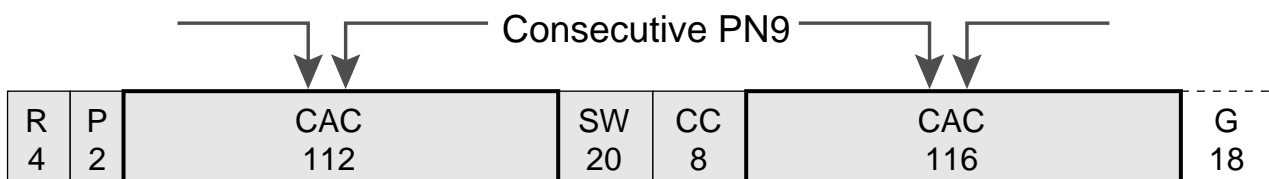
Trigger: Timing for synchronizing sub frames (frame trigger)

Uplink frame configuration



The first unit of UPCH does not output. Does not support super frame (SW is always the same for any frames).

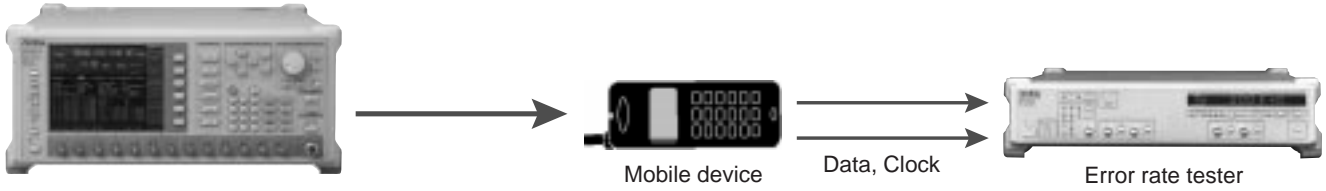
Slot configuration of physical channels for Uplink packet communication (UPCH, the second and subsequent unit)



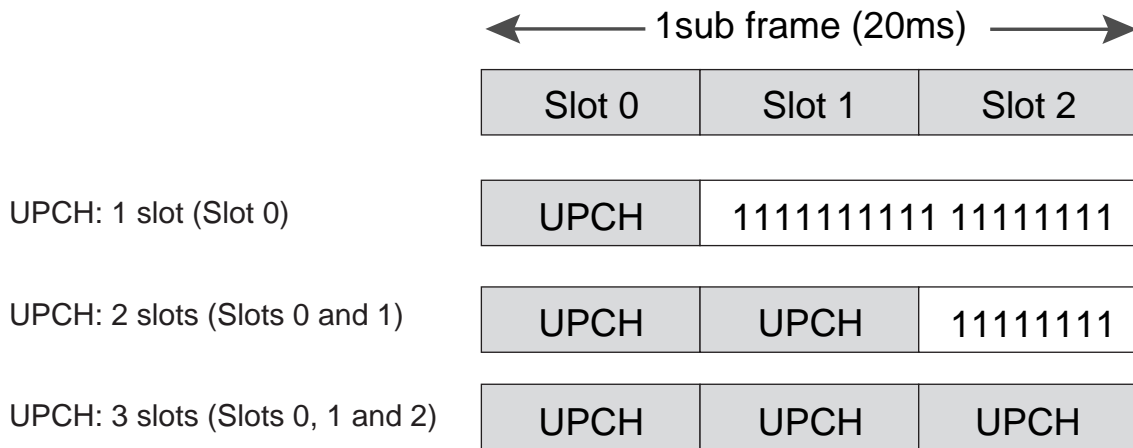
Mobile station test

UPCH communication receiver tests (BER: Bit Error Rate) can be performed by selecting a downlink UPCH pattern required for testing the mobile station.

Receiver test

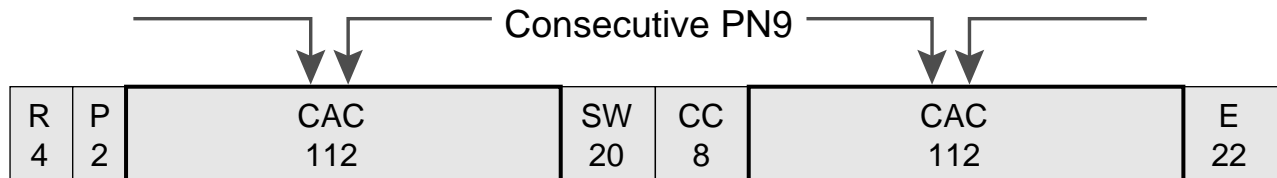


Downlink frame configuration



Does not support super frame (SW is always the same for any frames).

Slot configuration of physical channels for Downlink packet communication (UPCH)



Specifications

MX368034A PDC PACKET software

Supported systems/Modulation method	RCR STD-27 (PDC), $\pi/4$ DQPSK, UPCH format	
Baseband filter	Root Nyquist, Roll-off factor $\alpha = 0.5$	
Modulation data	DOWNLINK1	Slot 0 only: UPCH, Slots 1 and 2: All 1 UPCH: PN9 data allocated to adjacent CAC area, SW does not support super frame.
	DOWNLINK2	Slots 0 and 1 only: UPCH, Slot 2: All 1 UPCH: PN9 data allocated to adjacent CAC area, SW does not support super frame.
	DOWNLINK3	All slots (slot 0 to 2): UPCH UPCH: PN9 data allocated to adjacent CAC area, SW does not support super frame.
	UPLINK1	Slot 0 only: UPCH, Slots 1 and 2: Burst off UPCH: Format for the second and subsequent units, PN9 data allocated to adjacent CAC area, SW does not support super frame.
RF signal	Frequency range	10 to 3,000 MHz
	Output level	-143 to +13 dBm
	Level accuracy	Within ± 1.0 dB ($\leq +5$ dBm) compared with CW output level [At modulation data DOWNLINK1- 3]
	Vector error	≤ 1.8 % (rms)
	Adjacent channel leakage power	At output of +5 dBm, PLL mode: Normal, 100 to 1,600 MHz, RBW: 1 kHz, VBW: 3 kHz ≤ -63 dBc (50 kHz offset, BW: 21 kHz), -67 dBc (100 kHz offset, BW: 21 kHz) [At modulation data DOWNLINK3]
	Burst On/Off ratio	≥ 65 dB ($\leq +5$ dBm) [At modulation data UPLINK1]
I/Q signal	Output level	$\sqrt{I^2 + Q^2} = 359$ mV (rms)
Transmit speed	Symbol rate	21 ksps
	Transmit speed accuracy	Depends on basic signal accuracy of MG3681 (except for the case of external synchronization).
Firmware backup space	CPU: 137.3 kbyte, FPGA: 49.5 kbyte (within MU368030A universal modulation unit)	

UPCH: User Packet Channel

Ordering Information

Please specify the model, name and quantity when ordering.

Model	Name
MG3681A*1	Main frame
	Digital Modulation Signal Generator
MU368030A*2	Expansion unit
	Universal Modulation Unit
MX368034A	Software
	PDC PACKET Software*3
	Standard accessories
W2073AE	MX368034A Operation Manual: 1 copy

*1: Refer to catalogue for MG3681A.

*2: Refer to catalogue MU368010A/MU368040A/MU368030A for MU368030A.

*3: Supplied with Compact Flash Card*3 (with adapter) or ATA flash memory card.

*4: CompactFlashTM is a trademark of SanDisk Corporation.



Specifications are subject to change without notice.

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