The MP1630B is a general-purpose bit error measuring instrument that can provide simultaneous measurements of multi-channel signals and burst signal measurements up to 200 MHz. The MP1630B is not only for continuous signals – it can measure burst-signal bit error rates as well. Consequently, it is easily able to handle burst signals used by TDMA (Time Domain Multiplex Access) methods and packet/cell transmissions, etc. Both a pulse pattern generator unit and an error detector unit can be installed in the MP1630B to measure simultaneously parallel data for 16 channels using just one unit.

**Features**
- 16 channel PPG and ED in one cabinet
- Eye diagram measurement based on BER

**Applications**
- Testing multi-channel modules for optical interconnection
- E/O, O/E evaluation for optical networks (PON/PDS)
- Testing SDH/ATM equipment and modules
- Testing cable modems for digital CATV
- R&D on TDMA
- R&D on wireless LAN peripherals
- Evaluating next-generation PC interfaces (fiber channel, IEEE 1394, SSA, ATM-25)
- Evaluating digital demodulators including QPSK/QAM, etc.
- Evaluating IrDA communications equipment
- Evaluating communications LSIs, ASICs/FPGAs, and CCDs, etc.

**Performance and functions**
- **Simultaneous bit error measurement of 16 channels**
  The MP1630B has 16-channel Pulse Pattern Generator and Error Detector units and can measure bit errors in parallel and simultaneously. Using the MP1630B shortens the time required to measure each device to 1/N, thereby greatly improving production efficiency.
- **For both continuous and burst data**
  Continuous data is used in the PDH/SDH transmission system; burst data is used in the PON (Passive Optical Network) subscriber TDMA transmission system, as well as in the burst cell unit ATM-PON transmission system. The MP1630B can handle bit error measurement of both continuous and burst data. It can output burst data for up to 16 channels, and the burst cycle, guard time, preamble length, and data length can all be varied.

**Mixed pattern generation, selective BER measurement**
With the MP1630B, a test pattern can be selected and set for each channel. Not only can both PRGM and PRBS patterns be used, but a mixed pattern composed of both PRGM and PRBS patterns can be generated, too. The packet type and cell type data can be configured smoothly from the overhead and payload parts. Moreover, the pattern field can split in two to 32 blocks, and a PRGM or PRBS pattern can be allocated to each column individually. As a result, it is possible to create pseudo-test signals for SDH/ATM, etc., as well as signals for evaluating complex communication protocols.

**Superior basic functions**
A high-performance frequency synthesizer is built into the MP1630B. It generates stable, accurate signals with high resolution in the 10 kHz to 200 MHz band. In addition, when the optional digital modulator function is used, the jitter tolerance of communications equipment and devices can also be measured.

In addition to TTL, LVTTL, ECL, and PECL, the pulse pattern generator clock and data output levels can be set to any output (0.25 to 2.5 V at 50 Ω termination; 0.5 to 5.0 V at high) for a variety of interfaces. The data and clock output delay can be varied at high resolution for each channel, and there is no need to adjust the cable length for each signal.

32 Block mixed pattern setting screen

NEW

**GPIB OPTION**
• Evaluating error correction function using burst error insertion
  In addition to having the earlier cyclic and single error-mode insertion functions, the MP1630B has burst-mode insertion functions, making it ideal for evaluating the efficiency of error-correction codes used by each type of communication protocol. In particular, it is especially effective for testing digital transmission methods used by broadcast satellites and mobile phones, etc.

• Evaluating data waveform quality using eye margin measurement
  The MP1630B eye margin measurement function can automatically measure the threshold voltage and phase range below the specified error rate. It has two measurement modes: the Margin mode and the Diagram mode. These modes can be selected according to the application.

• One-key/one-parameter operation using customized screens
  Measurement of general multi-channel data requires complex operations to manage the large number of measurement parameters. To make measurement settings simpler, the MP1630B has convenient customized screens based on the one-key/one-parameter operation used previously in the Anritsu BERTS. It also has a Grouping function which groups together the same measurement items used for each channel. Common settings (all or pattern-only) are saved as files on the large internal hard disk.

• Powerful pattern editor function
  The MP1630B pulse pattern generator and error detector PRGM patterns can be edited easily using the keyboard, mouse, or cursor keys. There are three editing modes matching the various applications: Time, State, and Dump. The Time mode puts time on the horizontal axis and displays the pattern for each channel as a horizontal line. The State mode displays the data of channel 1 as the MSB and parallel 16 bits (corrected 1 bit from each channel at a time) as one data item. The Dump mode displays the pattern for the specified channel as a memory dump image using either binary or hexadecimal code.
### Specifications

#### Clock

- **Internal**
  - Operating frequency: 10 kHz to 200 MHz (accuracy: ±2 ppm)
  - Resolution: 1 kHz steps (>1 to 200 MHz), 100 Hz steps (10 kHz to 1 MHz)

- **External**
  - Input frequency range: 10 kHz to 200 MHz
  - Input level: AC, 0.5 to 2.0 Vp-p (50 Ω), BNC connector
  - External (at locked)
  - Input frequency range: 10 MHz ±100 ppm, 64 kHz ±100 ppm
  - Input level: AC, 0.5 to 2.0 Vp-p (50 Ω), BNC connector

#### Jitter modulation function (option)

- **External modulation input**
  - Modulation frequency range: 10 Hz to 1.3 MHz
  - Input level range (sine wave): –1 to +1 V (75 Ω), BNC connector

- **Reference output (jitter-free output):** AC, 1 Vp-p (50 Ω), SMA

- **Jitter:** 0 to 50.5 UIp-p (clock frequency: >100 to 200 MHz) *Switchable to 50 UI/2 UI range

#### Test pattern (pulse pattern generator, error detector)

- **PRBS Pattern:** $2^n - 1$ (n: 7, 9, 11, 15, 20, 23, 31), variable mark ratio, logic selectable
- **Zero substitution pattern:** $2^n$ (n: 7, 9, 11, 15); pattern length: n to $2^n - 1$, logic selectable
- **PRGM pattern:** 2 to 65,536 bits/channel bit length, logic selectable
- **Mixed pattern:** Mixed PRGM and PRBS pattern, logic selectable

- **Block numbers:** 2 to 32 [PRGM bit length/block: 8 to 8,912 bits; PRBS bit length/block: 8 to 131,072 bits (depend on block numbers)]

- **PON pattern** [TDMA test patterns with preamble inserted in ahead of Mixed patterns (PRGM and PRBS)]

- **Preamble (1010...):** 0 to 64 bits; guard time: –2,097,083 to 2,097,067 bits (1 bit resolution)

- **Burst mode:** Internal (burst cycle: 0.1 to 10 ms), external (enable length: 8 to 2,097,144 bits)

- **Error insertion**
  - Each channel, simultaneous or independently
  - Error type: Normal, burst
  - Insert area: Entire area, selected blocks (in Mixed pattern or PON pattern)
  - Burst mode (internal/external)
  - Error rate: $10^{-n}$ (n: 2 to 9)
  - Internal enable length: 20 to 140 ms (resolution: 20 ms)
  - Internal cycle: 1 to 10 s (resolution: 1 s)

- **Output No.:** 16 (multipin connector), output on/off and logic selectable

- **Input No.:** 16, logic selectable, multipin connector

- **Measurement data**
  - Channel No.: 16 channels simultaneous measurement (selectable measurement channels)
  - Signal format: Continuous or burst (internal/external)

- **Bit error measurement**
  - Error detection: All, insertion, omission
  - Measurement region: All, PRGM, PRBS selectable, and each block selectable with block configuration

- **Display**
  - Error rate: $0 \times 10^{-16}$ to $1.0000 \times 10^5$
  - Error count: 0 to 9,999,999
  - Error interval: 0 to 9,999,999

- **Error free interval:** 0.0000 to 100.0000%

- **Error performance:** ITU-T Rec. G.821

- **Measurement mode:** Single, repeat, untimed (1 second to 99 days 23 hours 59 minutes 59 seconds)
  - Auto sync: ON/OFF switchable [threshold value: $1 \times 10^{-6}$ (n: 2 to 8)], with autosearch function

- **Alarm measurement**
  - Detected items: Power loss, clock loss, pattern sync loss (PRGM, PRBS)

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Continued on next page
**Digital Transmission Measuring Instruments**

**Frequency Measurement**
- Measurement range: 10 kHz to 200 MHz
- Effective digits: 6 digits
- Resolution: 100 Hz
- Accuracy: ± (1 count ±10 ppm)

**Eye Margin Measurement (based on BER)**
- Measures eye margin or eye diagram of specified data (1 channel)
- Eye margin: Displays threshold margin and phase margin as numeric values
- Eye diagram: Displays width of eye aperture as two-dimensional graph using bit-error measurement

**Delay Measurement**
- Mode: Single/repeat
- Unit: Time/bit numbers
- Range:
  - Time: 0 to 999 µs (1 µs steps), 1 to 999 ms (1 ms steps), 1 to 10 s (1 s steps)
  - Bits: 231 bits (max.)
- Time out: 0.5, 1, 2, 5, 10 s

**I/O Signal for Burst BER Measurement**
- **Pulse Pattern Generator**
  - External burst input
    - Level: TTL (H: Enable, L: Disable), BNC connector
  - Burst trigger output (index signal for each burst data)
    - Output No.: 16 (for each data output), bit delay function
  - Level: ECL, –2 V (50 Ω), multipin connector
  - Auxiliary output (PON system envelope, or AGC reset signal; usable as normal control signal)
    - Output No.: 8 (selectable channel), 1 (OR output for each channel), bit delay function, logic selectable
  - Level: ECL or TTL (≤100 Mb/s), multipin connector

**Error Detector**
- Burst trigger input
  - Input No.: 16 (for each data input)
  - Level: ECL, –2 V (50 Ω), multipin connector

**Other I/O Signals**
- Sync signal output (pulse pattern generator, error detector)
  - Sync source: 1/1 clock, 1/8 clock, PRGM pattern, PRBS pattern
  - Level: 0/–1 V (50 Ω), BNC connector
- External error input (pulse pattern generator)
  - Error mode: Normal, burst
  - Level: TTL, BNC connector
- Trigger output (pulse pattern generator)
  - Trigger source: Unique pattern index for delay measurement or pattern block index in MIX/PON pattern
  - Level: 0/–1 V (50 Ω), multipin connector
- Trigger input (error detector)
  - Trigger source: For delay measurement
  - Level: 0/–1 V (50 Ω), multipin connector

**System Environment**
- Platform: Microsoft Windows operating system version 3.1
- Display: Color LCD, touch screen, 640 x 480 dots, 256 colors
- Printer: Parallel port for printer, D-sub 25-pin connector
- Keyboard: 101 keys (English), PS2 mini-DIN 6-pin connector
- Mouse: Serial, PS2 mini-DIN 6-pin connector
- FDD: 2 mode (1.44 MB, 740 KB)
- HDD
  - C drive: >380 MB (for measurement data, patterns)
  - D drive: 30 MB (not released to user, interface: IDE)

**Remote Control**
- RS-232C (standard), GPIB (option): IEEE488.2, Ethernet (option): 10 Base-T

**Other Functions**
- Sound: When error or alarm detected, panel lock function, self check function

**EMC**
- EN55011: 1991, Group 1, Class A
- EN50082-1: 1992

**Safety**
- EN61010-1: 1993 (Installation Category II, Pollution Degree 3)

**Power**
- 100 to 120/200 to 240 Vac, 47.5 to 63 Hz, ≤1,000 VA

**Dimensions and Mass**
- 426 (W) x 221.5 (H) x 451 (D) mm, ≤29 kg

**Operating Temperature**
- 5˚ to 40˚C

The specifications are with the MU163000A (200M Clock Generator Unit), MU163020B (200M 16CH Pulse Pattern Generator Unit), and MU163040B (200M 16CH Error Detector Unit) installed in the MP1630B main frame.
Ordering information,
Please specify model/order number, name, and quantity when ordering.

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<th>Model/Order No.</th>
<th>Main frame</th>
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<td>Digital Data Analyzer</td>
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