SERIES 541XXA
NETWORK ANALYZER

MAINTENANCE MANUAL

Software Version: 2.08

Anritsu

490 JARVIS DRIVE ● MORGAN HILL, CA 95037-2809

P/N: 10410-00166
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WARRANTY

The ANRITSU product(s) listed on the title page is (are) warranted against defects in materials and workmanship for one year from the date of shipment.

ANRITSU's obligation covers repairing or replacing products which prove to be defective during the warranty period. Buyers shall prepay transportation charges for equipment returned to ANRITSU for warranty repairs. Obligation is limited to the original purchaser. ANRITSU is not liable for consequential damages.

LIMITATION OF WARRANTY

The foregoing warranty does not apply to ANRITSU connectors that have failed due to normal wear. Also, the warranty does not apply to defects resulting from improper or inadequate maintenance by the Buyer, unauthorized modification or misuse, or operation outside of the environmental specifications of the product. No other warranty is expressed or implied, and the remedies provided herein are the Buyer's sole and exclusive remedies.

TRADEMARK ACKNOWLEDGEMENTS

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NOTICE

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Chapter 1 General Service Information

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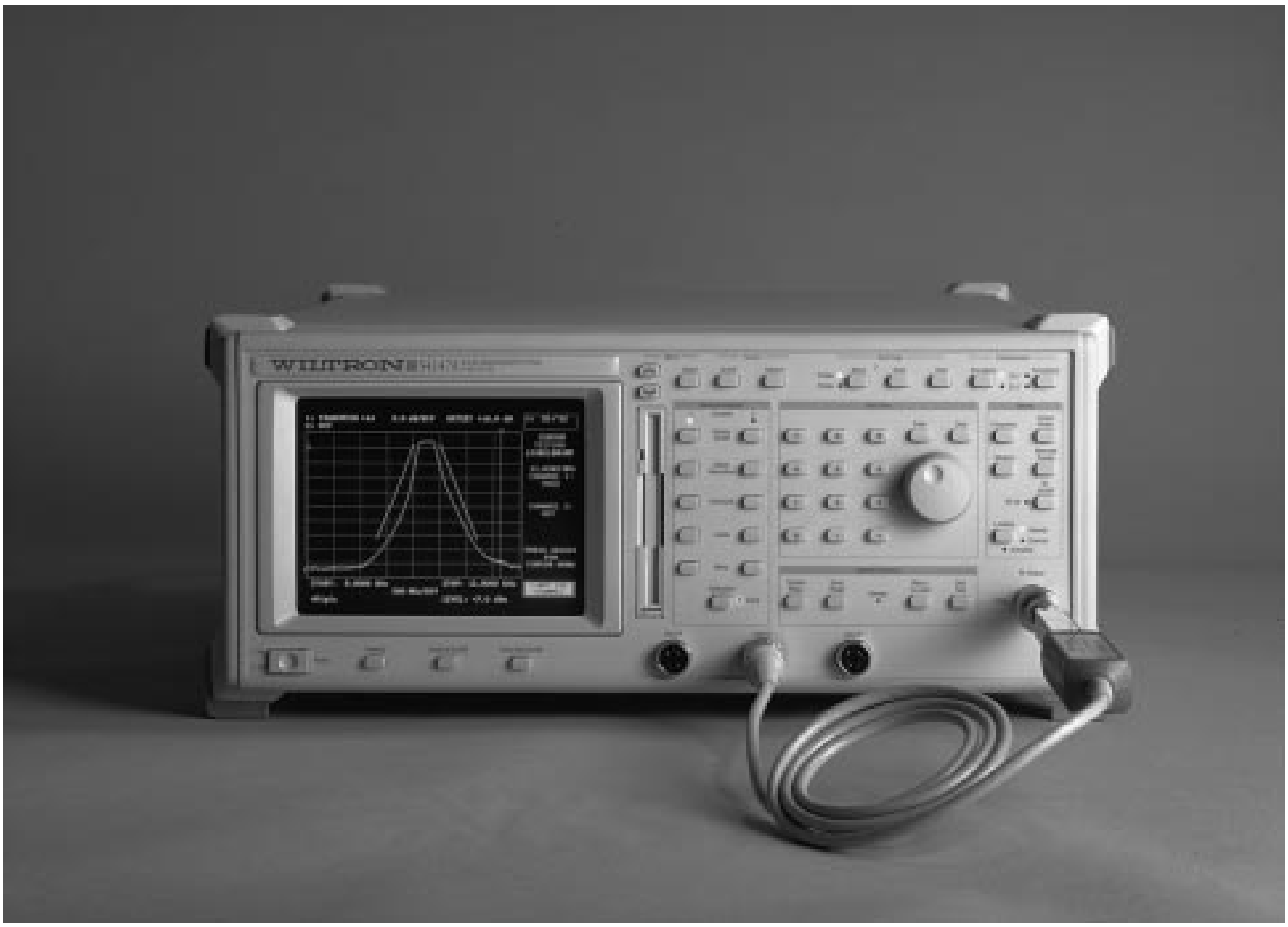


Figure 1-1. *Model 54147A Network Analyzer (Shown with 560-7 Series Detector Attached to Input A)*

NOTE: ANRITSU Company was formerly known as WILTRON Company.

Chapter 1
General Service Information

1-1 SCOPE OF THE MANUAL

This manual provides general service and preventative maintenance information, replaceable parts information, circuit descriptions, troubleshooting procedures, and adjustment procedures for ANRITSU Series 541XXA Network Analyzer. Throughout this manual, the system will be referred to as "541XXA."

1-2 INTRODUCTION

This chapter of the manual provides a general description of 541XXA, system serial numbers, frequency ranges, and related manuals. Also included is information about the level of maintenance covered in this manual, preventative maintenance procedures, and static-sensitive component handling precautions. A list of recommended test equipment is also provided.

1-3 IDENTIFICATION NUMBER

All ANRITSU instruments are assigned a six-digit ID number, such as "101001." This number appears on a decal affixed to the rear panel. Please use this identification number during any correspondence with ANRITSU Customer Service about this instrument.

1-4 DESCRIPTION OF 541XXA SYSTEM

Series 541XXA systems are microprocessor controlled network analyzers. They are used to make scalar (magnitude) transmission, reflection, distance-to-fault (DTF), and absolute power measurements. A typical model (54147A) is shown in Figure 1-1 (facing page).

All measurement functions are selectable by using the front panel keys and controls in conjunction with the display screen menus. Refer to the 541XXA Network Analyzer Operation Manual for information about operation of these systems. Refer also to that manual for information about system options, SWR Autotesters, detectors, and other accessories used with series 541XXA Systems.

Table 1-1. Frequency Ranges

Model	Frequency Range (GHz)		
54107A	0.001	to	1.5
54109A	0.001	to	2.2
54111A	0.001	to	3.0
54117A	0.01	to	8.6
54119A	2.0	to	8.6
54128A	8.0	to	12.4
54130A	12.4	to	20.0
54131A	10.0	to	16.0
54136A	17.0	to	26.5
54137A	2.0	to	20.0
54147A	0.01	to	20.0
54154A	2.0	to	32.0
54161A	0.01	to	32.0
54163A	2.0	to	40.0
54169A	0.01	to	40.0
54177A	0.01	to	50.0

The measurement frequency range of the 541XXA is determined by:

- The range of the internal signal source of the particular model.
- The external SWR Autotester and/or detector used with the 541XXA.

The table at left lists the frequency ranges of all 541XXA models. For information about the frequency ranges and characteristics of ANRITSU SWR Autotesters and RF detectors normally used with series 541XXA models, refer to the 541XXA Network Analyzer Operation Manual or to the technical data sheet in Appendix D.

The 541XXA provides remote operation using the IEEE–488 General Purpose Interface Bus (GPIB). This operation allows all 541XXA front panel control functions (except POWER on/off) to be controlled remotely from an external computer/controller using GPIB commands. Refer to the 541XXA Network Analyzer Operation Manual for information about other options and accessories available for 541XXA models.

1-5 LEVEL OF MAINTENANCE

Maintenance and troubleshooting of the 541XXA consists of:

- Troubleshooting the 541XXA to a replaceable subassembly
- Repair by replacing the failed subassembly
- Performance Verification
- Adjustments
- Preventive Maintenance

Troubleshooting and Repair

Most faults involving the 541XXA are field repairable by replacing a faulty subassembly. The procedures contained in this manual provide troubleshooting to this level. Refer to Chapter 3, Troubleshooting.

This manual also contains procedures for replacing defective detector diodes for Series 560-7XXX RF Detectors and for 5400-71B75 RF Detectors. These procedures are contained in Appendix A.

Replaceable Subassemblies and Parts

Chapter 2 provides replaceable parts information for all 541XXA models. It lists all field-replaceable subassemblies and parts. It also identifies all subasemblies that are presently covered by the ANRITSU exchange assembly program.

Performance Verification

Performance verification procedures that allow the 541XXA performance to be verified without removing covers are provided in Chapter 5. Use these procedures, in conjunction with the Adjustment in Chapter 6, to ensure that the 541XXA is operating at the peak of its performance curve.

Adjustments

Procedures for adjustment of the 541XXA after repair or replacement of one or more subassemblies is described in Chapter 6.

Preventive Maintenance

Fan filter replacement, described in paragraph 1-7.

1-6 RELATED MANUALS

The 541XXA Scalar Measurement Systems Operation Manual (10410-00141) describes the front panel operation for all 541XXA models. It also contains general information, specifications, and Performance Verification procedures for all models.

Operation of the 541XXA remotely via the IEEE-488 General Purpose Interface Bus (GPIB) is described in the 541XXA Series Network Analyzer GPIB User's Guide (10410-00147). This user's guide is located at the rear of the 541XXA Network Analyzer Operation Manual.

1-7 PREVENTIVE MAINTENANCE

The 541XXA must always receive adequate ventilation. Check and clean the rear panel fan filter periodically. Clean this filter more frequently in dusty environments. Proceed as follows:

Models with a removable filter:

Step 1 Remove the the fan grill.

Step 2 Remove the fan filter.

Step 3 Vacuum the filter to clean it.

Step 4 Replace the filter and fan grill by reversing the previous steps.

Step 5 Snap the fan grill securely.

Models with a fixed metal filter:

Step 1 Turn the instrument off.

Step 2 With a soft bristle brush remove excess dust from the metal filter.

1-8 STATIC SENSITIVE COMPONENT HANDLING PRECAUTIONS

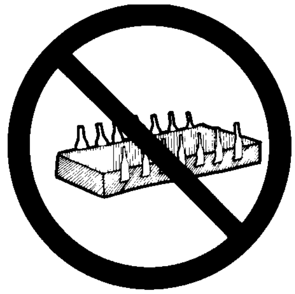
The 541XXA contains components that can be damaged by static electricity. Figure 1-2 illustrates the precautions that should be followed when handling static-sensitive subassemblies and components. If followed, these precautions will minimize the possibilities of static-shock damage to these items.

NOTE

Use of a grounded wrist strap when removing and/or replacing subassemblies or parts is strongly recommended.

1-9 RECOMMENDED TEST EQUIPMENT

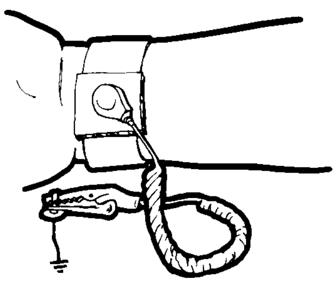
The recommended test equipment for the adjustment and troubleshooting procedures presented in this manual are listed in Table 1-2.

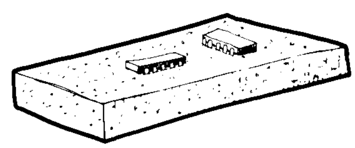


1. Do not touch exposed contacts on any static sensitive component.

2. Do not slide static sensitive component across any surface.

3. Do not handle static sensitive components in areas where the floor or work surface covering is capable of generating a static charge.

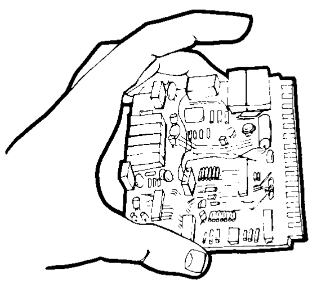


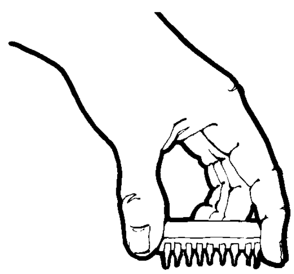


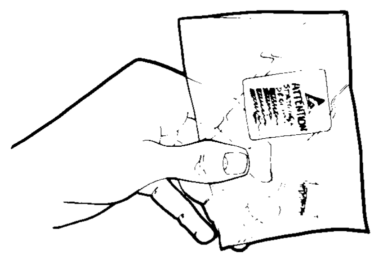
4. Wear a static-discharge wristband when working with static sensitive components.

5. Label all static sensitive devices.

6. Keep component leads shorted together whenever possible.







7. Handle PCBs only by their edges. Do not handle by the edge connectors.

8. Lift & handle solid state devices by their bodies – never by their leads.

9. Transport and store PCBs and other static sensitive devices in static-shielded containers.

10. ADDITIONAL PRECAUTIONS:

- Keep workspaces clean and free of any objects capable of holding or storing a static charge.
- Connect soldering tools to an earth ground.
- Use only special anti-static suction or wick-type desoldering tools.

Figure 1-2. *Static Sensitive Component Handling Procedures*

Table 1-2. *Recommended Test Equipment (1 of 2)*

INSTRUMENT	CRITICAL SPECIFICATION	RECOMMENDED MANUFACTURER/MODEL	USE#
Adaptor Cable	Connection to 541XXA Channel Inputs	ANRITSU Model 560-10BX	P, A
Detector Simulator	Simulates ANRITSU RF Detectors	ANRITSU T1492 (see Appendix B)	A
Computer/Controller	Personal computer, equipped with National PCIIA GPIB interface card	Any IBM compatible	P
RF Detector	1. 50Ω input, 1.0 to 3000 MHz* 2. 75Ω input, 1.0 to 3000 MHz** 3. 0.01 to 20 GHz 4. 0.01 to 40 GHz‡ 5. 0.01 to 50 GHz	ANRITSU Model 5400-71N50 ANRITSU Model 5400-71N75 ANRITSU Model 560-7N50B ANRITSU Model 560-7K50 ANRITSU Model 560-7VA50	P, A, T
Impedance Adapter	Converts from 50Ω to 75Ω	ANRITSU Model 12N75B	P, A, T
Digital Multimeter	Resolution: 4-1/2 digits (to 20V) *DC Accuracy:* 0.002% + 2 counts *DC Input Impedance:* 10 MΩ *AC Accuracy:* 0.07% +100 cts (≤20 kHz) AC Input Impedance: 1 MΩ	John Fluke Mfg Co. Inc., Model 8840A, with Option 8840A-09, True RMS AC	A, T
Frequency Counter	*Frequency:* 0.1 to 26.5 GHz *Input Impedance*: 50Ω	EIP Microwave, Inc., Model 578A	P, A
Modulation Meter	*Bandwidth:* 15 kHz Accuracy: ±3% of FSD at 1 kHz	Anritsu Corp., Model MS616B	P, A
Oscilloscope	*Bandwidth*: DC to 100 MHz *Sensitivity:* 2 mV *Horiz. Sensitivity:* 50 ns/division	Tekronics Inc. Model TAS485	A, T
Power Meter, with: Power Sensor* 50Ω input Power Sensor** 75Ω input Power Sensor Power Sensor# Atten, Calibration	*Power Range:* +10 to –55 dBm *Other:* 50 MHz Calibrated Output Frequency Range: 1.0 MHz to 2.0 GHz *Power Range:* –30 to +20 dBm Frequency Range: 1.0 MHz to 5.5 GHz *Power Range:* –30 to +20 dBm Frequency Range: 0.10 to 18.0 GHz *Power Range:* –30 to +20 dBm *Power Range:* –70 to –20 dBm Frequency Range: 0.05 to 26.5 GHz *Power Range:* –30 to +20 dBm *Power Range:* –70 to –20 dBm Atten: 30 dB, used with MA4702A/04A	Anritsu Corp., Model ML4803A Anritsu Corp., Model MA4601A Anritsu Corp., Model MA4603A with J0365 Conversion Connector Anritsu Corp., Model MA4701A Anritsu Corp., Model MA4702A Anritsu Corp., Model MA4703A Anritsu Corp., Model MA4704A Anritsu Corp., Model MP47A	P, T
Power Meter, with: Power Sensor## 50Ω input	*Power Range:* +10 to –55 dBm *Other:* 50 MHz Calibrated Output Frequency Range: 50 MHz to 50 GHz	Hewlett Packard 436A Hewlett Packard 8487A	P, A
Printer	Parallel Interface operation	Canon BJ10-SX, BJ30, or equivalent	P, T
Spectrum Analyzer	*Frequency Range:* 0.01 to 26.5 GHz *Power Range: +10 dB to –60 dBm*	Anritsu Corp., Model MS2802A	P, T
Step Attenuator	*Attenuation Range:* 60 dB, 10 dB/step 0.000 to 18.0 GHz 0.000 to 26.5 GHz	 Hewlett-Packard, Model 8495B Hewlett-Packard, Model 8495D	P, A

Table 1-2. Recommended Test Equipment (2 of 2)

INSTRUMENT	CRITICAL SPECIFICATION	RECOMMENDED MANUFACTURER/MODEL	USE#
Voltage Standard	Range: 0 mV to –1.462V Accuracy: 0.002% of set value.	John Fluke Mfg Co. Inc., Model 343A	P, A
Precision Adaptors ##.	V female to K male, V male to K female V male to N female K male to N female	ANRITSU 34VFK50 ANRITSU 34VKF50 ANRITSU 34RVNF50 ANRITSU 34RKNF50	P, A, T
∗ Required for models 54107A, 54109A, and 54111A with 50Ω output. ∗∗ Required for models 54107A, 54109A, and 54111A with 75Ω output, only. ‡ Required for model 54136A, and 54154A through 54169A only. ## Required for Model 54154A through 54177A		# Use Code: A Adjustment P Performance verification procedures T Troubleshooting	

Chapter 2
Replaceable Parts

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Chapter 2
Replaceable Parts

2-1 INTRODUCTION

This chapter provides replaceable parts information for all 541XXA models. The location of the major replaceable assemblies is shown in Figures 2-1 and 2-2 (pages 2-4 and 2-5).

2-2 EXCHANGE ASSEMBLY PROGRAM

ANRITSU maintains a module exchange program for selected subassemblies of all 541XXA models. If a malfunction occurs in one of these subassemblies, the defective item can be exchanged. Upon receiving your request, ANRITSU will ship the exchange subassembly to you, typically within 24 hours. You then have 45 days in which to return the defective item. All exchange subassemblies or RF assemblies are warranted for 90 days from the date of shipment, or for the balance of the original equipment warranty, whichever is longer.

Please have the exact model number and serial number of your unit available when requesting this service, as the information about your unit is filed according to the instrument's model and serial number. For more information about the program, contact your local sales representative or call ANRITSU Customer Service direct (paragraph 2-4).

2-3 REPLACEABLE SUBASSEMBLIES AND PARTS

Table 2-1 (page 2-6) lists the major replaceable subassemblies and parts for the 541XXA that are presently covered by the ANRITSU exchange assembly program. Table 2-2 (page 2-8) provides a listing of replaceable common parts.

2-4 PARTS ORDERING INFORMATION

All parts listed in Table 2-1 may be ordered from your local ANRITSU service center (Table 2-3, page 2-10). Or, they may be ordered directly from the factory at the address shown below.

ANRITSU Company
ATTN: Customer Service
490 Jarvis Drive
Morgan Hill, CA 95037-2809

Telephone: (408)-778-2000
FAX: (408)-778-0239

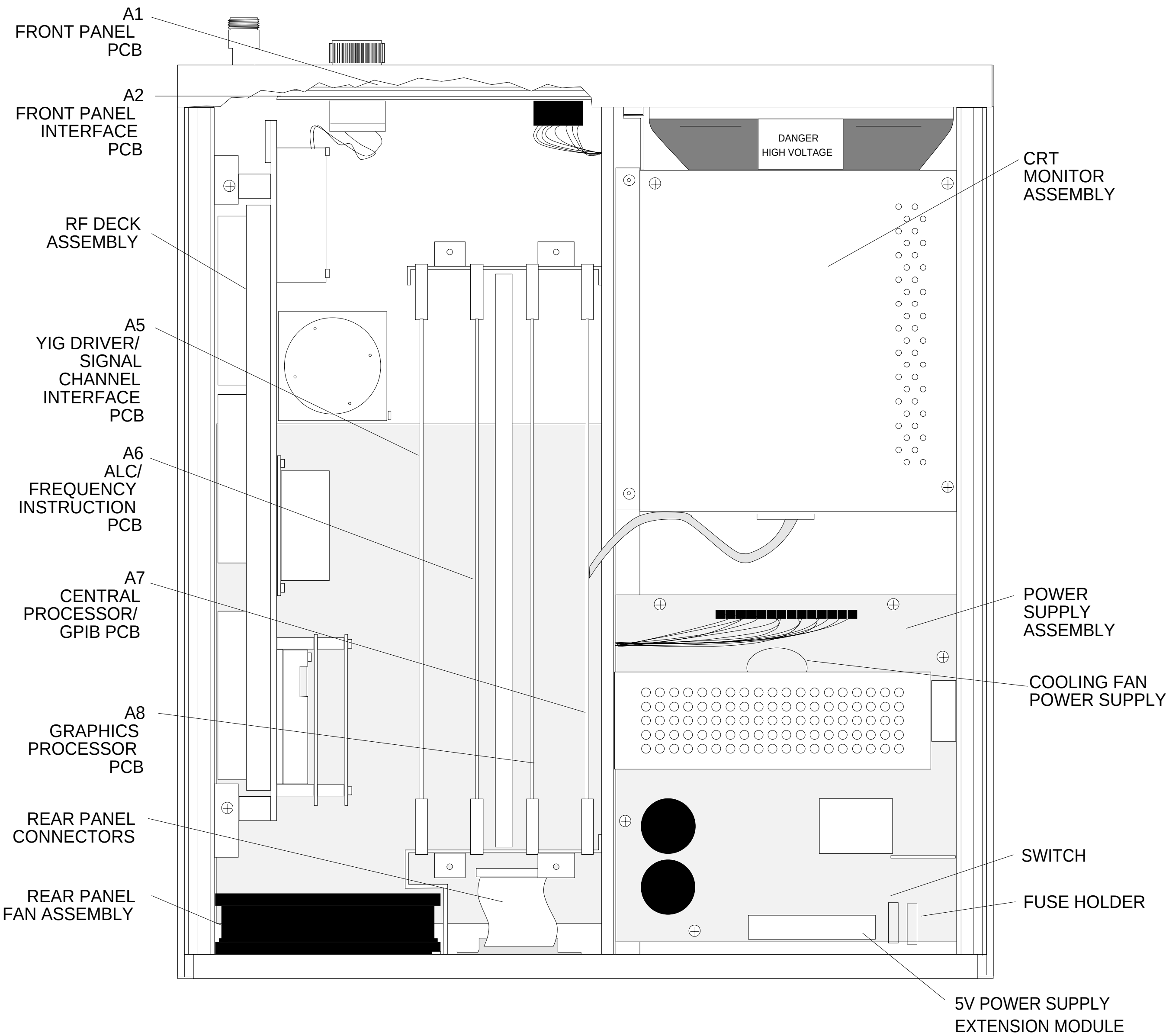

Figure 2-1. 541XXA Major Assemblies Location Diagram (Top View)

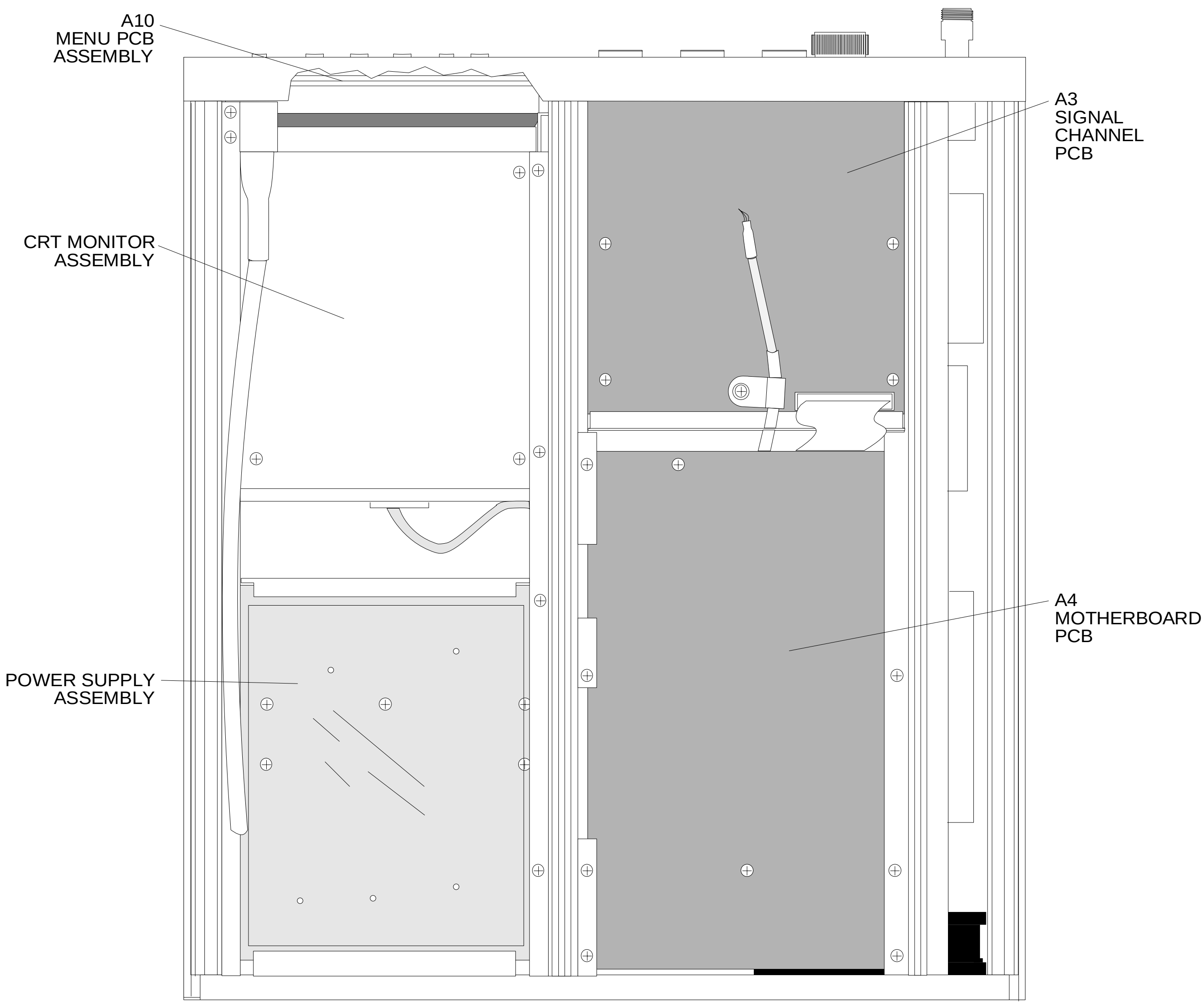

***Figure 2-2.** 541XXA Major Assemblies Location Diagram (Bottom View)*

Table 2-1. Exchange Assemblies

	54100A Series PC Boards
D40051-3	A1 Front Panel Switch PCB Assembly
D40052-3	A2 Front Panel Interface PCB Assembly
D40036-3	A2 Front Panel Interface PCB Assembly
D40053-3	A3 Signal Channel PCB Assembly with Option 05
D40045-3	A3 Signal Channel PCB Assembly without Option 05
D35358-4	A5 YIG Driver and Signal Channel Interface PCB Assembly, 54117A, 54119A
D35358-5	A5 YIG Driver and Signal Channel Interface PCB Assembly, 54128A
D35358-6	A5 YIG Driver and Signal Channel Interface PCB Assembly, 54130A
D35358-7	A5 YIG Driver and Signal Channel Interface PCB Assembly, 54131A
D35358-8	A5 YIG Driver and Signal Channel Interface PCB Assembly, 54136A
D35358-9	A5 YIG Driver and Signal Channel Interface PCB Assembly, 54137A, 54147A
D35358-10	A5 YIG Driver and Signal Channel Interface PCB Assembly, 54107A, 54109A,
ND37738-1	A6 Frequency Instruction and ALC PCB Assembly, 54107A
ND37738-2	A6 Frequency Instruction and ALC PCB Assembly, 54109A
ND37738-3	A6 Frequency Instruction and ALC PCB Assembly, 54111A
ND37738-4	A6 Frequency Instruction and ALC PCB Assembly, All other Models
ND41035-1	A6 Frequency Instruction and ALC PCB Assembly, 54154A, 54161A, 54163A, 54169A
ND41035-2	A6 Frequency Instruction and ALC PCB Assembly, 54177A
D40057-4	A7 CPU PCB Assembly
D40057-6	A7 CPU with Option 3 GP-IB PCB Assembly
D40057-7	A7 CPU with Option 7 DTF, Option 3 GP-IB PCB Assembly
D35066-3	A8 Graphics System Processor PCB Assembly
D40070	Power Supply Assembly, Run 4 and below, Replaced by ND40967
ND40967	Power Supply Assembly, Run 4 and below
D40066	Power Supply Assembly, Replaced by D40079
D40079	Power Supply Assembly, 54100A
B40108-3	5 Volt Power Supply Extension PCB Assembly
B40060-3	A10 Menu PCB Assembly
ND39447	A11, C35329 500 MHz Sampler/Marker Assembly
C35398	A11 500 MHz Sampler/Marker Assembly, Multiband Models, Replaced by ND26500
C35192	A12/A13 500 MHz VCO/Power Amplifier Assembly
C35396	A12/A13 500 MHz VCO/Power Amplifier Assembly, Multiband Models
C35194-7	A14 25 MHz Marker Assembly, 54128A, 54130A, 54131A, 54136A
C35194-11	A14 25 MHz Marker Assembly, 54117A, 54119A
C35397-7	A14 25 MHz Marker Assembly, 54137A, 54147A, Replaced by ND26500
ND26500	A11/A14 500/25 MHz Marker Assembly, Multiband Models
C35287-3	A17 RF Deck Distribution Panel Assembly
C35286-3	A18 Switched Filter Driver Assembly
D35430-3	A19 Multiband Controller PCB Assembly
D40049-3	A23 Multiband Controller PCB Assembly
D40049-3	A23 Multiband Controller PCB Assembly 32 GHz
D40047	Monitor Assembly
2000-612	Floppy Drive Assembly
	54100A Series YIG Oscillators
C11282	8 to 12.4 GHz Oscillator
C14770-1	12.4 to 20 GHz Oscillator
C21620	2 to 20 GHz Oscillator
C22550	10 to 13 GHz Oscillator

54100A Series YIG Oscillators (Continued)

Table 2-1. Exchange Assemblies

C22560	10 to 16 GHz Oscillator
C22570	2 to 8.4 GHz Oscillator
C24436	2 to 8.6 GHz Oscillator
C29963	17 to 26.5 GHz Oscillator
54100A Series RF Components	
D24335	Step Attenuator 70dB, 3 GHz
4412K	Step Attenuator 70dB, 20 GHz
4512K	Step Attenuator 70dB, 26.5 GHz
4612K	Step Attenuator 70dB, 40 GHz
D27315	Step Attenuator 90dB, 50 GHz
B35283	Output Connector Assembly 50 ohm, 3 GHz and below
B35284	Output Connector Assembly 75 ohm, 3 GHz and below
C18640-1	Output Connector Assembly "K "
C18650-1	Output Connector Assembly " N "
ND40910	Output Connector Assembly "V"
D21450	Coupler 20 GHz
D21452	Coupler 40 GHz
D28179	Coupler 50 GHz, Replaced by D28481
D28481	Coupler 50 GHz
D27063	Down Convertor Assembly 0.01 to 2 GHz
D26947	Down Convertor Assembly 0.01 to 3 GHz
D22870	Modulator Assembly, 2 to 8.5 GHz
D22880	Modulator Assembly, 8 to 12.4 GHz
D22890	Modulator Assembly, 10 to 16 GHz
D22900	Modulator Assembly, 12 to 20 GHz
D22910	Modulator Assembly, 18 to 26.5 GHz
D22040	Switched Filter Assembly, 54137A, 54147A
D23800	Switched Filter Assembly, 54117A, 54119A
D26805	Switched Filter Assembly, 54145A, 54161A, 54163A, 54169A
D26800	Switched Filter Assembly, 54177A
D25432	3 GHz Marker Package
D41075	SDM 20 to 32 GHz
D28535	SDM 20 to 40 GHz
D28185	SQM 40 to 50 GHz

Table 2-2. Replaceable Common Parts

Part Number	Description
D40107	Cover, Top
D40107	Cover, Bottom
2000-633	Cover, Side (Handle)
D40111	Cover, Side
783-830	Handle, Side Carrying
B37056	Strap Handle
900-714	Screw, Handle, Side Carrying
B37105	End Cap (for strap handle)
551-152	Connector, Front Panel Input
2000-548	Foot, Rear, Bottom Left
2000-549	Foot, Rear, Bottom Right
2000-552	Foot, Rear, Top Left
2000-553	Foot, Rear, Top Right
2000-560	Screw, Green Head
631-16	Fuse, 4A, 3AG Slow Blow (115 Vac Operation)
631-67	Fuse, 2A, Time Lag, 20 mm (230 Vac Operation)
533-221	Fuse Holder, 3AG Type (Used on B35375, Figure 2-3)
533-387	Fuse Holder, 3AG Type (Used on B35375, Figure 2-3)
533-240	Fuse Holder, 5 x 20 mm Type (Used with Updated Line Input, Figure 2-4)
533-386	Fuse Holder, 5 x 20 mm Type (Used with Updated Line Input, Figure 2-4)
C40217	Fan Assembly, Rear Panel
783-841	Finger Guard, Fan (with filter, black)
790-442	Finger Guard, Fan (with filter, aluminum)
2000-641	Knob, Data Entry
B35375	Line Module Assembly, Rear Panel (Figure 2-3)
	541XXA Models Without Front Handles
2000-546	Foot, Front, Bottom Left
2000-547	Foot, Front, Bottom Right
2000-550	Foot, Front,Top Left
2000-551	Foot, Front,Top Right
	541XXA Models With Front Handles
B37147	Upper Insert
C37170	Foot, Bottom Left
C37171	Foot, Bottom Right
D37168-3	Handle, Left

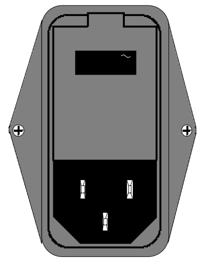

Figure 2-3. *Line Voltage Module, Part Number B35375*

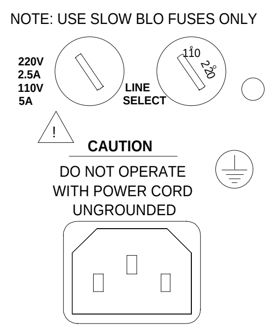

Figure 2-4. *Line Input Configuration, Updated Rear Panel*

Table 2-3. *ANRITSU Service Centers*

UNITED STATES
ANRITSU COMPANY
685 Jarvis Drive
Morgan Hill, CA 95037-2809
Telephone: (408) 776-8300
FAX: 408-776-1744

ANRITSU COMPANY
10 Kingsbridge Road
Fairfield, NJ 07004
Telephone: (201) 227-8999
FAX: 201-575-0092

AUSTRALIA
ANRITSU PTY. LTD.
Unit 3, 170 Foster Road
Mt Waverley, VIC 3149
Australia
Telephone: 03-9558-8177
Fax: 03-9558-8255

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ANRITSU ELECTRONICA LTDA.
Praia de Botafogo, 440, Sala 2401
CEP22250-040, Rio de Janeiro, RJ, Brasil
Telephone: 021-28-69-141
Fax: 021-53-71-456

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ANRITSU INSTRUMENTS LTD.
215 Stafford Road, Unit 102
Nepean, Ontario K2H 9C1
Telephone: (613) 828-4090
FAX: (613) 828-5400

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ANRITSU BEIJING SERVICE
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Beijing Fortune Building
416W, 5 Dong San Huan Bei Lu
Chaoyang qu
Beijing 100004, China
Telephone: 010-501-7559
FAX: 010-501-7558

FRANCE
ANRITSU S.A
9 Avenue du Quebec
Zone de Courtaboeuf
91951 Les Ulis Cedex
Telephone: 016-44-66-546
FAX: 016-44-61-065

GERMANY
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Grafenberger Allee 54-56
D-40237 Dusseldorf
Germany
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FAX: 0211-68 33 53

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New Delhi 110 016
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FAX: 011-686-6720

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TECH-CENT, LTD
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Tel-Aviv 69701
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FAX: (03) 64-78-334

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FAX: 02-782-4590

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ANRITSU (SINGAPORE) PTE LTD
3 Shenton Way #24-03
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Singapore 0106
Telephone: 2265206
FAX: 2265207

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Waterfall Park
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Fax: 011-315-2175

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Chapter 3
Troubleshooting

Table of Contents

Many of the troubleshooting procedures presented in this chapter require the removal of instrument covers to gain access to printed circuit assemblies and other major assemblies.

WARNING

Hazardous voltages are present inside the instrument when ac line power is connected. Turn off the instrument and remove the line cord before removing any covers or panels. Trouble shooting or repair procedures should only be performed by service personnel who are fully aware of the potential hazards.

CAUTION

Many assemblies in the 541XXA contain static-sensitive components. Improper handling of these assemblies may result in damage to the assemblies. ***Always*** observe the static-sensitive component handling precautions described in Chapter 1, Figure 1-2.

Chapter 3 Troubleshooting

3-1 INTRODUCTION

This chapter provides information for troubleshooting 541XXA Network Analyzers. The troubleshooting operations presented in this chapter support fault isolation down to a replaceable subassembly. (Remove and replace procedures for major 541XXA assemblies are contained in Chapter 7.)

3-2 RECOMMENDED TEST EQUIPMENT

The recommended test equipment for the troubleshooting operations presented in this chapter is listed in Chapter 1, Table 1-2 (page 1-7).

3-3 ERROR CODES/MESSAGES AND CAUSES

The 541XXA operating software includes internal diagnostics that are initiated during power-up of the unit, or when the SELF TEST key is pressed. These diagnostics also check for fault conditions during normal operation. Any fault or error conditions found are reported as described below. Tables 3-1 and 3-2 (pages 3-4 and 3-5) list all possible error messages. For each specific error message, the table provides either a possible cause of the fault, or a reference to another troubleshooting table that contains more detailed troubleshooting operations. There are four primary types of error messages that are reported by the diagnostics:

- Power-Up Errors
- Self Test Errors
- Calibration Errors
- Normal Operation Error and Warning Messages

Condition/Fault	Audible Beeps
No Random Access Memory (RAM)	3
CPU Error	5
Less than 640 K of RAM	6
No Peripheral Chip/No Serial BIOS	8
EPROM Checksum Error	9
CMOS Checksum Error	10

Power-Up Errors

Serious A7 Central Processor PCB malfunctions detected during power up will be flagged by sounding the internal speaker. The table at left lists all possible audible beeps for associated A7 Central Processor PCB malfunctions. For all of these conditions, replace the A7 PCB.

Self Test Errors

Serious system malfunctions detected during self test will be flagged by a bold **FAILED TESTS** screen display. Specific fault messages will also be reported; for example: **A5 SIGNAL CHANNEL ADC fail**. These self test fault conditions are also indicated by the flashing of one or more front panel LED indicators. A specific LED flashes steadily after completion of the self test for each fault detected. Table 3-1 shows which error message and LED indicator correspond to each major fault condition. Note that the flashing LED indicator provides exactly the same information as the CRT failure message. Should the CRT fail, this technique can be used as a troubleshooting aid. The faults listed in Table 3-1 generally indicate malfunctions in the major PCB assemblies of the 541XXA.

Table 3-1. *Error Messages and Front Panel LED Indicators for Power-Up / Self-Test Errors*

Condition/Fault	Associated Front Panel LED	Recommended Action
A2 KEYBOARD INTERFACE fail	REMOTE	Replace A2 PCB. Refer to PCB removal procedures, paragraph 7-5.
A3 SIGNAL CHANNEL PRESENT or A5 SIGNAL CHANNEL ADC fail	CALIBRATION UNCAL	Replace A3 PCB, then Replace A5 PCB, as necessary. Refer to PCB removal procedures, paragraphs 7-3 and 7-8.
Self Test completed	Display, Channel 1 and 2	

Calibration Errors

After self test, and prior to starting normal operation, the 541XXA performs an internal frequency lock calibration. These calibrations are also performed periodically during normal operation. If a frequency calibration test fails, one or more "calibration error" messages will be displayed along with the **FAILED TESTS** display (example: **fails het band 500 miss**); refer to Tables 3-2A and 3-2B.

Calibration error messages generally indicate RF deck related problems. During normal operation, a failed calibration is indicated by a failure code displayed in the lower right corner of the screen display. These error codes are listed in Table 3-3 along with suggested remedial action.

Table 3-2. *Displayed Error Message Heading and Message Text for Calibration-Related Faults and Errors*

A ERROR MESSAGE HEADINGS*		B ERROR MESSAGE TEXT*	
Heading	**Category/Type**	**Message**	**Meaning**
GENERAL	Major errors	no 500	500 MHz markers cannot be found during GENERAL test
START-MAIN	Calibration of START DAC (using main coil)	500 miss	500 MHz marker missing during START-MAIN DAC or WIDTH-MAIN DAC calibrations
ERROR	Calibration of ERROR DAC (using FM coil)	1st wrong	For START-MAIN DAC or WIDTH-MAIN DAC calibrations: Cannot find two markers with correct spacing in first group of three at top of frequency range. For HET BAND calibration: Offset between main band 500 MHz markers and HET band 25 MHz markers is out of specification.
WIDTH-MAIN	Calibration of WIDTH DAC (using main coil)	500 size	500 MHz markers not large enough during START-MAIN DAC or WIDTH-MAIN DAC calibrations
WIDTH-FM	Calibration of WIDTH DAC (using FM coil)	spacing	Cannot find two markers with correct spacing in group of three during ERROR, WIDTH-FM, or HET BAND calibrations (using FM coil).
HET BAND	Verification of Downconverter and 25 MHz Marker Box operation	Error Codes 210 to 212	This series of error codes will be displayed after a Frequency Calibration if an error occurs (Refer to paragraph 3-3 and Table 3-3.).
		Error Codes 213 and above	This series of error codes will be displayed only during fault diagnosis in the Engineering Mode of operation. To put 541XXA in this mode, refer to Chapter 6, paragraph 6-4 “YIG Driver Adjustment” procedure. After entering into the Engineering Mode, press Data Entry keys “4 and “1” in sequence to turn on Calibration Error Codes. To return to normal mode, press the Self Test key. Refer Table 3-3 for explanations of the error codes.

* These headings and messages are displayed on the CRT Monitor. When 541XXA reverts to normal screen display, the corresponding error codes will be displayed in the lower right corner of the screen display. The error codes are described in Table 3-3.

Normal Operation Error and Warning Messages

When an abnormal condition is detected during normal operation, an error or warning messages is displayed in the message box located in the lower right corner of the screen display, as described below. If more than one fault is detected, the highest priority error message will be displayed. Error messages take precedence over warning messages.

Error Messages — These messages report malfunctions that occur either during self test or during normal operation. They can be identified by the presence of a failure code; example: **500 MHz markers 201**. Table 3-3 lists these codes and suggested remedies.

Warning Messages — These messages report procedural errors; example: **NO CAL DATA**. They do not report fault conditions or malfunctions, but they do indicate that an invalid operation has been attempted. A Warning message can be distinguished from an error message by the absence of an error code following the message. Refer to the 541XXA Operation Manual for descriptions of warning messages and remedies.

3-4 QUICK TROUBLESHOOTING GUIDES

Tables 3-4 and 3-5 (pages 3-9 and 3-10) provide quick help for troubleshooting common problems.

3-5 DETAILED TROUBLESHOOTING PROCEDURES

Detailed, structured-text procedures are provided and start on page 3-12. These procedures provide a step-by-step method for isolating malfunctions to a replaceable subassembly. In cases where any of several subassemblies are suspect, subassembly replacement is indicated. The recommended replacement order is for the most-likely subassemblies to be replaced first.

NOTE

The 54154A through 54177A are fitted with an A24 ALC frequency instruction PCB and A23 Multiband Controller PCB, rather than A6 and A19 PCBs. Whereas, the PCBs are not interchangeable, the test points are the same.

Table 3-3. Error Codes for Calibration Related Faults / Errors (1 of 2)

Calibration Error Code	Error Description	Refer to Page
201	General, no 500 MHz or 75 MHz markers	3-12
202	START DAC main band, 500 MHz or 75 MHz marker(s) missing; or, top or bottom frequency(s) not correctly set	3-12
203	START DAC main band, 1st MHz markers (top) wrong	3-12
204	START DAC main band, 500 MHz or 75 MHz marker size error	3-12
205	ERROR DAC, 25 MHz marker spacing wrong	3-14
206	WIDTH DAC main band, 500 MHz or 75 MHz marker(s) missing	3-12
207	WIDTH DAC main band, 1st MHz markers (top) wrong	3-12
208	WIDTH DAC main band, 500 MHz or 75 MHz marker size error	3-12
209	WIDTH DAC fm, 25 MHz marker spacing wrong	3-14
210	HET band, 500 MHz or 75 MHz marker missing	3-12
211	HET band, 25 MHz and 500 MHz marker spacing wrong	3-14
212	HET band, 25 MHz marker spacing wrong	3-14
213	Start lb, START DAC, 500 MHz or 75 MHz marker missing	3-12
214	Start lb, 25 MHz slow lock fail	3-14
215	Stop lb, WIDTH DAC, 500 MHz or 75 MHz marker missing	3-12
216	Stop lb, 25 MHz slow lock fail	3-14
217	Start mb, START DAC, 500 MHz or 75 MHz marker missing	3-12
218	Start mb, 25 MHz slow lock fail	3-14
219	Stop mb, WIDTH DAC, 500 MHz or 75 MHz marker missing	3-12
220	Stop mb, 25 MHz slow lock fail	3-14
221	Start hb, START DAC, 500 MHz or 75 MHz marker missing	3-12
222	Start hb, 25 MHz slow lock fail	3-14
223	Stop hb, WIDTH DAC, 500 MHz or 75 MHz marker missing	3-12
224	Stop hb, 25 MHz slow lock fail	3-14

Legend: **lb, low band; mb, mid band; hb, high band**

Table 3-3. Error Codes for Calibration Related Faults / Errors (2 of 2)

Calibration Error Code	Error Description	Refer to Page
225	lb chan1 error, multiple slow lock fail	3-16
226	lb chan2 error, multiple slow lock fail	3-16
227	mb chan1 error, multiple slow lock fail	3-16
228	mb chan2 error, multiple slow lock fail	3-16
229	hb chan1 error, multiple slow lock fail	3-16
230	hb chan2 error, multiple slow lock fail	3-16
231	lb chan1 error, 25 MHz slow lock fail	3-14
232	lb chan2 error, 25 MHz slow lock fail	3-14
233	mb chan1 error, 25 MHz slow lock fail	3-14
234	mb chan2 error, 25 MHz slow lock fail	3-14
235	hb chan1 error, 25 MHz slow lock fail	3-14
236	hb chan2 error, 25 MHz slow lock fail	3-14
237	lb mb chan1 error, 25 MHz fast lock fail	3-14
238	lb mb chan2 error, 25 MHz fast lock fail	3-14
239	mb chan1 error, 25 MHz fast lock fail	3-14
240	mb chan2 error, 25 MHz fast lock fail	3-14
241	hb chan1 error, 25 MHz fast lock fail	3-14
242	hb chan2 error, 25 MHz fast lock fail	3-14
243	lb chan1 error, 25 MHz ref fast lock fail	3-14
244	lb chan2 error, 25 MHz ref fast lock fail	3-14
245	mb chan1 error, 25 MHz ref fast lock fail	3-14
246	mb chan2 error, 25 MHz ref fast lock fail	3-14
247	hb chan1 error, 25 MHz ref fast lock fail	3-14
248	hb chan2 error, 25 MHz ref fast lock fail	3-14

Legend: **lb, low band; mb, mid band; hb, high band**

Table 3-4. 541XXA Main System Quick Troubleshooting Guide (1 of 1)

Faulty	Possible Problem PCB/Assembly (Listed in order of most-to-least probable)
Front panel is dead (no lights), and fan is inoperative	**1.** Fuse **2.** Power Supply Assembly
Fan is inoperative.	**1.** Fan **2.** Power Supply Assembly
Monitor has no display; however, fan runs and front panel LEDs are blinking	Power Supply Assembly (The LED indicator on the power supply motherboard will be blinking)
Monitor has no display; however, fan functions and front panel seems normal	**1.** Monitor **2.** A8 Graphic Processor PCB **3.** Power Supply Assembly
Abnormal monitor display	**1.** Monitor **2.** A8 Graphic Processor PCB **3.** Power Supply Assembly
Unable to complete power-up routine, but fan runs	**1.** A7 Central Processor PCB **2.** Power Supply Assembly
Self Test error code	Refer to detailed procedures on pages 3-12 through 3-16
Excessive residual FM	**1.** A5 YIG Driver/Signal Channel Interface PCB **2.** YIG Oscillator (Full Band) **3.** Down Converter Assembly (Het Band) **4.** Power Supply Assembly
Excessive harmonics	See Table 3-5, RF Deck Quick Troubleshooting Guide
Abnormal output power	**1.** See Table 3-5, RF Deck Quick Troubleshooting Guide **2.** A6/A24 ALC/Frequency Instruction PCB **3.** A19/A23 Multiband Controller Assembly (Models 54137A —54177A)
Inaccurate output frequency	See Table 3-5, RF Deck Quick Troubleshooting Guide
Malfunctioning Frequency Locking System	See Table 3-5, RF Deck Quick Troubleshooting Guide
Front panel keys do not respond	**1.** A1 Front Panel PCB or A10 Menu PCB Assembly **2.** A7 Central Processor PCB
Signal channel input is unstable	A3 Signal Channel PCB
Incorrect signal channel power level reading	**1.** A3 Signal Channel PCB **2.** A5 YIG Driver/Signal Channel Interface PCB
External leveling malfunctioning	A6/A24 ALC/Frequency Instruction PCB
Printer output is erratic	**1.** Printer malfunctioning or configuration is incorrect **2.** A8 Graphic Processor PCB

Table 3-5. *RF Deck Quick Troubleshooting Guide (1 of 2)*

Faulty	Possible Problem PCB/Assembly (Listed in order of most-to-least probable)
No or low output power (Models 54107A, 54109A, 54111A)	**1.** Step Attenuator (if installed) **2.** Down Converter **3.** YIG oscillator
No or low output power (Models 54117A through 54147A)	**1.** Step Attenuator (if installed) **2.** Control Modulator (output above 2 GHz) **3.** Down Converter (output below 2 GHz) **4.** Switch Filter (54137A and 54147A, only) **5.** YIG oscillator
No or low output power (Models 54154A through 54177A)	**1.** Step Attenuator (if installed) **2.** Down Converter (output below 2 GHz) **3**. Switch Filter if power missing from 2 GHz to 20 GHz. **4.** Switch Doubler no power from 20 GHz to 40 GHz. **5**. Switch Quadrupler no power from 40 GHz to 50 GHz.
Output power rolls off at low-end frequency	**1.** Step Attenuator (if installed) **2.** Down Converter
Inaccurate attenuation	Step Attenuator (if installed)
Unleveled LED blinking or lit constantly *All models, except 54107A, 54109A, and 54111A*	**1.** Directional Coupler (output above 2 GHz) **2.** Control Modulator or Switch Filter for 54137A and 54147A (output above 2 GHz) **3.** Down Converter (output below 2 GHz) **4.** YIG oscillator
Models 54107A, 54109A, 54111A	Down Converter
Inaccurate output frequency *All models, except 54107A, 54109A, and 54111A*	**1.** Switch Filter (above 2 GHz) (54137A and 54147A) **2.** Control Modulator (output above 2 GHz) **3.** Down Converter (output below 2 GHz)
Models 54107A, 54109A, 54111A	Down Converter
Excessive harmonics *All models, except 54107A, 54109A, and 54111A*	**1.** Switch Filter (output above 2 GHz) **2.** Down Converter (output below 2 GHz) **3.** YIG oscillator
Models 54107A, 54109A, 54111A	Down Converter

Table 3-6. RF Deck Quick Troubleshooting Guide (2 of 2)

Faulty	Possible Problem PCB/Assembly (Listed in order of most-to-least probable)
No frequency calibration marker	
All models, except 54107A, 54109A, and 54111A	**1.** Control Modulator **2.** 500 MHz VCO/Power Amplifier **3.** YIG oscillator
Models 54107A, 54109A, 54111A	**1.** Down Converter **2.** Marker Module Assembly **3.** YIG oscillator
25 MHz Marker missing	
All models, except 54107A, 54109A, and 54111A	**1.** 25 MHz Marker module (above 2 GHz) **2.** 500 MHz Marker module (above 2 GHz) **3.** 500 MHz VCO/Power Amplifier (above 2 GHz) **4.** Marker Module Assembly (below 2 GHz)
Models 54107A, 54109A, 54111A	**1.** Down Converter **2.** Marker Module Assembly
500 MHz Marker missing	**1.** 500 MHz Marker module **2.** 500 MHz VCO/Power Amplifier
75 MHz Marker missing	**1.** Down Converter **2.** Marker Module Assembly

Error Messages 201, 202, 203, 204, 206, 207, 208, 210, 213, 215, 217, 219, 221, or 223

For Models 54107A, 54109A, or 54111A:

The RF deck components listed below, if faulty, can cause the 541XXA to display the Error Messages listed above.

- Down Converter.
- Marker Module Assembly.

Troubleshooting Procedure

Step 1. Reset unit to factory default setup. (Default power level is shown below.)

Model	Without Attenuator	With Attenuator
54107A, 54109A, 54111A–50Ω output	+12 dBm	+10 dBm
54107A, 54109A, 54111A–75Ω output	+10 dBm	+8 dBm
54117A, 54119A, 54128A, 54130A, 54131A, 54136A, 54137A, 54147A	+10 dBm	+7 dBm
54154A, 54161A, 54163A, 54169A,	+4	+1
54177A	+1	–2

Step 2. Use a detector to check the RF output power level of the 541XXA.

Step 3. If output level is incorrect or the unleveled LED is flashing or lit constantly, replace Down Converter and perform YIG Driver adjustment procedure (Chapter 6, paragraph 6-9) and ALC adjustment procedure (Chapter 6, paragraphs 6-10 or 6-11).

Step 4. If output level is correct, replace Marker module Assembly (Chapter 7, paragraph 7-15 through -18, as appropriate for model).

Step 5. If the fault condition still exists, call Customer Service for assistance.

For Models 54117A through 54177A:

The RF deck components listed below, if faulty, can cause the 541XXA to display the Error Messages listed above.

- 500MHz VCO/PA Module Assembly
- 500MHz IF Module
- Control Modulator
- Switched Filter Module (for 54137A through 54177A)

Troubleshooting Procedure

Step 1. Reset 541XXA to factory default setup. (See table for Step 1 on page 6-12.)

Step 2. Use a detector to check the RF output power level of the 541XXA.

Step 3. If output level is incorrect, replace Control Modulator or Switched Filter Module (for 54137A through 54177A) (Chapter 7, paragraph 7-18, 7-19, or 7-20), and perform Marker Adjustment procedure (Chapter 6, paragraph 6-8).

Step 4. If output level is correct, perform Marker Adjustment procedure (Chapter 6, paragraph 6-8).

Step 5. If previous steps do not correct the fault condition, replace 500 MHz IF Module (Chapter 7, paragraph 7-15 through -20, as appropriate for model) and perform marker adjustment procedure (Chapter 6, paragraph 6-8).

NOTE

For 54137A through 54177A, the 500 MHz IF Module replacement kit also includes the 25 MHz IF Module.

Step 6. If previous steps do not correct the fault condition, replace 500 MHz VCO/PA Module Assembly (Chapter 7, paragraph 7-15 through -20, as appropriate for model), and perform marker adjustment procedure (Chapter 6, paragraph 6-8).

Step 7. If the fault condition still exists, call Customer Service for assistance.

Error Messages 205, 209, 211, 212, 214, 216, 218, 220, 222, 224, or 231 through 248

For Models 54107A, 54109A, or 54111A:

The RF deck components listed below, if faulty, can cause the 541XXA to display the Error Messages listed above.

- Down Converter.
- Marker Module Assembly.

Troubleshooting Procedure

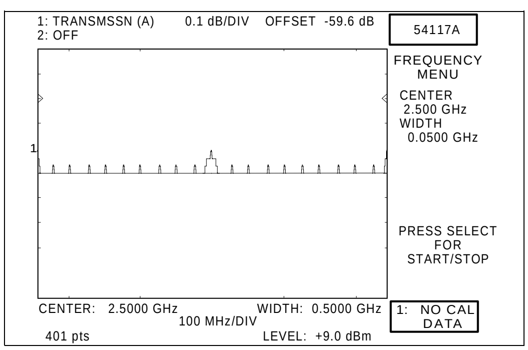
Step 1. Reset 541XXA to factory default setup.

Step 2. Set the 541XXA to operate in Service mode as follows: Press the Self Test key; when the Channel Display On/Off LED's flash during self test, sequentially press the Frequency, Markers and Leveling keys.

Step 3. Press the Data Entry "2" key to select "diagnostic markers" sequence.

Step 4. Press the Data Entry "1" to activate the marker display.

Step 5. Press Self Test key, which will normalize the 541XXA display. The display should be a flat line with wide and narrow pips. (If the 541XXA fails self test, press Select key to obtain a measurement display.)



Step 6. Press the Frequency and Select keys to display the CENTER/WIDTH menu.

Step 7. Set **CENTER** frequency to mid band and **WIDTH** to 500 MHz

Step 8. Verify all markers are equally spaced, change **CENTER** frequency if necessary. If any marker is missing, replace appropriate 25 MHz or 500 MHz Marker Module (Chapter 7, paragraph 7-15 through -18, as appropriate for model).

Step 9. If previous step does not correct the fault condition, replace Down Converter and perform YIG Driver adjustment procedure (Chapter 6, paragraph 6-5) and ALC adjustment procedure (Chapter 6, paragraphs 6-10 or 6-11, as appropriate).

Step 10. If the fault condition still exists, call Customer Service for assistance.

For 54117A through 54177A:

The RF deck components listed below, if faulty, can cause the 541XXA to display the Error Messages listed above.

- 25 MHz IF Module.
- 500 MHz VCO/PA Module Assembly.
- 500 MHz IF Module.
- Marker Module Assembly (For 54117A and 54147A only).
- Frequency Converter (For 54117A and 54147A only).

Troubleshooting Procedure

For 54119A through 54137A, 54154A, 54163A:

Step 1. Perform Marker Adjustment procedure (Chapter 6, paragraph 6-8).

Step 2. If any 25 MHz marker is missing or spurious markers are presented, replace 25 MHz IF Module and repeat Step 1.

Step 3. If previous step does not correct the fault condition, replace 500 MHz VCO/PA Module Assembly (Chapter 7, paragraph 7-15 through -18, as appropriate for model), and repeat Step 1.

Step 4. If the fault condition still exists, call Customer Service for assistance.

For 54117A, 54147A, 54161A, 54169A, 54177A:

Troubleshooting Procedure

Step 1. If fault condition occurs above 2 GHz, follow steps 1-5 of troubleshooting procedure for 54119A through 54137A, 54154A, 54163A.

Step 2. If fault condition occurs below 2 GHz, perform Heterodyne Band 25 MHz marker verification (Chapter 6, paragraph 6-8) and follow steps 7 and 8 of troubleshooting procedure for 54107A, 54109A, or 54111A.

Error Messages 225 through 230

Troubleshooting Procedure

Step 1. Perform Marker Adjustment procedure (Chapter 6, paragraph 6-8).

Step 2. If the fault condition still exists, call Customer Service for assistance.

RF Deck Problems

Some fault conditions of the RF Deck are not reported by the diagnostic; therefore, no Error Message is displayed after self test and during normal operation. These unreported fault conditions are:

- Power output problem.
- Auto Level Control problem.
- Harmonics and Spurious problem.
- YIG Oscillator problem.
- Residual FM problem.

NOTE

Models 54154A through 54169A are essentially the same as a 54147A with frequency doubling and quadrupling microwave components added to generate the higher frequencies. The doubler produces frequencies between 20 and 40 GHz. The Quadrupler produces frequencies between 40 and 50 GHz. If microwave power is not present in these upper bands but is present below 20 GHz, the relavent high frequency component or it's power supply may be defective. The is a separate additional power supply unit (PSU) that is mounted on the rear panel. It produces +10V and +8V which are only used by the high frequency RF components. See Power Supply fault finding for more information.

Output Power Problems

Symptoms:

- Output power level has inaccurate attenuation.
- Output power level rolls off at low frequency.
- Output power is lower than expected.
- No output power in Heterodyne or Microwave bands.

Troubleshooting Procedure

Step 1. Reset 541XXA to factory default setup.

Step 2. Set Channel 1 to measure POWER on Channel A, and turn Channel 2 off.

Step 3. Connect a Series 560 or 5400 RF detector between the RF Output and Input A connectors.

Step 4. For Heterodyne Band (0.01–2 GHz) power loss, verify signal and bias voltage to Down Converter (below).

Control Signal	Location	Value*
Mod Control	A6 PCB, TP16	Approx. +14V to –4V (pulse chain)
Mod Bias	A6 PCB, TP17	Approx. +14V to –14V (pulse chain)

* All values ±0.5V

Step 5. For Microwave Bands power loss, verify signal and bias voltage to Control Modulator (below).

Control Signal	Location	Value*
Mod Control	A6 PCB, TP18	Approx. +14V to –4 V (pulse chain)
Mod Bias	A6 PCB, TP19	Approx. +14V to –14V (pulse chain)

* All values ±0.5V

Step 6. If signal is correct, replace Down Converter or Control Modulator, as appropriate (Chapter 7, paragraph 7-15 through -20, as appropriate for model). If signal is incorrect, replace A6 PCB (Chapter 7, paragraph 7-3).

Step 7. Vary the power level setting in 10 dB step and verify that the output power level changes.

Step 8. If any output power level rolls off at low frequency, replace the Step Attenuator assembly. (Chapter 7, paragraph 7-15 through -20, as appropriate for model).

Step 9. If any output power level is incorrect, verify the drive signals for each attenuator step. TTL levels should be as shown in Table 3-6 or 3-7, as appropriate for model.

Step 10. If any drive signal is incorrect, replace the A7 Centrol Processor PCB (Chapter 7, paragraph 7-3).

Step 11. If drive signals are correct, replace step attenuator assembly.

Table 3-6. *Step Attenuator Drive Signals for RF Band Models 54107A, 54109A, and 54111A*

A4 Motherboard Connector J6 Pin No.	Attenuator Step*							
	0	10	20	30	40	50	60	70
1	Not used							
2	H	H	H	H	L	L	L	L
3 & 4	Not used							
5	H	H	H	H	H	H	L	L
6	H	H	H	H	H	H	H	H
7 & 8	Not used							
9	H	L	H	L	H	L	H	L
10	H	H	L	L	L	L	L	L
11 thru 14	Not used							

* To set 541XXA to desired attenuator step, set RF output level to same value as step; e.g., 0 dBm for step 0, –10 dBm for step 10… etc.
H = approx 24V
L = approx 0V

Table 3-7. Step Attenuator Drive Signals for Microwave Band Models 54117A through 54177A

A4 Motherboard Connector J6 Pin No.	Attenuator Step							
	0	10	20	30	40	50	60	70
1	Not used							
2	H	L	H	L	H	L	H	L
3	L	L	L	L	H	H	H	H
4	Not used							
5	H	H	L	L	H	H	L	L
6	H	H	H	H	H	H	H	H
7 & 8	Not used							
9	H	H	H	H	L	L	L	L
10	Not used							
11	L	L	H	H	L	L	H	H
12	Not used							
13	L	H	L	H	L	H	L	H

* To set 541XXA to desired attenuator step, set RF output level to same value as step; e.g., 0 dBm for step 0, –10 dBm for step 10… etc.
H = approx 24V
L = approx 0V

Auto Level Control Problem

Symptoms:

- Leveled LED is flashing or lit constantly above 2 GHz.
- Output power level displays clipping characteristic.

For 54107A, 54109A, or 54111A and 54117A, 54147A, 54161A, 54169A, 54177A below 2 GHz:

Troubleshooting Procedures

Step 1. Reset 541XXA to factory default setup.

Step 2. Set output power to 2 dB above factory default setting (below).

Model	Without Attenuator	With Attenuator
54107A, 54109A. 54111A 50Ω output	+14 dBm	+12 dBm
54107A, 54109A. 54111A 75Ω output	+12 dBm	+10 dBm
54117A, 54119A, 54128A, 54130A, 54131A, 54136A, 54137A, 54147A	+10 dBm	+7 dBm
54154A, 54161A, 54163A, 54169A,	+4	+1
54177A	+1	–2

Step 3. Set Channel 1 to measure POWER and turn Channel 2 off.

Step 4. Use a detector to measure the power out at the front panel and press Auto Scale key.

Step 5. If there is clipping showing on the display and Leveled LED is flashing or lit constantly, perform ALC adjustment (Chapter 6, paragraph 6-10 or 11, depending on model).

Step 6. If previous step does not correct the fault condition, replace Down Converter (Chapter 7, paragraph 7-15 through -18, as appropriate for model), and perform ALC adjustment (Chapter 6, paragraph 6-8).

Step 7. If previous step does not correct the fault condition, replace A6 ALC PCB (Chapter 7, paragraph 7-3), and perform ALC adjustment.

For 54117A through 54177A:

Troubleshooting Procedures

Step 1. Reset 541XXA to factory default setup.

Step 2. Set output power to 2 dB above factory default setting.

Step 3. Set Channel 1 to measure POWER and turn Channel 2 off.

Step 4. Use a detector to measure the power out at the front panel and press Auto Scale.

Step 5. If the display is clipped and the Leveled LED is flashing or lit constantly above 2GHz, perform ALC adjustment.

Step 6. If previous step does not correct the fault condition, replace Directional Coupler (Chapter 7, paragraph 7-15 through -20, as appropriate for model), and perform ALC adjustment.

Step 7. If previous step does not correct the fault condition, replace A6 ALC PCB (Chapter 7, paragraph 7-3), and perform ALC adjustment.

Harmonics and Spurious Problems

Symptoms:

- Excessive Harmonics and Spurious.

For 54107A, 54109A, or 54111A:

Troubleshooting Procedures

Step 1. Replace A5 YIG Driver PCB (Chapter 7, paragraph 7-3) and perform YIG Driver adjustment procedure (Chapter 6, paragraph 6-4).

Step 2. If previous step does not correct the fault condition, replace Down Converter (Chapter 7, paragraph 7-15 through -18, as appropriate for model), and perform perform YIG Driver adjustment procedure (Chapter 6, paragraph 6-4) and ALC adjustment procedure (Chapter 6, paragraphs 6-10 or 6-11, as appropriate).

Step 3. If the fault condition still exists, call Customer Service for assistance.

For 54119A through 54136A:

Troubleshooting Procedures

Step 1. Replace A5 YIG Driver PCB and perform YIG Driver adjustment procedure (Chapter 6, paragraph 6-5).

Step 2. If the fault condition still exists, call Customer Service for assistance.

For 54117A, 54137A through 54177A:

Troubleshooting Procedures

Step 1. Replace A5 YIG Driver PCB and perform YIG Driver adjustment procedure.

Step 2. If previous step does not correct the fault condition, replace Switch Filter Module Assembly (Chapter 7, paragraph 7-15 through -18, as appropriate for model).

Step 3. If the fault condition still exists, call Customer Service for assistance.

YIG Oscillator Problems

Symptoms:

- Low output power level.

Troubleshooting procedure

Step 1. Reset 541XXA to factory default setup. For 54117A, 54147A, 54161A, 54169A, 54177A, set start frequency to 2 GHz.

Step 2. Disconnect YIG output cable from YIG Oscillator output.

Step 3. Use a detector to measure the YIG Oscillator power output.

Step 4. Verify the minimum power output of the YIG Oscillator. The minimum power level should be as shown in Chapter 4, Figures 4-18 through 4-21.

Step 5. If output power is lower than the expected power level, measure the signal and bias voltages to the YIG Oscillator. Voltages should be as shown below for the two different type YIG oscillators.

CAUTION

It is dangerous to measure voltages directly on the YIG connector PCB. We recommned that Test points be used where possible.

YIG Oscillator, not 2 to 20 GHz

Control Signal	Location	Value*
+15V Bias	YIG Assembly Connector	+15V
–5V Bias	YIG Assembly Connector	–5V
FM Coil Signal**	A5 PCB, TP1 (reference TP2)	–10V to +10V
Main Coil Tuning Ramp	A5 PCB, TP5 (reference TP4)	0V to +10V

* All values ±0.5V, unless noted.
** Set WIDTH to <40 MHz.

2 to 20 GHz YIG Oscillator

Control	Location	Value
+15V Bias	A4/J3 Pins 4 & 3 (Ground)	+15V ±1.0V
–5V Bias	A4/J3 Pins 1 & 3 (Ground)	–5V ±0.5V
+22V Heater	A4/J3 Pins 2 & 3 (Ground)	+22V ±2.0V
+8V 2-8.4GHz	A19/A23 TP 7 & 5 (Ground)	+8V ±0.16V
+8V 8.4-20GHz	A19/A23 TP 8 & 5 (Ground)	+8V ±0.16V
+6V Bias	A19/A23 TP 10 & 5 (Ground)	+6V ±0.06V
FM Coil Signal**	A5 PCB, TP1 (reference TP2)	–10V to +10V
Main Coil Tuning Ramp	A5 PCB, TP5 (reference TP4)	0V to +10V

Step 6. If the voltages are correct, replace YIG Oscillator (Chapter 7, paragraph 7-15 through -20, as appropriate for model).

Step 7. If the voltages are incorrect, replace A5 PCB (Chapter 7, paragraph 7-3).

Residual FM Problems

Symptoms:

- Excessive residual FM.

Troubleshooting Procedure

Step 1. Replace A5 PCB (Chapter 7, paragraph 7-3).

Step 2. If previous step does not correct the fault condition, replace YIG Oscillator (Chapter 7, paragraph 7-15 through -20, as appropriate for model).

Step 3. If the fault condition still exists, call Customer Service for assistance.

CRT Monitor Problems

Symptoms:

- Distorted display
- No display

Troubleshooting procedures

Step 1. Measure +12V power supply voltage across pins 10 and 11 of A9J2. (For location, refer to Table 3-8 and associated figure on page 3-27).

Step 2. If +12V is not present, refer to the troubleshooting procedure for a Power Supply problem.

Step 3. If +12V is present, either perform the CRT adjustment procedures as described in Chapter 6, paragraph 6-15 (distorted display), or replace the CRT monitor assembly as described in Chapter 7, paragraph 7-10 (no display).

Step 4. If the previous steps do not correct the fault condition, replace A8 Graphic Processor PCB (Chapter 7, paragraph 7-3).

Step 5. If the fault condition still exists, call Customer Service for assistance.

Power Supply Problems

Symptoms:

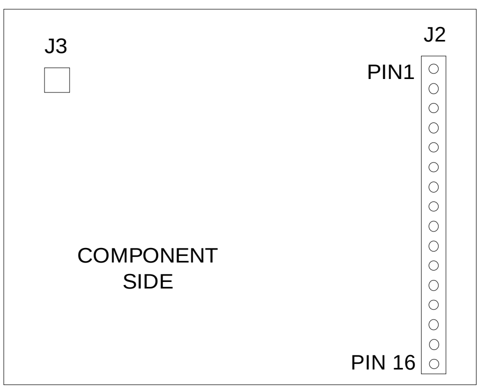
- No indication of power on.
- Front Panel LED's turn on and off periodically.
- Monitor has no display.
- No microwave power above 20 GHz for 54154A thru 54177A. See trouble shooting for ad-dtional PSU.

Troubleshooting Procedure for main A9 Power Supply PCB

Step 1. Clean the rear panel fan filter, check the fuse and verify the voltage selector setting.

Step 2. Turn unit on and verify LED on power supply mother board is off.

Step 3. If LED is flashing, go to Step 6.



A9 Power Supply Motherboard Connector Location & Orientation

Table 3-8. *Power supply Voltages*

Nominal Voltage	Measure: A9J2 Pin No.	Reference: A9J2 Pin No.	Voltage Value
+5	2, 4	1, 3	+5V ± 0.5
+12	12, 11	10, 14	+12V ± 0.5
+15	6, 7	8, 16	+15V ± 0.5
–15	9	ground	–15V ± 0.5
–18	15	ground	–18V ± 0.5
+22	13	ground	+22V ± 0.5

Step 4. Verify power supply voltages per Table 3-8 and associated figure.

Step 5. If voltages are incorrect, go to next step.

- Replace power supply assembly (Chapter 7, paragraph 7-9).

Troubleshooting Procedure for Rear Panel Mounted PSU Module

NOTE

This PSU only installed on 54154A through 54177A. The +8 and +10 voltages it generates are used only by the frequency doubling and quadrupling microwave components mounted on the RF deck.

Confirm the voltages on motherboard connector A4J23 are as shown below:-

Nominal Volts	Measure: A4J23 Pin No.	Reference: A4J23 Pin No.	Voltage Value
–15	1	3	–15 ±1.0
–5	2	3	–5 ±0.25
+10	4	3	+10 ±0.5
+8	6	3	+8 ±0.4

Measurement Channel Problems

Symptoms:

- Input connector unstable.
- Noise floor unstable.

Troubleshooting Procedure

Step 1. Replace A3 PCB (Chapter 7, paragraph 7-8) and perform Signal Channel Adjustment Procedure (Chapter 6, paragraph 6-3 and 6-4).

Step 2. If the fault condition still exists, call Customer Service for assistance.

Symptom:

- One of the inputs does not measure

Troubleshooting Procedure

Step 1. Replace A3 PCB and perform Signal Channel Adjustment Procedure.

Step 2. If previous step does not correct the fault condition, replace A5 PCB (Chapter 7, paragraph 7-3).

Step 3. If the fault condition still exists, call Customer Service for assistance.

Chapter 4 Functional Description

Table of Contents

Chapter 4 Functional Description

4-1 INTRODUCTION

This chapter provides descriptions of the functional operation of the major assemblies contained in each of the models of the 541XXA series Network Analyzers. The operation of each of the major circuit blocks is described so that the reader may better understand the function of the major assembly as part of the overall operation of the 541XXA. (The CRT monitor assembly is not covered in this chapter — this assembly is replaced as an entire unit.)

4-2 OVERVIEW OF SERIES 541XXA SYSTEMS

Sixteen models comprise the 541XXA Network Analyzer series. The RF models (Table 4-1) cover a frequency range of 1.0 MHz to 3.0 GHz. The microwave models cover a frequency range of 10 MHz to 50 GHz.

Table 4-1. *541XXA Model Frequency Ranges*

Model Group	Model	Frequency Range (GHz)	Output Power Without Attenuator (dBm)	Output Power With Attenuator (dBm)
RF	54107A	0.001 to 1.5	+12	+10
	54109A	0.001 to 2.2	+12	+10
	54111A	0.001 to 3.0	+12	+10
Microwave	54117A	0.01 to 8.6	+10	+7
	54119A	2.0 to 8.6	+10	+7
	54118A	8.0 to 12.4	+10	+7
	54131A	10.0 to 16.0	+10	+7
	54130A	12.4 to 20.0	+10	+7
	54136A	17.0 to 26.5	+10	+7
	54137A	2.0 to 20.0	+10	+7
	54147A	0.01 to 20.0	+10	+7
	54154A	2.0 to 32.0	+4	+1
	54161A	0.01 to 32.0	+4	+1
	54163A	2.0 to 40.0	+4	+1
	54169A	0.01 to 40.0	+4	+1
	54177A	0.01 to 50.0	+1	–2

The frequency range of measurements that can be made by each model is determined by the signal source (Table 4-1) and by the SWR Autotester and/or RF detector(s) used with the analyzer section of the 541XXA. The frequency ranges and characteristics of ANRITSU SWR Autotesters and RF detectors for series 541XXA systems are described fully in the 541XXA Operation Manual.

The CW frequency accuracy of the signal sources of the RF models is ±100 kHz (±200 kHz below 10 MHz). The CW frequency accuracy for the microwave models is ±200 kHz.

The analyzer section of the 541XXA is normally equipped with two measurement channels (A and B) as standard. The measurement range of each channel is +16 dBm to –63 dBm. An additional channel (R) is available as an option. The R channel is equal in performance to channels A and B and may be used as a reference channel when performing ratio measurements. For a detailed description of the characteristics and specifications for all 541XXA models, refer to the 541XXA Operation Manual.

4-3 541XXA MAJOR FUNCTIONAL BLOCKS

The major circuit blocks that comprise a 541XXA system are shown in Figure 4-1. As shown in the figure, the circuitry for each block may be located on multiple printed circuit boards, or assemblies, that are located throughout the 541XXA. Refer to Figure 4-1 while reading the functional descriptions of these circuit blocks on the following pages.

Central Processor

The central controller is the heart of the 541XXA and coordinates *all* of its functions. This controller is a 32-bit microprocessor that is mounted on the A7 CPU PCB. It directly or indirectly controls all measurement functions, display functions, and any input/output functions that are being performed by the 541XXA. It is directly linked via a dedicated data and address bus to the A8 Graphics System Processor PCB, the A6 ALC/Frequency Instruction PCB, the A5 YIG Driver/Signal Channel Interface PCB, the A3 Signal Channel PCB, and the A1/A2 Front Panel PCB's.

541XXA User Interfaces

The standard operator-interfaces to the 541XXA central processor are the front panel control keys and the function menus displayed on the internal CRT monitor. The control keys, indicator LED's, and associated circuitry are located on the A1 and A2 PCB's.

GPIB operation adds interface and control circuitry for the IEEE-488 Interface Bus (GPIB) to the A7 PCB. This operation allows the 541XXA internal processor to be controlled remotely by an external computer/controller running a suitable operating program. The over 400 device-specific GPIB commands recognized by the 541XXA software are described and explained in the 541XXA Series Network Analyzer GPIB User's Guide.

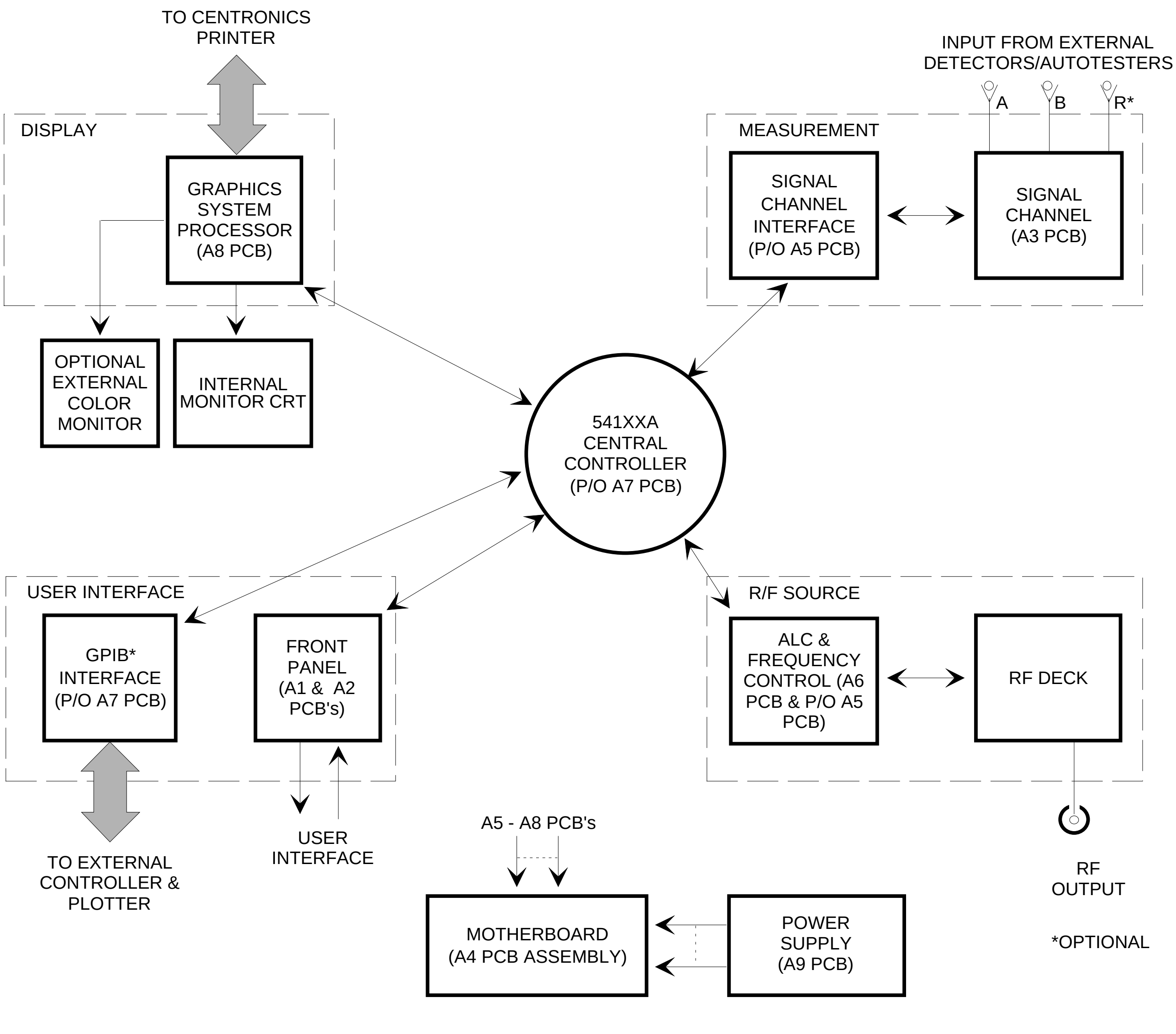


Figure 4-1. *Overall Block Diagram of Typical 541XXA Network Analyzer*

Graphics Processor Sub-System

The graphics processor, which is located on the A8 Graphics System Processor PCB, generates the various elements that make up the screen display on the internal VGA monochrome monitor. Similarly, it produces the screen display signals that drive an external VGA color monitor. It also formats and controls the output to the Centronics printer interface.

The graphics processor is controlled by the graphics system processor, which is a dedicated microprocessor located on the A8 PCB. The functions of this controller (and subsystem) are controlled and coordinated indirectly by the A7 Central Processor PCB using high level commands.

RF Power Output and Frequency Control

The output frequency and power level of the 541XXA signal source are controlled by the central controller via control latches and DACs located on the A6 or A24 ALC/ Frequency Instruction PCB. (The A24 PCB is used with 54154A through 54177A.) The ALC level control circuits on this PCB generate analog control signals that are fed to the RF deck. For microwave models, the Control Modulator produces the desired output power level. For the RF models, the control modulator in the Down Converter performs this function.

A portion of the RF output is detected by an internal RF detector. The detector output signal is used as feedback to the ALC circuits to maintain the desired output level at all output frequencies. Option 6 adds a rear panel External ALC Input connector. This connector allows the use of an external RF detector for leveling.

The frequency control information is converted to an analog signal on the A6/A24 PCB. It then goes to the YIG driver circuitry located on the A5 YIG Driver/Signal Channel Interface PCB. There, these circuits generate the appropriate control signals that cause the YIG tuned-oscillator to produce the desired output frequency.

The YIG-tuned oscillator, Control Modulator, Directional Coupler, and other devices that generate and control the signal source RF output signal are located on the RF deck assembly. This assembly is mounted on the right hand side of the 541XXA. It can easily be removed as a complete unit for servicing. The functioning of the RF deck is explained in detail in later paragraphs.

Measurement Channel Signal Processing

The low-level analog signals from the external SWR Autotester(s) and/or detectors go from the front panel input connectors to the A3 Signal Channel PCB. This PCB is positioned behind the input connectors and underneath the RF deck in a screened metal cage.

The standard A3 PCB is multiplexed to provide two measurement channels, A and B. This circuitry is basically an analog signal conditioner that amplifies and filters the DC signal voltage(s) from the front panel input(s).

Option 5 adds a third measurement channel (R), which can serve as a reference channel. This channel is totally separate from the main measurement channel. This allows for accurate ratio measurements.

The outputs from the main and (optional) R channel circuits go to the A5 YIG Driver/Signal Channel Interface PCB. The A5 PCB multiplexes these signals onto the input of a 12-bit analog-to-digital converter. The resultant digital information goes to the A7 Central Processor PCB. There, it is processed into finished measurement data to be displayed or printed.

A9 Power Supply Assembly

The A9 Power Supply Assembly produces all of the DC voltages used by the 541XXA printed circuit boards, RF deck components, rear panel fan, and CRT monitor assembly. The operation of the power supply is explained in detail in later paragraphs.

Motherboard and Rear Panel

The A4 Motherboard Assembly and associated cables provide the data bus interconnections, signal paths, and DC voltage buses that link all of the 541XXA printed circuit boards and other major assemblies.

The rear panel includes connectors for the External VGA Monitor, GPIB/IEEE-488 Instrument Interface, Centronics Parallel Printer Interface, External ALC Input, and Horizontal (Sweep) Output. The cables associated with these connectors go to the A4 Motherboard, which serves as a distribution medium. The wiring/cable assembly associated with the rear panel line voltage module connects it directly to the power supply module.

4-4 A7 CENTRAL PROCESSOR PCB

The A7 Central Processor PCB (Figure 4-2) is an IBM AT compatible computer fitted onto a single circuit board. The A7 PCB also contains the circuits for the IEEE-488/GPIB inteface bus, the floppy drive controller, and three 8-bit I/O ports. One of the I/O ports provides 24 volt relay drive signals to drive the optional 70 dB attenuator. One standard I/O port is used to drive the Switched Filter, which is part of the RF deck on models 54117A, 54119A, and 54137A through 54177A.

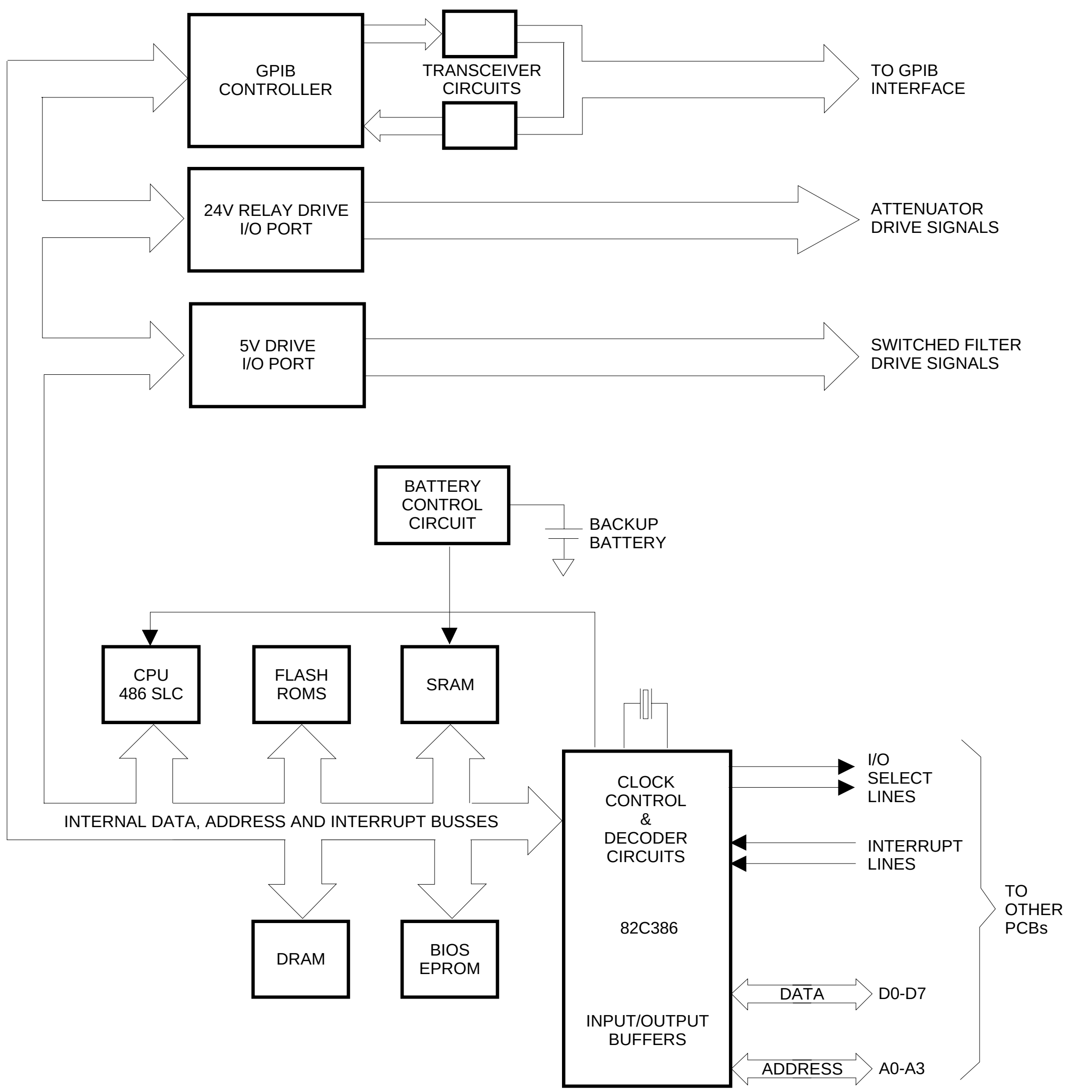


Figure 4-2. Block Diagram of A7 Central Processor PCB

Central Processor Circuits

The A7 Central Processor PCB uses a 486SLC processor running at 25 MHz. It also uses a 82C386 ASIC that provides a number of timing and control address decoding functions. The 82C386 ASIC also includes a number of PC/AT compatible I/O peripheral circuits.

The A7 PCB may also contain an 80387SX math coprocessor running at 25 MHz, if option 7 is installed.

The following three type of memory on the A7 PCB are accessible by the central processor:

- 2 MB of DRAMs for program operation.
- 256KB of SRAMs (with battery backup) for storing trace data, stored setups, and unit identification information.
- 1 MB of Flash ROMs for storing operating software.

When the 541XXA is powered up, the central processor is reset. It then performs the following initial operations:

- It runs the instrument self-test routine.
- It reads the instrument model identification and configuration from the A6/A24 PCB.
- It down-loads the display software to the A8 Graphics System Processor PCB.
- It sets up the unit with the last used front panel control configuration.
- It starts normal instrument operation.

GPIB Circuits

Two GPIB data bus transceiver chips and a GPIB controller chip comprise the GPIB interface circuits (Figure 4-2). The transceiver chips connect to the rear panel GPIB connector via the A4 Motherboard and associated connector cable assembly. The central microprocessor controls the GPIB controller and passes data to and from it via the internal data, address, and interrupt buses on the A7 PCB.

4-5 A8 GRAPHICS SYSTEM PROCESSOR PCB

The A8 Graphic System Processor (GSP) PCB (Figure 4-3) is an intelligent subsystem that is loosely controlled by the A7 Central Processor PCB. It produces the video signals for the internal CRT monitor screen display and for the external VGA monitor interface. It also produces the data and control signals for the Centronics printer interface. There are no adjustments on this PCB.

Major GSP Circuits

The major circuit block on the A8 PCB are

- *The Graphics Controller Chip (34010):* This controller interprets the commands from the A7 PCB Central Processor and produces appropriate command signals and data streams that produce the desired CRT monitor display or printer output. The GSP controller communicates with the GSP memory, video output circuits and printer interface circuits via the internal GSP Data Bus (Figure 4-3).

- *Clock Signal Generation:* The 40 MHz clock chip produces the INCLK signal that is used by

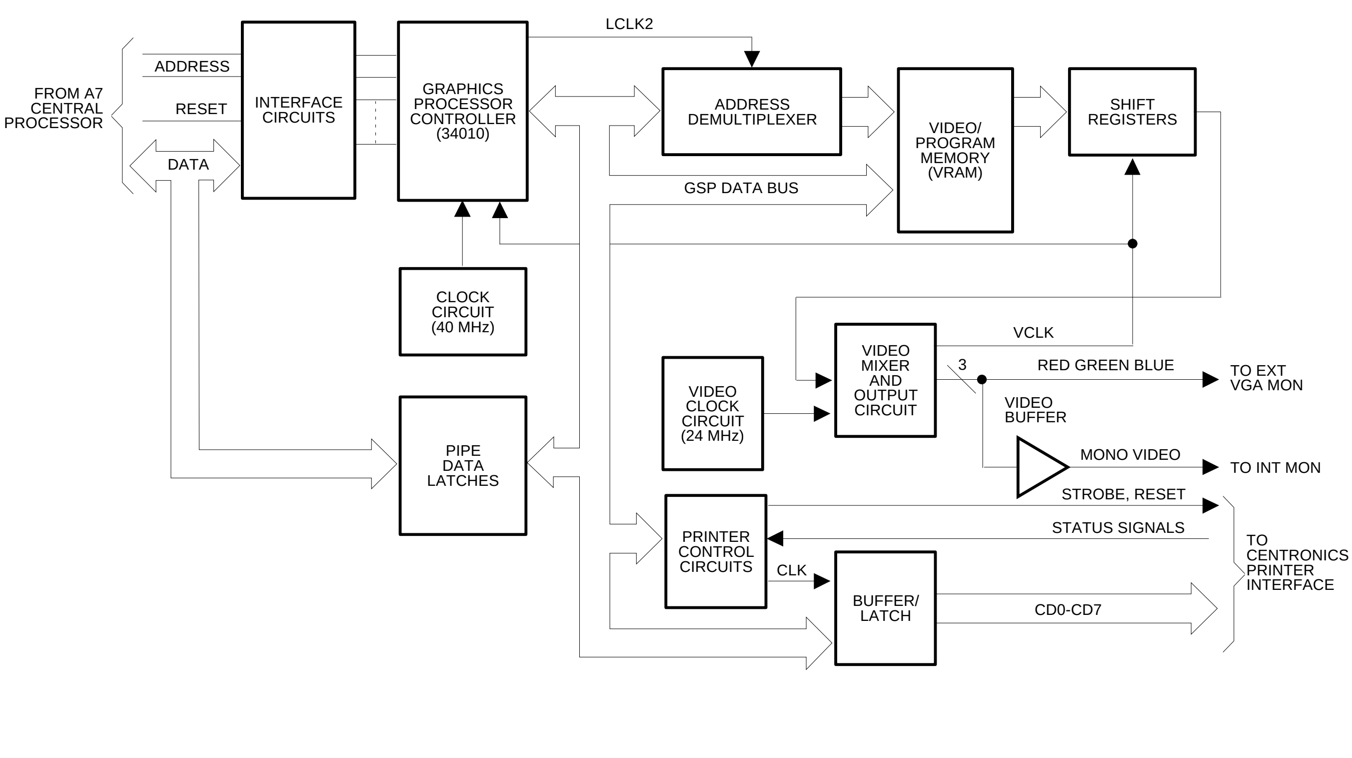


Figure 4-3. *Block Diagram of A8 Graphics System Processor PCB*

the GSP controller to derive all program related timing signals. The controller divides this signal by eight to produce the LCLK2 signal that clocks data into and out of the GSP memory. The controller also produces other timing and control signals related to this clock.

The video clock oscillator and associated divider circuits produce the 6 MHz video clock signal,VCLK. This signal establishes the rate at which the video information is clocked from the GSP memory to the video output circuits.

NOTE

For troubleshooting, all program-related cycles should be observed synchronized to LCLK2 (test point 2). All video cycles should be observed synchronized to VCLK (test point 3).

- *Data Interface Circuits:* These circuits interface the GSP processor to the data and address bus lines from the A8 central processor. The graphics processing control program is down-loaded through this interface.

- *Data “Pipe”:* Two latches form a data pipe that allows direct communication from the A7 Central Processor PCB to/from the GSP processor via the GSP Data Bus (Figure 4-3).

- *Video/Program Memory:* Four 256K x 4 Video Dynamic RAMs (VRAMs) comprise the memory for the GSP subsystem. This memory is used to store the GSP control program and the video data that will produce the CRT monitor screen display output.

- *Video Output Circuits:* Two shift registers, a video clock oscillator chip, a video mixer chip and a video amplifier/buffer circuit comprise the video output circuits. These circuits shift the video data out of the GSP memory and convert it into the Red, Green, and Blue signals for the VGA Monitor Interface and the mono-video signal for the internal CRT monitor.

- *Centronics Printer Interface:* A data buffer/latch, a printer interface controller chip and a portion of a data latch comprise the interface circuitry for the Centronics printer interface. This circuitry provides the formatted data, data strobe, and control signals for the printer interface. It also receives and stores the status signals from the printer.

GSP Controller Operation

In operation, the GSP controller receives the graphics processing program, which was down-loaded to it from the A7 Central Processor PCB at power-up. The GSP controller stores the GSP control program in the *high* memory locations of the GSP Video/ Program Memory. It starts it on command from the central processor. (Low memory locations are used for video data.) The control program is run continuously until the 541XXA is powered-down.

The GSP control program controls all aspects of the operation of the GSP subsystem, which include:

- Timing of communication operations from/to the central processor
- Setting up the CRT scanning
- Generating and maintaining the graphic elements of the CRT display
- Formatting and controlling the data output to the Centronics printer interface

A preliminary step performed by the program is the setting up of timing information for the video output signals. This information places certain control codes into the A8 PCB internal registers. (Upon execution, the contents of these registers are processed in the same manner as memory location data.) These codes control internal clock dividers that generate the required Horizontal and Vertical Synchronization signals for the output video signal. The Video blanking signal is also generated in this manner. The timing of these signals is compatible with the VGA Standard, so that standard VGA monitors may be used with the 541XXA (rear panel EXTERNAL MONITOR interface connector).

The GSP control program causes the GSP controller to wait for instructions and data that are sent to it from the central processor via the pipe interface (Figure 4-3). The commands used by the central processor to control the GSP are high level commands such as **draw line** and **write text**. The GSP controller translates these commands into primitive instructions which it can directly execute. It then performs the necessary sub-tasks to produce the desired results.

For example, the command **draw line** performs the following operations: It generates primitive commands that instruct the GSP controller to produce a series of memory fetch cycles from the video data stored in the *low* memory locations of the GSP memory. After each fetch, it modifies the video data and returns it to memory. This process alters the contents of video memory. Memory is altered such that when its contents are displayed on the CRT monitor, the desired line appears. The GSP controller performs these graphic memory fetch cycles interleaved with control program fetches from the *high* memory locations of the GSP memory.

The GSP control program does not control the overall content of the CRT monitor display — it produces graphic elements and puts them into video memory as instructed by the central processor. The central processor, itself, controls the content and placement of the graphic elements that make up the display. After the video information for a complete screen display has been built up in memory (as explained above), it is shifted out to the video output circuits.

Printer Interface Operation

The GSP processor sends formatted printer output data and control signals to the printer interface circuits via the GSP data bus. The printer interface controller chip provides the data strobe that clocks the output data from the GSP bus into the data buffer/ latch (Figure 4-3). It also provides the LSTB (strobe) and PRINTER RESET signals to the printer. Along with associated data latch circuits, it receives the printer status signals and sends them to the GSP controller via the GSP bus.

Video Output Circuit Operation

The 24 MHz signal from the video clock oscillator is divided down and gated by divider circuits and the video mixer chip to produce the video dot-rate clock signal, VCLK. This signal, and other clock signals derived from it, are used to transfer the video data out of the GSP memory and shift it into the video mixer chip. This chip converts the video data signals into a combination of Red, Green, and Blue signals that are output to the External VGA Monitor interface.

These signals are mixed to produce a composite monochrome signal. This signal then goes to the input of the video buffer amplifier. This amplifier boosts the signal to the 3 to 5V level required to drive the internal CRT monitor.

Internal CRT Monitor

The video and synchronization signals from the A8 Graphics System Processor PCB, along with the required DC power, go to the CRT monitor via a cable assembly that connects to the A4 Motherboard PCB. The monitor is not field repairable. It should be replaced with an exchange unit if defective.

NOTE

The adjustment potentiometers for these units are set at the factory and should require no further adjustment.

4-6 A6/A24 ALC/FREQUENCY INSTRUCTION PCB

NOTE
The Frequency/Instruction PCB is the A6 assembly in models 54107A through 54147A; it is A24 in 54154A through 54177A.

The A6/A24 ALC/Frequency Instruction PCB (Figure 4-4) generates control signals that

- Set the RF power output level of the 541XXA internal source to the value instructed by the A7 Central Processor.
- Maintain the RF output power level flat throughout the selected operating frequency range.
- Set the frequency of the internal source to the value instructed by the A8 Central Processor.
- Maintain the RF output frequency at the selected values.

In addition, the A6/A24 PCB contains circuits that allow the A7 Central Processor to read the 25 MHz and 500 MHz marker signals that are generated on the RF Deck. (This information is used to create frequency correction data that is fed back to the A6/A24 PCB.) It also contains a Unit Identification Circuit. This circuit is read by the A7 Central Processor at power-up to determine model type and configuration.

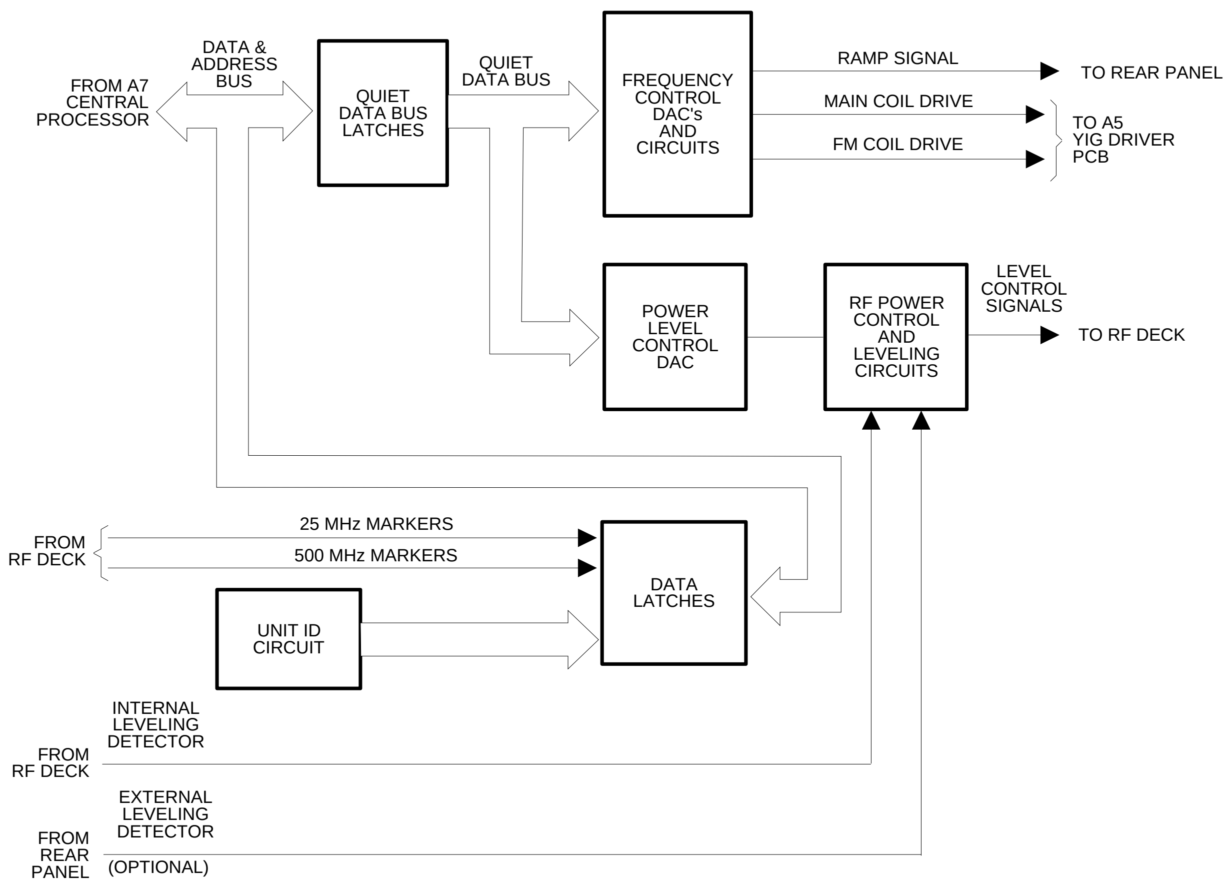


Figure 4-4. *Overall Block Diagram of A6 ALC/Frequency Instruction PCB*

ALC Circuit Operation

The ALC circuits control the RF power output level and flatness of the internal source. These circuits receive instructions and data from the A7 Central Processor PCB and convert them into a voltage that represents the desired output level. This voltage is converted into control currents that drive the PIN attenuator circuits located in the control modulator on the RF deck. These circuits attenuate the signal from the YIG-tuned oscillator to the desired level.

NOTE

The RF output level is controlled by the internal control modulator circuits located in the down converter in models 54107A, 54109A, and 54111A.

The source output is maintained at the desired level by the servo action of the ALC control circuits. These circuits use the output signals from detectors located in the down converter and directional coupler as negative feedback. Option 6 to the 541XXA provides a rear panel external ALC input connector for use with a suitable external RF detector. This feature allows the RF output to be leveled at points in the external test path instead of internal to the 541XXA.

ALC Circuit Groups

The circuit groups listed below comprise the A6 ALC. These circuits are described in following paragraphs. See block diagrams in Figure 4-4 and Figure 4-5 (on page 4-19).

- Power Level Set
- Control Modulator driver
- Down Converter Modulator Driver
- Internal Leveling
- External Leveling
- Quiet Data Bus

Power Level Set Circuits

The RF power level information from the A7 Central Processor PCB is transferred to the power control DAC and to the temperature compensation circuit DAC by the quiet data bus on the A6/A24 PCB (Figure 4-5). The input to the power control DAC is a frequency sweep voltage that is derived from the main coil and FM coil drive signals. The input to the temperature compensation circuit DAC is either the feedback voltage from the down converter thermistor or the directional coupler thermistor (as selected by the A7 Central Processor PCB).

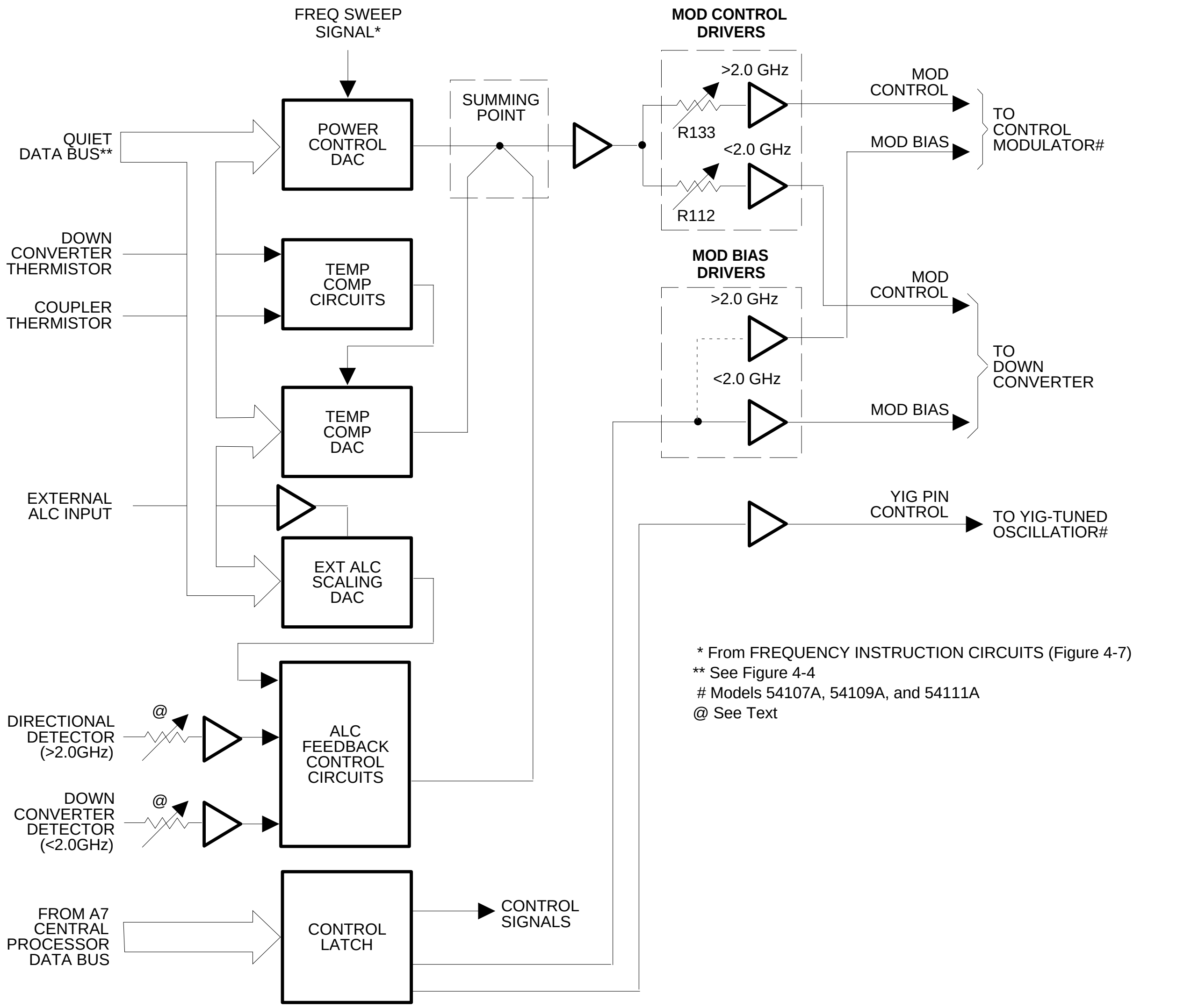


Figure 4-5. *Block Diagram of ALC Power Control Circuits*

The output voltages from the two DACs are summed with the feedback voltage from the internal (or external) ALC detectors to produce the ALC LEVEL control signal. This signal, which represents the desired RF output level, provides the input to the Control Modulator and Down Converter Modulator driver circuits.

Control Modulator Driver Circuits

The Control Modulator controls the RF output power level above 2.0 GHz. There are two circuits located on the A6/A24 PCB that drive the control modulator (Figure 4-5). The Mod Bias circuit drives the control modulator PIN switches used to switch the RF power on and off. The logical state of this circuit is controlled by commands from the A7 Central Processor PCB.

The second circuit, Mod Control, drives the control modulator PIN switches that control the RF power output level. This circuit is activated by commands from the A7 Central Processor PCB and controlled by the output of the power level set circuits. Potentiometer R133 controls the circuit bandwidth. It is adjusted during circuit alignment to assure that no oscillation of the driver circuit occurs.

Down Converter Modulator Driver Circuits

The down converter controls the RF output power level in models 54107A, 54109A, and 54111A. (The down converter also performs this function in models 54117A, 54147A, 54161A, 54169A, and 54177A for output frequencies below 2.0 GHz). The two A6/A24 PCB driver circuits that control the down converter PIN modulators are similar in operation to those described above for the Control Modulator (Figure 4-5). These circuits are selected by commands from the A7 Central Processor PCB as appropriate for the model and output frequency selected. Potentiometers R112 and R183 (A6 only) in the Mod Control driver circuit control the circuit bandwidth and offset of the feedback loop. They are adjusted during circuit alignment to assure that no oscillation of the driver circuit occurs.

YIG PIN Switch Driver Circuit

The YIG-tuned oscillators used in Models 54107A, 54109A, and 54111A contain a PIN switch circuit that attenuates the RF signal on and off. The YIG PIN Control driver circuit for this function is located on the A6/A24 PCB (Figure 4-5). Its logical state is switched by commands from the A7 Central Processor PCB.

Internal Leveling Circuits

The source RF output is leveled by a closed feedback loop. For microwave band models 54117A through 54177A, the ALC feedback signal is produced by a directional detector located on the RF deck. For models 54107A, 54109A, and 54111A, (and for models 54117A, 54147A, 54161A, 54169A, and 54177A at output frequencies below 2.0 GHz), the feedback signal is produced by a detector located in the down converter.

The internal ALC feedback signals are conditioned by two separate amplifier chains, one for above 2.0 GHz and one for below 2.0 GHz. The outputs of these circuits are switched to the ALC summing point amplifier by commands from the A7 Central Processor PCB, as appropriate for the model and output frequency selected.

The overall output RF power of the source is controlled by adjusting the amount of feedback supplied to the ALC loop by these amplifier chains. During circuit alignment, potentiometer R62 is used to adjust the upper power level output in the >2.0 GHz amplifier chain. The low power output is adjusted by R196. Potentiometer R56 is the high power output adjustment and potentiometer R190 is the low power output adjustment in the <2.0 GHz amplifier chain.

External Leveling Circuits

The signal voltage from the (optional) rear panel EXTERNAL ALC INPUT connector is fed to signal conditioning circuits that include an absolute value circuit. The absolute value circuit ensures that a signal with the correct polarity is fed to the input of the ALC Scaling DAC.

To allow external RF detectors with different voltage outputs to be used, a method of calibrating the external ALC input signal is required. This operation is controlled by commands from the A7 Central Processor PCB, as follows:

- The external detector feedback signal from the scaling DAC is compared with the feedback voltage generated by the internal ALC detector.
- The central processor causes the External ALC Scaling DAC to adjust the amplitude of the external detector signal until it is equal to the internal detector voltage.
- The resultant external ALC signal is then switched to the ALC summing point amplifier.

“Quiet” Data Bus Circuits

This bus is used to transfer data between the A6/A24 PCB data latch circuits and the Frequency Instruction DAC’s and Power Level Control DAC’s (Figure 4-4). The quiet data bus is buffered from the A7 Central Processor PCB Data Bus to insulate these circuits from noise on the main bus.

Frequency Instruction Circuits Operation

The frequency instruction circuits located on the A6/A24 PCB control the frequency of the 541XXA RF output signal. These circuits receive instructions and data from the A7 Central Processor PCB. They then convert them into control signals for the YIG-tuned oscillator main coil and FM coil drive circuits. These circuits are located on the A5 YIG Driver/ Channel Interface PCB (Figure 4-7 on page 4-25).

The two main output signals from the frequency instruction circuits are Main Coil Sweep and FM Coil Sweep. Each is a composite signal that normally has variable DC and ramp elements. (The ramp element is not present for CW operation.) These circuits also produce a sweep ramp signal for the rear panel HORIZONTAL OUTPUT connector and a frequency compensation signal for the ALC control circuits.

Frequency Instruction Circuit Groups

The four circuit groups that comprise the frequency control group are RAMP DAC, WIDTH DAC, START DAC, and ERROR DAC. Each circuit group contains a 12-bit DAC and associated operational amplifiers and control circuits (Figure 4-7). Each of these circuits receive data from the A7 Central Processor PCB via the A6/A24 PCB quiet data bus (Figure 4-4). The control signals for these circuits are produced by A6/A24 PCB data latches that are controlled by the Central Processor data bus.

RAMP DAC Circuits

The A7 Central Processor PCB sequentially programs the RAMP DAC, thereby producing a ramp output signal containing 4,000 steps. This ramp signal goes to the WIDTH DAC, where it is further modified to produce either the Main Coil Sweep signal or the FM Coil Sweep signal. The ramp signal is also buffered and fed to the rear panel Horizontal Output connector.

The signal produced by the RAMP DAC always has the same voltage range (number of steps) when the 541XXA is sweeping, regardless of the selected sweep width. The A7 Central Processor PCB may halt the update of the DAC at any time (e.g., when dealing with interrupts, etc.). This will produce steps of varying duration, which will produce a ramp with a shape that is irregular rather than smooth and continuous. However, this does not effect the displayed sweep in any way.

WIDTH DAC Circuits

The input to the WIDTH DAC is the ramp signal from the RAMP DAC. The WIDTH DAC output is a ramp signal. The ramp magnitude is scaled by the data that it receives from the A7 Central Processor PCB. Thus the ramp signal, as controlled by the central processor, produces a sweep signal that tunes the YIG oscillator over the required range.

Example: To produce a sweep over half the maximum range of the 541XXA , the A7 Central Processor PCB programs the WIDTH DAC to output a ramp with an amplitude that is half of the DACs' maximum range. The input to the WIDTH DAC is a 0V to –10V ramp; therefore, the output signal will be a 0V to +10V ramp.

For sweep widths greater than 40 MHz, the drive signal goes to the main coil of the YIG-tuned oscillator. For sweep widths of 40 MHz or less, the drive signal goes to the FM coil of the YIG-tuned oscillator. This signal switching is performed by analog switches that transfer the WIDTH DAC output signal to either the Main Coil Sweep or FM Coil Sweep signal output circuits (Figure 4-7). These switch circuits are controlled by commands from the A7 Central Processor PCB.

A proportion of the WIDTH DAC output signal goes to the 25 MHz marker generator circuits located on the RF deck. This signal ensures that the marker width remains constant throughout the full frequency range of the unit.

START DAC Circuits

The output of the START DAC is a 0 to 10 Vdc voltage that is controlled by the A7 Central Processor PCB. This voltage is summed with the WIDTH DAC ramp signal at the input to the Main Coil Sweep circuit. It thereby controls the dc component of the composite Main Coil Sweep signal. This allows the A7 Central Processor PCB to set the center frequency of the sweep range to the desired value.

ERROR DAC Circuits

The output of the ERROR DAC is a dc voltage that is used as a frequency source lock error correction signal. The A7 Central Processor PCB sets the magnitude and polarity of this signal using error information obtained by processing the 500 MHz and 25 MHz marker read signals from the A6/A24 PCB.

The output of the ERROR DAC is a –10 to +10 Vdc voltage. This voltage goes through a summing resistor to the input of the FM Coil Sweep signal output circuit. It thereby controls the dc component of the composite FM Coil Sweep signal. This dc signal causes the YIG FM coil to produce a frequency offset that cancels the frequency error. For sweep widths of 40 MHz or less, the WIDTH DAC ramp signal is summed with the error signal at the input of the FM Coil Sweep signal output circuit.

500MHz and 25 MHz Markers Read Circuits

The 500 MHz and 25 MHz marker signals generated by the marker modules on the RF deck are read by the encoder circuits located on the A6/A24 PCB. The outputs of these A6/A24 PCB circuits are stored in a data buffer latch that is read by the A7 Central Processor PCB. This information is used by the Central Processor to generate frequency-source-lock error correction data. This data is fed back to the ERROR DAC.

Unit Type Identification Circuit

This circuit consists of an 8-position jumper block (J3), a bank of eight pull-up resistors, and an 8-bit latch, as shown in Figure 4-6. An open jumper in any position will be sensed by the associated latch input as a logic-1 and a closed jumper will be sensed as a logic-0. The jumpers are configured at the factory to identify the unit model type and configuration. The outputs of the data latch are read by the A7 Central Processor PCB at power-up.

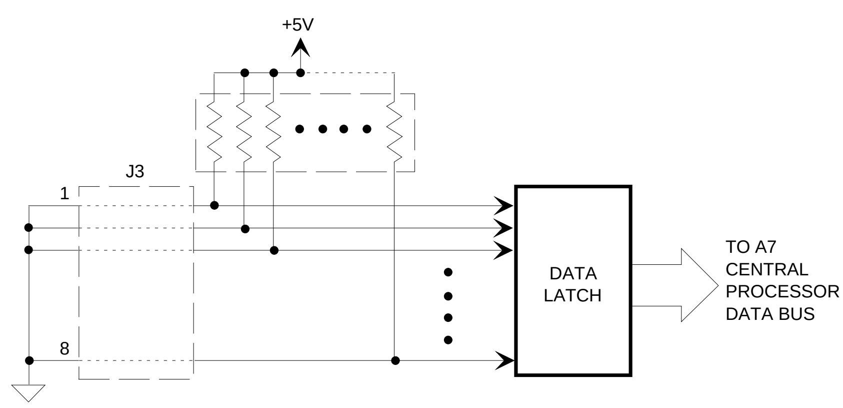


Figure 4-6. *Unit Type Identification Circuit*

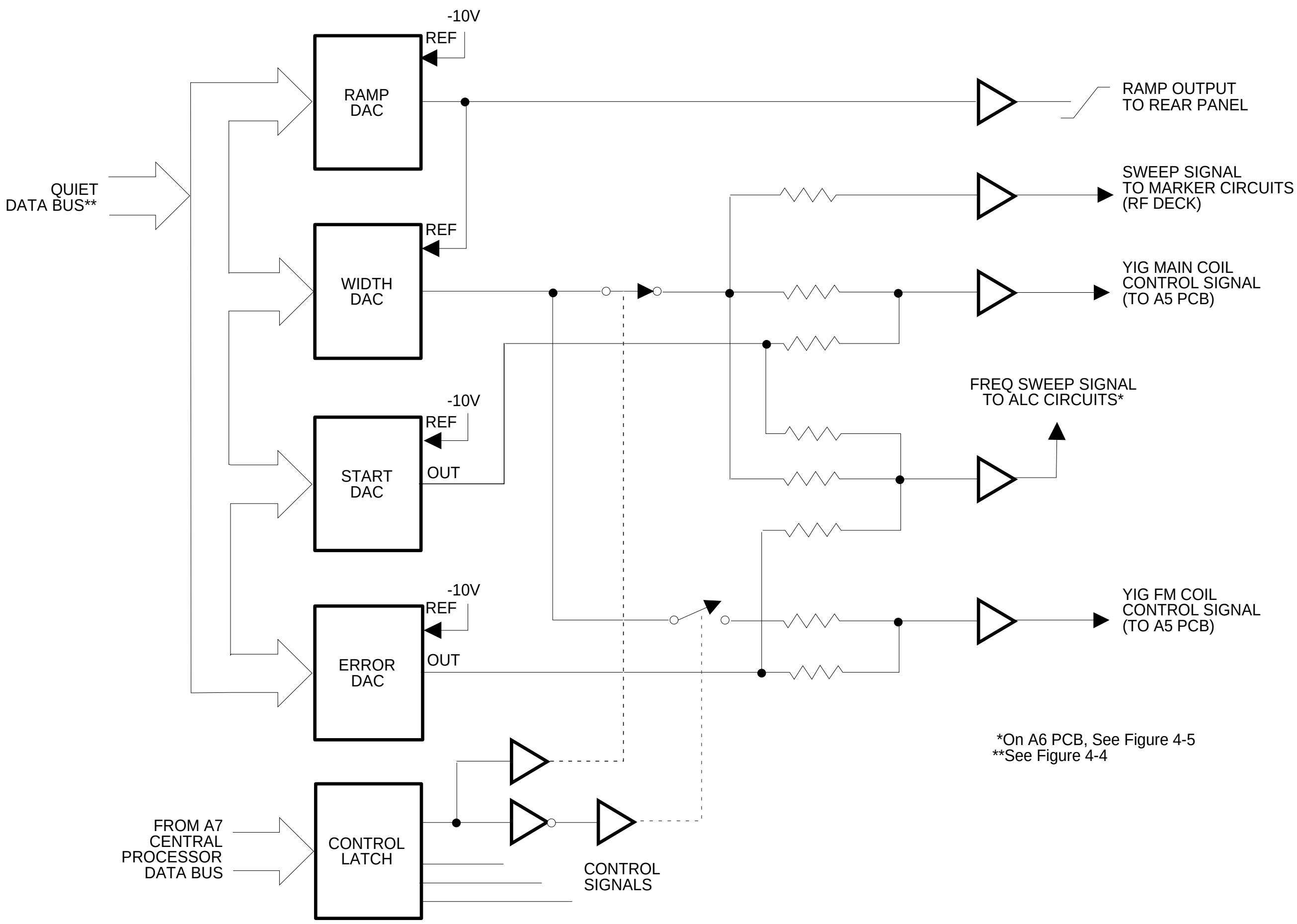


Figure 4-7. *Block Diagram of A6/A24 PCB Frequency Instruction Circuits*

4-7 A5 YIG DRIVER/ SIGNAL CHANNEL INTERFACE PCB

The A5 YIG Driver/Signal Channel Interface PCB contains two main circuits, the Main Coil Driver and the FM Coil Driver. These two circuits receive the YIG Main Coil and FM Coil control signals from the A6/A24 ALC/Frequency Instruction PCB and convert them into the drive currents for the YIG tuning coils.

The circuits that interface with and control the A3 Signal Channel PCB are also located on the A5 PCB. These circuits receive commands from the A7 Central Processor PCB and generate appropriate control signals to the A3 Signal Channel PCB. They receive the multiplexed measurement signal from the A3 Signal Channel PCB, digitize it, and send the resultant data to the A7 Central Processor PCB via the central processor data bus. They also process the status signals from the A3 PCB and send appropriate status signals back to the to the A7 Central Processor PCB. These circuits are described in later paragraphs in this chapter.

YIG Driver Operation

The YIG-tuned oscillator (YTO) requires current drive to its coils to create the magnetic fields that cause oscillation. The operating frequency of the YTO is controlled by adjusting the magnitude of the currents sent to these coils. The main coil of the YTO provides the main magnetic field and requires a drive current with a single polarity. The YTO can be swept over its entire frequency range by varying the magnitude of the main coil current in an appropriate manner.

The FM coil has a more limited frequency range and a higher sensitivity. It can be driven in either direction so that its magnetic field either augments or diminishes the main coil field. By this means fine control of the YTO output frequency is achieved.

The Main Coil Control and FM Coil Control signals from the A6/A24 ALC/Frequency Instruction PCB are voltages. The YIG Driver circuits on the A5 PCB provide the necessary voltage to current conversion (and power amplification) to drive the YTO coils. Both coil driver circuits are designed to drive floating loads.

Main Coil Driver Circuit

Figure 4-8 shows the YIG Main Coil driver and FM Coil driver circuits. The input to the main coil driver is the Main Coil Control signal from the A6/A24 PCB. This signal is a voltage in the range of 0 to –10V. The resultant output is a drive current that flows in one direction only.

When the 541XXA is in the CW mode, or is sweeping using the FM coil, the bandwidth of the Main coil driver is reduced by switching a low-pass filter into the driver circuit. This results in reduced noise and residual FM on the RF output.

When the 541XXA is sweeping using the FM coil, the rapidly changing field causes a voltage to be induced in the main coil. This effect (and the action of the low-pass filter) causes a frequency shift to occur. To counteract this, a linearization transformer couples some of the FM coil drive signal into the main coil driver circuit. This signal causes a field in the main coil that cancels out the frequency shift error.

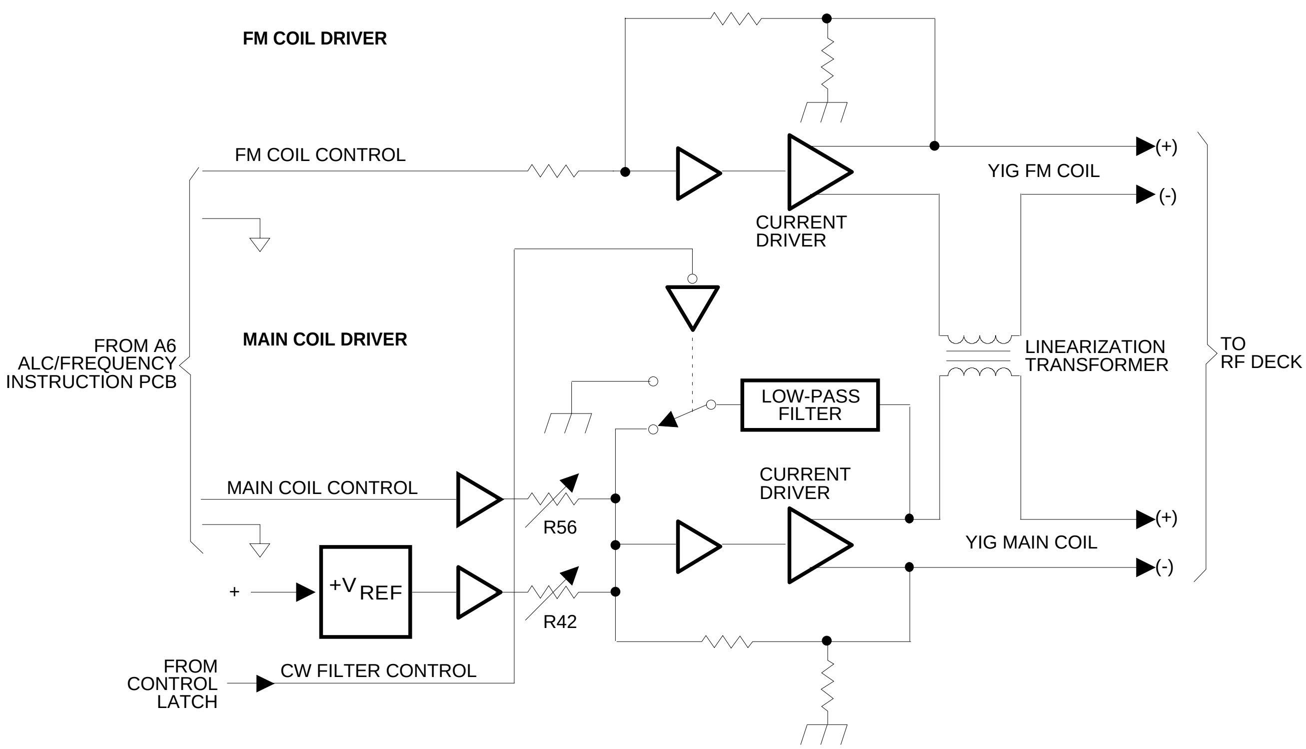


Figure 4-8. *Block Diagram of YIG Driver Circuits*

Potentiometer R4 provides adjustment of the YTO lower frequency limit, and potentiometer R2 provides adjustment of the total sweep range. These potentiometers are adjusted during circuit alignment of the unit.

To match the characteristics of the various YIG Driver assemblies used in different 541XXA models, the values of various coil driver components are different. This is reflected in the different part numbers of the A5 PCB's used (see Chapter 2).

The Main coil sensitivity of YTO varies somewhat from band to band but is of the order of 20 to 30 MHz per mA. The Main coil driver therefore must supply over 1.2 amperes when driving a high frequency YIG-tuned oscillator.

FM Coil Driver Circuit

The input to the FM coil driver circuit is the FM Coil Control signal from the A6/A24 PCB. This signal is a voltage in the range of +10 to –10V. The resultant output is a drive current that flows in either direction, depending upon the input signal.

The FM coil sensitivity of YTOs is in the range of 300 to 450 kHz per mA. The maximum frequency range covered is normally ±60 MHz. Therefore, the FM coil driver is required to supply up to ±200 mA maximum.

Signal Channel Interface Circuits

Figure 4-9 (page 4-29) is a block diagram of the A5 PCB signal channel interface circuits. The major circuit blocks are

- Sample-and-Hold
- Analog-to-Digital Converter
- Detector Recognition
- Address Decode
- Quiet Data Bus

Sample-and-Hold Circuits

There are two separate sample-and-hold circuits, one for the A/B channel measurement signal and one for the R channel measurement signal. Both circuits are identical. The ANALOG A/B input signal from the A3 Signal Channel PCB contains time multiplexed signals for the A and B channels (if both are active). They include the measurement signals, Log Conformity signals, and Temperature (detector thermistor) signals. (These signals are multiplexed by circuits on the A3 PCB under control of the A7 Central Processor PCB.) Similarly, the ANALOG R input signal contains the multiplexed signals for Channel R. This signal is active only if the 541XXA is equipped with Option 5, and the R Channel is selected as being active.

Both input signals are fed to the A5 PCB inputs via a shielded cable. Differential amplifiers are used in the circuit inputs to ensure good common-mode-noise rejection. The outputs of the sample-and-hold circuits are fed to the input of the Analog-to-Digital Converter (ADC). The ADC circuit converts only positive polarity signals (negative polarity signals are ignored). Therefore, the sample-and-hold circuits are designed to add a 100 mV positive offset to the measurement signal. The A7 Central Processor automatically subtracts this offset when processing the measurement signal data.

Analog-to-Digital Converter Circuit

The output of each sample-and-hold circuit is fed to the input of the Analog-to-Digital Converter circuit via an analog switch. These switches are controlled by the A7 Central Processor PCB and programmed so that only one switch is active at any given time. The 12-bit output of the ADC is stored by two data latches. It is then transferred to the A7 Central Processor PCB in two 8-bit bytes.

Detector Recognition Circuits

The A, B, and R Detector Sense signals from the A3 Signal Channel PCB are buffered and stored in a data latch that outputs to the quiet data bus. This allows the A7 Central Processor PCB to determine if a particular channel input has an RF detector or SWR Autotester connected. The three detector sense signals are also OR'd to produce a status signal that is read by the A7 Central Processor PCB before reading the output of the ADC. If this status signal is false (no input connected) an error interrupt occurs.

Address Decode and Data Latch Circuits

The A5 PCB address decoder circuits produce control signals and data strobes that control the various circuit functions on the A3 Signal Channel PCB and locally on the A5 PCB. These circuits decode the instrument address lines and I/O select lines from the A7 Central Processor PCB bus to produce the control signals and data strobes. The timing of these signals is controlled by the A7 Central Processor PCB.

Quiet Data Bus Circuits

The A3 PCB and A5 PCB communicate via a quiet data bus. This bus is also used to transfer data between circuits on the A5 and A3 PCBs and locally between circuits on the A5 PCB. The quiet data bus is buffered from the A7 Central Processor PCB Data Bus to ensure that the sensitive measurement circuits are insulated from any noise on the main bus. The operation of the quiet data bus is carefully controlled so that there is no data transfer or other activity while measurement signals are being processed.

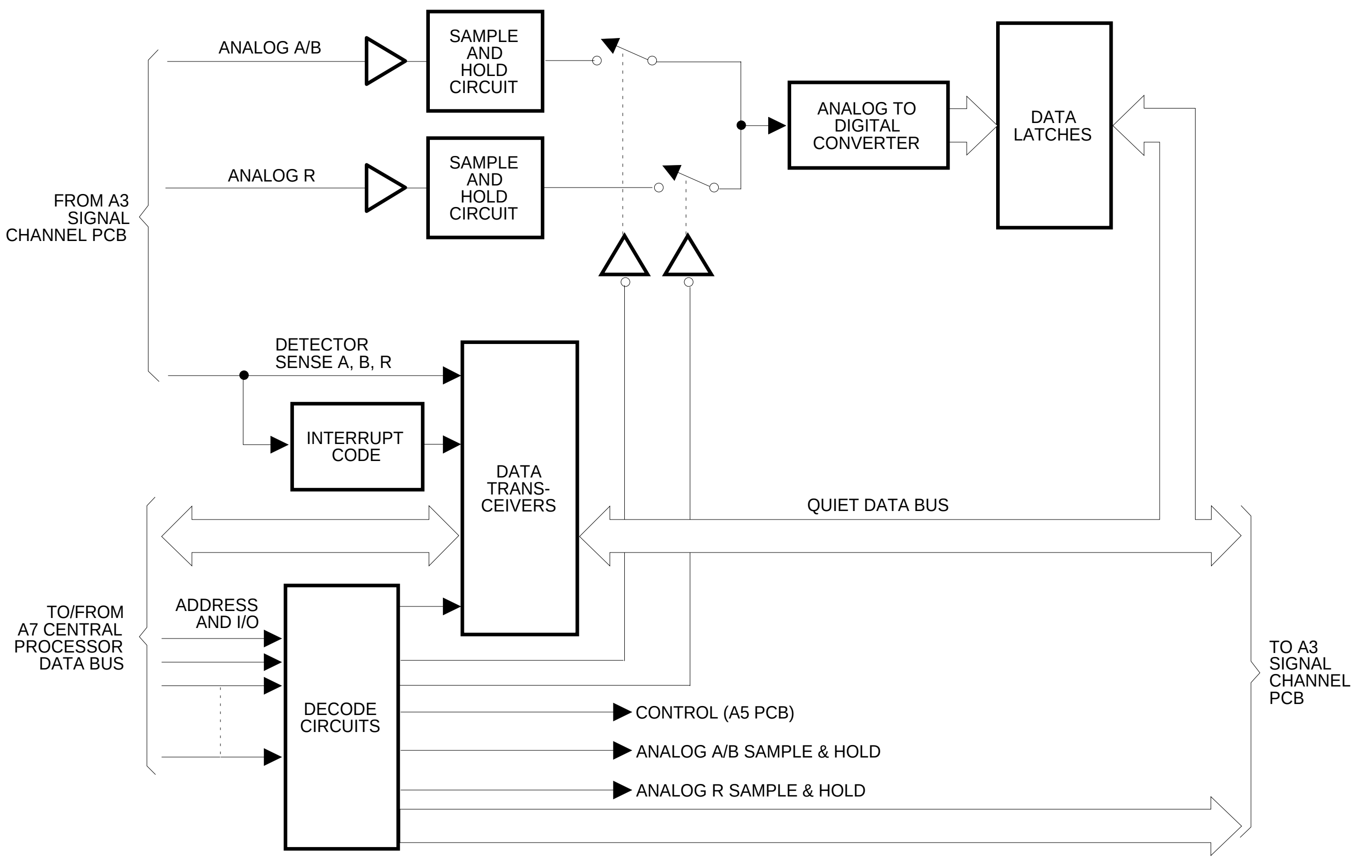


Figure 4-9. Block Diagram of Signal Channel Interface Circuits

4-8 A3 SIGNAL CHANNEL PCB

The standard A3 Signal Channel PCB has two measurement signal inputs, A and B. These input signals from these inputs are multiplexed together by an input switching circuit and then fed to an amplifier chain (Figure 4-13 on page 4-37). The resultant A/B measurement signal is filtered and sent to the output multiplexer circuits. These circuits multiplex the measurement signal with the Log Conformity and Temperature Sense signals from the A and B input connectors. The resultant output signal then goes to the A5 YIG Driver/Signal Channel Interface PCB where it is digitized. The data then goes to the A7 Central Processor PCB.

If the 541XXA is equipped with Option 5, the A3 PCB will also include a third measurement signal input (R). The signal channel circuits associated with this input are identical to those for the A/B channel, except they do not include an input switching circuit.

Channel Input Circuits

The Detector/Auto Tester output signals from the front panel input connectors go to the Channel A, B, and (optional) R input circuits on the A3 PCB. These signals are typically low level dc signals that contain low-frequency AC components. The A and B input circuit includes two low-pass filter networks and a switching network composed of FET switches. The output of this circuit is a time multiplexed signal that represents the measurement signals for Channels A and B. The R input circuit contains only a low-pass filter network.

Input Amplifier Circuits

An instrumentation amplifier, and associated gain control and auto-zero circuits, comprise the Input Amplifier circuit block (Figure 4-10). The gain of this amplifier is set to either X1, X10, or X100, by the action of the gain control circuit. This circuit is controlled by signals from the A5 YIG Driver/Signal Interface PCB. Potentiometers R199 and R201 are the X10 and X100 gain adjustments, respectively. They are adjusted during circuit alignment.

Variable Gain Amplifier Circuits

The Variable Gain Amplifier block consists of four operational amplifiers that provide an overall programmable gain of one-to-ten-thousand (1:10,000). The gain control circuit associated with these amplifiers is also controlled by signals from the A5 PCB. Potentiometer R118 is the overall gain adjustment for these circuits. The variable gain amplifier block combined with the input amplifier circuit comprise an amplifier chain that has an overall programmable gain of one-to-one-million (1:1,000,000), programmable in factors of ten (X1,X10, X100…).

Auto-Zero Circuits

When the amplifier chain is operated at high gain settings, the errors due to overall amplifier dc offset and wide band noise from the internal RF source must be eliminated. An autozero circuit performs this function. This circuit consists of a Zener diode dc voltage source, a DAC integrated circuit, and associated operational amplifiers. This output goes to a separate input on the instrumentation amplifier. Identical circuits are used for the Channel A/B and Channel R amplifier chains.

The autozero nulling procedure is performed under control of the A7 Central Processor PCB at the end of each frequency sweep, as follows:

- ☐ The amplifier chain is set to maximum gain and the dc offset is measured (by the A5 PCB).
- ☐ The autozero circuit is programmed to produce a voltage that will cancel out the offset error.
- ☐ The resultant compensation voltage value is used for subsequent measurements during the next sweep.

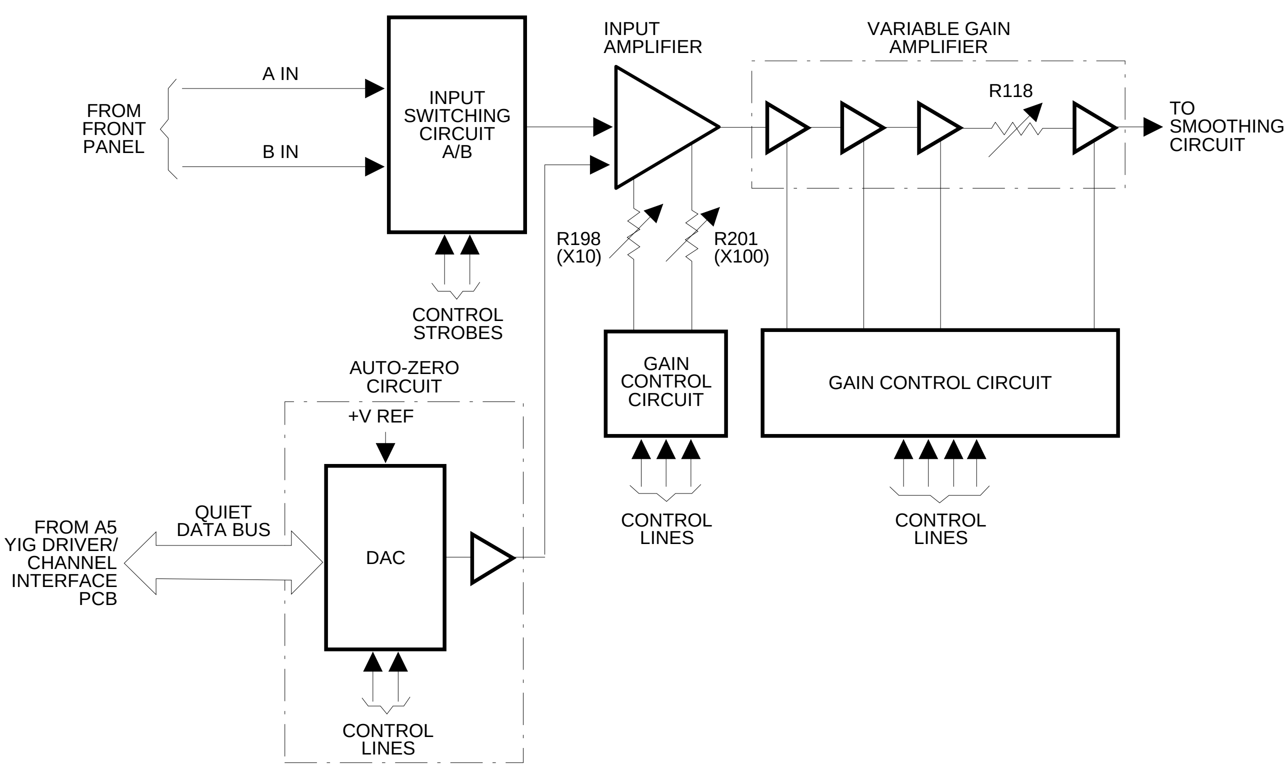


Figure 4-10. *Block Diagram of Signal Channel Input Switching and Amplifier Chain Circuits*

Smoothing Circuits

The output signal from the amplifier chain contains appreciable high frequency noise when processing low level input signals. To reduce this noise, five levels of filtering can be applied by the A3 PCB smoothing circuit. This circuit consists of a programmable RC filter network, as shown in Figure 4-11.

Resistor R148 is permanently connected in the signal path of this circuit. When Smoothing Level 1 (minimum) is selected, a capacitor is connected from the output end of R148 to ground. A separate capacitor is used for Channel A measurements (C38) and another for Channel B (C39). These capacitors are connected by analog switches that are controlled by the A7 Central Processor PCB.

The other four levels of smoothing are achieved by switching resistor R155, R154, R153, or R152 in parallel with R148. The output of the smoothing circuit is fed to the input of the output multiplexer circuits (Figure 4-13 on page 4-37). The Channel R smoothing circuit contains only one filter capacitor.

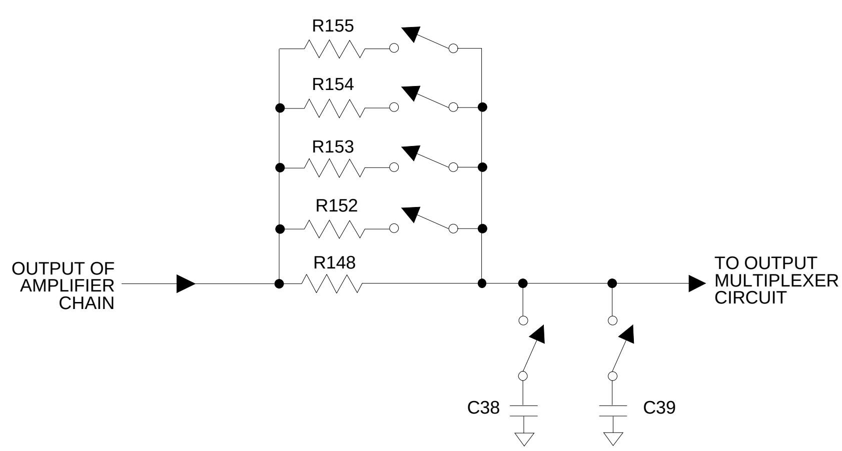


Figure 4-11. *Signal Channel Smoothing Circuit*

Log Conformity Circuits

ANRITSU RF Detectors and SWR Autotesters have built-in circuitry designed to match the log characteristic of the detector diode used. The Log Conformity Sense circuits (Figure 4-12) output a voltage value. Variable resistor R108 is used to calibrate the Input A log conformity circuit with a "standard detector" connected to the front panel INPUT A connector. Variable resistor R109 performs the same function for the Input B log conformity sense circuit.

The outputs from the A and B Log Conformity Sense circuits are read by the ADC circuit on the A5 YIG Driver/Signal Channel PCB (via the output multiplexer circuits). The resultant log conformity data is read by the Central Processor and used by it when processing measurement data.

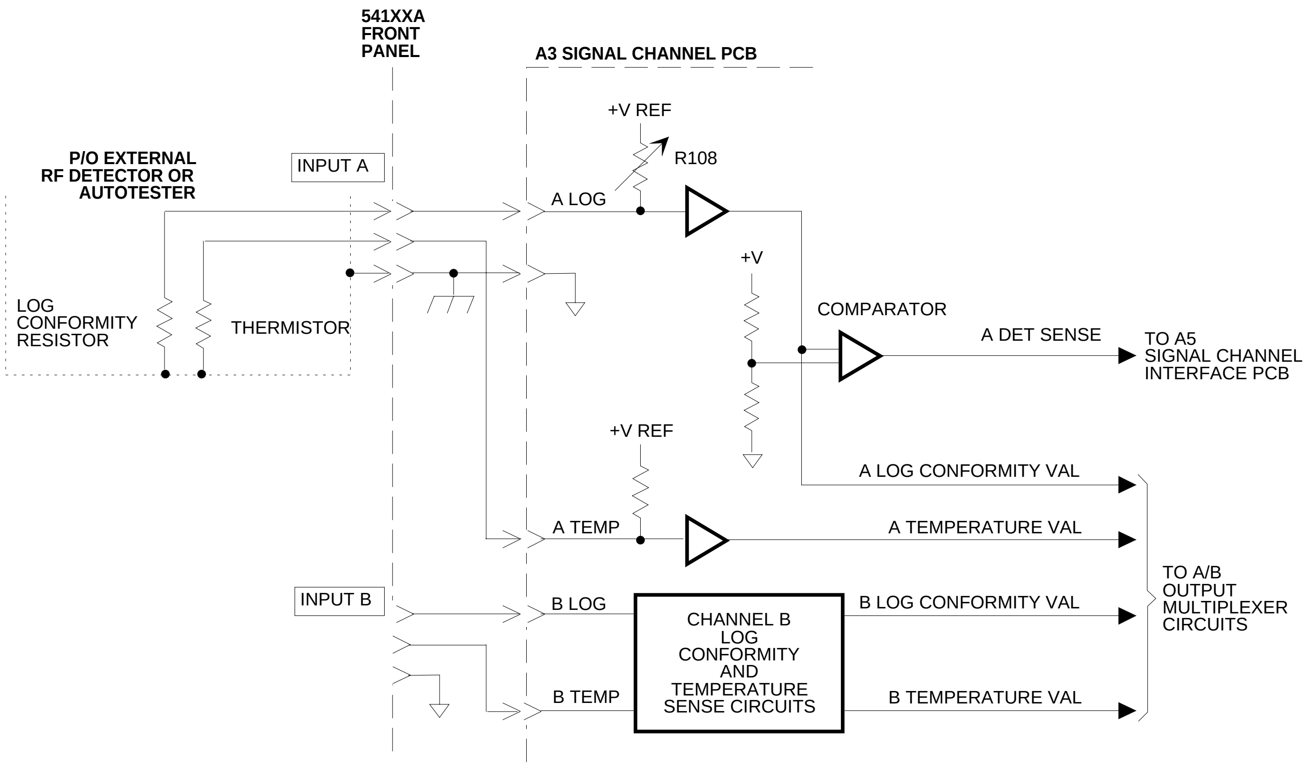


Figure 4-12. *Block Diagram of Log Conformity and Temperature Compensation Circuits*

The output from each Log Conformity Sense circuit also goes to an associated Comparator circuit. The output of the comparator is used as a status signal. This status signal indicates that a RF detector or SWR Autotester is connected to the associated input. These signals are fed to the A5 PCB and are included along with other status bits read by the A7 Central Processor PCB. The log conformity and detector connect sense circuits for Input R are identical to those for Inputs A and B.

Temperature Sense Circuits

Also contained in the RF Detector and SWR Autotester is a thermistor that is used to sense the working temperature of the detector diode (Figure 4-12). The resistance value of the thermistor is converted to a voltage and read in the same manner as for the log conformity resistor. The resultant temperature sensing data is read by the A7 Central Processor PCB and used by it when processing measurement data. The temperature sensing circuits for Inputs A, B and R are identical.

The Termistor and Log Conformity values can be monitored on the 541XXA crt display as follows:

- Press the Channel x Menu key and select **POWER** from the menu.
- Press the Calibration key, select **DC CAL** from the menu, then press ENTER.
- The **LOG/TEMP READINGS** will appear in the menu area of the display.

Output Multiplexer Circuits

The output multiplexer circuit for Channels A and B consists of five solid state relay switches and an operational amplifier. This circuit switches the five signal lines listed below onto a single signal path (ANALOG A/B) that is fed to the inputs of the sample-and-hold circuits on the A5 PCB. The five signal lines multiplexed are

- A/B measurement signal
- A Log Conformity Value
- A Temperature Sense Value
- B Log Conformity Value
- B Temperature Sense Value

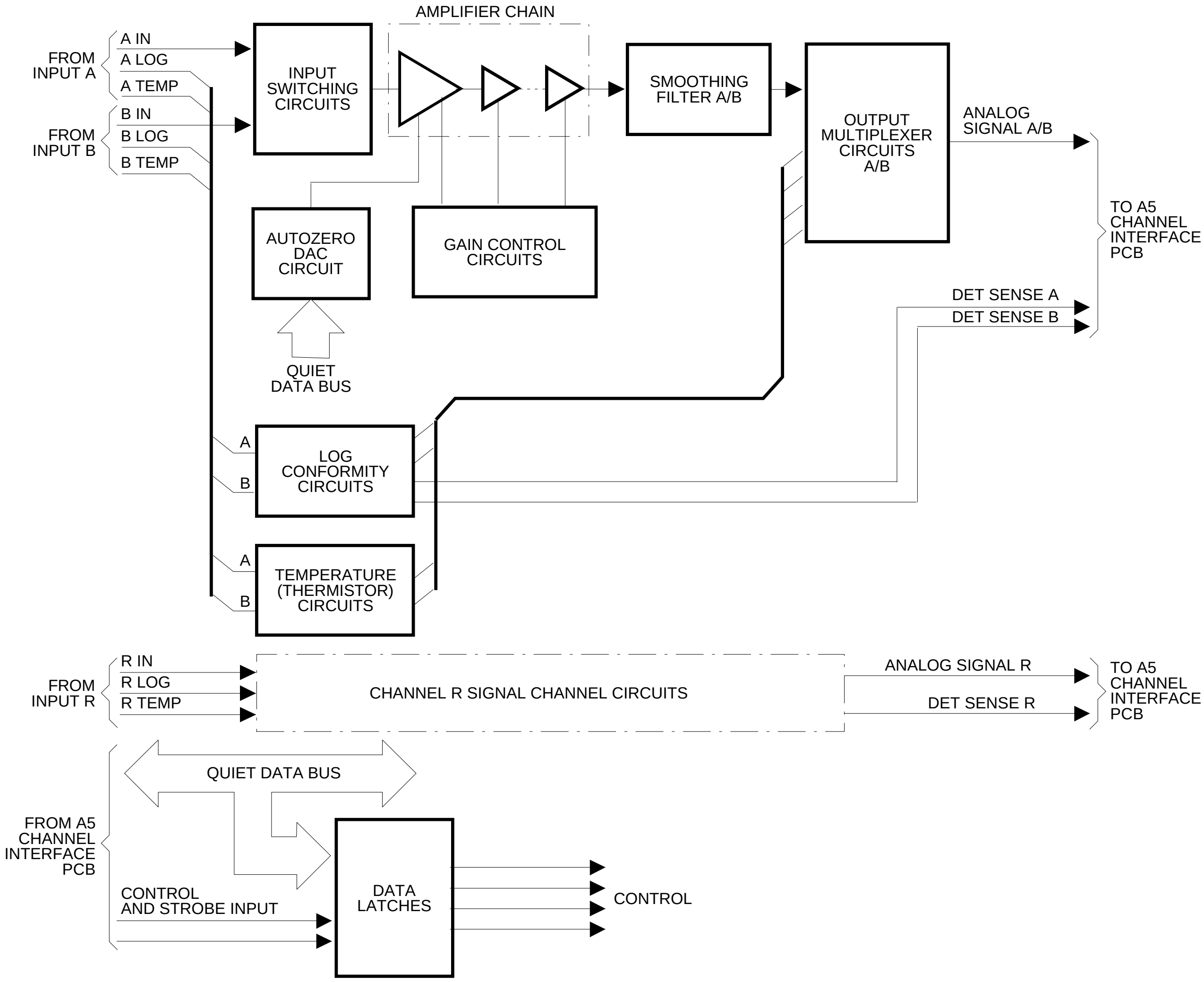


Figure 4-13. *Overall Block Diagram of A3 PCB Signal Channel Circuits*

Control Latch Circuits

The quiet data bus lines, control signals, and data strobes from the A5 YIG Driver/Signal Channel PCB go to five control latches on the A3 PCB. The outputs of these latches form the control lines and data strobes that control all the circuit functions on the A3 PCB.

4-9 A1, A2, & A10 FRONT PANEL PCBs

The Front Panel Assembly circuitry is contained on three printed circuit boards: A1 Front Panel PCB, A2 Front Panel Interface PCB, and A10 Menu PCB Assembly (Figure 4-14). These circuits form a sub-system that

- Detects Control Key closures
- Generates Interrupt for key closure
- Identifies Control Key that was pressed
- Detects Data Entry Knob rotation
- Generates Interrupts for Data Entry Knob CW and CCW rotation
- Receives and stores drive data for front panel LED indicators
- Drives front panel LED indicators

The A1 Front Panel PCB is mounted on the rear surface of the front panel and contains the control key switches and indicator LEDs for the main portion of the front panel. In all, 47 switches and 14 LEDs. The operation of the switch interface circuits is described in a following paragraph.

The A10 Menu PCB contains the three control key switches that are located on the lower portion of the front panel. (The POWER switch is a separate assembly.)

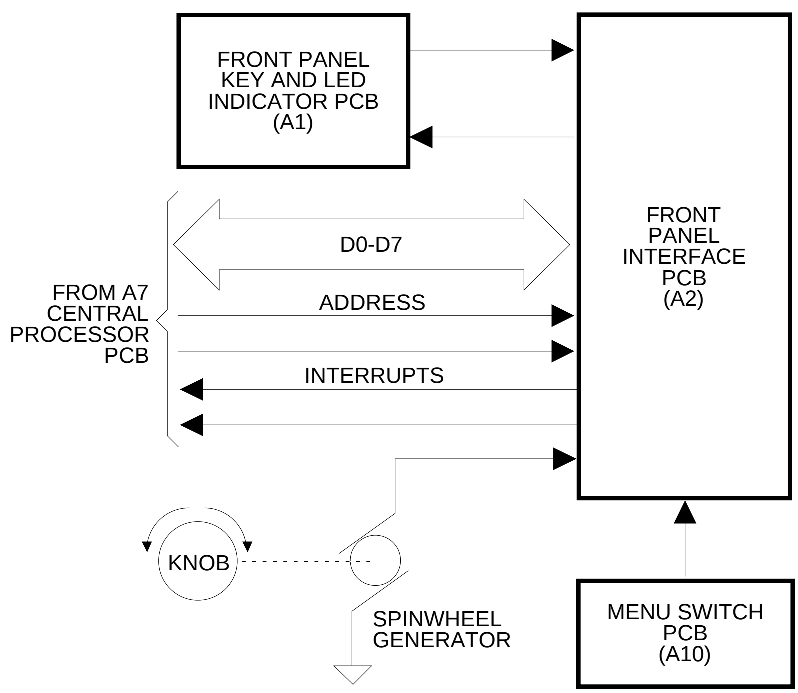


Figure 4-14. Front Panel Assembly Overall Block Diagram

The A2 Front Panel Interface Board provides the interface between the A7 Central Processor PCB and the A1 and A10 front panel PCBs. The main circuit blocks on this PCB are

- Keyboard interface
- LED indicator data latches and driver circuits
- Data Entry Knob interface
- Address decode and control circuits

Keyboard Interface Circuits

The switches on the A1 Front Panel PCB & A10 Menu PCB are connected into a two-dimensional matrix consisting of eight X-lines and eight Y-lines (Figure 4-15). Each switch point forms a unique X/Y coordinate (i.e., address). Closing any switch connects one of the Y-lines to one of the X-lines.

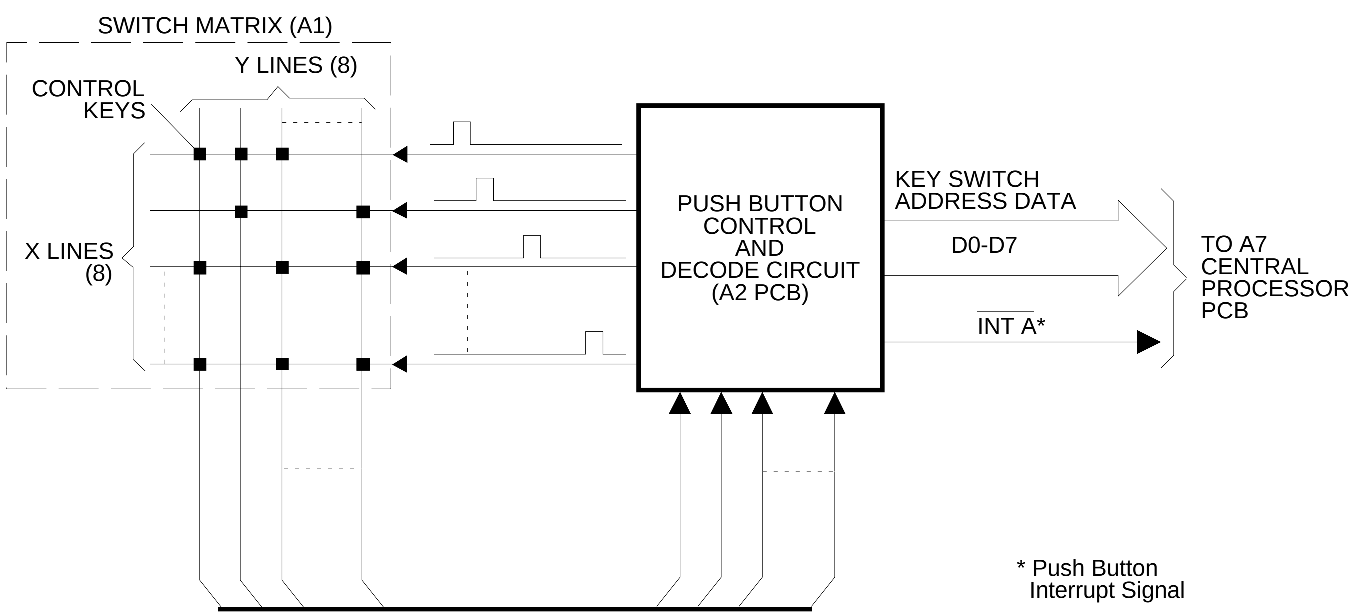


Figure 4-15. *Control Key Matrix and Decode Circuits Block Diagram*

The Switch Controller/Decoder circuit on the A2 PCB sequentially pulses the eight X-lines and also monitors each of the eight Y-lines for the presence of pulses. A pulse detected on a Y-line signifies a switch closure, which causes the controller/decoder circuit to send a Control Key Interrupt signal to the A7 Central Processor PCB. The unique switch address determined by the X-line/Y-line combination leaves the controller/decoder circuit as a data byte. This data byte goes to the Central Processor Data Bus. Upon receiving the interrupt, the A7 Central Processor PCB reads the address byte to determine which key was pressed.

LED Indicator Latch Circuits

The 14 LED indicators located on the A1 PCB are controlled by latches on the A2 PCB (Figure 4-16). The A7 Central Processor PCB causes an individual LED indicator to be lit by writing a logic-1 into the latch bit associated with the selected LED. A control strobe from the control decode circuit clocks the data into the data latches. Each latch output line contains a current limiting resistor for the associated LED.

Data Entry Knob Interface

The Data Entry Knob is fixed to the shaft of a small dc motor that is used as a generator. When the knob is rotated, the motor produces a dc voltage that is proportional to the speed of rotation. The polarity of the voltage indicates the direction of rotation of the knob. The output of the motor is connected to the Data Knob Interface Circuits (Figure 4-16). The input portion of these circuits consists of two comparators: one that produces a pulse train for clockwise knob rotation and a second that produces a pulse train for counter-clockwise knob rotation.

The pulse rate of the CW and CCW pulse trains is determined by the rate of knob rotation. These signals are fed to the Knob Interrupt Circuits, which produce the CW and CCW Interrupt signals that are sensed by the A7 Central Processor PCB.

CPU Interface Circuits

The A2 PCB Address Decode Circuits decode the address lines of the Central Processor Data Bus to produce strobe signals that control the interface circuits located on the A2 PCB. These signals clock data from the data bus into the Keyboard Interface Circuit and the LED Indicator data/driver latches. They also control the clocking of interrupt signals and keyboard address data onto the data bus.

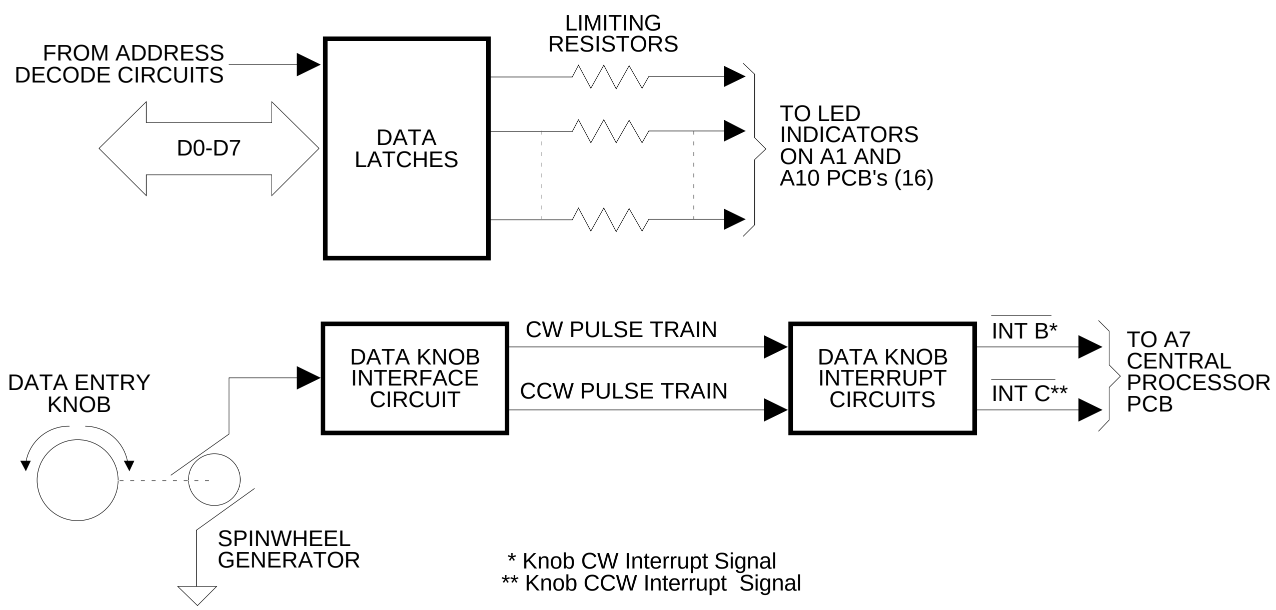


Figure 4-16. *LED Indicator and Data Entry Knob Interface Circuits Block Diagram*

4-10 A9 and A16 POWER SUPPLY PCBs

The 541XXA power supply circuits consist of a half-bridge line rectifier coupled to a high efficiency dc/dc switching type power converter. These circuits produce the following output voltages:

- ☐ +5 V High Current Supply
- ☐ +12V High Current regulated supply
- ☐ +12V Low Current regulated supply
- ☐ +15V regulated supply
- ☐ –15V regulated supply
- ☐ –18V regulated supply
- ☐ +22V regulated supply

The power supply circuits are located on the A9 Power Supply Motherboard PCB, the A16 Power Supply Converter PCB, the rear panel assembly, and the front panel (Figure 4-17). In addition to the output voltages listed above, a +12V Start-Up Power Supply is also included on the A9 PCB. This power supply is used internally on the A9 PCB.

WARNING

Hazardous voltages are present throughout the switching power supply and at the front and rear panels. When performing maintenance, use extreme care to avoid electrical shock.

Front and Rear Panel Components

The POWER ON/OFF switch is located on the front panel and connects to the A9 Power Supply Motherboard PCB. The line voltage selector module is located on the rear panel. It provides primary circuit switching for 115V/230 Vac line operation and contains the fuses for operation at these voltages. The rear panel fan operates on 12 Vdc power, which it obtains from the A9 Power Supply Motherboard PCB.

Power Supply Motherboard PCB Circuits

The major circuits located on the A9 Power Supply Motherboard PCB are:

- ☐ Start-up Power Supply, transformer and regulator
- ☐ Line Circuit Rectifier/Doubler circuit
- ☐ Soft Start Control circuit
- ☐ Pulse Width Modulator and Control Amplifier circuits
- ☐ Over Current Sense, Over Voltage Sense and Shut Down Timer circuits
- ☐ +12V, +15V, –15V, –18V, and +22 V regulator circuits

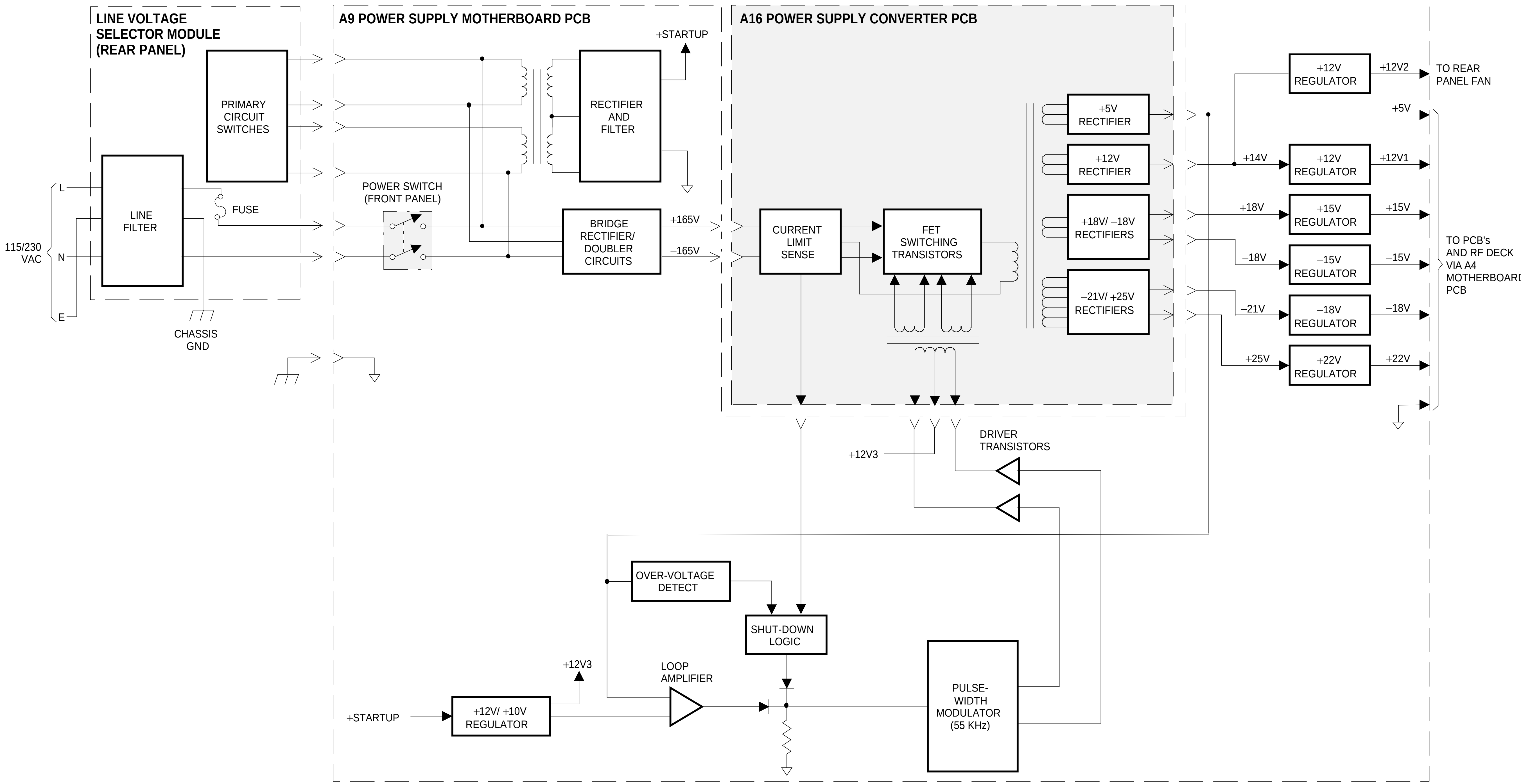


Figure 4-17. *Block Diagram of 541XXA Power Supply Circuits*

Power Supply Converter PCB Circuits

The major circuits located on the A16 Power Supply Converter PCB are

- Switching Transistors
- Over-Current Sense
- Output Voltage Transformer
- Output Rectifiers

Power Supply Circuits Operation

The switches contained within the line voltage selector module configure the primary windings of the Start Up Power Supply transformer for 115 Vac or 230 Vac operation, as selected.

The line voltage selector module also configures the line rectifier circuit as either a full wave voltage doubler (115 Volt line operation) or a full wave bridge rectifier (230 Volt line operation). The output voltages from the rectifier circuit in either mode will be +165 Vdc and –165 Vdc, which are fed to the dc isolator switching transistors on the A16 Power Supply Converter PCB.

The switching transistors alternately switch +165 Vdc and –165 Vdc to the primary windings of the output transformer at a 65 kHz rate. The driving signals for these transistors are supplied by the Pulse Width Modulator (PWM) circuit on the A9 PCB. The drive signals are two pulse trains with a variable duty cycle that is determined by the output from the Control Amplifier circuit during normal operation. During power up (or fault recovery) operation, these signals are controlled by the Soft Start Control circuit. During a fault condition, they are controlled by the Shut Down Timer circuit.

The four secondary windings of the Output Voltage Transformer produce reduced voltages that go to rectifier and filter circuits also located on the A16 PCB. These circuits contain inductors that function as integrators. The output of the +5V rectifier/filter is fed to the A9 PCB where it is sensed by the Control Amplifier. The action of the Control Amplifier and PWM circuits cause the +5V output (and other power supply outputs) to be regulated to their correct values.

The outputs produced by the other three windings and associated rectifier/filter circuits are: +14V, +18V, –18V, –21V, and +25V. These voltages go to the final regulator circuits on the A9 PCB.

The main input to the Control Amplifier is the +5V output sense line. Any change in the +5V output cause the control amplifier to force the PWM to change the duty cycle of the drive signals so that the +5V power supply output is regulated back to +5V.

At power up, the +12V output of the Start-up Power supply is used to charge a capacitor. The voltage across the capacitor is sensed by the PWM circuit, which causes it to set the drive signal duty cycle for a minimum output from the +5V supply. As the capacitor charges, the drive signal duty cycle increases, causing the +5V output (and other power supply outputs) to gradually reach full operating value.

The Over-Current Sense circuit monitors the currents through the switching transistors. The Over-Voltage Sense circuit monitors the output of the +5V supply. The outputs of these circuits are inputs to the Shut Down Timer circuit. When activated by either of these inputs, the Shut Down Timer circuit generates a shut down signal to the PWM, which causes the switching transistors to turn off. The shut down signal has a duration of approximately one half second. When the Shut Down Timer circuit resets, the power supply soft starts, as described above. If the condition causing the shut down is still present, the circuit will generate another pulse and shut down the power supply again. This mode of operation will repeat until either the over voltage/current condition is removed or the line power is removed.

The final regulator circuits on the A9 PCB produce the +12V HC (high current), +12V LC (low current), +15V, –15V, –18V, and +22V power supply outputs. These regulator circuits are driven by the outputs from the A16 PCB as follows:

- The +12V HC and 12V LC are driven by the +14V supply.
- The +15V regulator is driven by the +18V supply.
- The –15V regulator is driven by the –18V supply.
- The –18V regulator is driven by the –21V supply.
- The +22V regulator is driven by the +25V supply.

4-11 A4 MOTHERBOARD PCB

The Motherboard PCB provides interconnection between all the PCBs and assemblies in the 541XXA. The motherboard connects directly to the following:

- A5 YIG Driver/Signal Channel Interface PCB
- A6/A24 ALC/Frequency Instruction PCB
- A7 Central Processor/GPIB PCB
- A8 Graphics System Processor PCB

The motherboard distributes the various power supply voltages throughout the 541XXA. It connects to the A1/A2 and A3 PCB’s, power supply PCB, RF Deck, and rear panel connectors via various cables. Table 4-2 lists the cable connectors on the A4 Motherboard and denotes their cable destination.

Table 4-2. *A4 Motherboard PCB Cable Connectors*

Connector	Cable Destination
J1	A3 Signal Channel PCB (ribbon cable)
J2	A2 Front Panel Interface PCB (ribbon cable)
J3	YIG Oscillator Assembly
J4	Downconverter
J5	Control Modulator
J6	70 dB Step Attenuator (Optional)
J7	Directional Coupler
J8	Distribution PCB
J9	Horizontal Output connector (rear panel)
J10	Centronics Printer output (rear panel)
J12	GPIB Interface connector (rear panel)
J13	(not used)
J14	A9 Power Supply motherboard
J15	Internal CRT monitor
J16	A3 Signal Channel PCB Output Cable
J17	External Monitor connector (rear panel)
J18	3GHz Marker Pack Connector (54107/109/111A)
J20	External ALC Input connector (rear panel)*
J23	PSU Extension (54154A through 54177A)
J24	A23 Multi-Band Controller (54154 through 54177)

4-12 RF DECK ASSEMBLY

NOTE
The Frequency/Instruction PCB is the A6 assembly in models 54107A through 54147A; it is A24 in 54154A through 54177A.

The RF deck assembly contains the components that generate CW and swept frequency RF signals. It also routes these signals to the front panel RF OUTPUT connector. The RF decks used in the 541XXA series are designed around a single YIG-tuned oscillator configuration. In these units, the YIG frequency is controlled by the frequency instruction and YIG driver circuitry located on the A6/A24 and A5 PCB's. In addition to the components used to generate and route the RF signals, each RF deck assembly also contains components that produce the markers used by the central processor to control the accuracy of the output frequency.

RF Deck Configurations

There are seven different configurations of the RF deck assembly. One configuration covers the RF models (54107A thru 54111A); the other six configurations cover the Microwave Band models (54117A thru 54177A). The frequency range of these sixteen models is 1.0 MHz to 50 GHz.

The block diagram of the RF Deck for Models 54117A and 54119A is shown in Figure 4-18 on page 4-53. This diagram, includes all of the RF components found on a typical RF deck assembly for 541XXA series microwave band models. Refer to this block diagram during the descriptions of common RF components and frequency control circuits presented below.

Common RF Deck Components

Many RF components are common to all RF deck assembly configurations. These common components are described in Table 4-3. Refer to this table as necessary while reading the descriptions of 541XXA RF decks in the following paragraphs. RF components that are peculiar to a specific RF deck configuration are described as part of the description for that particular RF deck.

Table 4-3. *Common RF Deck Component Descriptions*

YIG-tuned Oscillator

Each RF deck assembly contains a single YIG-tuned oscillator. The YIG-tuned oscillator generates high-power RF output signals that have low broadband noise and low spurious content.

The YIG-tuned oscillator is driven by the FM and Main tuning coil currents from the A5 YIG Driver PCB. During CW mode, the main tuning coil current tunes the oscillator to within a few megahertz of the final output frequency. The frequency control circuitry then fine adjusts the FM tuning coil current to make the output frequency exact.

In the sweep mode, with sweep widths greater than 40 MHz, the main tuning coil current tunes the oscillator through the swept frequency range. For sweep widths of 40MHz or less, the FM tuning coil current tunes the oscillator throughout the swept frequency range.

Control Modulator

Each RF deck assembly contains a control modulator (Figure 4-18). In some configurations the control modulator is located inside another component such as the Down Converter (models 54107A, 54109A, and 54111A), It may also be located in the Switched Filter Assembly (models 54137A, 54147A, 54161A, 54169A, 54177A).

The control modulator contains PIN switches that control the output power of the YIG-tuned oscillator. The modulator bias input drives the PIN switches that switch the RF power on and off; the modulator control input drives the PIN switches that control the output RF power level. A portion of the RF input to the modulator is picked off for use by the frequency source-lock circuitry.

Filters

The filters provide lowpass filtering of the RF signals to reduce harmonic emissions.

Directional Detector

Each RF deck assembly contains a directional detector that transfers the RF output signal to the RF OUTPUT connector. It also couples a portion of the RF output signal to an integral RF detector. The detected output is used as the "internal" ALC sense signal that is input to the power leveling circuits located on the A6/A24 ALC/Frequency Instruction PCB.

The directional detector assembly also includes a thermistor that senses the detector's temperature that is also connected to the A6/A24 PCB power leveling circuits. In models 54107A, 54109A, and 54111A, the directional detector is located inside the Down Converter.

Step Attenuator

The optional step attenuators provide up to 70 dB attenuation of the RF output in 10 dB steps. The step attenuator control and driver circuits are located on the A7 Central Processor PCB. There are three versions of these attenuators, which are model dependant. Refer to the 541XXA Network Analyzer Operation Manual for further details.

Frequency Control and Source-Lock

The A7 Central Processor controls the output frequency of the YIG-tuned Oscillator through the frequency instruction circuits located on the A6/A24 ALC/ Frequency Instruction PCB. These circuits convert the digital instructions from the central processor into analog control signals for the YIG main coil and FM coil driver circuits located on the A5 YIG Driver/ Channel Interface PCB. The main coil and FM coil driver circuits convert the control signals into currents that drive the coils of the YIG-tuned oscillator to produce an output RF signal. The output RF signal from the YIG-tuned oscillator goes to the Control Modulator. In the control modulator, a portion of the RF signal is picked off and routed to the Sampler as an input to the frequency source-locking circuitry.

The frequency accuracy of the 541XXA series is based upon an internal 10 MHz crystal oscillator (75 MHz crystal oscillator for models 54107A, 54109A, and 54111A). The output of this 10 MHz reference oscillator, located in the Divider Module, is used to phase-lock the 500 MHz VCO located in the 500 MHz VCO/Power Amplifier Module. The output of the 500 MHz VCO goes via a power amplifier to a step recovery diode (SRD).

The SRD produces a 500 MHz comb signal throughout the full range of the 541XXA, 10 MHz to 26.5 GHz. The 500 MHz comb signal then goes to the Sampler where it is used to switch the sampling diodes. (The sampler is physically part of the 500 MHz Marker Module.) The other input to the sampler is the RF signal picked off in the control modulator. The sampling diodes sample the RF input signal at the 500 MHz comb signal rate. The RF signal output of the sampler goes to the 500 MHz Marker Module where it is amplified and filtered to produce 500 MHz markers. The 500 MHz markers then go to a data buffer on the A6/A24 PCB to be read by the central processor.

The 500 MHz VCO/Power Amplifier module (Figure 4-18) also produces a 25 MHz output using the divider circuitry in the Divider module. This 25 MHz signal goes to the 25 MHz Marker Module. There it is amplified and applied to a SRD producing a 25 MHz comb signal. The 25 MHz comb signal goes to the sampler. There it turns on the sampling diodes. These diodes sample the dc to 250 MHz IF signal input that was generated in the 500 MHz Marker module. The resultant output is 25 MHz markers that cover the frequency range of 2.0 to 26.5 GHz. The 25 MHz markers also go to a data buffer on the A6/A24 PCB to be read by the central processor.

The central processor processes the 500 MHz and 25 MHz marker read signals from the A6/A24 PCB. If the marker read signals indicate that the frequency is not source-locked, the central processor generates error correction instructions, which it sends to the A6/A24 PCB. In the A6/A24 PCB, the frequency error correction circuitry outputs a voltage to the A5 PCB that is the frequency source-lock error correction signal. In the A5 PCB, this signal produces a current to drive the FM coil. This coil is used to offset the frequency error and source-lock the YIG-tuned oscillator.

The RF decks of models 54117A and 54147A RF have a 10 MHz to 2 GHz Down Converter installed. A portion of the down-converted RF signal is picked off and routed to an additional 25 MHz Marker Generator. This marker generator produces 25 MHz markers that cover the frequency range of 10 MHz to 2.0 GHz. The central processor uses these 25 MHz markers to achieve frequency source-lock in exactly the same manner as described in the preceding paragraphs.

The RF models 54107A, 54109A, and 54111A use 75 MHz and 25 MHz markers to achieve frequency source-lock. A description of the 75 MHz/25 MHz Marker Generator is included as a part of the functional description of the RF deck assembly.

RF Decks for Models 54117A/ 54119A

The RF decks of microwave band models 54117A (10 MHz to 8.6 GHz) and 54119A (2.0 to 8.6 GHz) are very similar. However, model 54117A contains two additional components, a Down Converter and a 25 MHz Marker Generator. These additional components enable the 54117A to generate RF outputs in the frequency range of 10 MHz to 2.0 GHz. (This band of frequencies is referred to as the "hetrodyne band;" Model 54147A also operates in this band.) Refer to Figure 4-18 during the following functional description.

The output RF signal from the YIG-tuned oscillator goes to the Control Modulator. In the control modulator, a portion of the RF signal is picked off for input to the frequency source-lock circuitry (previously described). There are two inputs to the control modulator that control the RF output power level — the modulator bias input and the modulator control input. Both of these inputs come from the A6 ALC/Frequency Instruction PCB. The modulator bias input drives the control modulator PIN switches that switch the RF power on and off. The modulator control input drives the PIN switches that control the power level of the RF output. The RF output signal from the control modulator is sent to the Switched Filter.

In the 54117A, the control modulator has an additional RF output for the Down Converter. When the unit is generating RF signals in the frequency range of 10 MHz to 2.0 GHz, a 6.31 to 8.3 GHz signal is sent to the down converter. There it is mixed with a 6.3 GHz signal from the down converter's internal oscillator. The resulting 10 MHz to 2.0 GHz signal is sent through a 2 GHz Low-Pass Filter, amplified, and then output to the Switched Filter.

A portion of the down-converted RF signal is picked off and sent as an input to the 25 MHz Marker Generator. In the marker generator, it goes to the input sampler where it is sampled by the sampling diodes at a 25 MHz comb signal rate. The resultant output is 25 MHz markers that are used by the central processor to achieve frequency source-lock.

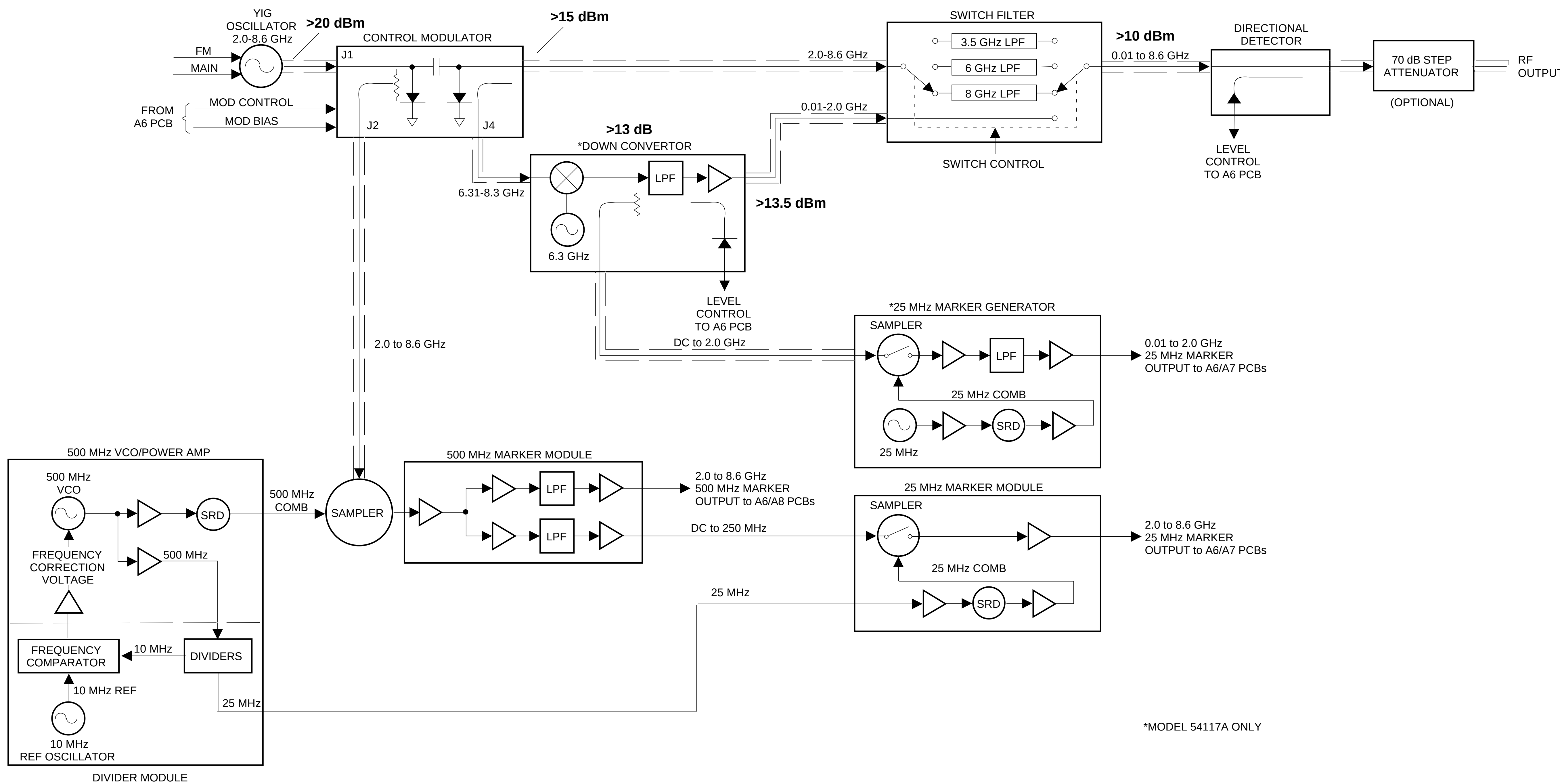


Figure 4-18. *Block Diagram of RF Decks for Models 54117A/54119A*

A portion of the RF output signal from the down converter is detected (by the directional detector), and sent to the ALC circuitry on the A6 PCB. This is the feedback signal for the internal ALC function.

The directional detector also contains a built-in thermistor that outputs a resistance representing the detector's temperature. This resistance is converted to a voltage by the A6 PCB and monitored by the central processor. As the ambient temperature changes, the central processor compensates for the output level to provide a stable RF output-vs-temperature characteristic.

The Switched Filter provides rejection of the harmonics generated by the 2.0 to 8.6 GHz YIG-tuned oscillator. The RF deck of models 54117A, 54147A, 54161A, 54169A, and 54117A have a 10 MHz to 2.0 GHz Down Converter. The Switched Filter multiplexes between these down converter signals and the 2.0 GHz to 8.6 GHz oscillator signals during full band sweeps. Drive current for the switched filter is provided by the A18 Switch Filter Driver PCB that is mounted on top of the switched filter assembly. The 2.0 to 8.6 GHz RF signal from the control modulator has three filtering paths; the 3.5 GHz filter path, the 6 GHz filter path, and the 8 GHz filter path. The down converter provides filtering for the 10 MHz to 2.0 GHz RF signal; therefore, the signal is multiplexed through to the switched filter output.

The RF signal output from the switched filter is sent to the Directional Detector and transferred to the RF OUTPUT connector. A portion of the RF output signal is detected and coupled out as feedback to the ALC circuitry on the A6 PCB. In the ALC circuitry, the detected RF sample is summed with the control voltage that represents the desired RF output level. The resulting voltage is sent to the control modulator driver circuitry which then drives the control modulator PIN switches to adjust the RF power level output.

RF Decks for Models 54128A, 54130A, 54131A, and 54136A

The RF decks of models 54128A (8 to 12.4 GHz), 54130A (12.4 to 20 GHz), 54131A (10 to 16 GHz), and 54136A (17 to 26.5 GHz) have an identical configuration. Refer to Figure 4-19 during the following functional description.

The output signal from the YIG-tuned oscillator goes to the Control Modulator. In the control modulator, a portion of the RF signal is picked off for input to the frequency source-lock circuitry, which was previously described in the general description (page 4-48).

There are two inputs to the control modulator that control the RF output power level — the modulator bias input and the modulator control input. Both of these inputs come from the A6 ALC/Frequency Instruction PCB. The modulator bias input drives the control modulator PIN switches that switch the RF power on and off. The modulator control input drives the PIN switches that control the power level of the RF output.

The output from the control modulator is sent to the Directional Detector for transfer to the RF OUTPUT connector. A portion of the RF output signal is detected and sent as a feedback signal to the ALC circuitry located on the A6 PCB. This signal is summed with the control voltage that represents the desired RF output level. The resulting voltage is sent to the control modulator driver circuitry which then drives the control modulator PIN switches to adjust the RF power level output to the desired level.

The directional detector also contains a built-in thermistor that outputs a resistance representing the detector's temperature. This resistance is converted to a voltage by the A6 PCB and monitored by the central processor. As the ambient temperature changes, the central processor compensates for the output level to provide a stable RF-output-vs-temperature characteristic.

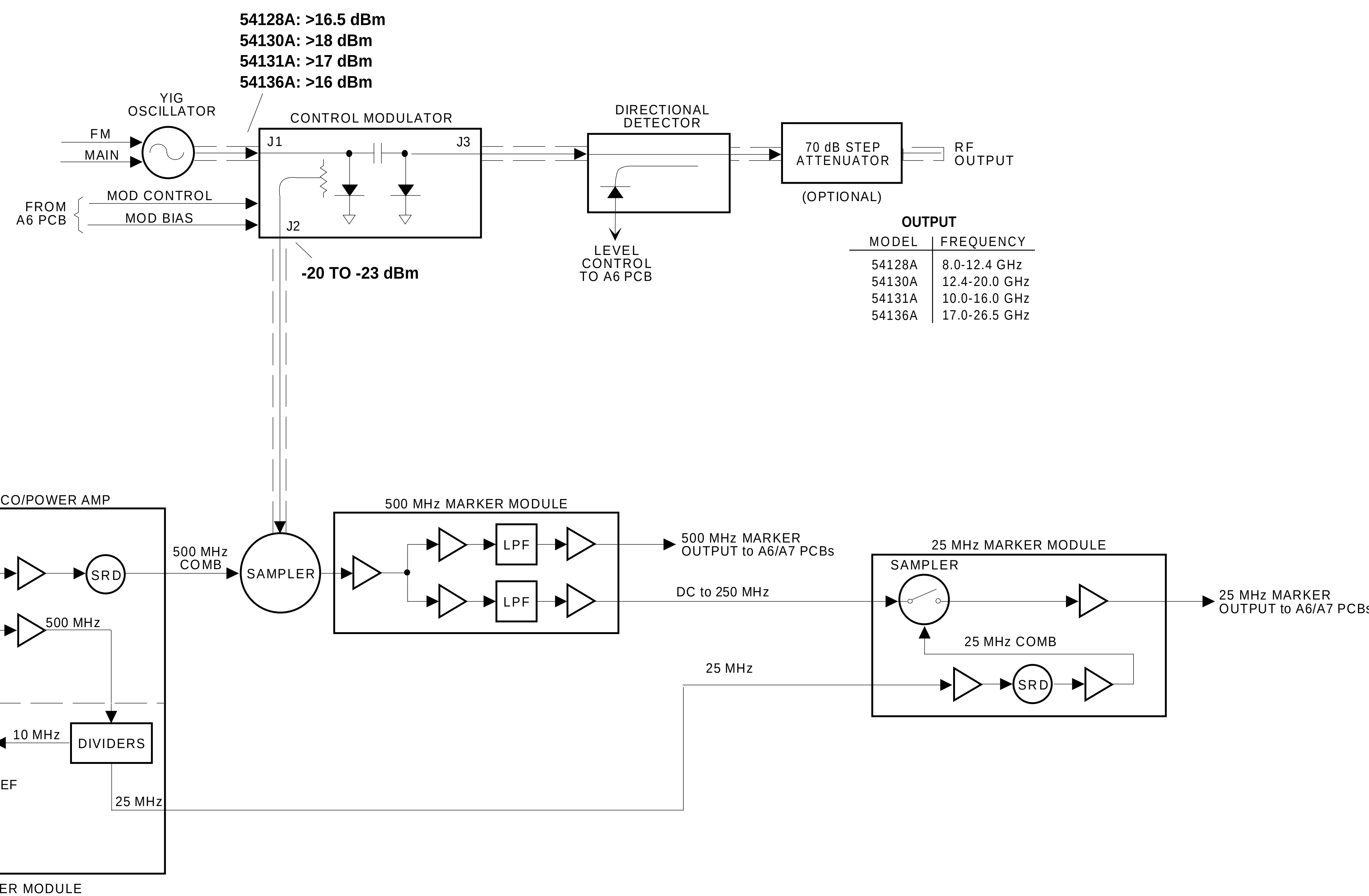


Figure 4-19. *Block Diagram of RF Decks for Models 54128A, 54130A, 54131A, and 54136A*

RF Decks for Models 54137A and 54147A

The RF decks of microwave band models 54137A (2.0 to 20 GHz) and 54147A (10 MHz to 20 GHz) are very similar. However, model 54147A contains two additional components, a Down Converter and a 25 MHz Marker Generator. These additional components enable the 54147A to generate RF signals in the frequency range of 10 MHz to 2.0 GHz. Refer to Figure 4-20. during the following functional description.

The output signal from the YIG-tuned Oscillator goes to the Switched Filter Assembly. As shown in Figure 4-20, the switched filter assembly contains a control modulator and a switched filter. After amplification, a portion of the RF signal is sent to the frequency source-lock circuitry (previously described).

There are two inputs to the control modulator section that control the RF output power level — the modulator bias input and the modulator control input. Both of these inputs come from the A6 ALC/ Frequency Instruction PCB. The modulator bias input drives the control modulator PIN switches that switch the RF power on and off. The modulator control input drives the PIN switches that control the power level of the RF output signal.

The output signal from the control modulator section is sent to the switched filter, which contains a coupler to provide a signal for the Down Converter. Whenever the model 54147A is generating RF signals in the frequency range of 10 MHz to 2.0 GHz, a 6.31 to 8.3 GHz RF signal is coupled out of the switched filter, through an 8 GHz filter path, and routed to the down converter. In the down converter, this signal is mixed with a 6.3 GHz signal from the down converter’s internal oscillator. The resulting 10 MHz to 2.0 GHz signal is sent through a 2 GHz Low-Pass Filter, amplified, and then output to the switched filter. A portion of the down-converted signal is picked off and is input to the 75 MHz/25 MHz Marker Generator.

Inside the marker generator, the output from the local 75 MHz crystal oscillator is split into two paths. In one path, the 75 MHz signal is amplified, then goes to the sampler assembly. In the sampler assembly, the step recovery diode produces a 75 MHz comb signal that drives the sampling diodes. These diodes sample the RF signal from the down converter (above). The output of the sampler is amplified and filtered to produce 75 MHz markers (the 75 MHz markers are not used in this application). In the other path, the 75 MHz signal is amplified, then divided to produce a 25 MHz signal. This 25 MHz signal is applied as the gate input to a FET (field-effect transistor). The source input is a dc to 75 MHz signal from the 75 MHz marker circuitry. The FET output is amplified and filtered to produce 25 MHz markers.

The 25 MHz markers are used by the central processor to achieve source-lock. A portion of the RF output signal from the down converter is detected and coupled out as feedback to the ALC circuitry on the A6 PCB. The directional detector also has a built-in thermistor that outputs a resistance representing the detector's temperature as an input to the A6 PCB.

The switched filter provides rejection of the harmonics that are generated by the 2.0 to 20 GHz YIG-tuned oscillator. In model 54147A, it also multiplexes between the 10 MHz to 2.0 GHz and 2.0 GHz to 20.0 GHz signals from the down converter during full band sweeps. The 2.0 to 20 GHz RF signal from the control modulator has four filtering paths and one through path. The four filtering paths are:

- 3.3 GHz path
- 5.5 GHz path
- 8.6 GHz path
- 13.5 GHz path

Signals above 13.5 GHz are routed via the through path to the switched filter output. The down converter provides filtering for the 10 MHz to 2.0 GHz RF signal; therefore, the RF signal is multiplexed through to the switched filter output.

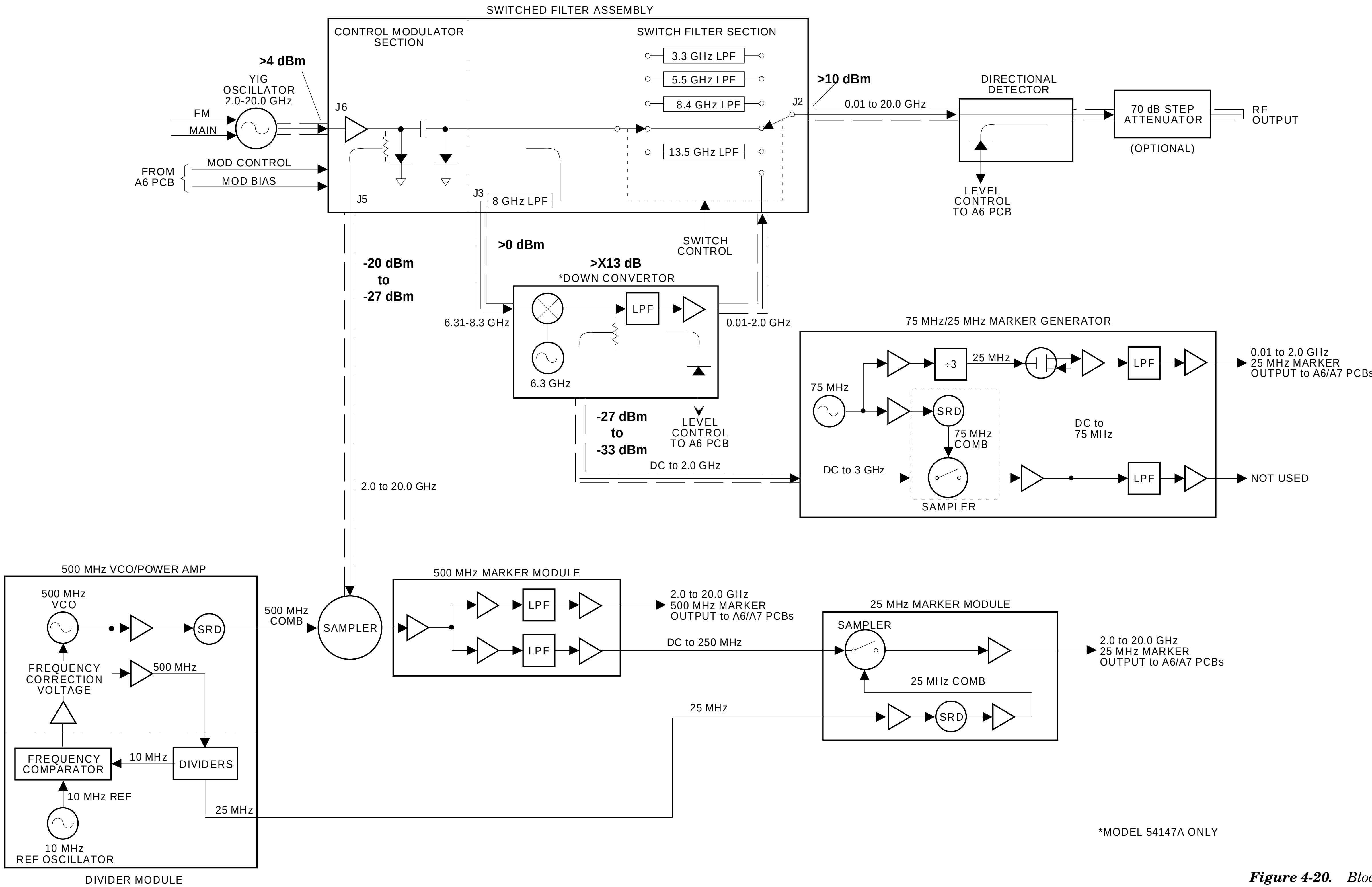


Figure 4-20. *Block Diagram of RF Decks for Models 54137A and 54147A*

The RF signal output from the switched filter is sent to the Directional Detector for transfer to the RF OUTPUT connector. A portion of the RF output signal is detected and coupled out as feedback to the ALC circuitry on the A6 PCB. In these circuits, the detected RF sample is summed with the control voltage that represents the desired RF output level. The resulting voltage is sent to the control modulator driver circuitry which then drives the control modulator PIN switches to adjust the RF power level output.

The directional detector also has a built-in thermistor that outputs a resistance representing the detector's temperature. This resistance is converted to a voltage by the A6 PCB and monitored by the central processor. As the ambient temperature changes, the central processor compensates for the output level to provide a stable RF-output-vs-temperature characteristic.

RF Decks for Models 54107A, 54109A, and 54111A

The RF decks of the models 54107A (1.0 MHz to 1.5 GHz), 54109A (1.0 MHz to 2.2 GHz), and 54111A (1.0 MHz to 3.0 GHz) contain identical components. Refer to Figure 4-21 during the following functional description.

The RF output signal from the YIG-tuned Oscillator goes to the Down Converter through an Isolator. The isolator prevents the reflection of RF energy back into the YIG-tuned oscillator. In the down converter, the 10 to 13 GHz RF signal from the YIG-tuned oscillator is mixed with a 10 GHz signal from the down converter's internal oscillator. The resulting 1.0 MHz to 3.0 GHz RF signal goes to the control modulator.

The control modulator is used to control the RF output power level of the unit. The modulator control output signal from the A6 ALC/Frequency Instruction PCB drives the modulator PIN switches that control the power level of the output signal. From the control modulator, the RF signal goes through a Low-Pass Filter, is amplified, and then routed to the RF OUTPUT connector.

A portion of the RF output signal from the down converter is detected and coupled out as feedback to the ALC circuitry on the A6 PCB. On the A6 PCB, the detected RF sample is summed with the control voltage that represents the desired RF output level. The resulting voltage is sent to the control modulator driver circuitry that drives the control modulator PIN switches to adjust the RF power output level.

The directional detector in the down converter also has a built-in thermistor that outputs a resistance representing the detector's temperature. This resistance is converted to a voltage by the A6 ALC circuits and monitored by the central processor. As the ambient temperature changes, the central processor compensates for the output level to provide a stable RF output-vs-temperature characteristic.

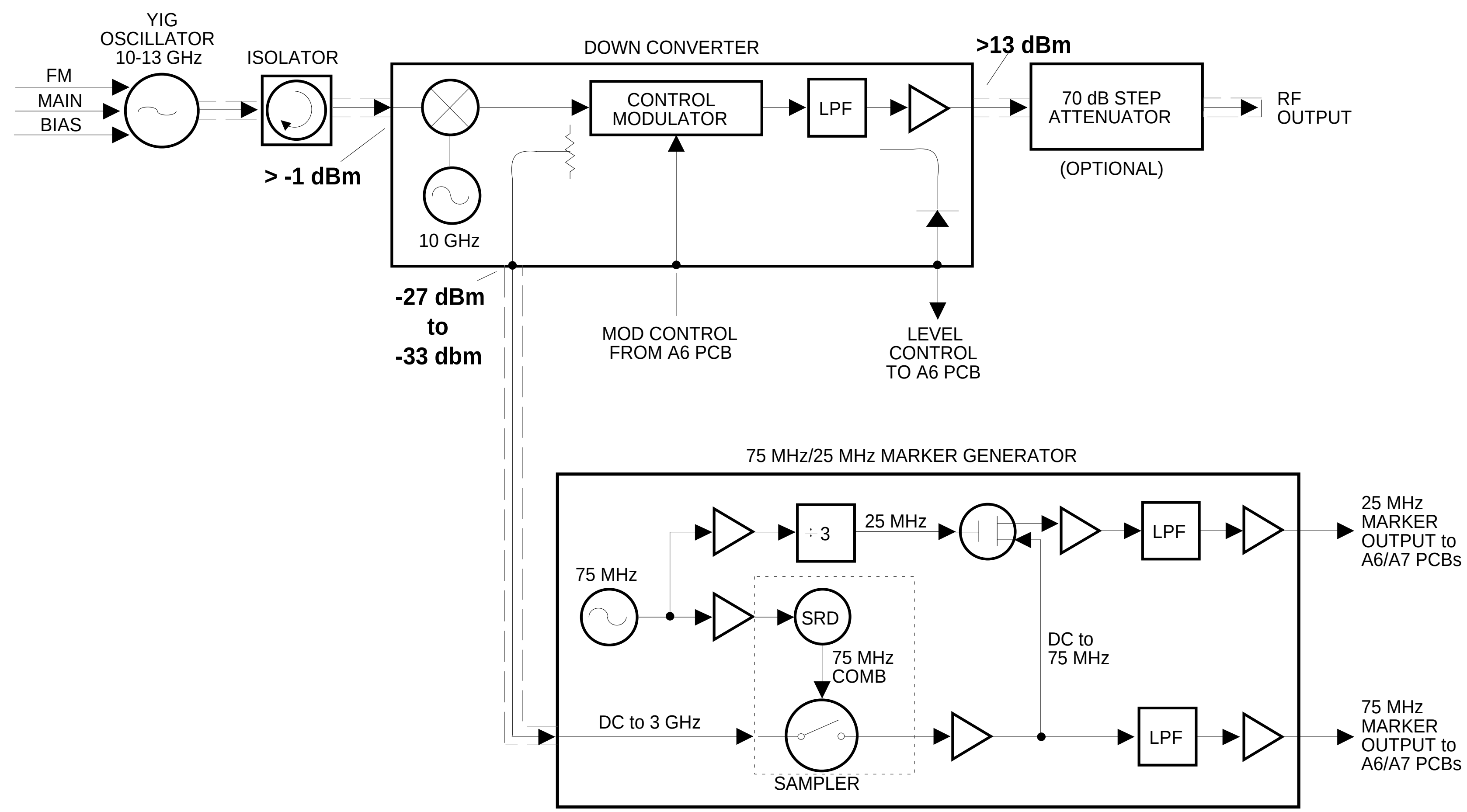


Figure 4-21. *Block Diagram of RF Decks for Models 54107, 54109A, and 54111A*

Within the down converter, a portion of the down-converted RF signal is picked off for input to the 75 MHz/25 MHz Marker Generator. Inside the marker generator, the 75 MHz crystal oscillator output is split into two paths. In one path, the 75 MHz signal is amplified, then goes to the sampler assembly. In the sampler assembly, the step-recovery diode produces a 75 MHz comb signal. This comb signal turns on the sampling diodes that sample the RF signal from the down converter. The output of the sampler is amplified and filtered to produce 75 MHz markers.

In the other path, the 75 MHz signal is amplified, then divided to produce a 25 MHz signal. This 25 MHz signal is applied as the gate input to a FET (field-effect transistor). The source input is a dc to 75 MHz signal from the 75 MHz marker circuitry. The FET output is amplified and filtered to produce 25 MHz markers. The 25 MHz and 75 MHz markers go to a data buffer on the A6 PCB to be read by the central processor.

The central processor processes the 75 MHz and 25 MHz marker read signals from the A6 PCB. If the marker-read signals indicate that the frequency is not source-locked, the A7 central processor generates error correction instructions that are sent to the A6 PCB frequency error correction circuitry. These circuits output a frequency source-lock error correction signal that is sent to A5 YIG Driver/Channel Interface PCB. The output from the A5 YIG driver circuit is a current that causes the FM coil to offset the frequency error, thus producing source-lock of the YIG-tuned oscillator.

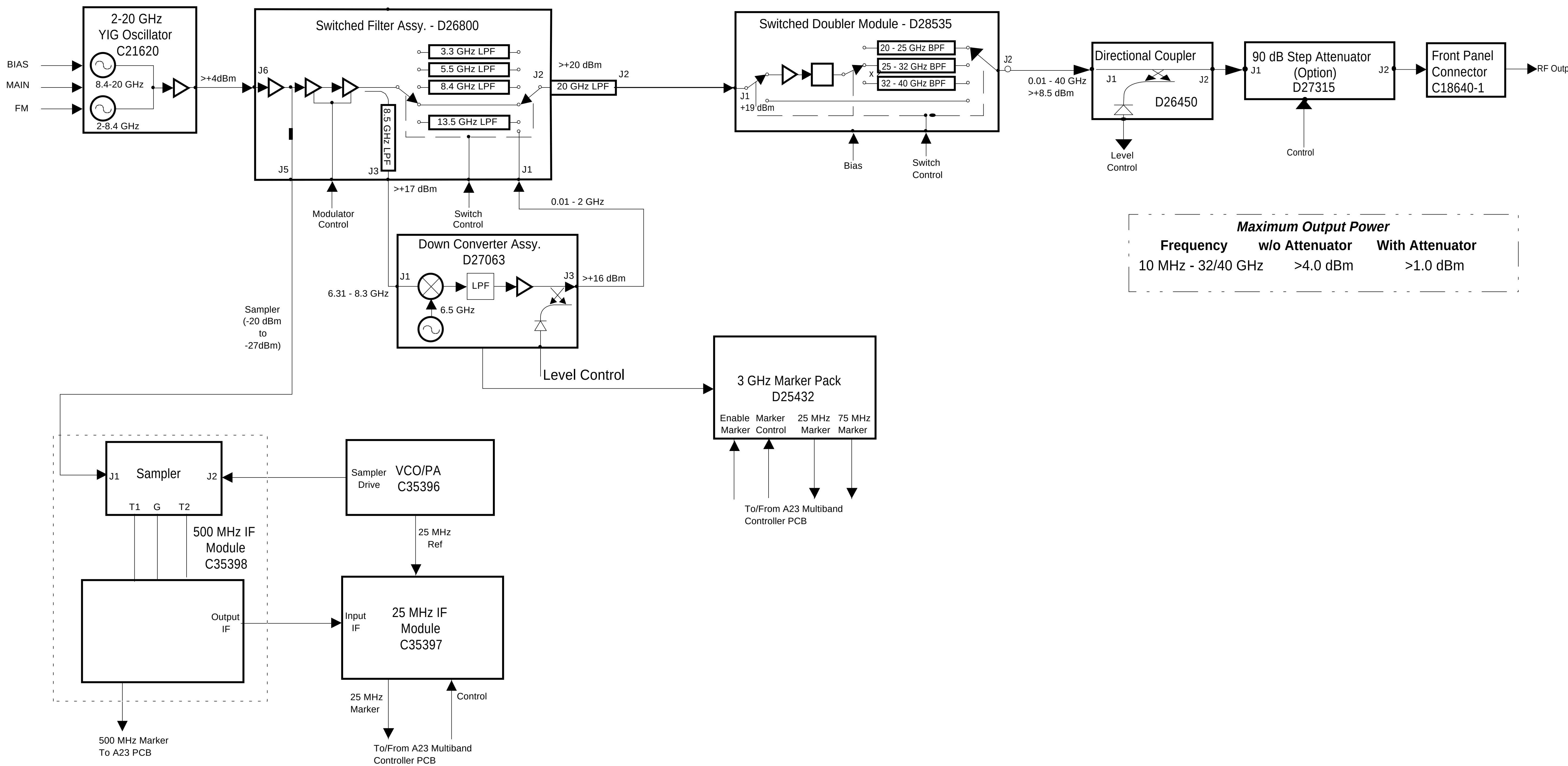
RF Decks for Models 54154A through 54169A

The RF decks of microwave band models 54154A (2.0 to 32 GHz), 54161A (0.01 to 32 GHz), 54163A (2.0 to 40 GHz) and 54169A (0.01 to 40 GHz) are very similar. However, models 54161A and 54169A contain two additional components, a Down Converter and a 25 MHz Marker Generator. These additional components enable these two models to generate RF signals in the frequency range of 10 MHz to 2.0 GHz. Refer to Figure 4-22. during the following functional description.

The output signal from the YIG-tuned Oscillator goes to the Switched Filter Assembly. As shown in Figure 4-22, the switched filter assembly contains a control modulator and a switched filter. After amplification, a portion of the RF signal is sent to the frequency source-lock circuitry (previously described).

There are two inputs to the control modulator section that control the RF output power level — the modulator bias input and the modulator control input. Both of these inputs come from the A24 ALC/ Frequency Instruction PCB. The modulator bias input drives the control modulator PIN switches that switch the RF power on and off. The modulator control input drives the PIN switches that control the power level of the RF output signal.

The output signal from the control modulator section is sent to the switched filter, which contains a coupler to provide a signal for the Down Converter. Whenever these models are generating RF signals in the frequency range of 10 MHz to 2.0 GHz, a 6.31 to 8.3 GHz RF signal is coupled out of the switched filter, through an 8 GHz filter path, and routed to the down converter. In the down converter, this signal is mixed with a 6.3 GHz signal from the down converter's internal oscillator. The resulting 10 MHz to 2.0 GHz signal is sent through a 2 GHz Low-Pass Filter, amplified, and then output to the switched filter. A portion of the down-converted signal is picked off and is input to the 75 MHz/25 MHz Marker Generator.



Maximum Output Power

Frequency	w/o Attenuator	With Attenuator
10 MHz - 32/40 GHz	>4.0 dBm	>1.0 dBm

Figure 4-22. *Block Diagram of RF Deck for Models 54154A through 54169A*

Inside the marker generator, the output from the local 75 MHz crystal oscillator is split into two paths. In one path, the 75 MHz signal is amplified, then goes to the sampler assembly. In the sampler assembly, the step recovery diode produces a 75 MHz comb signal that drives the sampling diodes. These diodes sample the RF signal from the down converter (above). The output of the sampler is amplified and filtered to produce 75 MHz markers (the 75 MHz markers are not used in this application). In the other path, the 75 MHz signal is amplified, then divided to produce a 25 MHz signal. This 25 MHz signal is applied as the gate input to a FET (field-effect transistor). The source input is a dc to 75 MHz signal from the 75 MHz marker circuitry. The FET output is amplified and filtered to produce 25 MHz markers.

The 25 MHz markers are used by the central processor to achieve source-lock. A portion of the RF output signal from the down converter is detected and coupled out as feedback to the ALC circuitry on the A24 PCB. The directional detector also has a built-in thermistor that outputs a resistance representing the detector’s temperature as an input to the A24 PCB.

The switched filter provides rejection of the harmonics that are generated by the 2.0 to 20 GHz YIG-tuned oscillator. In the three 0.01 to 2 GHz models, it also multiplexes between the 10 MHz to 2.0 GHz and 2.0 GHz to 20.0 GHz signals from the down converter during full band sweeps. The 2.0 to 20 GHz RF signal from the control modulator has four filtering paths and one through path. The four filtering paths are:

- 3.3 GHz path
- 5.5 GHz path
- 8.6 GHz path
- 13.5 GHz path

Signals above 13.5 GHz are routed via the through path to the switched filter output. The down converter provides filtering for the 10 MHz to 2.0 GHz RF signal; therefore, the RF signal is multiplexed through to the switched filter output.

The RF signal output from the switch filter is sent via the Switch Doubler to the directional detector for transfer to the RF OUTPUT connector. A portion of the RF output signal is detected and coupled out as feedback to the ALC circuitry on the A24 PCB. In these circuits, the detected RF sample is summed with the control voltage that represents the desired RF output level. The resulting voltage is sent to the control modulator driver circuitry which then drives the control modulator PIN switches to adjust the RF power level output.

For frequencies of 20 GHz to 39.9999 GHz, the RF signal is passed into the switched doubler. Here, the frequency is doubled and filtered before going to the directional detector. For frequencies between 10 MHz and 19.9999 GHz, the switched doubler is set to through-path to allow the RF to pass unmodified to the directional detector.

The directional detector also has a built-in thermistor that outputs a resistance representing the detector's temperature. This resistance is converted to a voltage by the A24 PCB and monitored by the central processor. As the ambient temperature changes, the central processor compensates for the output level to provide a stable RF-output-vs-temperature characteristic.

RF Decks for Model 54177A

The RF deck of microwave band model 54177A (0.01 to 50 GHz) contains a Down Converter and a 25 MHz Marker Generator. These components provide for generating RF signals in the 10 MHz to 2.0 GHz-frequency range. Refer to Figure 4-23. during the following functional description.

The output signal from the YIG-tuned Oscillator goes to the Switched Filter Assembly. As shown in Figure 4-23, the switched filter assembly contains a control modulator and a switched filter. After amplification, a portion of the RF signal is sent to the frequency source-lock circuitry (previously described).

There are two inputs to the control modulator section that control the RF output power level — the modulator bias input and the modulator control input. Both of these inputs come from the A24 ALC/ Frequency Instruction PCB. The modulator bias input drives the control modulator PIN switches that switch the RF power on and off. The modulator control input drives the PIN switches that control the power level of the RF output signal.

The output signal from the control modulator section is sent to the switched filter, which contains a coupler to provide a signal for the Down Converter. Whenever these models are generating RF signals in the frequency range of 10 MHz to 2.0 GHz, a 6.31 to 8.3 GHz RF signal is coupled out of the switched filter, through an 8 GHz filter path, and routed to the down converter. In the down converter, this signal is mixed with a 6.3 GHz signal from the down converter's internal oscillator. The resulting 10 MHz to 2.0 GHz signal is sent through a 2 GHz Low-Pass Filter, amplified, and then output to the switched filter. A portion of the down-converted signal is picked off and is input to the 75 MHz/25 MHz Marker Generator.

Inside the marker generator, the output from the local 75 MHz crystal oscillator is split into two paths. In one path, the 75 MHz signal is amplified, then goes to the sampler assembly. In the sampler assembly, the step recovery diode produces a 75 MHz comb signal that drives the sampling diodes. These diodes sample the RF signal from the down converter (above). The output of the sampler is amplified and filtered to produce 75 MHz markers (the 75 MHz markers are not used in this application). In the other path, the 75 MHz signal is amplified, then divided to produce a 25 MHz signal. This 25 MHz signal is applied as the gate input to a FET (field-effect transistor). The source input is a dc to 75 MHz signal from the 75 MHz marker circuitry. The FET output is amplified and filtered to produce 25 MHz markers.

The 25 MHz markers are used by the central processor to achieve source-lock. A portion of the RF output signal from the down converter is detected and coupled out as feedback to the ALC circuitry on the A24 PCB. The directional detector also has a built-in thermistor that outputs a resistance representing the detector's temperature as an input to the A24 PCB.

The switched filter provides rejection of the harmonics that are generated by the 2.0 to 20 GHz YIG-tuned oscillator. It also multiplexes between the 10 MHz to 2.0 GHz and 2.0 GHz to 20.0 GHz signals from the down converter during full band sweeps. The 2.0 to 20 GHz RF signal from the control modulator has four filtering paths and one through path. The four filtering paths are:

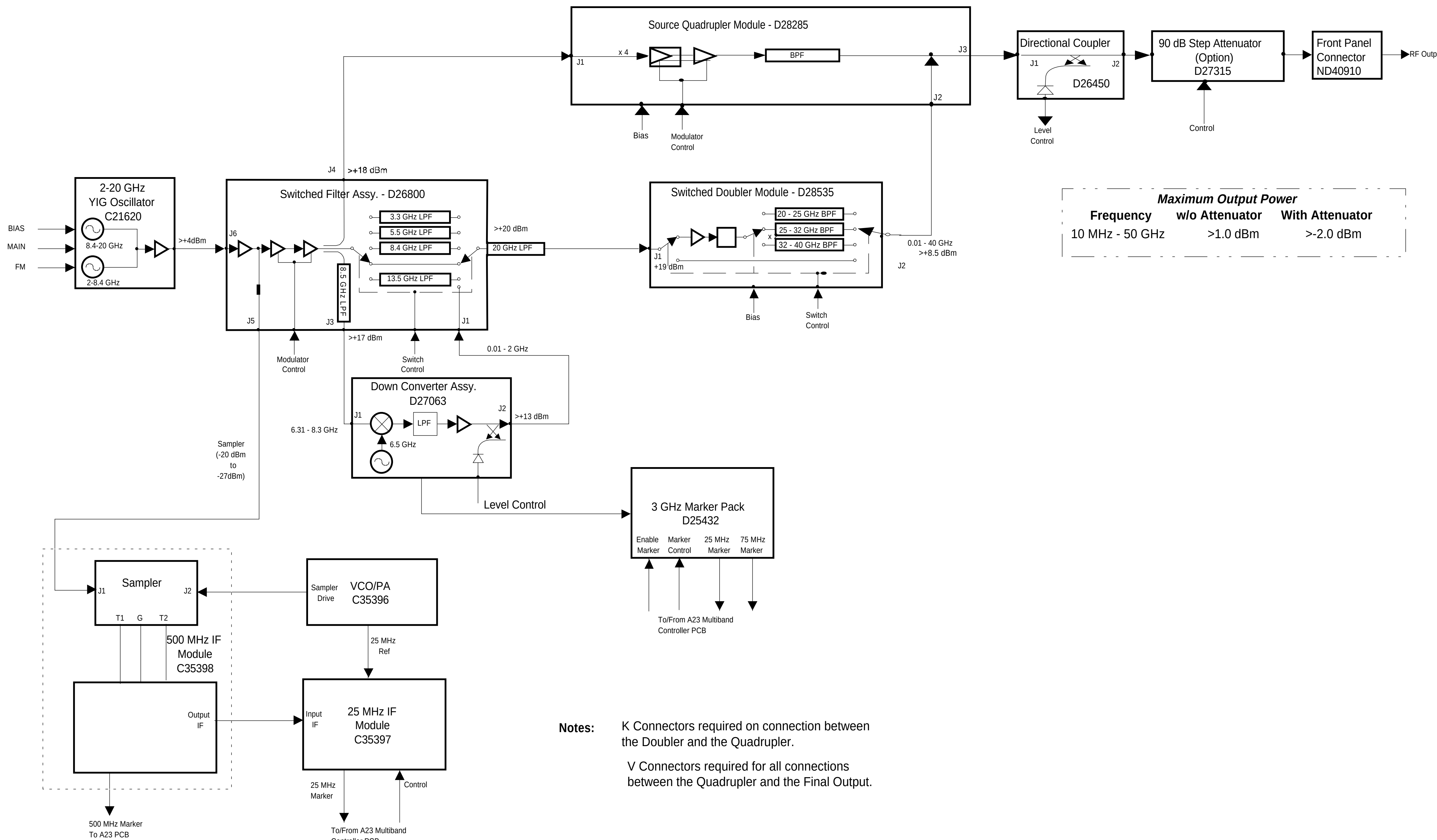
- 3.3 GHz path
- 5.5 GHz path
- 8.6 GHz path
- 13.5 GHz path

Signals above 13.5 GHz are routed via the through path to the switched filter output. The down converter provides filtering for the 10 MHz to 2.0 GHz RF signal; therefore, the RF signal is multiplexed through to the switched filter output.

The RF signal output from the switch filter is sent via the Switch Doubler to the directional detector for transfer to the RF OUTPUT connector. A portion of the RF output signal is detected and coupled out as feedback to the ALC circuitry on the A24 PCB. In these circuits, the detected RF sample is summed with the control voltage that represents the desired RF output level. The resulting voltage is sent to the control modulator driver circuitry which then drives the control modulator PIN switches to adjust the RF power level output.

For frequencies of 20 GHz to 39.9999 GHz the RF signal is passed into the switched doubler. Here the frequency is doubled and filtered before going to the directional detector via the forward coupler. The forward coupler is used to connect either 0.01 GHz to 40 GHz or 40 GHz to 50 GHz RF to the directional detector. The forward coupler is a passive component and is not driven by DC supplies or PIN driver circuits. For frequencies between 10 MHz and 19.9999 GHz the switched doubler is set to through path to allow the RF to pass unmodified to the directional detector. For frequencies between 40 GHz and 50 GHz, the switched doubler is left open-circuit and the quadrupler module is driven by the switched filter. The output from the quadrupler module is routed to the directional detector via the forward coupler.

The directional detector also has a built-in thermistor that outputs a resistance representing the detector's temperature. This resistance is converted to a voltage by the A24 PCB and monitored by the central processor. As the ambient temperature changes, the central processor compensates for the output level to provide a stable RF-output-vs-temperature characteristic.



Maximum Output Power

Frequency	w/o Attenuator	With Attenuator
10 MHz - 50 GHz	>1.0 dBm	>-2.0 dBm

Notes: K Connectors required on connection between the Doubler and the Quadrupler.

V Connectors required for all connections between the Quadrupler and the Final Output.

Figure 4-23. *Block Diagram of RF Deck for Model 54177A*

4-13 PSU EXTENSION MODULE

The PSU (power supply unit) extension module (Figure 4-24) is only installed on Models 54154A through 54177A. It is mounted on the inside rear panel next to the line input filter. It provides additional DC voltages that are both used on the RF deck and routed through the A23 Multiband Controller PCB.

The circuit taps the +165V and –165V rectified DC from the main A9 Power Supply PCB, then it DC-to-DC converts it to +12 volts. This voltage is then regulated by three discrete DC regulators to produce three additional supplies –5V, +10V and +8V.

The PSU will not power up until it senses the presence of –15 volts from the A9 PCB. This voltage then generates the –5 volts, which turns the DC to DC converter on. This control is isolated using optical isolator IC U1.

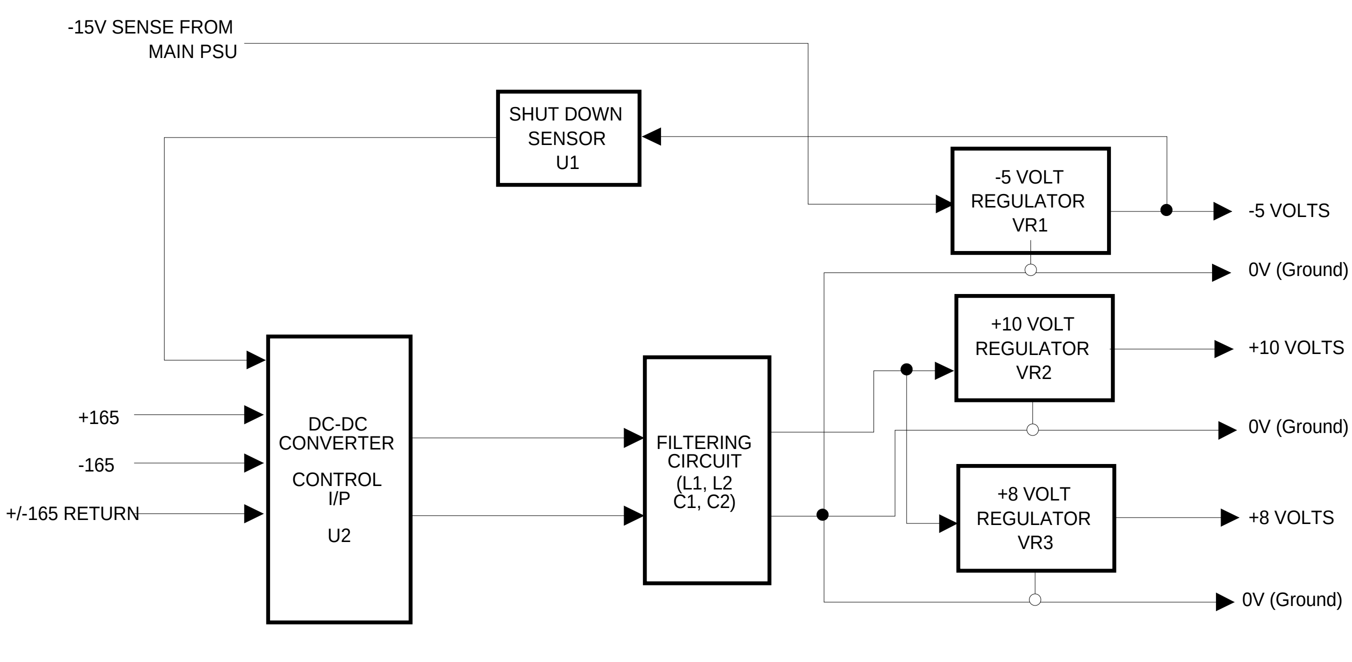


Figure 4-24. *Power Supply Unit (PSU) Extension Module*

4-14 A19/A23 MULTIBAND CONTROLLER PCB

This A19 Multiband PCB is used on Models 54137A and 54147A, and the A23 Multiband PCB is used on 54154A through 54177A. Their circuitry is virtually identical. They peform the following main functions :-

- Power supply voltages are generated for the Switched Filter and the YIG Oscillator. There are six separate DC power supplies generated on the PCB. A +7V and +8V supply is generated by VR1 and VR2, respecitively, for the Switched Filter. Two +8V supplies for the YIG oscillator generated by Q1, Q2, and Q3 for the 2—8.4 GHz frequency range and Q5, Q6, and Q7 for the 8.4—20 GHz frequency range. These two +8V supplies are turned on and off by control circuitry U11, U2 and U3. Note only one +8V supply is on at one time. The fixed suplies to the YIG +6V and -5V are generated by Q8, Q9, Q10, and U5 for the +6V and Q11 and U4 for the -5V supply.
- Pin switch filter drivers are used to control filter and frequency switching elements located in the Switched Filter. They are located and controlled on the board. The drivers are controlled by analog switches U9, U10 and U18. The current for the pin switches comes from transistors U12, U13, Q12 thru Q20 and Q29.
- The ALC modulator driver for the levelling loop below 40 GHz. Analogue switch U8 and amplifier U6 make up part of the levelling loop control on this board.
- Connections from the A4 Motherboard PCB to the VCO/PA module, the 500/25MHz modules and 0.1 to 2.0GHz 25MHz marker module are routed through the PCB. DC supplies and signal/control line connect at J1 and are redistributed via J4 for the VCO/PA module, J5 for the 500/25MHz module, J6 the 0.01—2.0GHz 25MHz marker pack asembly and J9 for the Quadrupler assembly.
- The YIG notch filter driver is located on the board. Analogue switch U10 and currect driver U13 provide control of the notch filter.
- A +10 volt reference circuit generated by U1.
- Pin switch drivers used to control filter and frequency switching elements located in the Switched Doubler module are located and controlled on the board. The drivers are controlled by data latch U14 and address decoder U16. The pin driver control lines are driven by U15, U17, and Q21 through Q28.

Chapter 5
Performance Verification Procedures

Table of Contents

Chapter 5
Performance Verification Procedures

5-1 INTRODUCTION

This chapter provides performance verification procedures for all standard models of ANRITSU 541XXA Network Analyzers. All of the tests in this chapter are performed using the 541XXA front panel controls and screen displays. No internal circuits or adjustments are disturbed. If the results of all tests are within specification, the 541XXA is operating normally and does not require calibration.

5-2 RECOMMENDED TEST EQUIPMENT

The recommended test equipment for each of the performance verification tests is listed along with the procedure for each test. All of the test equipment used in these tests is also listed in Table 1-11 (in Chapter 1, “General Information”). If the recommended equipment is not available, then other test equipment with suitable characteristics may be substituted.

NOTE

Allow all test equipment to warm up at least 30 minutes prior to performing any of the performance verification tests.

5-3 TEST RECORDS

Pages 5-35 through 5-46 contain test record forms that can be photocopied and used to keep an accurate performance verification test record for your 541XXA. These tables are included as part of the performance verification procedures and individual procedures contain test information for applicable 541XXA models.

5-4 CW FREQUENCY ACCURACY TEST

This test verifies that the CW frequency accuracy of the 541XXA tested is within specification. Pages 5-35, 5-39, and 5-43 contain a test records that you can copy and use to record the results of the tests.

Equipment Required

☐ Microwave Frequency counter, EIP Microwave Inc. model 578A, or equivalent.

☐ Impedance Adaptor, 50Ω to 75Ω, ANRITSU 12N75B. (Required only for 541XXA's with 75Ω Signal Source outputs.)

☐ N-female-to-N-female adapter, 50Ω.

☐ Precision adaptor, V to K female, 34VKF50

Procedure

Step 1. Connect the test equipment as shown in Figure 5-1 and turn the equipment on.

SYSTEM MENU
DISK UTILITIES
SYSTEM SETUP
DATA POINTS
RESET
CONFIGURE:
SOURCE
ANALYZER
PLOTTER
APPLICATIONS
GPIB MODE
USE ◆ THEN
PRESS SELECT

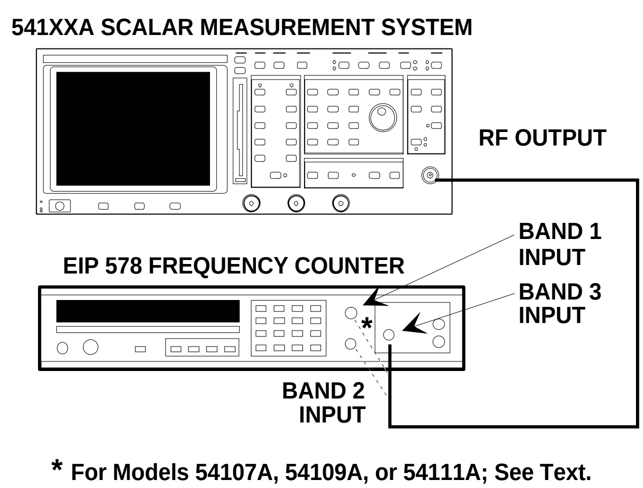


Figure 5-1. *Test Setup for CW Frequency Accuracy Test*

Step 2. Press the System Menu key and select **RESET** from the displayed menu (left) using the Menu up/down and Select keys.

RESET MENU

RESET IS
CONFIGURED
TO KEEP:

CAL DATA

MARKERS

LIMITS

RESET

RESET TO FACTORY DEFAULTS

USE ◆ THEN
PRESS SELECT

Step 3. From the RESET MENU (top left) select **RESET TO FACTORY DEFAULTS.**

Step 4. Turn both 541XXA measurement channels off using the DIsplay On/Off keys.

Step 5. Set the Frequency Counter to measure 1 kHz resolution.

For models with 75Ω output, connect to the counter input using the 12N75 Impedance Adaptor.

FREQUENCY MENU

CENTER
XX.XXXX GHz:

WIDTH
0.0000 GHz

PRESS SELECT
FOR
START/STOP

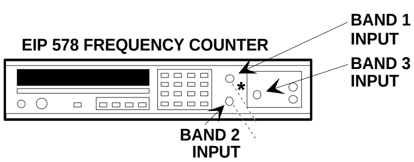
Step 6. Press the 541XXA Frequency key; then press the Select key. This displays the Center/Width menu (middle left).

Step 7. Set the **WIDTH** value to 0.0000 GHz (or MHz, depending on model).

Step 8. Set the **CENTER** frequency to the first test frequency for the model being tested (Page 5-35, 5-39, or 5-43).

NOTE

When a frequency is entered, it is Frequency Locked to the reference and then released. After being released, the frequency may drift. Pressing the CLEAR key and then the Select key re-locks the frequency. (During normal operation, the frequency is locked at the start of every sweep, even if the width is set to zero.)



Step 9. Set the counter to the correct range, and connect the 541XXA to the correct counter input (Band 1, Band 2, or Band 3, bottom left) for the frequency being measured.

NOTE

For 54107A, 54109A, or 54111A, connect to the Band 1 input.

Step 10. Verify that the counter reading is within ±100 kHz of the value shown on the test record for 54107A, 54109A, and 54111A. For all other models, verify that it is within ±200 kHz.

Step 11. Record the counter readings in the appropriate test record (Page 5-35, 5-39, or 5-43).

Step 12. Enter the next test frequency from the test record into the 541XXA. Repeat steps 6 thru 11 until all the test frequencies in the test record have been tested.

5-5 OUTPUT POWER ACCURACY/ FLATNESS TEST

This test verifies that the output power produced by the 541XXA RF source is within specified limits throughout the frequency range of the unit. The specifications for each model are listed in Table D-5 (Appendix D). A test record that you can copy and use to record test results is contained on applicable pages 5-35, 5-40, and 5-44.

Equipment Required

☐ Anritsu ML4803A Power Meter.

☐ Anritsu MA4601A power sensor for 54107A, 54109A, and 54111A with 50Ω Signal Source output.

☐ Anritsu MA4603A power sensor and J0365 Conversion Connector for 54107A,54109A, and 54111A with 75Ω Signal Source output.

☐ Anritsu MA4701A/MA4702A power sensors for 54117A through 54131A and model 54147A.

☐ Anritsu MA4703A/MA4704A power sensors for 54136A.

☐ HP436A power meter, Sensor 8487A, and Precision Adaptor 34VKF50 for 54154A through 54169A.

☐ HP436A power meter and Sensor 8487A, for 54177A.

Refer to Chapter 1, Table 1-2 (Recommended Test Equipment) for further information, as required.

Procedure

For 54111A through 54147 connect high-power sensor MA4701A or MA4703A, as appropiate, to the power meter. Perform a calibration as instructed in the Anritsu ML4803A operations and service manual.

For models 54107A, 54109A, and 54111A equipped with a 50Ω signal source output: connect the MA4601A power sensor to the power meter and perform a calibration.

For units equipped with a 75Ω signal source output, the J0365 Conversion Connector must be used in conjunction with the MA4603A power sensor. Refer to the operating procedure in the Anritsu ML4803A operations and service manual.

For 54154 through 54177A use the HP436A power meter and the 8487A sensor. For 54154 through 54169 use a 34VFK50 precision adaptor to connect sensor to RF Output connector.

Step 1. Set up the equipment as shown in Figure 5-2, and turn the equipment on.

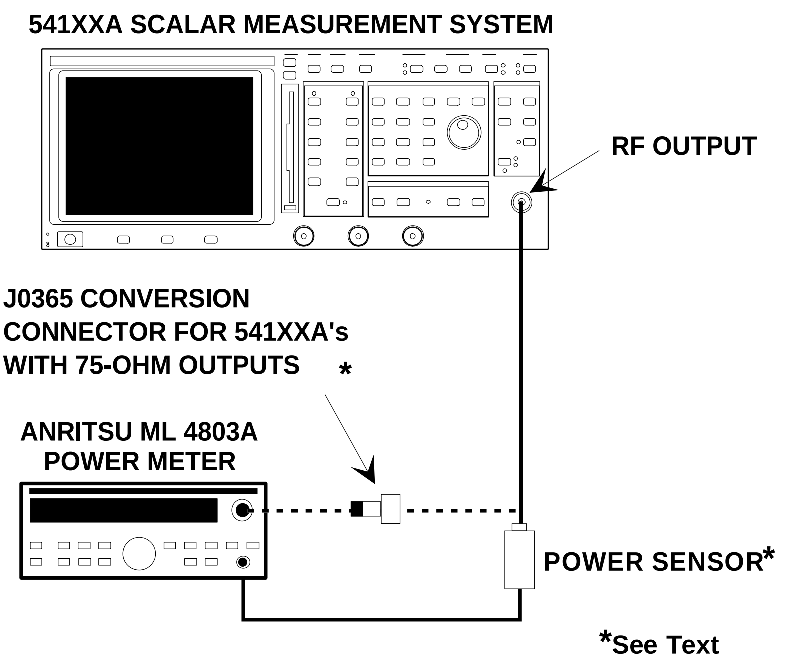


Figure 5-2. *Test Setup for Output Power Accuracy/ Flatness Test*

SYSTEM MENU
DISK UTILITIES
SYSTEM SETUP
DATA POINTS
RESET
CONFIGURE:
SOURCE
ANALYZER
PLOTTER
APPLICATIONS
GPIB MODE
USE ◆ THEN PRESS SELECT

Step 2. Press the System Menu key and select **RESET** from the displayed menu (top left) using the MENU up/down and SELECT keys.

RESET MENU
RESET IS CONFIGURED TO KEEP:
CAL DATA
MARKERS
LIMITS
RESET
RESET TO FACTORY DEFAULTS
USE ◆ THEN PRESS SELECT

Step 3. From the RESET MENU (bottom left) select **RESET TO FACTORY DEFAULTS.**

Step 4. Turn both measurement channels off using the Display On/Off keys.

Step 5. Press the Output Power key and set the power as shown in the applicable test record.

FREQUENCY MENU

CENTER
XX.XXXX GHz:

WIDTH
0.0000 GHz

PRESS SELECT FOR START/STOP

Step 6. Press the Frequency key then press the Select key to display the Center/Width menu (left).

NOTE

Having several copies of the test record available as worksheets will prove to be useful while performing the remainder of this procedure.

Step 7. Set the frequency **WIDTH** to 0.0000 GHz (or MHz, depending on model).

Step 8. Set the **CENTER** frequency to the first value listed in appropriate test record page 5-35, 5-39, or 5-45. For example: 0.0100 GHz for the 54117A.

NOTE

Ensure that the power meter sensor is connected to the 541XXA RF output and that the power meter Cal Factor is set correctly for the frequency under test.

Step 9. Read and record (on scratch paper) the power meter value.

Step 10. Verify that the power level is within the "Power Level Accuracy" specification in Table 5-1 or 5-2.

Step 11. Change the 541XXA **CENTER** frequency to the next frequency listed in the test record.

Step 12. Read and record (on scratch paper) the power meter value.

Step 13. Verify that the power level is within the "Leveled Power Variation" specification in Table 5-1 or 5-2.

Step 14. Repeat steps 11 and 13 until the 541XXA RF power has been measured at all of the frequencies listed in the test record. Record the highest and lowest power readings in the applicable test record.

NOTES

For 54111A equipped with 75Ω signal source output, *this measurement is possible only to 2.0 GHz, maximum.*

Step 15. Calculate the power flatness by substracting the "Min Power dBm" value recorded in the test record from the"Max Power dBm" value.

Step 16. Record the calculated flatness value in the "Flatness Difference, Max–Min" column of the test record.

Step 17. Verify that the max-min values are within the "Leveled Power Variation" specification listed in Table 5-1.

Step 18. Set the power level to the next value shown in the applicable test record. For power levels below –20 dBm see notes below.

Step 19. Low power sensors are not available for frequencies above 26 GHz. Therefore, go to step 21 for either of the conditions listed below.

- For 54154A through 54169A with an internal attenuator and a set-power of less than –9 dBm.
- For 54177A with internal step attenuator and a set-power of less than –12 dBm.

Step 20. Repeat steps 6 thru 18 until all the power levels in the applicable test record have been tested.

NOTES

- When measuring –20 dBm and below, use the appropriated power sensor as described below.

  For all models, 54117A thru 54147A: When measuring power levels –20 dBm and below, connect the appropriate low power sensor (MA4702A or MA4704A) to the power meter. Perform a calibration and set the Cal Factor for the 541XXA frequency being measured.

  For models 54107A, 54109A, and 5411A equipped with 50Ω signal source output: When measuring power levels –20 dBm and below, connect the *MA4702A low power sensor* to the power meter. Perform a calibration and set the Cal Factor for the 541XXA frequency being measured. *Use 10 MHz as the lowest frequency when performing these tests.*

- For units equipped with 75Ω signal source output, measurement below –30 dBm is not possible with the equipment specified.

Table 5-1. *Output Power Specifications, RF Band Models*

Specification[1]		Units	Models		
			54107A	54109A	54111A
Output Power	Internally Leveled, Maximum	dBm	+12[2]	+12[2]	+122
	With Option 2, 2A, or 2B; 70 db Step Attenuator (10 dB Steps)	dBm	+10[2]	+102	+10[2]
Power Level Accuracy	With Leveled Power	dB	±1.0[3]	±1.0[3]	±1.0[3]
	With Option 2, 2A, or 2B; 70 db Step Attenuator (10 dB Steps)	Add dB	±1.0[3]	±1.0[3]	±1.5[3]
	Step Attenuator Accuracy, Between 10 dB Steps	dB	±0.4	±0.4	±0.4
Leveled Power Variation	With Frequency	dB	±0.3[3]	±0.4[3]	±0.6[3]
	With Option 2, 2A, or 2B; 70 db Step Attenuator (10 dB Steps)	dB	±1.0[3]	±1.1[3]	±1.3[3]

1, At maximum specified output power
2, For Option 4, 75W output, substract 2.0 dB
3, For Option 4, 75W output, add 0.2 dB

Table 5-2. *Output Power Specifications, Microwave Models*

Specification[1]		Units	Models 541_ _												
			17A	19A	28A	30A	31A	36A	37A	47A	54A	61A	63A	69A	77A
Output Power	Internally Leveled, Maximum	dBm	+10	+10	+10	+10	+10	+7	+10	+10	+4	+4	+4	+4	+1
	With Option 2, 2A, or 2B; 70 db Step Attenuator (10 dB Steps)	dBm	+7	+7	+7	+7	+7	+4	+7	+7	+1	+1	+1	+1	–2
Power Level Accuracy	With Leveled Power	dB	±1.0	±1.0	±1.0	±1.0	±1.0	±1.0	±1.0	±1.0	±1.0	±1.0	±1.0	±1.0	±1.0
	With Option 2, 2A, or 2B; 70 db Step Attenuator (10 dB Steps)	Add dB	±1.5	±1.5	±1.5	±1.5	±1.5	±3.0	±1.9	±1.9	±3.0	±3.0	±3.0	±3.0	±4.0
Leveled Power Variation	With Frequency	dB	±0.5	±0.5	±0.4	±0.5	±0.4	±1.0	±0.5	±0.75	±2.0	±2.0	±2.0	±2.0	±3.0
	With Option 2, 2A, or 2B; 70 db Step Attenuator (10 dB Steps)	dB	±1.0	±0.9	±0.9	±1.0	±0.9	±2.5	±1.0	±1.0	±2.0	±2.0	±2.0	±2.0	±3.0

1, At maximum specified output power
2, For Option 4, 75W output, substract 2.0 dB
3, For Option 4, 75W output, add 0.2 dB

SYSTEM MENU
DISK UTILITIES
SYSTEM SETUP
DATA POINTS
RESET
CONFIGURE:
SOURCE
ANALYZER
PLOTTER
APPLICATIONS
GPIB MODE
USE ◆ THEN PRESS SELECT

RESET MENU
RESET IS CONFIGURED TO KEEP:
CAL DATA
MARKERS
LIMITS
RESET
RESET TO FACTORY DEFAULTS
USE ◆ THEN PRESS SELECT

NOTE

Flatness measurements for 54154A through 54177A at low power levels are made using a detector not a power sensor. Therefore a new set up and measurement procedure is required for these units only at low power levels. Only do steps 21 to 32 for these models. For all others go to paragraph 5-6, Signal Channel Verification.

Step 21. Press the System Menu key and select **RESET** from the displayed menu.

Step 22. Press the Channel 2 Display On/Off key to off.

Step 23. Press the Channel 1 Menu key

Step 24. Using the Menu up/down and Select keys, configure the 541XXA for a power measurement using Input A , as follows:

- Choose **SELECT INPUT**, from the CHANNEL menu (below).
- Choose **NON-RATIO A**, from the SELECT INPUT menu (below).

CHANNEL: 1 INPUT: A
TRANSMISSION
RETURN LOSS
SWR
POWER
DTF
VIEW CAL
SELECT INPUT
TRACE MEMORY
REF LINE
USE ◆ THEN PRESS SELECT

CHANNEL: 1 SELECT INPUT
NON-RATIO
A
B
R
RATIO:
A/R
B/R
USE ◆ THEN PRESS SELECT

SYSTEM MENU

DISK UTILITIES

SYSTEM SETUP

DATA POINTS

RESET

CONFIGURE:

SOURCE

ANALYZER

PLOTTER

APPLICATIONS

GPIB MODE

USE ◆ THEN PRESS SELECT

Step 25. Select **POWER,** when you are returned to the CHANNEL menu.

Step 26. Press the Output Power key, and set power level as shown below.

- For 54154A through 54169A: –14 dBm.
- For 54177A: –17 dBm.

Step 27. Press the System Menu key and select **DATA POINTS** from the displayed menu (top left).

Step 28. Select **101** from the **FREQUENCY DATA POINTS** menu (bottom left).

Step 29. Connect a detector from the RF Output connector to the signal channel A connector.

FREQUENCY DATA POINTS

51

101

201

401

USE ◆ THEN PRESS SELECT

AVERAGING CHANNEL 1
OFF
2 SWEEPS
4 SWEEPS
8 SWEEPS
16 SWEEPS
32 SWEEPS
64 SWEEPS
128 SWEEPS
256 SWEEPS
SET CHAN 2
COUPLE CHANNELS
USE ◆ THEN PRESS SELECT

Step 30. For power levels of –44 dBm or below:

- Press the Averaging key.
- Select **64 SWEEPS** from the displayed menu (left), using the Menu up/down and Select keys.
- Press Autoscale.
- Wait for the averaging counter to reach 64; then press the Cursor and Select keys.
- Select **OPTIONS** from the displayed menu (bottom left).
- Select **SEARCH FOR MIN-MAX** from the ensuing menu (below).

CURSOR OPTIONS CHANNEL 1
SEARCH FOR MIN-MAX
XX.X dB L FROM MAX
REPEAT SRCH EACH SWEEP
MAIIN MENU
USE ◆ THEN PRESS SELECT

CHANNEL 1 MOVE CURSOR
TO
MAXIMUM
MINIMUM
NEXT MKR
ACTIVE MKR
dB SEARCH X.XX dBr L
SETUP
OPTIONS
SET CHAN 2
USE ◆ THEN PRESS SELECT

- Observe that the results of the search appear in **dB SEARCH** arear of the menu at bottom left. Record this value in the column labeled “541XXA Cursor Reading dBm,” in the test record (page 5-42).
- Verify that the recorded value from the above step is within the leveled “Leveled Power Variation” tolerance specified in Table 5-2.

Step 31. Press the Output Power key and enter the next power level value from the test record.

Step 32. Repeat Step 30.

5-6 SIGNAL CHANNEL VERIFICATION TESTS, OVERVIEW

The signal channel verification is made up of three separate procedures.

- The first procedure (paragraph 5-7) is a DC voltage calibration method test where a known DC voltage is injected into the input of the 541XXA.
- The second procedure (paragraph 5-8) is a 50 MHz RF verification test using the Anritsu power meter 50 MHz, 0dBm power reference as a standard.
- The third procedure (paragraph 5-9) is a mid-band frequency test that uses a known RF input. This test is susceptible to various measurement uncertainties, which are explained at the beginning of the procedure.

5-7 SIGNAL CHANNEL VERIFICATION, DC VOLTAGE METHOD

The dc voltage method uses highly accurate dc voltages to simulate input RF power inputs. This test introduces the fewest source errors. A 560-10BX adaptor cable is used to connect the output of the DC Voltage Calibrator to the input of the 541XXA.

SYSTEM MENU
DISK UTILITIES
SYSTEM SETUP
DATA POINTS
RESET
CONFIGURE:
SOURCE
ANALYZER
PLOTTER
APPLICATIONS
GPIB MODE
USE ◆ THEN PRESS SELECT

Equipment Required

☐ Fluke 343A DC Voltage Calibrator

☐ ANRITSU 560-10BX Adapter Cable

☐ BNC-female-to-banana-plug adapter

Procedure

Step 1. Set up the equipment as shown in Figure 5-3, and turn the equipment on.

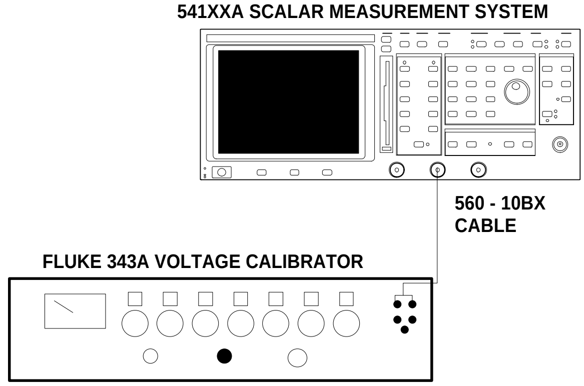


Figure 5-3. *Signal Channel Verification, DC Voltage Method Test Setup*

RESET MENU
RESET IS CONFIGURED TO KEEP:
CAL DATA
MARKERS
LIMITS
RESET
RESET TO FACTORY DEFAULTS
USE ◆ THEN PRESS SELECT

Step 2. Press the System Menu key and select **RESET** from the displayed menu (top left), using the Menu up/down and Select keys.

Step 3. From the **RESET MENU** (bottom left) select **RESET TO FACTORY DEFAULTS**.

Step 4. Press the Channel 2 Display On/Off key to off.

CHANNEL: 1
INPUT: A

TRANSMISSION

RETURN LOSS

SWR

POWER

DTF

VIEW CAL

SELECT INPUT

TRACE MEMORY

REF LINE

USE ◆ THEN
PRESS SELECT

Step 5. Press the Channel 1 Menu key

Step 6. Using the Menu up/down and Select keys, configure the 541XXA for a power measurement using Input A , as follows:

- Choose **SELECT INPUT**, from the CHANNEL menu (top left)

- Choose **NON-RATIO A**, from the SELECT INPUT menu (middle left).

- Select **POWER,** when you are returned to the CHANNEL menu.

CHANNEL: 1
SELECT INPUT

NON-RATIO

A

B

R

RATIO:

A/R

B/R

USE ◆ THEN
PRESS SELECT

Step 7. Turn the dc voltage calibrator output to off.

This calibrator will be used as a zero volt reference input to the 541XXA.

CALIBRATION

START CAL

DETECTOR
OFFSETS

DC CAL MENU

PRESS CLEAR
TO RETURN TO
MEASUREMENT
MODE

USE ◆ THEN
PRESS SELECT

Step 8. Press the Calibration key.

Step 9. Select **DC CAL MENU,** from the displayed menu (bottom left).

Step 10. Allow the 541XXA to sweep for 5 seconds.

SET DC CAL

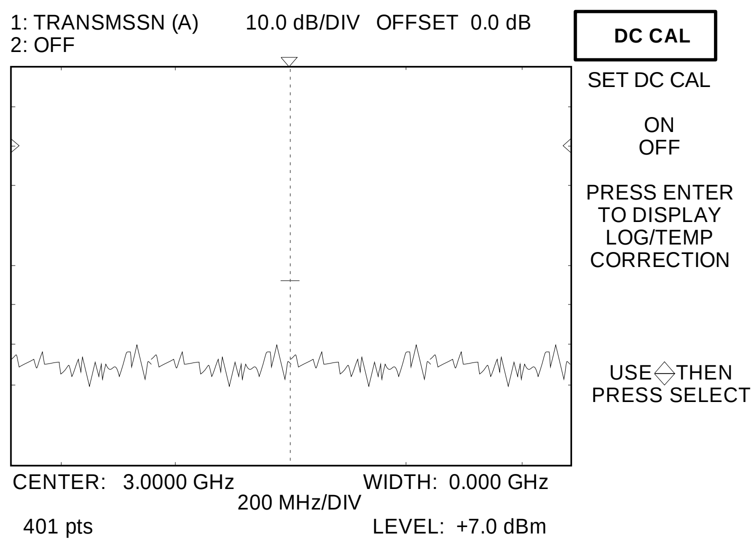
ON
OFF

PRESS ENTER
TO DISPLAY
LOG/TEMP
CORRECTION

USE ◆ THEN
PRESS SELECT

Step 11. With the **SET DC CAL** menu (left) displayed , use the Menu up/down keys to highlight **ON**; then press the Select key.

Step 12. Observe that the 541XXA displays a noise floor on Channel 1 in power mode (below), and that **DC CAL** is displayed in the top right hand corner of the screen display.



CURSOR

1: XX.XX dB
2: XX.XX dB
XX.XXXX GHz
(XX.XXXX GHz)

PRESS SELECT
FOR
CURSOR MENU

Step 13. Set the dc voltage calibrator output to the first value listed in the applicable test record (pages 5-35 through 5-46).

Step 14. Press the Cursor On/Off key to obtain a cursor readout on the 541XXA display.

Step 15. Verify that the cursor menu (bottom left) readout value is within the tolerance specified in the test record. Record the readout value in the table.

Step 16. Repeat steps 14 and 15 for the remaining two voltage values in the test record.

Step 17. Move the dc voltage calibrator connection to Input B

Step 18. Repeat steps 6 through 16 for signal channel input **NON-RATIO B**.

Step 19. Move the dc voltage calibrator connection to Input R, if installed.

Step 20. Repeat steps 6 through 16 for signal channel input **NON-RATIO R.**

5-8 SIGNAL CHANNEL VERIFICATION, 50MHz ACCURACY TEST

For the below models do not perform this test; skip to paragraph 5-9.

54107A
54109A
54111A
54117A
54147A
54161A
54169A
54177A

This test confirms the performance of the 541XXA at 50 MHz using reference signals of 0 dBm and –30 dBm.

NOTE

If the 541XXA being tested is one of the models shown in the table at left, skip this test and go directly to paragraph 5-9 (Mid-Band Frequency RF Test).

The 50 MHz calibration output of the Anritsu power meter is used as the 0 dBm reference signal for this test. This same reference signal is used in conjunction with the 30 dB attenuator from the Anritsu MA4702A power sensor to produce the –30 dBm reference signal. The measurement performance of the 541XXA at 50 MHz can thus be confirmed at these two levels.

During the test, the 541XXA is set to the DC CAL mode to measure the fixed power output of the power meter. This mode enables the 541XXA to make accurate power measurements by disabling the auto zero function of each signal channel.

Equipment Required

☐ Anritsu ML4803A Power Meter

☐ Anritsu MP47A 30 dB Attenuator

☐ RF Detector, ANRITSU 560-7N50B for all models except 54136A
RF Detector, ANRITSU 560-7K50 for 54136A

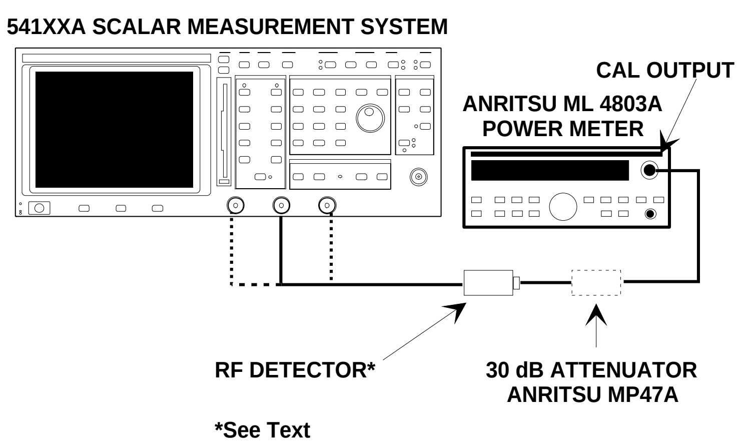


Figure 5-4. *Signal Channel Verification, 50 MHz Accuracy Test Setup*

Procedure

Step 1. Set up the equipment as shown in Figure 5-4, and turn the equipment on.

Step 2. Press the System Menu key and select **RESET** from the displayed menu (top left), using the Menu up/down and Select keys.

SYSTEM MENU
DISK UTILITIES
SYSTEM SETUP
DATA POINTS
RESET
CONFIGURE:
SOURCE
ANALYZER
PLOTTER
APPLICATIONS
GPIB MODE
USE ◆ THEN PRESS SELECT

Step 3. From the **RESET MENU** (bottom left) select **RESET TO FACTORY DEFAULTS**.

RESET MENU
RESET IS CONFIGURED TO KEEP:
CAL DATA
MARKERS
LIMITS
RESET
RESET TO FACTORY DEFAULTS
USE ◆ THEN PRESS SELECT

Step 4. Turn Channel 2 off by pressing the Channel 2 Display On/Off key.

Step 5. Press the Channel 1 Menu key

Step 6. Using the Menu up/down and Select keys, configure the 541XXA for a power measurement using Input A , as follows:

- Choose **SELECT INPUT**, from the CHANNEL menu (below)

CHANNEL: 1 INPUT: A
TRANSMISSION
RETURN LOSS
SWR
POWER
DTF
VIEW CAL
SELECT INPUT
TRACE MEMORY
REF LINE
USE ◆ THEN PRESS SELECT

CHANNEL: 1 SELECT INPUT
NON-RATIO
A
B
R
RATIO:
A/R
B/R
USE ◆ THEN PRESS SELECT

- Choose **NON-RATIO A**, from the SELECT INPUT menu (below).
- Select **POWER,** when you are returned to the CHANNEL menu (below)..

CALIBRATION
START CAL
DETECTOR OFFSETS
DC CAL MENU
PRESS CLEAR TO RETURN TO MEASUREMENT MODE
USE ◆ THEN PRESS SELECT

Step 7. Connect the RF detector to the 541XXA Input A connector and to the power meter 50 MHz reference signal connector (CAL OUTPUT).

Step 8. Switch the power meter reference signal off.

Step 9. Press the Calibration key.

Step 10. Select **DC CAL MENU,** from the displayed menu (top left).

Step 11. Allow the 541XXA to sweep for 5 seconds.

Step 12. With the **SET DC CAL** menu (middle left) displayed, use the Menu up/down keys to highlight **ON**; then press the Select key.

SET DC CAL
ON
OFF
PRESS ENTER TO DISPLAY LOG/TEMP CORRECTION
USE ◆ THEN PRESS SELECT

Step 13. Switch the power meter 50 MHz reference signal ON.

Step 14. Press the Cursor key to obtain a cursor menu readout (bottom left).

Step 15. Verify that the 541XXA cursor menu reading is 0.00 dBm ±0.30 dBm.

Step 16. Record the reading in the applicable test record on page 5-36, 5-41, or 5-45.

Step 17. Disconnect the detector from the power meter CAL OUTPUT connector.

Step 18. Connect the 30 dB attenuator between the detector and the CAL OUTPUT connector.

CURSOR
1: XX.XX dB
2: XX.XX dB
XX.XXXX GHz (XX.XXXX GHz)
PRESS SELECT FOR CURSOR MENU

Step 19. Verify that the 541XXA cursor menu readout is 30.00 ±0.45 dBm.

Step 20. Record the reading in the applicable test record or page 5-36, 41 or 5-45.

Step 21. Move the detector connection to Input B

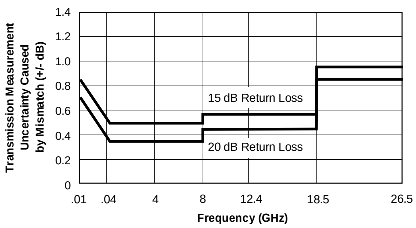
Step 22. Repeat steps 6 through 19 for signal channel input **NON-RATIO B.**

Step 23. Move the detector connection to Input R, if installed.

Step 24. Repeat steps 6 through 19 for signal channel input **NON-RATIO R**.

5-9 SIGNAL CHANNEL VERIFICATION, RF TEST

These measurements confirm the power measurement accuracy of the complete system, including each of the analyzer signal channel inputs. The tests are performed at two points in the dynamic range of the analyzer's signal channels at the a mid-band frequency for the particular 541XXA model. These measurements have inherent inaccuracies, which are explained below. Test records on pages 5-37, 5-42, or 5-46 can be copied and used to provide a test records.

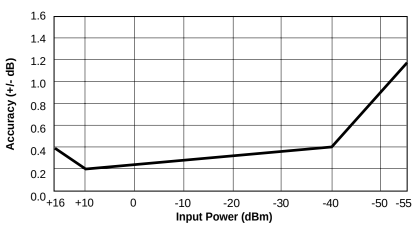


Detector/Source Match Interaction Uncertainty

The mismatch between the RF source and the RF detector contributes a possible error source known as source match uncertainty. This uncertainty is dependent on the return loss of the detector, the input source impedance, and the power level measured. The chart at top-left shows the possible mismatch error related to the return loss of the detector and the frequency measured.

Source Harmonics

In the linear range of the RF detector between +16 dBm and –15 dBm, harmonics of the 541XXA source contribute to errors in measurement.



Signal Channel Accuracy

The 541XXA signal channel measurement accuracy varies with input signal power. As the power level being measured decreases the error increases, as shown in the chart at bottom-left.

Detector Frequency Response

The frequency response of the 560-7 series detector introduces a possible measurement error. This error has been characterized as

- ☐ ±0.5 dB at <18 GHz
- ☐ ±2.0 dB at <20 GHz
- ☐ ±2.0 dB at <26.5 GHz (7S50), ±1.25 dB at <26.5 (7K50, 7VA50)
- ☐ ±2.2 dB at <32 GHz
- ☐ ±2.5 dB at <40 GHz
- ☐ ±3 dB at <50 GHz

Equipment Required

- ☐ Anritsu ML4803A Power Meter.
- ☐ Anritsu MA4601A power sensor for models 54107A, 54109A, and 54111A with 50Ω Signal Source output.
- ☐ Anritsu MA4603A power sensor and J0365 Conversion Connector for models 54107A, 54109A, and 54111A with 75Ω Signal Source output.

☐ Anritsu MA4701A/MA4702A power sensors for models 54117A through 54131A and model 54147A through 54177. (See Precision Adapters, below.)

☐ Anritsu MA4703A/MA4704A power sensors for model 54136A.

☐ RF Detector, ANRITSU 5400-71N50 for models 54107A, 54109A, and 54111A with 50Ω Signal Source output.

☐ RF Detector, ANRITSU 5400-71N75 for models 54107A, 54109A, and 54111A with 75Ω Signal Source output.

☐ RF Detector, ANRITSU 560-7N50B for models 54117A through 54131A and 54147A through 54177A.

☐ RF Detector, ANRITSU 560-7K50 for model 54136A.

☐ RF Detector, ANRITSU 560-7V50 for model 54154A–54169A.

☐ 60 dB Step Attenuator, Hewlett Packard Model 8495B or 8495D (0.00 to 26.5 GHz). (Used only for 541XXA's not equipped with internal attenuator).

☐ Precision Adapters. Use Precision Adapters to convert the RF output on 54154A through 54177 to N female, as follows:

☐ 34RVNF50, V male to N female converts the 54177 V Connector output to N female.

☐ 34RKNF50, K male to N Female converts the 54154 through 54169A K Connector output to N female.

Procedure

Step 1. Calibrate the power meter high-power sensor using the procedure described below.

☐ *For 54117A thru 54177A:*

- Connect the MA4701A or MA4703A, as appropriate, to the power meter.
- Perform a calibration as instructed in the Anritsu ML4803A operations and service manual.
- Do *NOT* connect the power sensor to the 541XXA RF Output connector yet.

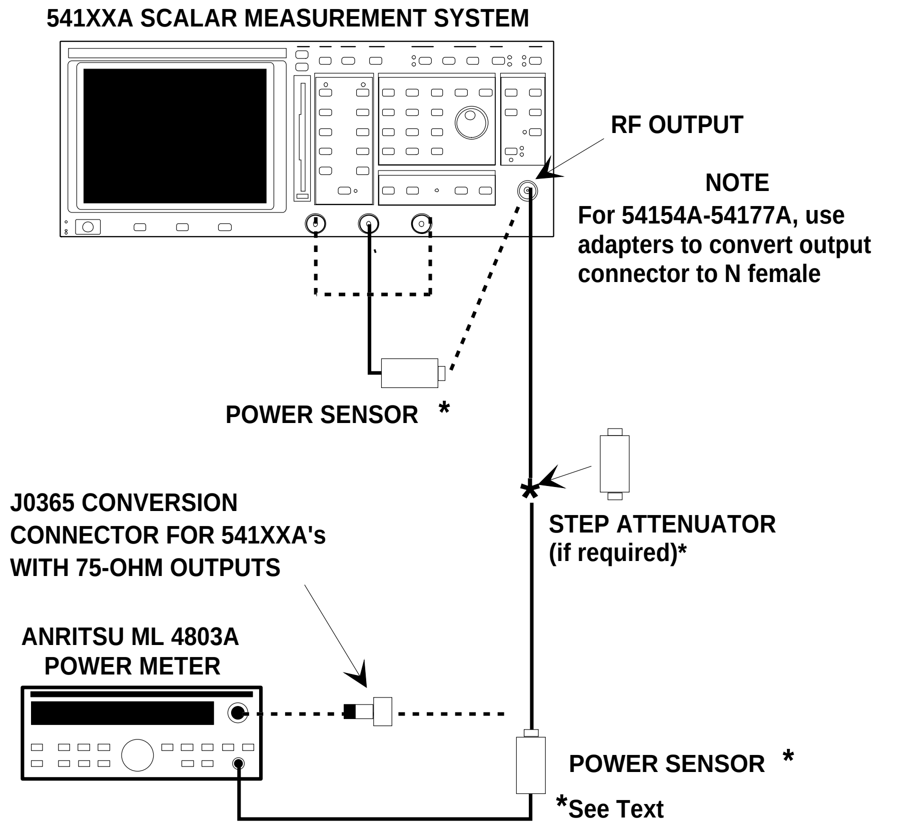


Figure 5-5. *Signal Channel Verification, RF Test Setup*

☐ *For 54107A, 54109A, and 54111A models:*

- For units equipped with a 50Ω signal source output, connect the MA4601A power sensor to the power meter.
- For units equipped with a 75Ω signal source output, connect the MA4603A power sensor (in conjunction with the J0365 Conversion Connector) to the power meter (see Figure 5-5).
- Perform a calibration as instructed in the Anritsu ML4803A operations and service manual.
- Do *NOT* connect the power sensor to the 541XXA RF Output connector yet.

Step 2. Set up the equipment as shown in Figure 5-5, and turn the equipment on.

SYSTEM MENU
DISK UTILITIES
SYSTEM SETUP
DATA POINTS
RESET
CONFIGURE:
SOURCE
ANALYZER
PLOTTER
APPLICATIONS
GPIB MODE
USE ◆ THEN
PRESS SELECT

RESET MENU
RESET IS
CONFIGURED
TO KEEP:
CAL DATA
MARKERS
LIMITS
RESET
RESET TO FACTORY DEFAULTS
USE ◆ THEN
PRESS SELECT

FREQUENCY MENU
CENTER
XX.XXXX GHz:
WIDTH
00.0000 GHz
PRESS SELECT
FOR
START/STOP

Step 3. Select **RESET** from the displayed menu (top left), using the Menu up/down and Select keys.

Step 4. From the **RESET MENU** (middle left) select **RESET TO FACTORY DEFAULTS**.

Step 5. Press the Frequency key to display the CENTER/WIDTH menu (bottom left).

Step 6. Set the **WIDTH** to 0.0000 GHz (or MHz, depending on model).

Step 7. *Set the* **CENTER** frequency to the applicable test frequency (50 MHz or mid-range) for the model-under-test, per the test record on page 5-35, 5-39, or 5-43.

Step 8. Press the Output Power key.

Step 9. Set the power level to the applicable high-test power level (2 or 10 dBm) for the model-under-test, per Table 5-3 (page 5-25).

Step 10. Turn both measurement channels off using the Display On/Off keys.

Step 11. Press the System Menu key and select **DATA POINTS** from the displayed menu (below).

Step 12. Select **101** from the **FREQUENCY DATA POINTS** menu (below).

SYSTEM MENU
DISK UTILITIES
SYSTEM SETUP
DATA POINTS
RESET
CONFIGURE:
SOURCE
ANALYZER
PLOTTER
APPLICATIONS
GPIB MODE
USE ◆ THEN
PRESS SELECT

FREQUENCY DATA POINTS
51
101
201
401
USE ◆ THEN
PRESS SELECT

Table 5-3. *Maximum Allowable Signal Channel Uncertainty Values*

Model	Test Frequency*	Test Power (dBm)	Uncertainty (dB) Channel Accuracy @ Test Power	Uncertainty (dB) Detector Frequency Response (dB)**	Max. Allowable Signal Channel Error (dB)#
54107A 54109A 54111A (50Ω)	50 MHz	2	0.24	0.2	0.312
		–48 or –50	0.9		0.943
54107A 54109A 54111A (75Ω)	50 MHz	10	0.2	0.2	0.283
		–20	0.32		0.377
54117A 54147A 54161A 54169A 54177A	50 MHz	2	0.24	0.5	0.555
		–48 or –50	0.9		0.943
54119A	4 GHz	2	0.24	0.5	0.555
		–48 or –50	0.9		0.943
54128A	10 GHz	2	0.24	0.5	0.555
		–48 or –50	0.9		0.943
54130A	16 GHz	2	0.24	0.5	0.555
		–48 or –50	0.9		0.943
54131A	13 GHz	2	0.24	0.5	0.555
		–48 or –50	0.9		0.943
54136A	21.75 GHz	2	0.24	2.0	2.014
		–48 or –50	0.9		2.193
54137A	11 GHz	2	0.24	0.5	0.555
		–48 or –50	0.9		0.943
54154A	2 GHz	2	0.24	2.0	0.555
		–48 or –50	0.9		0.943
54163A	2 GHz	2	0.24	2.0	0.555
		–48 or –50	0.9		0.943

* Test frequency is 50 MHz for models having a 1 MHz or 10 MHz low-end frequency; it is the mid-range frequency for all other models.

** 5400-71XXX RF Detector is used for 54107A, 54109A, and 54111A. The 560-7XXX Detector is used for all other models.

Signal Channel Error is calculated using a Root-Sum-Sum method. The formula is

$$Signal\ Channel\ Accuracy = \sqrt{(Channel\ Accuracy)^2 + (Detector\ Frequency\ Response)^2}$$

CHANNEL: 1
INPUT: A
TRANSMISSION
RETURN LOSS
SWR
POWER
DTF
VIEW CAL
SELECT INPUT
TRACE MEMORY
REF LINE
USE ◆ THEN
PRESS SELECT

Step 13. Connect the power sensor to the 541XXA RF Output connector.

NOTE

Ensure that the power meter Cal Factor is set correctly for the frequency under test.

Step 14. Record the Power Meter Reading at 2.0 dBm or 10 dBm (as applicable) in the appropriate column of the test record.

Step 15. Disconnect the power sensor from the 541XXA.

Step 16. Connect the appropriate RF detector for the 541XXA model being tested between the 541XXA A Input and the RF Output connector. (See to Figure 5-5 and "Equipment Required," pages 5-22 and 5-23).

Step 17. Press the Channel 1 Menu key.

CHANNEL: 1
SELECT INPUT
NON-RATIO
A
B
R
RATIO:
A/R
B/R
USE ◆ THEN
PRESS SELECT

Step 18. Choose **SELECT INPUT**, from the CHANNEL menu (top left), using the Menu up/down and Select keys.

Step 19. Choose **NON-RATIO A**, from the SELECT INPUT menu (middle left).

Step 20. Select **POWER,** when you are returned to the CHANNEL menu.

Step 21. Press the Cursor key to obtain a cursor menu readout (bottom left).

Step 22. Record the 541XXA Cursor Reading at 2.0 dBm or 10 dBm (as applicable) in the space provided in the test record.

NOTE

The difference between the power meter reading taken in Step 14 and the cursor reading is the 541XXA Signal Channel Error.

CURSOR

1: XX.XX dB
2: XX.XX dB
XX.XXXX GHz
(XX.XXXX GHz)
PRESS SELECT
FOR
CURSOR MENU

Step 23. Record the difference value, as explained above, for 2.0 dBm or 10 dBm (as applicable) in the column headed "541XXA Signal Channel Error," on page 5-38, 5-42, or 5-46 of the test record.

Step 24. Verify that the error does not exceed the maximum allowable signal channel error, as indicated in Table 5-3 (page 5-25).

Step 25. Move the power sensor connection to Input B.

Step 26. Repeat steps 14 through 24 for signal channel input **NON-RATIO B.**

Step 27. Move the power sensor connection to Input R

Step 28. Repeat steps 15 through 24 for signal channel input **NON-RATIO R,** if applicable.

Step 29. Switch off measurement Channel 1 using the Display On/Off key.

Step 30. Calibrate the power meter low-power sensor using the procedure described below.

☐ *For models equipped with a 50Ω signal source output (including models 54107A, 54109A, and 54111A):*

- Connect the MA4702A, to the power meter.
- Perform a calibration as instructed in the Anritsu ML4803A operations and service manual.
- For 54107A, 54109A, and 54111A with 75Ω signal source output, repeat step 1 to 28. However, record power meter reading at 2.0 dBm or –20 dBm in appropriate column of test record.

For model 54136A:

- Connect the MA4704A to the power meter.
- Perform a calibration as instructed in the Anritsu ML4803A operations and service manual.

Step 31. *If internal step attenuator is not installed*, connect the external step attenuator to the 541XXA RF Output connector and set it for 50 dB attenuation. (See Figure 5-5 and "Required Equipment, page 5-22 and 5-23.) Skip to step 33.

For 54107A, 54109A, or 54111A, set RF Output power to +10 dBm and set the external step attenuator for 60 dB attenuation.

Step 32. *If internal step attenuator is installed,* press Output Power key set the power level to –50 dBm.

Step 33. Connect the power sensor to the applicable RF Output connector (attenuator or 541XXA front panel).

CHANNEL: 1
INPUT: A
TRANSMISSION
RETURN LOSS
SWR
POWER
DTF
VIEW CAL
SELECT INPUT
TRACE MEMORY
REF LINE
USE ◆ THEN
PRESS SELECT

CHANNEL: 1
SELECT INPUT
NON-RATIO
A
B
R
RATIO:
A/R
B/R
USE ◆ THEN
PRESS SELECT

CURSOR

1: XX.XX dB
2: XX.XX dB
XX.XXXX GHz
(XX.XXXX GHz)
PRESS SELECT
FOR
CURSOR MENU

Step 34. Press the 541XXA RF On/Off key to turn the RF power output off.

Step 35. Zero-set the power meter.

Step 36. Press the 541XXA RF On/Off key to On.

Step 37. Record the power meter reading at –48 dBm or –50 dBm, as applicable, in the column labeled "Power Meter Reading dBm."

Step 38. Disconnect the power sensor from the 541XXA.

Step 39. Connect the RF detector between the 541XXA Input A connector and the output of the step attenuator.

Step 40. Press the Channel 1 Menu key.

Step 41. Using the Menu up/down and Select keys, configure the 541XXA for a power measurement using Input A , as follows:

- Choose **SELECT INPUT**, from the CHANNEL menu (top left)
- Choose **NON-RATIO A**, from the SELECT INPUT menu (middle left).
- Select **POWER,** when you are returned to the CHANNEL menu.

Step 42. Press the Averaging key.

Step 43. Select **128 SWEEPS** from the displayed menu (next page), using the Menu up/down and Select keys.

Step 44. Wait for the averaging counter to reach 128; then press the Cursor key to obtain a cursor menu readout (bottom left).

Step 45. Record the cursor value at –48 or –50 dBm, as applicable, in the column labeled "541XXA Cursor Reading dBm," in the test record.

NOTE

The difference between the power meter reading taken in Step 37 and the cursor reading is the Signal Channel Error.

AVERAGING CHANNEL 1
OFF
2 SWEEPS
4 SWEEPS
8 SWEEPS
16 SWEEPS
32 SWEEPS
64 SWEEPS
128 SWEEPS
256 SWEEPS
SET CHAN 2
COUPLE CHANNELS
USE ◆ THEN PRESS SELECT

Step 46. Verify that the 541XXA cursor menu (left) reading is less than the calculated maximum allowable error, as indicated in the test record.

Step 47. Move the power sensor connection to Input B.

Step 48. Repeat steps 31 through 46 for signal channel input **NON-RATIO B.**

Step 49. Move the power sensor connection to Input R, if applicable, and repeat steps 31 through 46 for signal channel input **NON-RATIO R.**

5-10 RESIDUAL FM TEST

This test verifies that the residual FM of the 541XXA signal source is within specified limits.

The residual FM measurement is made at the highest signal source output frequency for the particular 541XXA model, as this is the frequency at which the residual FM is maximum. The Anritsu MS2802 spectrum analyzer is used to down convert the 541XXA signal source output so that the Marconi TF2304 Modulation meter can be used to measure the FM products.

SYSTEM MENU
- DISK UTILITIES
- SYSTEM SETUP
- DATA POINTS
- **RESET**
- CONFIGURE:
- SOURCE
- ANALYZER
- PLOTTER
- APPLICATIONS
- GPIB MODE
- USE ◆ THEN PRESS SELECT

RESET MENU
- RESET IS CONFIGURED TO KEEP:
- CAL DATA
- MARKERS
- LIMITS
- RESET
- **RESET TO FACTORY DEFAULTS**
- USE ◆ THEN PRESS SELECT

Equipment Required

☐ Anritsu MS2802 Spectrum Analyzer.

☐ Anritsu MS616B Modulation Meter.

Procedure

Step 1. Set up the equipment as shown in Figure 5-6, and turn the equipment on.

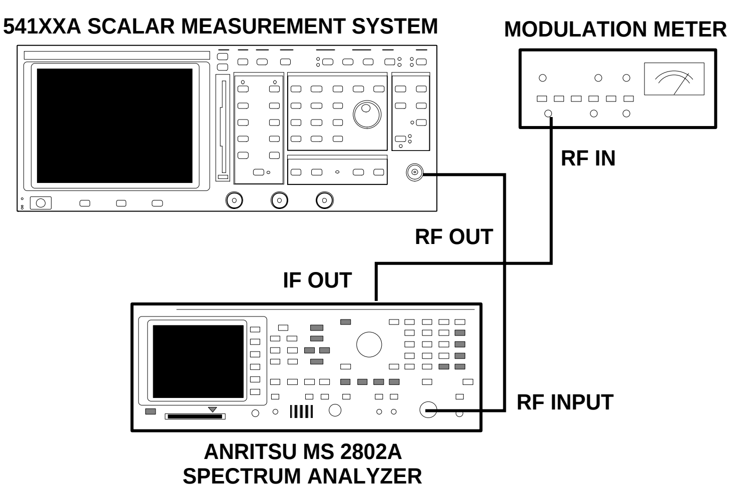


Figure 5-6. *Test Setup for CW Frequency Accuracy Test*

Step 2. Press the System Menu key and select **RESET** from the displayed menu (top left), using the Menu up/down and Select keys.

Step 3. From the **RESET MENU** (bottom left), select **RESET TO FACTORY DEFAULTS**.

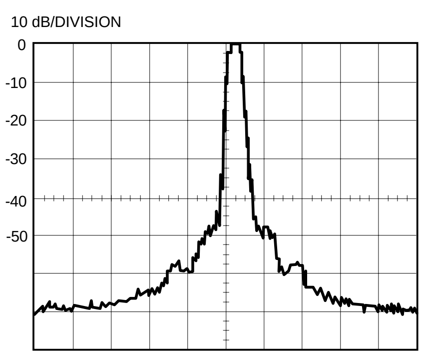
Step 4. Turn both measurement channels off using the Display On/Off keys.

FREQUENCY MENU

START
XX.XXXX GHz:

STOP
00.0000 GHz

PRESS SELECT
FOR
CENTER/WIDTH



Step 5. Press the Output Power key and set the power as shown below:

- For all 54154A through 54177A, to +2.0 dBm.
- For all others: to +4.0 dBm (+7 dBm for units without an internal step attenuator

Step 6. Press the Frequency key.

Step 7. Using the Menu up/down keys,

- For 54154A through 54177A, set the CENTER frequency to 19.90 GHz and the WIDTH to 0 MHz.
- For all other models, set the **START** frequency to the same value as the **STOP** frequency on the displayed menu (top left).

Step 8. Tune the spectrum analyzer to center the 541XXA output signal at the center frequency graticule line.

Step 9. Adjust the spectrum analyzer reference level to place the top of the waveform on the reference level graticule line.

Step 10. Set the spectrum analyzer frequency span/div to 100 kHz. The spectrum analyzer display should resemble the waveform shown at bottom left.

Step 11. Now set the frequency span/div to 10 mS (zero span).

Step 12. Readjust the tuning control to place the trace on the reference level graticule, as necessary.

Step 13. View the modulation meter and ensure that the HIGH and LOW indicators are off.

Step 14. Read the frequency deviation meter and verify that the value is less than 10 kHz, peak (for 54136A, <30 kHz peak).

Step 15. If the unit is a 54117A, 54147A, 54161A, 54169A, or 54177A, perform the following steps, otherwise go to paragraph 5-11,"Source Output Signal Test."

- Press the 541XXA Frequency key.

FREQUENCY
MENU

CENTER
01.9000 GHz:

WIDTH
00.0000 GHz

PRESS SELECT
FOR
START/STOP

- Press the Select key to display the Center/Width menu (top left)
- Set the **CENTER** frequency to 1.9000 GHz; thus setting the unit in the low-frequency band. Then repeat steps 8 through 14.

5-11 SOURCE OUTPUT SIGNAL PURITY TESTS

This test verifies that the harmonic and non-harmonic (spurious) signals from the 541XXA signal source are within the specified limits.

SYSTEM MENU
DISK UTILITIES
SYSTEM SETUP
DATA POINTS
RESET
CONFIGURE:
SOURCE
ANALYZER
PLOTTER
APPLICATIONS
GPIB MODE
USE ◆ THEN PRESS SELECT

Equipment Required

☐ Anritsu MS2802 Spectrum Analyzer

Procedure

Step 1. Set up the equipment as shown in Figure 5-7, and turn the equipment on.

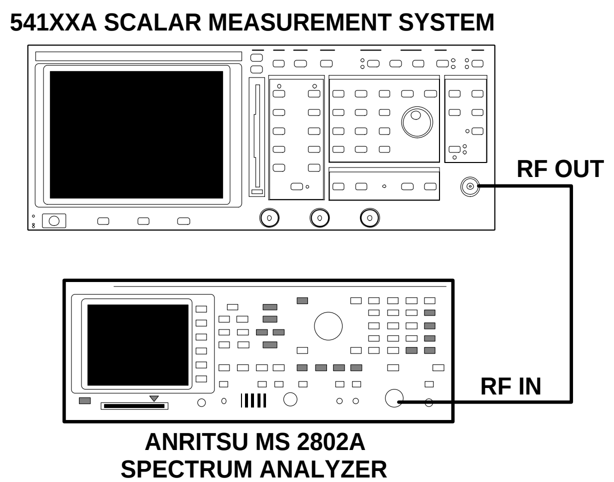


Figure 5-7. *Source Output Signal Purity Test Setup*

RESET MENU
RESET IS CONFIGURED TO KEEP:
CAL DATA
MARKERS
LIMITS
RESET
RESET TO FACTORY DEFAULTS
USE ◆ THEN PRESS SELECT

Step 2. Press the System Menu key and select **RESET** from the displayed menu (top left), using the Menu up/down and Select keys.

Step 3. From the **RESET MENU** (bottom left), select **RESET TO FACTORY DEFAULTS**.

FREQUENCY MENU
CENTER
01.9000 GHz:
WIDTH
00.0000 GHz
PRESS SELECT FOR START/STOP

Step 4. Turn both measurement channels off using the Display On/Off keys.

Step 5. Press the Output Power key and set the power to +4.0 dBm (+7 dBm for units without an internal step attenuator). Power level is shown as bottom of display.

Step 6. Press the Frequency key and then press the Select key to display the Center/Width menu (left).

Step 7. Set the **WIDTH** value to 0.0000 GHz (or MHz, depending on model).

Step 8. Set the **CENTER** frequency to the minimum value allowed

Use the data entry knob or enter the value from the keypad.

Step 9. Adjust the spectrum analyzer frequency span/div and resolution bandwidth controls to view the 541XXA output signal.

Step 10. Adjust the reference level control for 0 dB/Division.

Step 11. While monitoring the spectrum analyzer display, use the Data Entry knob to slowly increase the 541XXA frequency throughout its range.

Step 12. Verify that the harmonics and nonharmonics are within the specified limits shown below.

Model	541XXA Output Frequency	Harmonics (@50Ω load)	Non-Harmonics
54107A, 54109A 54111A	≤3 GHz	40 dBc	60 dBc
54117A	<2 GHz ≥2 GHz	40 dBc 50 dBc	50 dBc 60 dBc
54119A thru 54136A	All	50 dBc	60 dBc
All others	<2 GHz 2 to 20 GHz ≥20 GHz	40 dBc 60 dBc 42 dBc	50 dBc 50 dBc 50 dBc

5-12 *TEST RECORD FORMS*

Sample test record forms are provided in the following pages. These forms may be copies and used to provide a record of test results that can be used to establish benchmark values for future testing of the same 541XXA.

TEST RECORD
Model 54107A, 54109A, 54111A

Model:**__________________** ***Serial Number*****________________** ***Date:*****____________________**

Frequency Accuracy, ± 100 KHz

54107A MHz*	54107A Tested Value	54109A MHz*	54109A Tested Value	54111A MHz*	54111A Tested Value
1.00*		1.00*		1.00*	
250.00		250.00		250.00	
500.00		500.00		500.00	
750.00		750.00		750.00	
1000.00		1000.00		1000.00	
1250.00		1250.00		1250.00	
1500.00		1500.00		1500.00	
		1750.00		1500.00	
		2000.00		2000.00	
		2200.00		2250.00	
				2500.00	
				2750.00	
				3000.00	

* Specification for 1 MHz output is ±200 kHz. For all other 54107A, 54109A, and 54111A output frequencies, specification is ±100 kHz.

Output Power Accuracy and Flatness

Attenuator	Set Power (dBm)	Max Power (dBm)	Min Power (dBm)	Flatness Difference Max – Min (dB)
No	+12.0			
	+2.0			
Yes	+10.0			
	–1.0			
	–6.0			
	–16.0			
	–26.0*			
	–36.0*			
	–46.0*			
	–56.0*			

*Internal step attenuator measurement below –30 dBm is not possible for models equipped with 75Ω output.

Signal Channel Verification Test, DC Cal Method

DC Voltage	54XXA Cursor Readout Value Input A	Input B	Input R	Specified Limits dBm
–1.462 V	________	________	________	+16.00, –0.1, +0.25 (+15.90 to –16.25)
–0.6208 V	________	________	________	+9.00, –0.1, +0.12 (+8.90 to –9.12)
–1.313 mV	________	________	________	–26.00, ±0.34 (–25.66 to –26.34)

Signal Channel Verification Test, Standard 50 MHz Source Method

50 MHz Ref	54XXA Cursor Readout Value Input A	Input B	Input R	Specified Limits dBm
0.00 dBm	________	________	________	0.00, ±0.30 (–0.30 to +0.30)
–30.00 dBm	________	________	________	–30.00, ±0.45 (–29.55 to –30.45)

Signal Channel Verification Test, Mid Band RF Input Method

Input A

Measurement Power*	Power Meter Reading dBm	541XXA Cursor Reading	541XXA Signal Channel Error**
+2.00 dBm	______	______	______
–48.00 dBm or –50 dBm	______	______	______

Input B

Measurement Power*	Power Meter Reading dBm	541XXA Cursor Reading	541XXA Signal Channel Error**
+2.00 dBm	______	______	______
–48.00 dBm or –50 dBm	______	______	______

Input R

Measurement Power*	Power Meter Reading dBm	541XXA Cursor Reading	541XXA Signal Channel Error**
+2.00 dBm	______	______	______
–48.00 dBm or –50 dBm	______	______	______

* This test performed at 50 MHz for models
** Allowable limits and measurement error sources are explained in text.

Signal Channel Verification Test, Mid Band RF Input Method Models with 75 Ohm Output

Input A

Measurement Power, with Int. Step-Atten.*	Measurement Power, without Int. Step-Atten.**	Power Meter Reading dBm	541XXA Cursor Reading	541XXA Signal Channel Error**
+2.00 dBm	+2.00 dBm	______	______	______
–20.00 dBm	+10.00 dBm	______	______	______

Input B

Measurement Power*	Measurement Power, without Int. Step-Atten.**	Power Meter Reading dBm	541XXA Cursor Reading	541XXA Signal Channel Error**
+2.00 dBm	+2.00 dBm	______	______	______
–20.00 dBm	+10.00 dBm	______	______	______

Input R

Measurement Power*	Measurement Power, without Int. Step-Atten.**	Power Meter Reading dBm	541XXA Cursor Reading	541XXA Signal Channel Error**
+2.00 dBm	+2.00 dBm	______	______	______
–20.00 dBm	+10.00 dBm	______	______	______

* This test performed at 50 MHz
** Allowable limits and measurement error sources are explained in text.

TEST RECORD
Model 54117A, 54130A, 54137A, 54147A, 54154A
54161A, 54163A, 54169A, or 54177A

*Model:*__________________ *Serial Number*________________ *Date:*_____________________

Frequency Accuracy, ±200 kHz.

54117A 54169A
54147A 54177A
54161A

GHz	Tested Value
0.0100	
0.5000	
1.0000	
1.5000	
2.0000	

54117A 54161A
54137A 54163A
54147A 54169A
54154A 54177A

GHz	Tested Value
2.0000	
2.5000	
3.0000	
3.5000	
4.0000	
4.5000	
5.0000	
5.5000	
6.0000	
6.5000	
7.0000	
7.5000	
8.0000	
8.4000	
8.6000	

54137A 54163A
54147A 54169A
54154A 54177A
54161A

GHz	Tested Value
8.6000	
9.0000	
9.5000	
10.0000	
10.5000	
11.0000	
11.5000	
12.0000	
12.4000	

54163A
54154A 54169A
54161A 54177A

(For Power Accuracy and Flatness Test Only

GHz	Tested Value
25	
30	
32 (54154A & 54161A)	
35	
40	
45	
50	

54130A 54161A
54137A 54163A
54147A 54169A
54154A 54177A

GHz	Tested Value
12.4000	
13.0000	
13.5000	
14.0000	
14.5000	
15.0000	
15.5000	
16.0000	
16.5000	
17.0000	
17.5000	
18.0000	
18.5000	
19.0000	
19.5000	
20.0000	

Output Power Accuracy and Flatness

Model	Set Power (dBm)	Max Power (dBm)	Min Power (dBm)	Flatness Difference Max – Min (dB)
54117A/54147A No Attenuator	+10.0	______	______	______
	0.0	______	______	______
54117A/54147A With Attenuator	+7.0	______	______	______
	–3.0	______	______	______
	–8.0	______	______	______
	–18.0	______	______	______
	–28.0	______	______	______
	–38.0	______	______	______
	–48.0	______	______	______
	–58.0	______	______	______
54154A/54161A, 54163A/54169A No Attenuator	+4.0	______	______	______
	–6.0	______	______	______
54154A/54161A, 54163A/54169A With Attenuator	+1.0	______	______	______
	–9.0	______	______	______
	–14.0	______	______	______
	–24.0	______	______	______
	–34.0	______	______	______
	–44.0	______	______	______
	–54.0	______	______	______
54177A No Attenuator	+1.0	______	______	______
	–9.0	______	______	______
54177A With Attenuator	–2.0	______	______	______
	–12.0	______	______	______
	–17.0	______	______	______
	–27.0	______	______	______
	–37.0	______	______	______
	–47.0	______	______	______
	–57.0	______	______	______

Signal Channel Verification Test, DC Cal Method

DC Voltage	54XXA Cursor Readout Value Input A	Input B	Input R	Specified Limits dBm
–1.462 V	______	______	______	+16.00, –0.1, +0.25 (+15.90 to –16.25)
–0.6208 V	______	______	______	+9.00, –0.1, +0.12 (+8.90 to –9.12)
–1.313 mV	______	______	______	–26.00, ±0.34 (–25.66 to –26.34)

Signal Channel Verification Test, Standard 50 MHz Source Method

50 MHz Ref	54XXA Cursor Readout Value Input A	Input B	Input R	Specified Limits dBm
0.00 dBm	______	______	______	0.00, ±0.30 (–0.30 to +0.30)
–30.00 dBm	______	______	______	–30.00, ±0.45 (–29.55 to –30.45)

Signal Channel Verification Test, Mid Band RF Input Method

Input A

Measurement Power*	Power Meter Reading dBm	541XXA Cursor Reading	541XXA Signal Channel Error**
+2.00 dBm	______	______	______
–48.00 dBm or –50 dBm	______	______	______

Input B

Measurement Power*	Power Meter Reading dBm	541XXA Cursor Reading	541XXA Signal Channel Error**
+2.00 dBm	______	______	______
–48.00 dBm or –50 dBm	______	______	______

Input R

Measurement Power*	Power Meter Reading dBm	541XXA Cursor Reading	541XXA Signal Channel Error**
+2.00 dBm	______	______	______
–48.00 dBm or –50 dBm	______	______	______

* This test performed at 50 MHz for models 54117A, 54147A, 54161A, 54169A, 54177A.
** Allowable limits and measurement error sources are explained in text.

TEST RECORD
Model 54128A, 54131A, or 54136A

Model: ________________ ***Serial Number*** ________________ ***Date:*** ________________

Frequency Accuracy, ±200 kHz.

54128A

GHz*	Tested Value
8.0000	
8.5000	
9.0000	
9.5000	
10.0000	
10.5000	
11.0000	
11.5000	
12.0000	
12.4000	

54131A

GHz*	Tested Value
10.0000	
10.5000	
11.0000	
11.5000	
12.0000	
12.5000	
13.0000	
13.5000	
14.0000	
14.5000	
15.0000	
15.5000	
16.0000	

54136

GHz*	Tested Value
17.0000*	
17.5000	
18.0000	
18.5000	
19.0000	
19.5000	
20.0000	
20.5000	
21.0000	
21.5000	
22.0000	
22.5000	
23.0000	
23.5000	
24.0000	
24.5000	
25.0000	
25.5000	
26.0000	
26.5000	

Output Power Accuracy and Flatness, 54128A and 54131A

Attenuator	Set Power (dBm)	Max Power (dBm)	Min Power (dBm)	Flatness Difference Max – Min (dB)
No	+10.0	________	________	________
	0.0	________	________	________
Yes	+7.0	________	________	________
	–3.0	________	________	________
	–8.0	________	________	________
	–18.0	________	________	________
	–28.0	________	________	________
	–38.0*	________	________	________
	–48.0*	________	________	________
	–58.0*	________	________	________

Output Power Accuracy and Flatness, 54136A

Attenuator	Set Power (dBm)	Max Power (dBm)	Min Power (dBm)	Flatness Difference Max – Min (dB)
No	+7.0	________	________	________
	–3.0	________	________	________
Yes	+4.0	________	________	________
	–6.0	________	________	________
	–11.0	________	________	________
	–21.0	________	________	________
	–31.0*	________	________	________
	–41.0*	________	________	________
	–51.0*	________	________	________

Signal Channel Verification Test, DC Cal Method

DC Voltage	54XXA Cursor Readout Value Input A	Input B	Input R	Specified Limits dBm
–1.462 V	____________	____________	____________	+16.00, –0.1, +0.25 (+15.90 to –16.25)
–0.6208 V	____________	____________	____________	+9.00, –0.1, +0.12 (+8.90 to –9.12)
–1.313 mV	____________	____________	____________	–26.00, ±0.34 (–25.66 to –26.34)

Signal Channel Verification Test, Standard 50 MHz Source Method

50 MHz Ref	54XXA Cursor Readout Value Input A	Input B	Input R	Specified Limits dBm
0.00 dBm	____________	____________	____________	0.00, ±0.30 (–0.30 to +0.30)
–30.00 dBm	____________	____________	____________	–30.00, ±0.45 (–29.55 to –30.45)

Signal Channel Verification Test, Mid Band RF Input Method

Input A

Measurement Power	Power Meter Reading dBm	541XXA Cursor Reading	541XXA Signal Channel Error*
+2.00 dBm	______	______	______
–48.00 dBm or –50 dBm	______	______	______

Input B

Measurement Power	Power Meter Reading dBm	541XXA Cursor Reading	541XXA Signal Channel Error*
+2.00 dBm	______	______	______
–48.00 dBm or –50 dBm	______	______	______

Input R

Measurement Power*	Power Meter Reading dBm	541XXA Cursor Reading	541XXA Signal Channel Error*
+2.00 dBm	______	______	______
–48.00 dBm or –50 dBm	______	______	______

* Allowable limits and measurement error sources are explained in text.

Chapter 6
Adjustments

Table of Contents

Table 6-1. *Adjustments Following Repair or Replacement*

Replaceable Assembly	Procedure	Page
A1 Front Panel PCB	None	
A2 Front Panel Interface PCB	None	
A3 Signal Channel PCB	Signal Channel Adjustments	6-4, 6-6
A5 YIG Driver and Signal Channel Interface PCB	YIG Driver Adjustments	6-9
A6 Frequency Instruction and ALC PCB A24 Frequency Instruction and ALC PCB	ALC/RF Power Adjustments and Temperature Compensation	6-21, 6-38, 6-43, 6-50
A7 Graphics System Processor PCB	None	
A8 CPU PCB	None	
A9 Power Supply Assy	None	
A10 Menu PCB	None	
A11 C35329 500 MHz Sampler/Marker Assy	500 MHz and 25 MHz Marker Adjustments	6-26
A11/A14 500/25 MHz Marker Assy (54137A/54147A)		
A12/A13 500 MHz VCO/Power Amplifier Assy		
A14 25 MHz Marker Assy		
A17 RF Deck Distribution Panel Assy	None	
A18 Switched Filter Driver Assy	None	
A19 Multiband Controller PCB A23 Multiband Controller PCB	ALC/RF Power Adjustments	6-21, 6-50
D40047 Monitor Assy	Brightness, Contrast, and Horizontal Size Adjustment	6-72
2000-612 Floppy Drive Assy	None	
YIG Oscillator	YIG Driver Adjustments, ALC/RF Power Adjustment	6-9, 6-21
Step Attenuator	ALC/RF Power Adjustment	6-21
Output Connector Assy	None	
Directional Coupler	ALC/RF Power Adjustments and Temperature Compensation	6-21, 6-50
Down Converter Assy		

Chapter 6
Adjustments

6-1 INTRODUCTION

This chapter provides adjustment procedures for all models of series 541XXA Network Analyzers. Adjustments are performed only when needed, such as a failed performance verification step/procedures on the replacement/repair of a subassembly. A listing of repairable subassemblies and needed adjustments following repair/replacements is provided in Table 6-1 (facing page).

NOTE

Throughout these procedures, the terms “adjustment potentiometer”, “ potentiometer”, and “adjustment variable resistor” are used interchangeably.

WARNING

Hazardous voltages are present inside the instrument when ac line power is connected. Turn off the instrument and remove the line cord before removing any covers or panels. Trouble shooting or repair procedures should only be performed by service personnel who are fully aware of the potential hazards.

CAUTION

Many assemblies in the 541XXA contain static-sensitive components. Improper handling of these assemblies may result in damage to the assemblies. ***Always*** observe the static-sensitive component handling precautions described in Chapter 1, Figure 1-2.

6-2 RECOMMENDED TEST EQUIPMENT

The recommended test equipment for each adjustment procedure is listed at the beginning of the procedure. The full description and list of particulars for the test equipment is provided in Chapter 1, Table 1-2. If the recommended equipment is not available other test equipment with suitable characteristics may be substituted.

NOTE

Allow the 541XXA and all test equipment to warm up at least 30 minutes prior to performing any of the adjustments.

6-3 SIGNAL CHANNEL ADJUSTMENTS, LOG CONFORMITY

This paragraph provides a procedure for adjusting log conformity on the A3 Signal Channel PCB.

Required Test Equipment

☐ Detector Simulator — refer to Appendix B.

Preliminary

☐ Remove the front panel bezel (Chapter 7, paragraph7-4) to provide access a signal channel potentiometer R109.

☐ Remove the 541XXA bottom cover. (Refer to Chapter 7, paragraph 7-2 for instructions.)

☐ Connect the detector simulator to Input A, and turn the 541XXA on.

NOTE

Allow 30 minutes warm up before continuing with the adjustment procedure.

SYSTEM MENU
DISK UTILITIES
SYSTEM SETUP
DATA POINTS
RESET
CONFIGURE:
SOURCE
ANALYZER
PLOTTER
APPLICATIONS
GPIB MODE
USE ◆ THEN PRESS SELECT

Adjustment Procedure

Step 1. Press the System Menu key and select **RESET** from the displayed menu (top left) using the Menu up/down and Select keys.

Step 2. From the RESET MENU (bottom left) select **RESET TO FACTORY DEFAULTS.**

Step 3. Press the Channel 2 Display On/Off key to off.

RESET MENU
RESET IS CONFIGURED TO KEEP:
CAL DATA
MARKERS
LIMITS
RESET
RESET TO FACTORY DEFAULTS
USE ◆ THEN PRESS SELECT

CALIBRATION
START CAL
DETECTOR OFFSETS
DC CAL MENU
PRESS CLEAR TO RETURN TO MEASUREMENT MODE
USE ◆ THEN PRESS SELECT

Step 4. Press the Calibration key and select **DC CAL MENU** (below).

Step 5. Press the Enter key.

LOG/TEMP READINGS

INPUT A

L: +0.00
T: –0.00

INPUT B

L: - - - - -
T: - - - - -

INPUT R

L: - - - - -
T: - - - - -

Step 6. Observe that the log conformity (**L**) and temperature thermistor (**T**) values appear in the menu area (top left).

Step 7. With the detector simulator connected to signal channel Input A, the displayed **T** value should be 0.00 ±0.10.

Step 8. On the A3 PCB, adjust variable resistor A3R108 (Figure 6-1) to obtain a displayed **L** value of 0.00 ±0.01.

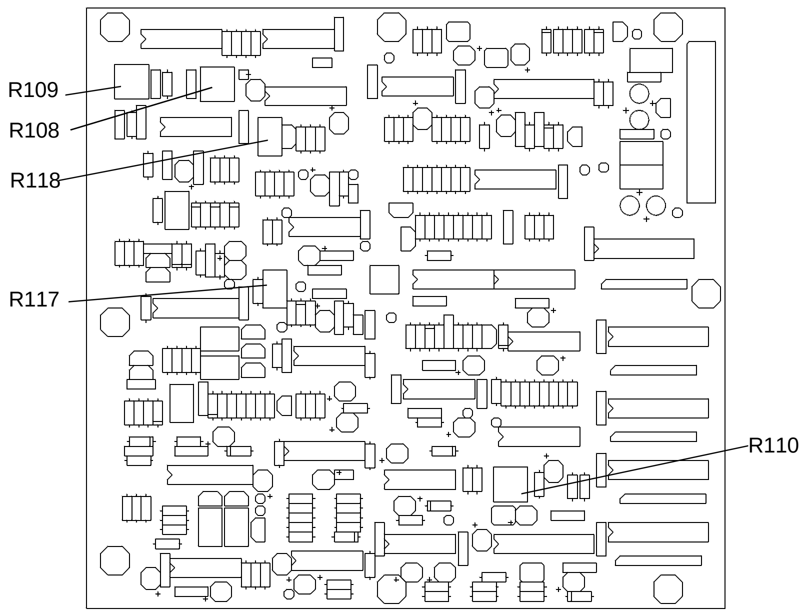


Figure 6-1. *A3 PCB Adjustments*

Step 9. Move the detector simulator to Input B.

Step 10. Observe that the displayed **T** value is 0.00 ±0.10.

Step 11. Adjust A3R109 to obtain a displayed **L** value of 0.00 ±0.01.

Step 12. Move the detector simulator to Input R (if present). Observe that the displayed **T** value is 0.00 ±0.10.

Step 13. Adjust variable resistor A3R110 to obtain a displayed **L** value of 0.00 ±0.01.

6-4 SIGNAL CHANNEL ADJUSTMENTS, SENSITIVITY

This paragraph provides a procedure for adjusting the sensitivity of the A3 Signal Channel PCB.

Required Test Equipment

☐ DC Voltage Standard — John Fluke Model 343A, or equivalent

☐ Adaptor Cable — ANRITSU 560-10BX

Preliminary

☐ Remove the 541XXA bottom cover. (Refer to Chapter 7, paragraph 7-2 for instructions.)

☐ Connect the equipment as shown in Figure 6-2, and turn it on.

SYSTEM MENU
DISK UTILITIES
SYSTEM SETUP
DATA POINTS
RESET
CONFIGURE:
SOURCE
ANALYZER
PLOTTER
APPLICATIONS
GPIB MODE
USE ◆ THEN PRESS SELECT

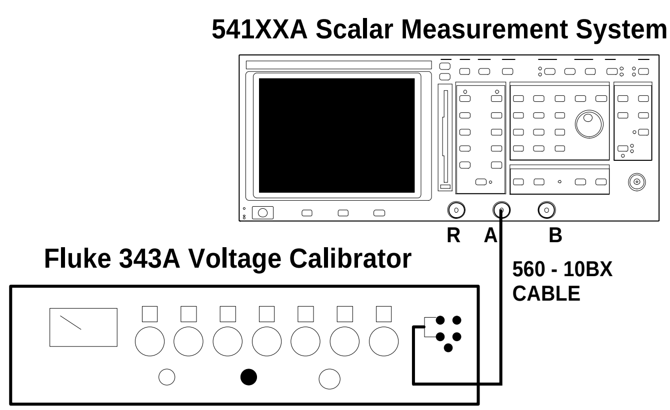


Figure 6-2. *Equipment Setup for Signal Channel Sensitivity Adjustment*

NOTE

Allow 30 minutes warm up before continuing with the adjustment procedure.

RESET MENU
RESET IS CONFIGURED TO KEEP:
CAL DATA
MARKERS
LIMITS
RESET
RESET TO FACTORY DEFAULTS
USE ◆ THEN PRESS SELECT

Adjustment Procedure

Step 1. Press the System Menu key and select **RESET** from the displayed menu (left) using the Menu up/down and Select keys.

Step 2. From the RESET MENU (bottom left) select **RESET TO FACTORY DEFAULTS.**

Step 3. Press the Channel 2 Display On/Off key to off.

CHANNEL: 1
INPUT: A

TRANSMISSION

RETURN LOSS

SWR

POWER

DTF

VIEW CAL

SELECT INPUT

TRACE MEMORY

REF LINE

USE ◆ THEN
PRESS SELECT

CHANNEL: 1
SELECT INPUT

NON-RATIO

A

B

R

RATIO:

A/R

B/R

CALIBRATION

START CAL

DETECTOR
OFFSETS

DC CAL MENU

PRESS CLEAR
TO RETURN TO
MEASUREMENT
MODE

USE ◆ THEN
PRESS SELECT

Step 4. Press the Channel 1 Menu key.

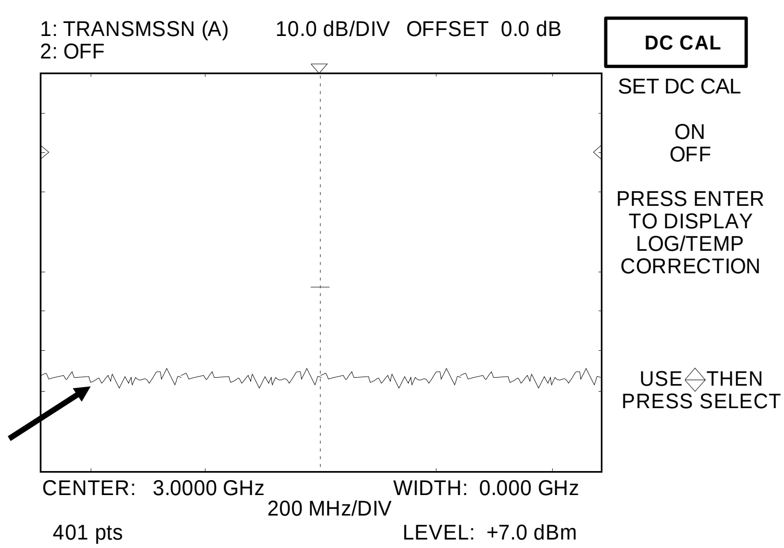
Step 5. Using the Menu up/down and Select keys, configure the 541XXA for a power measurement using Input A , as follows:

- Choose **SELECT INPUT**, from the CHANNEL menu (top left)
- Then choose **NON-RATIO A**, from the SELECT INPUT menu (middle left).
- Select **POWER,** when you are returned to the CHANNEL menu.

Step 6. Set the DC Voltage Standard for zero volts output.

Step 7. Press the Calibration key and select **DC CAL MENU** (bottom left).

Step 8. The 541XXA should now display a noise floor at approximately –63 dBm (below). Allow the 541XXA to sweep for 5 seconds.



SET DC CAL

ON
OFF
PRESS ENTER
TO DISPLAY
LOG/TEMP
CORRECTION
USE ◆ THEN
PRESS SELECT

CURSOR

1: +9.00 dBm
2: XX.XX dB
XX.XXXX GHz
(XX.XXXX GHz)
PRESS SELECT
FOR
CURSOR MENU

Step 9. Using the menu up/down keys, select **ON** from the **DC CAL MENU** (top left). The 541XXA will now display **DC CAL** in the top right hand corner of the screen display.

Step 10. Set the DC Voltage Standard for –0.6208 volts output.

Step 11. Press the 541XXA Cursor key to obtain a readout in the menu area of the 541XXA display (bottom left).

Step 12. Adjust A3R118 (Figure 6-1, page 6-5) to obtain a cursor readout of +9.00 dBm ±0.01 dBm.

Step 13. Set the DC Voltage Standard for –1.462 volts output. Observe that the 541XXA cursor readout is +16.00 dBm +0.25/–0.10 dBm.

Step 14. Set the DC Voltage Standard for –1.313 millivolts output. Observe that the cursor readout is –26.00 dBm ±0.34 dBm.

Step 15. Move the DC Voltage Standard to Input B.

Step 16. Press the Channel 1 Display On/Off key to off, and the Channel 2 Display On/Off key to on.

Step 17. Repeat steps 3 through 14 for Channel 2 and NON-RATIO B.

Step 18. Move the DC Voltage Standard to Input R (if present).

Step 19. Repeat steps 3 through 14 for Channel 2 and NON-RATIO R.

Step 20. Use A3R117 (Figure 6-1, page 6-5) to adjust the R channel gain, as necessary.

NOTE

Variable resistor A3R118 adjusts the gain for both Channel 1, Input A; and Channel 2, Input B. If there is a difference of more than ±0.02 dBm between the two channel's cursor readouts at +9.00 dBm, recheck the Log Conformity Adjustment on page 6-4.

6-5 YIG DRIVER ADJUSTMENTS

This paragraph provides a procedure for adjusting the A5 YIG Driver/Signal Channel Interface PCB. All variable resistors (Rx) and jumpers referred to in this procedure are located on the A5 PCB.

Required Test Equipment

- ☐ EIP 578A Frequency Counter

Preliminary

541XXA Model	J2 Pin Position
54107A thru 54119A, and 54130A	1 & 2
54131A, 54136A, 54154A, 54161A, 54163A, 54169A, and 54177A	3 & 4
54128A, 54137A, and 54147A	5 & 6

- ☐ Remove the 541XXA top cover. (Refer to Chapter 7, paragraph 7-2 for instructions.)
- ☐ Confirm that jumper J2 is positioned per table at left. (See Figure 6-4 for jumper location.)
- ☐ Connect the input of the test equipment as shown in Figure 6-3. Select the correct band input on the counter for the frequency to be measured.
- ☐ For 54177A, use an ANRITSU V to K precision adaptor 34VKF50 for connection to frequency counter.

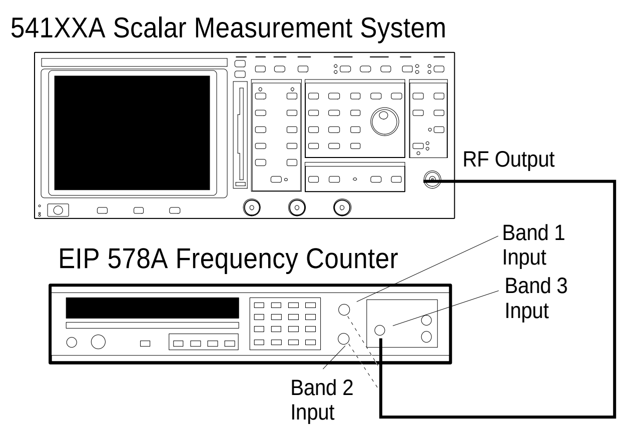


Figure 6-3. *Equipment Setup for YIG Driver Adjustment Procedure*

Adjustment Procedure

Step 1. Set the 541XXA for the Service Mode of operation, as follows:

- Press the Self Test key.
- When the Channel LED's begin flashing, sequentially press the Frequency, Markers, and Leveling keys. The 541XXA will now display the main service mode menu (below).

```
SERVICE MODE

1      - direct control of frequency dacs
2      - diagnostic markers on/off
3      - frequency locking on/off
4      - frequency error message on/off
5      - enable dual autozero
6      - extended cpu self-test mode
7      - additional start sweep locking enable/disable
8      - 100 ms delay at start of sweep enable/disable
9      - variable delay for each data point
0      - ALC square wave test

stest  return to normal operation
```

- Press the 541XXA Data Entry "1" key to select "direct control of frequency dacs" and display the frequency dac control screen (next page)

NOTE

If any key is pressed in error when in the frequency dac control section of the service mode, press the Self Test key and re-enter the service mode. This will ensure that the START, ERROR, WIDTH, and RAMP DAC settings are preset correctly for this adjustment. (It is possible to change the settings for these DAC's while in this section of the service mode.)

Step 2. Press the Data Entry "1" key twice to set the Start DAC to minimum frequency. The highlighted video block should now display "start dac" set to "min".

SERVICE MODE

frequency dac control

dac selection **************		action ******			
	1	2	3	4	5
1. start (width=0)	**min**	mid	max	sweep	het
2. error (width=0)	min	**mid**	max	sweep	
3. ramp (st=0, err=mid)	**min**	mid	max	stop	sweep
4. width (st=0, err=mid)	**min**	mid	max		
5. coil	fm	**main**			
6. cw filter	in	**out**			
7. switch filter output	dcu	**yig**			

enter dac selection digit first, then action digit
clear - return to service mode main menu
stest -return to normal operation

541XXA Model	Start DAC Calibration Freq (GHz)
54107A, 54109A, 54111A	0.069*
54117A, 54119A, 54154A, 54161A, 54163A, 54169A, and 54177A	1.800
54128A	7.800
54130A	12.200
54131A	9.8
54136A	16.800
54137A, 54147A	1.800

* This frequency is on the “other side” of the zero beat due to being offset below the band edge.

Step 3. *For models 54117A through 54177A:*

- Adjust A5R4 (Figure 6-4) for a counter reading that is 200 MHz ±10 MHz below the band start frequency of the model being tested (see table at left).

For models 54107A, 54109A, and 54111A:

- Adjust A5R4 for a counter reading 70 MHz ±2 MHz below the band start frequency for the model being tested (see table at left).

NOTE

A clockwise adjustment of A5R4 must increase the reading on the frequency counter. If this is not the case, the frequency adjustment is on the wrong side of the “zero-beat” and requires readjustment.

Step 4. *For all models except the 54136A:*

- Sequentially press the Data Entry “1” and “3” keys to set the Start DAC to maximum frequency. The highlighted video block should now display “start” set to “max.

For model 54136A:

- Sequentially press the Data Entry "1" and "5" keys to set the Start DAC to the top frequency. The highlighted video block should now display "start" set to "top."

Step 5. *For models 54117A through 54177A:*

- Adjust A5R2 (Figure 6-4) for a counter reading that is 200 MHz ±10 MHz above the band stop frequency of the unit. (These values are listed at left.)

541XXA Model	Stop DAC Calibration Freq (GHz)
54107A	1.570
54109A	2.270
54111A	3.070
54117A, 54119A	8.800
54128A	12.600
54131A	16.200
54130A 54137A, 54147A54154A, 54161A, 54163A, 54169A, and 54177A	20.200
54136A	26.400

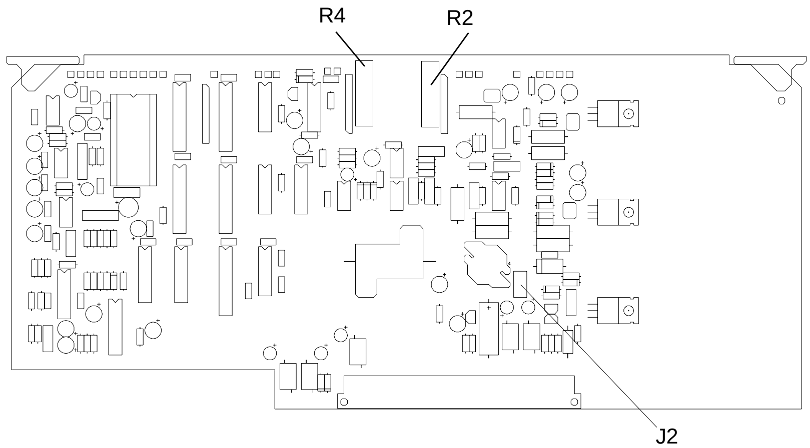


Figure 6-4. *A5 PCB Adjustments*

For models 54107A, 54109A, and 54111A:

- Adjust A5R2 for a counter reading that is 70 MHz ±2 MHz above the band stop frequency of the unit. (These values are listed at left.)

Step 6. Repeat steps 3 through 5 until no further adjustment is required.

Step 7. Press the Self Test key to return to normal instrument operation.

6-6 ALC PRE-ADJUSTMENT PROCEDURES FOR MICROWAVE BAND MODELS

These procedures ensure that the RF output power on 54117A through 54177A is approximately correct so that the 500 MHz and 25 MHz markers can be calibrated. *Perform these procedures only if the ALC PCB or RF Deck components have been changed.* Otherwise, go to paragraph 6-8.

NOTE

For models 54107A, 54109A, and 54111A, go to paragraph 6-7, RF Band ALC Pre-Adjustment Procedures for RF Band Models, which is located on page 6-19.

This procedure is in three parts: the Reference Voltage Adjustment procedure, the Power Output Adjustment Procedure and the ALC Operating Point Adjustment Procedure. Unless otherwise noted, all variable resistors (Rx) and test points (TPx) referred to in this procedure are on the ALC/ Frequency Instruction PCB. For the 54154A–54177A, this is A24; for all others, it is A6.

Required Test Equipment

☐ Digital Voltmeter, with 4-1/2 digits resolution

☐ Oscilloscope, dual channel with two X10 probes

☐ ANRITSU RF Detector

☐ Power Meter and Sensor

☐ Adapter (54154A, 54161A, 54163A, 54169A), V male to K female — ANRITSU VKF50

Preliminary

☐ Remove the 541XXA top cover. (Refer to Chapter 7, paragraph 7-2 for instructions.)

Reference Voltage Adjustment

This presets the ALC power level, allowing proper operation of the microwave band marker module.

Step 1. *For 54117A and 54147A*: If installed, adjust R112 fully clockwise.

Step 2. Set DVM for DC, 1V range (not autorange). Connect common lead to TP25; connect other lead to TP14 (Figure 6-5 or 6-6).

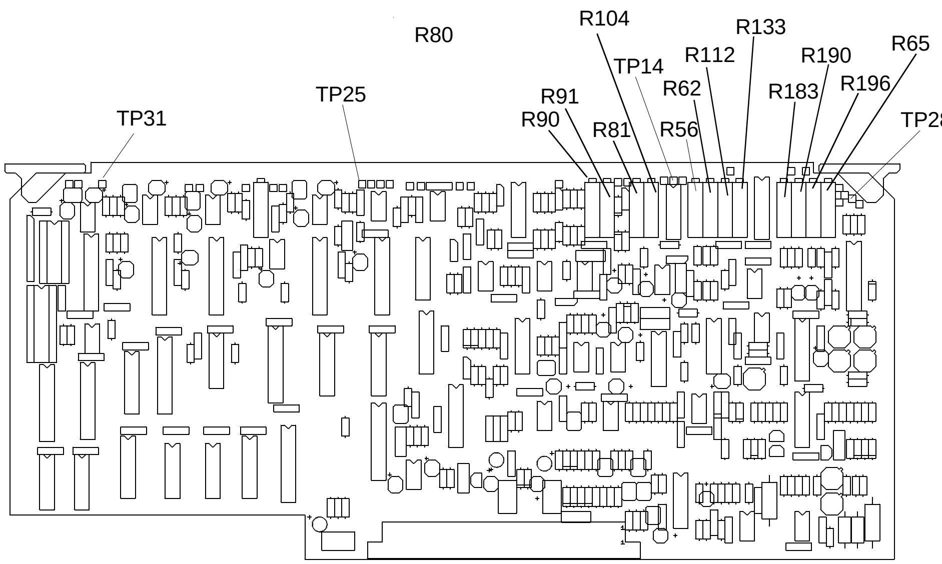


Figure 6-5. *Adjustments and Test Points, A6 ALC/Frequency Instruction PCB (all except 54154A thru 54177A)*

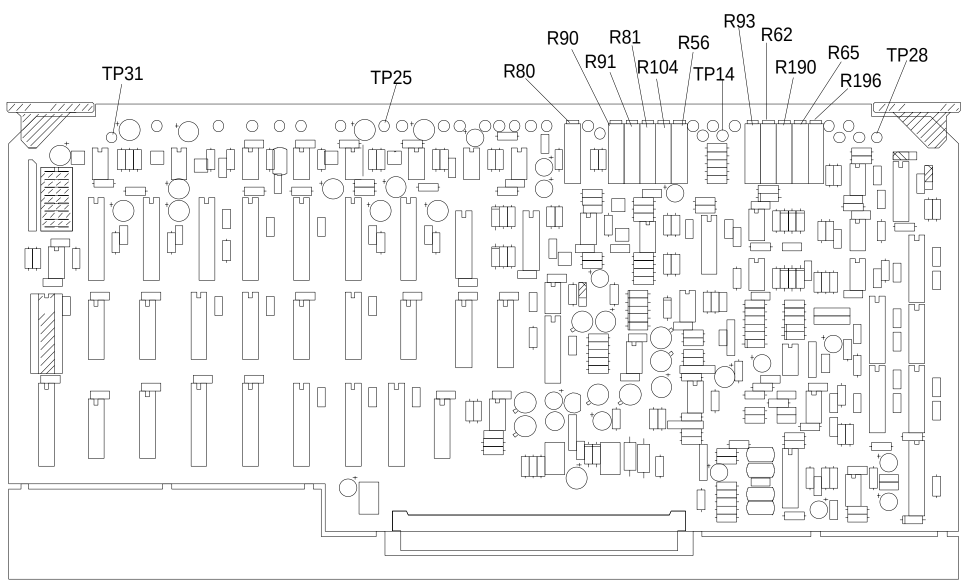


Figure 6-6. *Adjustments and Test Points, A24 ALC/Frequency Instruction PCB (54154A thru 54177A)*

SYSTEM MENU
DISK UTILITIES
SYSTEM SETUP
DATA POINTS
RESET
CONFIGURE:
SOURCE
ANALYZER
PLOTTER
APPLICATIONS
GPIB MODE
USE ◆ THEN PRESS SELECT

RESET MENU
RESET IS CONFIGURED TO KEEP:
CAL DATA
MARKERS
LIMITS
RESET
RESET TO FACTORY DEFAULTS
USE ◆ THEN PRESS SELECT

FREQUENCY MENU
CENTER
XX.XXXX GHz:
WIDTH
0.0000 GHz
PRESS SELECT FOR START/STOP

Step 3. Adjust variable resistor R65 (Figure 6-5 or 6-6, page 6-14), for a DVM reading of 1.0000V ±0.5 mV. For 54154A thru 54177A, go to Step 6.

Step 4. Connect common lead of DVM to TP25; connect other lead to TP31. Set voltmeter to autorange.

Step 5. Adjust variable resistor R183 (Figure 6-5 or 6-6) for a DVM reading of –4.1V ±0.1V (0.0±0.1V for 54117A, 54147A).

Step 6. Disconnect DVM.

Power Output Adjustment

Step 1. Press the System Menu key and select **RESET** from the displayed menu (top left) using the Menu up/down and Select keys.

Step 2. From the RESET MENU (bottom left) select **RESET TO FACTORY DEFAULTS.**

Step 3. Put the 541XXA in CW mode by setting measurement Channels 1 and 2 off.

Step 4. Press the Frequency and Select keys to select the CENTER/WIDTH menu (bottom left).

Step 5. Set **WIDTH** to 0 GHz, then set the **CENTER** frequency to the low-end frequency for the model being calibrated, as follows:

- Models 54117A, 54147A, 54161A, 54169A, and 54177A: 2.0 GHz
  All other models: Low-end frequency.

Step 6. *For all 54117A, 54119A, 54128A, 54130A, 54131A, 54137A, 54147A, and 54154A:*

- Connect a MA4701A power sensor to the Anritsu ML4803A power meter.

For model 54136A:

- Connect a MA4703A power sensor to the Anritsu ML4803A power meter.

For model 54161A through 54177A:

- Connect a HP8487D power sensor to the HP436A power meter. Attach a suitable adapter (Table 1-2), if required.

NOTES

- Perform a calibration as instructed in the power meter operation and service manual.
- Verify that the power meter Cal Factor is set correctly for the test frequency.

Step 7. Connect the power meter to the 541XXA as shown in Figure 6-7.

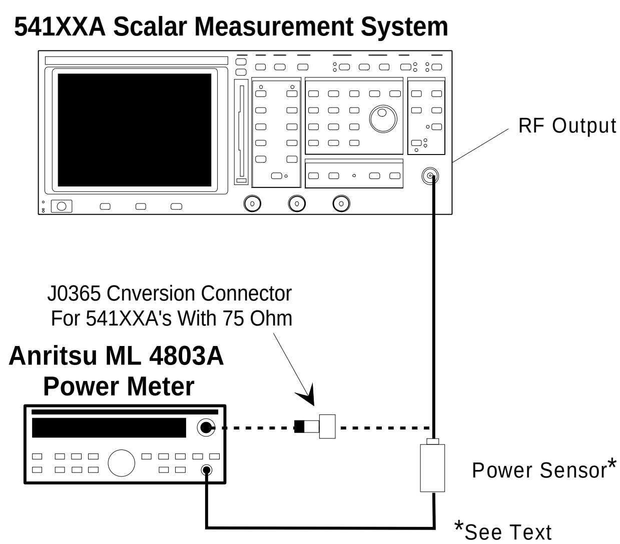


Figure 6-7. *Equipment Setup for ALC Pre-Adjustment Procedure*

Model	Without Attenuator	With Attenuator
54117A	+10 dBm	+9 dBm
54119A thru 54131A, 54136A, 54137A, 54147A	+10 dBm	+7 dBm
54154A, 54161A, 54163A, and 54169A	+4 dBm	+1 dBm
54177A	+1 dBm	–2 dBm

Step 8. Press the 541XXA RF On/Off key to Off. Zero the power meter, and then press RF On/Off key to On.

Step 9. Adjust variable resistor R62 (Figure 6-5 or 6-6, page 6-14) to give a power meter reading equal to the 541XXA reset power level ±0.5 dBm. These levels are listed in the table at left.

Step 10. Reduce the 541XXA RF output power by 10dB.

Step 11. Adjust variable resistor R196 to give a power meter reading equal to the 541XXA set power ±0.5 dBm.

FREQUENCY MENU
START
XX.XXXX GHz:
STOP
XX.XXXX GHz
PRESS SELECT FOR CENTER/WIDTH

CHANNEL: 1
INPUT: A
TRANSMISSION
RETURN LOSS
SWR
POWER
DTF
VIEW CAL
SELECT INPUT
TRACE MEMORY
REF LINE
USE ◆ THEN PRESS SELECT

CHANNEL: 1
SELECT INPUT
NON-RATIO
A
B
R
RATIO:
A/R
B/R
USE ◆ THEN PRESS SELECT

NOTE

Adjustments A6R62 and A6R196 (Figure 6-5 or 6-6) are interactive. Therefore, set RF output power to reset level (left) and repeat steps 9 through 11 until both power meter readings are within ±0.5 dBm of 541XXA indicated RF output power.

Step 12. Disconnect the power meter from the 541XXA RF Output connector.

ALC Operating Point Adjustment

Step 1. Restore 541XXA to its factory defaults, as described on the preceding page

Step 2. Press the Frequency key and Select keys to select the START/STOP menu (top left).

Step 3. Select **START** from the displayed menu, and set the frequency as shown below.

- 54117A, 54147A, 54161A, 54169A, and 54177A: 2 GHz
- All other models: Low-end frequency.

Step 4. Select **STOP** from the displayed menu, and set frequency for the model’s high-end frequency.

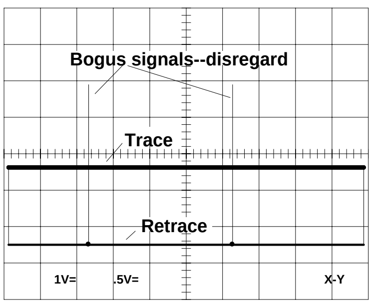
Step 5. Press the Channel 2 Display On/Off key to off.

Step 6. Press the Channel 1 Menu key

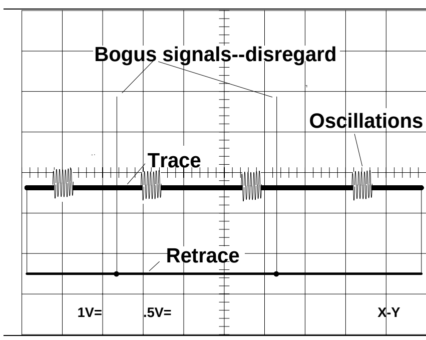
Step 7. Using the Menu up/down and Select keys, configure the 541XXA for a power measurement using Input A , as follows:

- Choose **SELECT INPUT**, from the CHANNEL menu (top left)
- Then choose **NON-RATIO A**, from the SELECT INPUT menu (middle left).
- Select **POWER,** when you are returned to the CHANNEL menu.

Model	Without Attenuator	With Attenuator
54117A	+12 dBm	+10 dBm
54119A thru 54131A, 54136A, 54137A, 54147A	+12 dBm	+9 dBm
54154A, 54161A, 54163A, and 54169A	–6 dBm	–9 dBm
54177A	–9 dBm	–12 dBm



Waveform at TP28, 54117–54136A



Waveform at TP28 with Oscillations

Step 8. Press the Output Power key, and set to the power level as shown in the table at top left.

Step 9. Press the Graticule On/Off key to on.

Step 10. Set Oscilloscope as follows:

- Horizontal Sweep: X-Y mode
- CH 1 vertical sensitivity: 1V/div
- CH 2 vertical sensitivity: 0.5V/div (with X10 probe)
- CH 1 input: DC
- CH 2 input: DC
- Display: CH1 and CH2 On

Step 11. Connect a suitable 560 or 5400 Series detector between the RF Output and Input A connectors.

Step 12. Press the Channel 1 AutoScale key to on.

Step 13. Connect oscilloscope CH 1 input to the 541XXA rear panel Horizontal Output connector using a BNC to BNC cable. Adjust the position controls for a flat trace in the center of the screen. For 54154A thru 54177A, go to Step 16.

Step 14. Connect the oscilloscope CH2 probe to TP28 (Figure 6-5 or 6-6, page 6-14); connect the probe ground clip to the 541XXA chassis.

Step 15. Observe that the oscilloscope displays a waveform similar to those shown at middle left.

NOTE

Bogus signals are any spikes that eminate from the retrace line. They may appear at frequencies other than those shown in the graphics at left.

Step 16. *For models 54117A through 54136A:*

- Adjust R133 (Figure 6-5 or 6-6) to move the oscilloscope trace more positive until the trace oscillates (bottom left) and/or the 541XXA Unleveled LED lights. Now adjust R133 back two turns.

For models 54137A and 54147A:

- Adjust A19R31 on the multiband controller (Figure 6-8) to move the oscilloscope trace more positive until the trace oscillates and/or the 541XXA Unleveled LED lights. Now adjust A19R31 back two turns (trace more negative).

For models 54154A through 54169A:

- Adjust A23R31 on the multiband controller (Figure 6-9) to move the oscilloscope trace more negative until the trace oscillates and/or the 541XXA Unleveled LED lights. Now adjust A23R31 back two turns (trace more positive).

For models 54177A:

- The oscilloscope will display a negative voltage forward trace. Adjust R31 on the A23 multi-band controller to move the oscilloscope trace more negative until the trace oscillates and or the unit becomes unlevelled. *Note the unit may not become unlevelled or oscillate.*

  Now adjust R31 two turns to make the oscilloscope trace more positive.

  The front part of the scope trace will move when R31 is adjusted. Adjust R93 on the ALC PCB as R31 was adjusted to set the end part of the trace to the correct level (that is, two turns more positive from the unlevelled and or oscillation point).

*This completes the microwave band pre-adjustment procedure. For all models except 54117A, 54147A, 54161A, 54169A, and 54177A proceed to the **500** MHz and **25** MHz Marker Adjustment, paragraph **6-8**, on page **6-26**.*

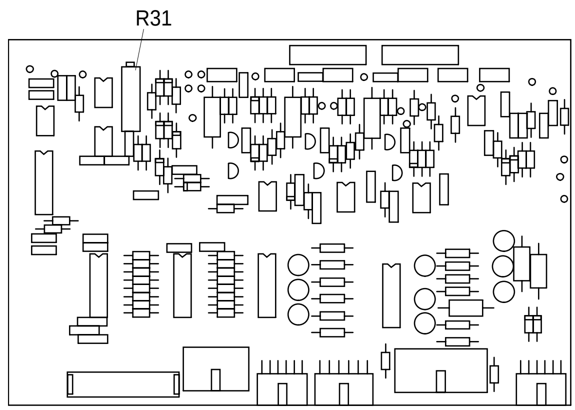


Figure 6-8. *A19 Multiband Controller PCB (54137A and 54147A)*

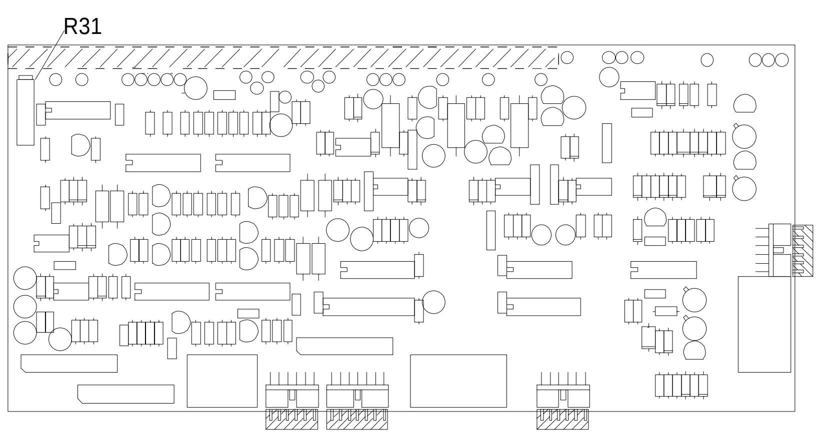


Figure 6-9. *A23 Multiband Controller PCB (54154A thru 54177A)*

6-7 ALC PRE- ADJUSTMENT PROCEDURES FOR RF BAND MODELS

These procedures ensure that the RF output power of models 54107A, 54109A, and 54111A is approximately correct so that the 75 MHz and 25 MHz markers can be calibrated. Use this procedure also for the RF (heterodyne) band of models 54117A, 54147A, 54161A, 54169A, and 54177A. *Perform these procedures only if the ALC PCB or RF Deck components have been changed.* Otherwise, go to paragraph 6-8.

This procedure is in three parts: the Reference Voltage Adjustment procedure, the Power Output Adjustment Procedure and the ALC Operating Point Adjustment Procedure. Unless otherwise noted, all variable resistors (Rx) and test points (TPx) referred to in this procedure are on the ALC/ Frequency Instruction PCB. For the 54154A–54177A, this is A24; for all others, it is A6.

Required Test Equipment

☐ Digital Voltmeter, with 4-1/2 digits resolution

☐ Oscilloscope, dual channel with two X10 probes

☐ ANRITSU RF Detector

☐ Power Meter and Sensor

Preliminary

☐ Remove the 541XXA top cover. (Refer to Chapter 7, paragraph 7-2 for instructions.)

Reference Voltage Adjustment:

This presets the ALC power level, allowing proper operation of the microwave band marker module.

Step 1. Set DVM for DC, 1V range (not autorange). Connect common lead to TP25; connect other lead to TP14 (Figure 6-5 or 6-6, page 6-14).

Step 2. Adjust variable resistor R65 (Figure 6-5 or 6-6) for a DVM reading of 1.0000V ±0.5 mV. For 54154A through 54177A, go to Step 5.

Step 3. Connect common lead of DVM to TP25; connect other lead to TP31. Set voltmeter to autorange.

Step 4. Adjust variable resistor R183 (Figure 6-5 or 6-6) for a DVM reading of -4.1V ±0.1V.

Step 5. Disconnect DVM.

SYSTEM MENU
DISK UTILITIES
SYSTEM SETUP
DATA POINTS
RESET
CONFIGURE:
SOURCE
ANALYZER
PLOTTER
APPLICATIONS
GPIB MODE
USE ◆ THEN PRESS SELECT

RESET MENU
RESET IS CONFIGURED TO KEEP:
CAL DATA
MARKERS
LIMITS
RESET
RESET TO FACTORY DEFAULTS
USE ◆ THEN PRESS SELECT

Power Output Adjustment

Step 1. Press the System Menu key and select **RESET** from the displayed menu (top left) using the Menu up/down and Select keys.

Step 2. From the RESET MENU (bottom left) select **RESET TO FACTORY DEFAULTS.**

Step 3. Press Channel 1 and 2 Display On/Off keys to off. This places the 541XXA in the CW mode.

Step 4. Press the Frequency and Enter keys to select the CENTER/WIDTH menu.

Step 5. Set **WIDTH** to 0 GHz, then set the **CENTER** frequency as shown below:

- For 54107A, 54109A, and 54111A, set to a value that is 0.75 times the band-end frequency.
  Example for 54111A: 3*0.75=2250 MHz
- For all other models: 50 MHz.

Step 6. *For models 54107A, 54109A, and 54111A equipped with 50Ω RF outputs:*

- Connect a MA4601A power sensor to the Anritsu ML4803A power meter.

For models 54107A, 54109A, and 54111A equipped with 75Ω *RF outputs:*

- Connect a MA4603A power sensor and a J0365 Conversion Connector to the Anritsu ML4803A power meter.

For models 54117A, 54147A, 54161A, 54169A, and 54177A:

- Connect a MA4701A power sensor and precision adapter to convert to K and V connectors (as appropriate) to the Anritsu ML4803A power meter.

NOTES

- Perform a calibration as instructed in the power meter operation and service manual.
- Verify that the power meter Cal Factor is set correctly for the test frequency.

Model	Without Attenuator	With Attenuator
54107A, 54109A, 54111A; 50Ω output	+12 dBm	+10 dBm
54107A, 54109A, 54111A; 75Ω output	+10 dBm	+8 dBm
54117A	+10 dBm	+9 dBm
54147A	+10 dBm	+7 dBm
54161A, 54169A	+4 dBm	+1 dBm
54177A	+1 dBm	–2 dBm

FREQUENCY MENU
START
XX.XXX GHz
STOP
XX.XXX GHz
PRESS SELECT FOR CENTER/WIDTH

Step 7. Connect the power meter to the 541XXA RF Output connector (Figure 6-7, page 6-16).

Step 8. Press the 541XXA RF On/Off key to off. Zero the power meter, and then press RF On/Off key to on.

Step 9. Adjust variable resistor R56 (Figure 6-5 or 6-6, page 6-14) to provide a power meter reading equal to the 541XXA reset power level ±0.5 dBm. These levels are listed in the table at left.

Step 10. Reduce the 541XXA RF output power by 10 dB.

Step 11. Adjust variable resistor R190 (Figure 6-5 or 6-6) to give a power meter reading equal to the 541XXA set power ±0.5 dBm.

Step 12. Adjustments R56 and R190 are interactive. Therefore, set RF output power to reset level and repeat steps 9 through 11 until both power meter readings are within ±0.5 dBm of 541XXA indicated RF output power.

Step 13. Disconnect the power meter from the 541XXA RF Output connector.

ALC Operating Point Adjustment

Step 1. Restore 541XXA to its factory defaults, as described in Steps 1 and 2 on the preceding page

Step 2. Press the Frequency key.

Step 3. Select **START** from the displayed menu, and set the frequency as shown below.

- 54107A–54111A: Low-end frequency
- 54117A, 54147A, 54161A, 54169A, and 54177A: 10 MHz

Step 4. Select **STOP** from the displayed menu, and set the frequency as shown below.

- 54107A–54111A: High-end frequency
- 54117A, 54147A, 54161A, 54169A, and 54177A: 2 GHz

Step 5. Press the Channel 2 Display On/Off key to off.

Step 6. Press the Channel 1 Menu key

CHANNEL: 1 **INPUT: A**
TRANSMISSION
RETURN LOSS
SWR
POWER
DTF
VIEW CAL
SELECT INPUT
TRACE MEMORY
REF LINE
USE ◆ THEN PRESS SELECT

CHANNEL: 1 **SELECT INPUT**
NON-RATIO
A
B
R
RATIO:
A/R
B/R
USE ◆ THEN PRESS SELECT

Model	Without Attenuator	With Attenuator
54107A, 54109A, 54111A; 50Ω output	+14 dBm	+12 dBm
54107A, 54109A, 54111A; 75Ω output	+12 dBm	+10 dBm
54117A, 54147A	+12 dBm	+9 dBm
54154A – 54169A	–6 dBm	–9 dBm
54177A	–9 dBm	–12 dBm

Step 7. Using the Menu up/down and Select keys, configure the 541XXA for a power measurement using Input A , as follows:

- Choose **SELECT INPUT**, from the CHANNEL menu (top left)
- Then choose **NON-RATIO A**, from the SELECT INPUT menu (middle left).
- Select **POWER,** when you are returned to the CHANNEL menu.

Step 8. Press the Output Power key, and set to the power level shown in the table at bottom-left.

Step 9. Press the Graticule On/Off key to on.

Step 10. Set the oscilloscope as follows:

- Horizontal Sweep: X-Y mode
- CH 1 vertical sensitivity: 1V/div
- CH 2 vertical sensitivity: 0.5V/div (with X10 probe)
- CH 1 input: DC
- CH 2 input: DC
- Display: CH1 and CH 2 On

Step 11. Connect a suitable detector from the 541XXA RF Output connector to Input A.

Step 12. Press the Channel 1 AutoScale key (turn on).

Step 13. Connect oscilloscope CH 1 input to the 541XXA rear panel Horizontal Output connector using a BNC to BNC cable. Adjust the position controls for a flat trace in the center of the screen.

Step 14. Connect the oscilloscope CH2 probe to TP28 (Figure 6-5 or 6-6, page 6-14); connect the probe ground clip to the 541XXA chassis.

Step 15. Observe that the oscilloscope displays a waveform with a negative dc component (see figure on page 6-18)).

Step 16. *For models 54107A, 54109A, and 54111A:*

- Adjust A6R112 fully clockwise. Adjust A6R183 for an oscilloscope level of approximately –3.5V.

For models 54117A and 54147A:

- Confirm that the Unleveled LED does not light and that the oscilloscope trace is not oscillating. If either condition exists, adjust A19R31 on the multiband controller (Figure 6-8, page 6-18), or A6R133 (Figure 6-5, page 6-14) for 54117A, to move the oscilloscope trace slightly more negative until the oscillations or unleveled condition stops.

For models 54161A, 54169A, and 54177A:

- Confirm that the Unleveled LED does not light and that the oscilloscope trace is not oscillating. If either condition exists, adjust A23R31 on the multiband controller (Figure 6-9, page 6-20), or A24R93 (Figure 6-6, page 6-14) to move the oscilloscope trace slightly more positive until the oscillations or unleveled condition stops. Now move the potentiometer one additional turn to further increase the positive movement.

*This completes the microwave band pre-adjustment procedure. Proceed to the **500 MHz and 25 MHz Marker Adjustment**, paragraph **6-8**.*

6-8 500 MHz AND 25 MHz MARKER ADJUSTMENT

Use this procedure to make adjustments to the 500 MHz and 25 MHz marker assemblies (on the RF Deck) and to the A6 or A24 ALC/Frequency Instruction PCB (A24 is used on 54154A–54177A). Perform this procedure only if:

- ☐ The unit is a model 54117A through 54177A. (For models 54107A, 54109A, and 54111A, go to paragraph 6-11 on page 6-43).
- ☐ The unit displays frequency errors.
- ☐ One or more RF Deck components—except Down Converter— has been replaced.

SYSTEM MENU
DISK UTILITIES
SYSTEM SETUP
DATA POINTS
RESET
CONFIGURE:
SOURCE
ANALYZER
PLOTTER
APPLICATIONS
GPIB MODE
USE ◆ THEN PRESS SELECT

RESET MENU
RESET IS CONFIGURED TO KEEP:
CAL DATA
MARKERS
LIMITS
RESET
RESET TO FACTORY DEFAULTS
USE ◆ THEN PRESS SELECT

Measurement Technique

☐ This procedure uses a special 541XXA operating mode that displays the 500 MHz and 25 MHz markers on the internal monitor. The marker waveforms appear on a screen display with the horizontal axis graduated in frequency units. (These units are meaningless and are used only to quantisize the waveform width.)

☐ During this procedure, if the 541XXA does not display the marker(s) as described it is probably due to a failure to frequency-lock with the current marker adjustment settings. To overcome this problem, adjust the 500 MHz and 25 MHz marker sensitivity variable resistors until markers are displayed and then press the Self Test key. The 541XXA will perform a major frequency calibration and produce an accurate display.

Required Test Equipment

☐ Oscilloscope, dual channel with two X10 probes

Preliminary

☐ Remove the 541XXA top cover. (Refer to Chapter 7, paragraph 7-2 for instructions.)

☐ Perform the ALC Pre-Adjustment procedure (paragraph 6-6) before performing this procedure.

Marker Adjustment

Step 1. Disconnect any detectors connected to the signal channel inputs.

Step 2. Press the System Menu key and select **RESET** from the displayed menu (top left) using the Menu up/down and Select keys.

Step 3. From the RESET MENU (bottom left) select **RESET TO FACTORY DEFAULTS.**

CHANNEL: 1
INPUT: A
TRANSMISSION
RETURN LOSS
SWR
POWER
DTF
VIEW CAL
SELECT INPUT
TRACE MEMORY
REF LINE
USE ◆ THEN
PRESS SELECT

CHANNEL: 1
SELECT INPUT
NON-RATIO
A
B
R
RATIO:
A/R
B/R
USE ◆ THEN
PRESS SELECT

Model	Without Attenuator	With Attenuator
54117A	+0 dBm	–1 dBm
54119A – 54147A	+0 dBm	–3 dBm
54154A – 54169A	– 6 dBm	–9 dBm
54177A	–9 dBm	–12 dBm

Step 4. Using the Menu up/down and Select keys, configure the 541XXA for a power measurement using Input A , as follows:

- Choose **SELECT INPUT**, from the CHANNEL menu (top left)
- Then choose **NON-RATIO A**, from the SELECT INPUT menu (middle left).
- Select **POWER,** when you are returned to the CHANNEL menu.

Step 5. Press Channel 2 Display On/Off key to off.

Step 6. Press the Output Power key, and set the power level 10 dB below the Reset level, as shown in the table at bottom left.

Step 7. Press the Frequency and Select keys to display the CENTER/WIDTH menu.

Step 8. Set the **WIDTH** to 0.4 GHz (Center frequency will be set in a later step; for now, leave it at its default value.)

Step 9. Set the 541XXA for the Service Mode of operation, as follows:

- Press the Self Test key.
- When the Channel LED's begin flashing, sequentially press the Frequency, Markers, and Leveling keys.
- The 541XXA will now display the main service mode menu (next page).

SERVICE MODE

```
1      - direct control of frequency dacs
2      - diagnostic markers on/off
3      - frequency locking on/off
4      - frequency error message on/off
5      - enable dual autozero
6      - extended cpu self-test mode
7      - additional start sweep locking enable/disable
8      - 100 ms delay at start of sweep enable/disable
9      - variable delay for each data point
0      - ALC square wave test

stest  return to normal operation
```

Step 10. Press the Data Entry "2" key to select the diagnostic markers status menu (below).

SERVICE MODE

```
diagnostic marker status

1      - markers on
2      - markers off

NOTE: if markers on and in cw mode, the cw
filter will be set according to sweep width.
clear  return to service mode main menu
stest  return to normal operation
```

Step 11. Press the Data Entry "1" key to turn the marker display on.

Step 12. Press the Self Test key.

Step 13. When self test completes, the display should resemble that shown in Figure 6-10.

NOTES

- If the 541XXA fails self test, press the Select key to obtain a measurement display.
- The 500 MHz markers are one graticle division in height; the 25 MHz markers are one-half division.

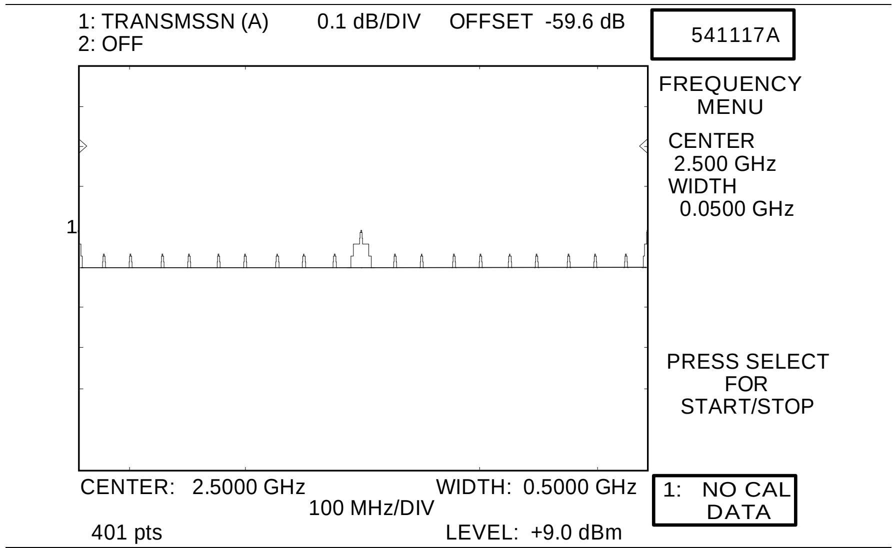


Figure 6-10. *Special Markers Mode Display*

541XXA Model	Set Frequency (GHz)
54117A, 54119A	8.400
54128A	12.2
54130A	19.800
54131A	15.800
54136A	26.300
54137A, 54147A, 54154A thru 54177A	19.800

Step 14. Load the RF output connector by connecting an appropriate 560 Series detector. However, DO NOT connect the detector to a channel input (Input A, B, or R).

Step 15. Press the Frequency key to display the CENTER/WIDTH menu

Step 16. Set the **CENTER** frequency to the value shown in the table at left for the model being tested.

Step 17. Connect a BNC-to-BNC cable from the 541XXA Horizontal Output connector to the oscilloscope "X" input.

Step 18. Place the oscilloscope in "XY" and adjust the horizontal gain for a full display.

541XXA Model	Level (Volts)
54117A, 54119A	–0.70
54128A	–1.25
54130A	–1.25
54131A	–2.00
54136A	–0.70
54137A thru 54177A	–0.60

541XXA Model	Frequency (GHz)
54117A, 54119A	2.5
54128A	8.5
54130A	13
54131A	10.5
54136A	17.5
54137A thru 54177A	2.5

Step 19. Remove the cover from the 25 MHz Module and connect a X10 probe between the oscilloscope CH2 Input and U3-pin 3 (Figure 6-11).

NOTE

Figure 6-11 shows the 25 MHz and 500 MHz modules ganged together, as they are for the 54137A and 54147A. Although the two units are separated on the other models, the adjustments are in the same relative locations.

Step 20. Adjust R80 (Figure 6-5 or 6-6, Page 6-14) for the voltage value shown in the table at left. (These voltages will be referred to as “trip” levels in a later step.)

Step 21. Set the 500 MHz I/F tracking potentiometer R21 (Figure 6-11) fully counter-clockwise.

Step 22. Press the Frequency and Select keys to select the CENTER/WIDTH menu.

Step 23. Set the **WIDTH** to 0.5 GHz and the **CENTER** frequency 0.5 GHz above the low band edge frequency of the unit, as shown in the table at left.

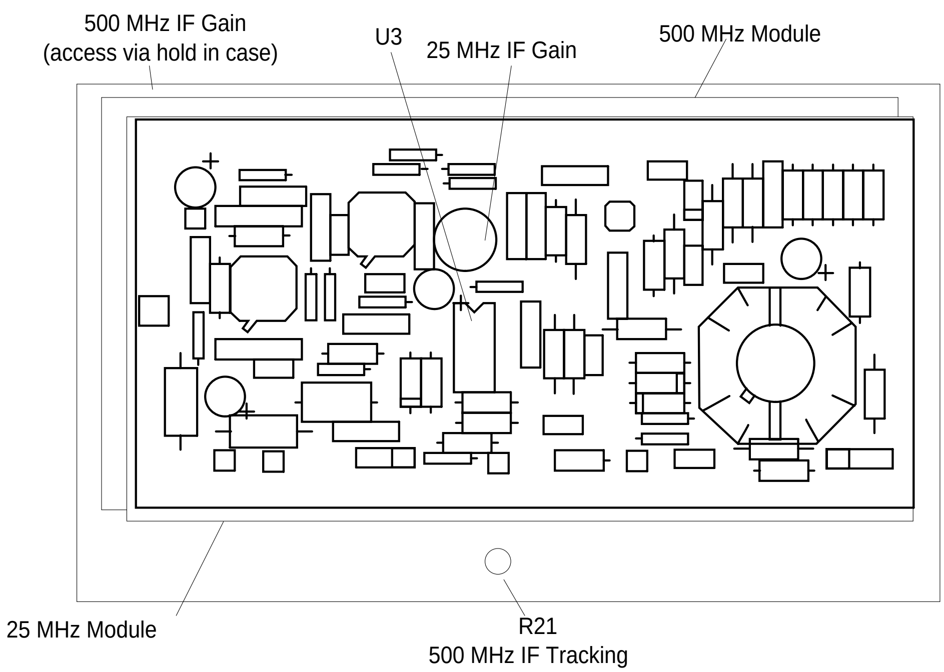


Figure 6-11. *25 MHz and 500 MHz Modules Adjustment Locations (54137A thru 54177A)*

541XXA Model	Frequency (GHz)
54117A, 54119A	8.0
54128A	12.0
54130A	19.5
54131A	15.5
54136A	26.0
54137A thru 54177A	19.5

Step 24. Adjust the 500 MHz IF gain and the 25 MHz IF gain potentiometers (Figure 6-11) to obtain all marker with no spurious, as observed on the 541XXA display (Figure 6-12).

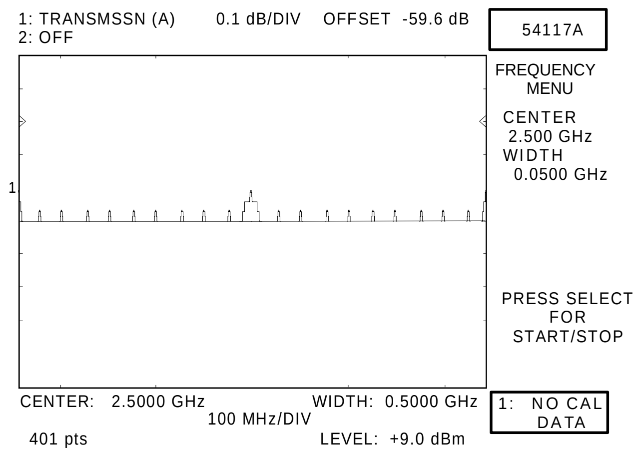


Figure 6-12. *541XXA Display of 500 MHz Markers*

NOTE

500 MHz spurious on the 54117A/54119A are acceptable provided they are less than 3 MHz. (To determine width, use the main and relative cursor, as described in steps 32 thru 36, below.)

Step 25. Set the **CENTER** frequency to 0.5 GHz below the model's high-end frequency, as shown in the table at top left.

541XXA Model	Frequency (GHz)
54117A, 54119A	2.5
54128A	8.5
54130A	13
54131A	10.5
54136A	17.5
54137A thru 54177A	2.5

Step 26. If fitted, adjust the 500 MHz I/F tracking potentiometer R21 (Figure 6-9) to obtain all marker with no spurious, as observed on the 541XXA display (Figure 6-10).

Step 27. Press the Self Test key. Repeat steps 24 through 26 until the unit passes self test.

Step 28. Press the Frequency and Select keys to display the CENTER/ WIDTH menu.

Step 29. Set **WIDTH** to 0.75 GHz and **CENTER** to 0.5 GHz above the model's low-end frequency, as shown in the table at left.

Step 30. On the 500 MHz module, increase the 500 MHz IF Gain potentiometer (Figure 6-11) until spurious 500 MHz markers appear, or until saturation occurs (Figure 6-13). Reduce the gain until the spurious markers disappear.

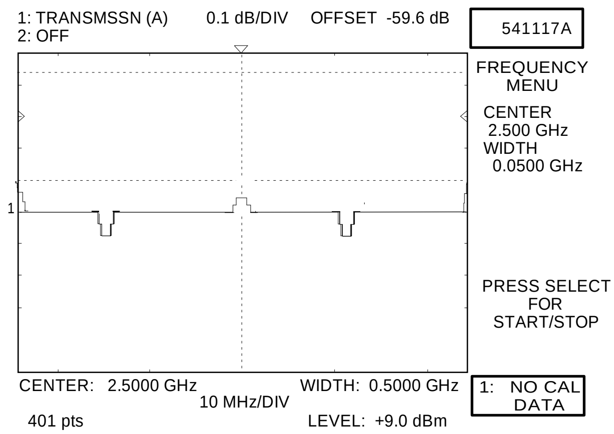


Figure 6-13. *500 MHz Markers in Saturation*

NOTE

For 54117A and 54119A spurious 500 MHz markers at mid 500MHz marker points (example: 2.750GHz for the 54117A) will normally be present when the gain is increased sufficiently to give adequate markers at 8.5 GHz. Confirm that these mid-marker-spurious widths are less than 3 MHz. Spurious markers close in on either side of the main 500 MHz marker, as shown in figure 6-14, are not acceptable and the gain should be reduced to remove them. (To determine width, use the main and relative cursor, as described in steps 32 thru 36, below.)

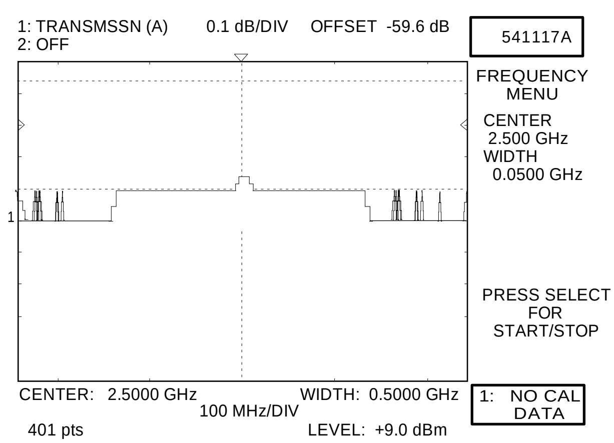


Figure 6-14. *500 MHz Markers Showing Spurious-Signal Response*

Step 31. Set **WIDTH** to 0.05 GHz.

Step 32. Press the Cursor On/Off key to on.

CURSOR
NON-RATIO
1: XX.XXdB
2: XXXX GHz

RELATIVE
1: XX.XXdBr
X.XXXX GHz

Between 17 and 23 GHz

541XXA Model	Frequency (GHz)
54117A, 54119A	8.0
54128A	12.0
54130A	19.5
54131A	15.5
54136A	26.0
54137A 54147A	19.5
54154A 54177A	19.5

541XXA Model	Frequency (GHz)
54117A, 54119A	2.5
54128A	8.5
54130A	13
54131A	10.5
54136A	17.5
54137A thru 54177A	2.5

Step 33. Rotate the Data Entry knob to position the main cursor to the low-frequency edge of the displayed marker.

Step 34. Press the Relative cursor key to display the relative cursor.

Step 35. Rotate the Data Entry knob to position the relative cursor to the high-frequency edge of the displayed marker.

Step 36. Read the relative cursor width from the displayed menu (left).

Step 37. Adjust the 500 MHz Gain potentiometer (Figure 6-11) for a marker width of 20 ±3 MHz.

Step 38. Press the Frequency and Select keys to display the CENTER/ WIDTH menu.

Step 39. Set **WIDTH** to 0.05 GHz and **CENTER** as shown in the table at middle-left.

Step 40. For all models that have R21 installed (Figure 6-11), adjust R21 to:

- Increase the width of the 500 MHz marker until saturation occurs (Figure 6-13).
- Decrease marker width until the marker just comes out of saturation; note its width value.
- Reduce marker width to 12.5 MHz; –0, +3.5 MHz, as observed on the CURSOR menu.

Step 41. For all units not fitted with R21 marker adjustment pot:

- Confirm that the 500MHz marker is present and of the correct width, 12-26MHz, as observed in the cursor menu.

Step 42. Press the Frequency and Select keys to display the CENTER/ WIDTH menu.

Step 43. Set **WIDTH** to 0.75 GHz and **CENTER** as shown in the table at bottom left.

Step 44. Connect the oscilloscope's CH 2 (Y-input) to U3, pin 2 (Figure 6-11), using a X10 probe.

Step 45. Remove the cover from the Divider Module and adjust C16 (Figure 6-15) for an optimum marker response, as shown in Figure 6-16.)

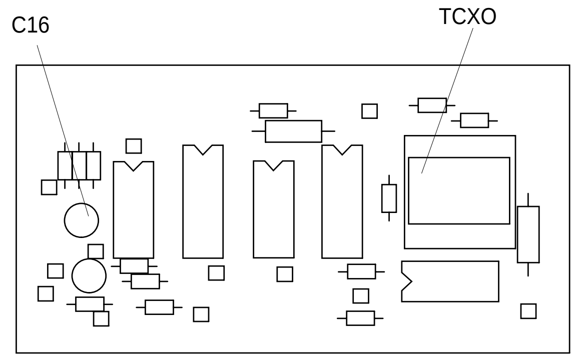


Figure 6-15. *Divider Module*

Step 46. Press the Frequency and Select keys to display the CENTER/ WIDTH menu.

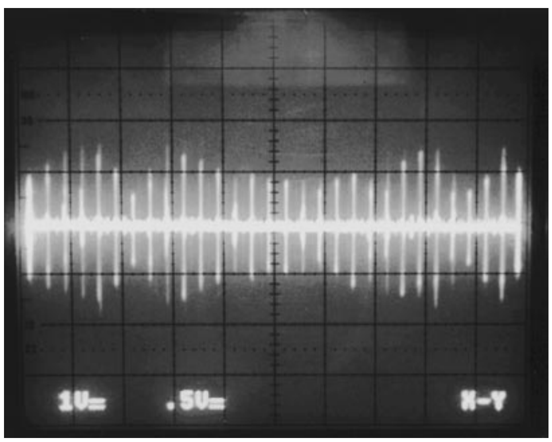


Figure 6-16. *Marker Reponse on Oscilloscope*

Step 47. Set **WIDTH** to 0.3 GHz.

Step 48. Reduce the **CENTER** frequency by 0.25 GHz.

Model	Maximum Spurious Marker Size (Volts)
54117A, 54119A	1.6
54128A, 54130A	1.2
54131A	1.5
54136A	1.0
54137A – 54177A	1.1

Step 49. Adjust the 25 MHz IF Gain potentiometer (Figure 6-11) to provide a spurious signal on oscilloscope (Figure 6-17). Ensure that the maximum value does not exceed that shown in the table at left for the model under test.

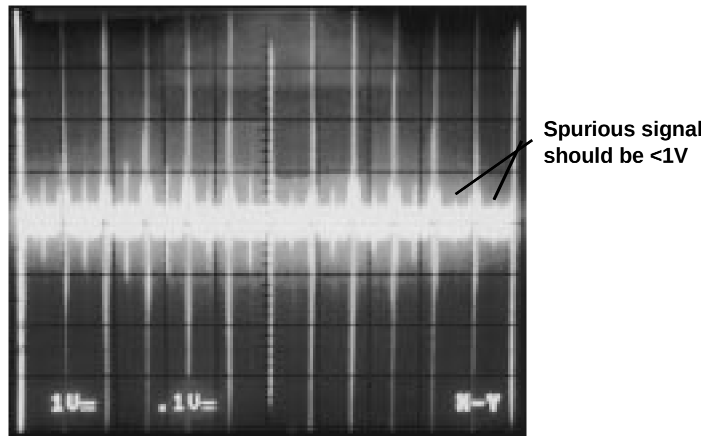


Figure 6-17. *Oscilloscope Spurious Signal Display*

Step 50. Increase the center frequency and observe the spurious-signal level, as follows:

- Note the level of the spurious signals at the current center frequency.
- While observing the spurious-signal levels for worst-case response (highest amplitude), increase the center frequency in 300 MHz increments to the high end of the range or until spurious markers are no longer visible.

NOTE

If the spurious signal is greater than the value listed in the table top left, adjust the 25MHz gain pot (figure 6-11) to reduce it to the level in the table.

- Return the center frequency to the point of worst-case spurious-signal response.

■ Record the values of the thick and thin portion of the displayed waveform (Figure 6-18).

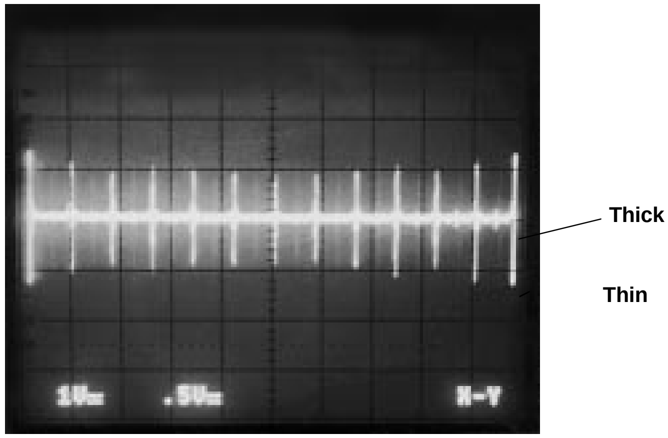


Figure 6-18. *Oscilloscope "Thick and Thin Portion" Display*

Model	Marker Size in Volts	
	Thick	Thin
54117A, 54119A	3.5	>5.0
54128A	2xTrip	>2xTrip
54130A	2xTrip	>2xTrip
54131A	1.5xTrip	>1.5xTrip
54136A	2xTrip	>2xTrip
54137A thru 54177A	3.5	>5.0

* The trip voltage is measured on U3, pin 3, in the 25 MHz module. This voltage varies with frequency and must be measured to determine its value at the 541XXA output frequency.

Step 51. Verify that the thick and thin portions of the above waveform exceed the values shown in the table at left.

Step 52. Set the oscilloscope CH2 input multiplier for 0.2 V/div.

Step 53. Verify that the noise level is 250 mV or less (Figure 6-19).

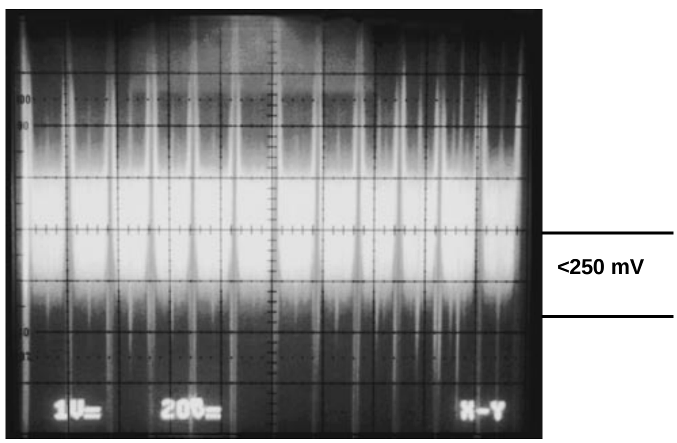


Figure 6-19. *Oscilloscope Noise Level Display*

Step 54. Connect a counter to the 25 MHz output from the divider module (Figure 6-15), and adjust the TCXO crystal for a counter reading of 25 MHz ±5Hz.

6-9 HETERODYNE BAND 25 MHz MARKER VERIFICATION FOR 54117A, 54147A, 54161A, 54169A, or 54177A

Use this procedure to check the 25 MHz markers throughout the heterodyne band of models 54117A, 54147A, 54161A, 54169A, 54177A . This procedure uses the same measurement technique as used in the 500 MHz and 25 MHz marker adjustment procedure to verify that the heterodyne band 25 MHz markers are present and of the correct width. If any problems are found, the unit is defective and no adjustment should be attempted.

Required Test Equipment

☐ Oscilloscope, dual channel with two X10 probes

Preliminary

☐ Remove the 541XXA top cover. (Refer to Chapter 7, paragraph 7-2 for instructions.)

FREQUENCY MENU

CENTER
XX.XXX GHz

WIDTH

0.025 GHz

PRESS SELECT
FOR
START/STOP

Procedure

Step 1. Perform steps 1 through 12 of the 500 MHz and 25 MHz Marker Adjustment procedure (page 6-26).

Step 2. Press the Frequency and Select keys to display the CENTER/WIDTH menu (left).

Step 3. Set **WIDTH** to 0.25 GHz and **CENTER** frequency to the first value listed in the table below.

Test	Set Frequency (GHz)	Test	Set Frequency (GHz)
1	0.135	6	1.100
2	0.300	7	1.300
3	0.500	8	1.500
4	0.700	9	1.700
5	0.900	10	1.900

Step 4. The 25 MHz markers should be displayed on the Channel 1 trace. Verify that there is a marker at each 25 MHz point and there are no spurious markers. Use the cursor as necessary to identify each 25 MHz point.

Step 5. Set the center frequency to each of the remaining frequencies in the table. Verify the markers as in step 4.

Step 6. Press the Output Power key and set the power level to 0 dBm or minimum output power level. Repeat steps 2 through 5.

6-10 ALC/RF POWER ADJUSTMENT FOR MODELS 54117A – 54147A

Use this procedure to make final adjustments to the A6 ALC/Frequency Instruction PCB for models 54117A through 54147A. For models 54107A, 54109A, and 54111A, go to paragraph 6-12, ALC/RF Power Adjustment For RF Band Models. For models 54154A through 54177A, go to paragraph 6-11, ALC/RF Power Adjustment For Models 54154A–54177A.

This procedure is in three parts: Reference Voltage Adjustment, Power Output Adjustment, and ALC Operating Point Adjustment. All variable resistors (Rx) and test points (TPx) referred to in this procedure are on the A6 ALC/Frequency Instruction PCB. The variable resistor designations (Rx) referenced in the following procedures are for the D35429-3 version of the A6 PCB.

Required Test Equipment

☐ Power Meter, with suitable matching power sensor

☐ Digital Voltmeter, with 4-1/2 digits resolution

☐ Oscilloscope, dual channel with two X10 probes

☐ ANRITSU RF Detector to match 541XXA model

Preliminary

☐ Remove the 541XXA top cover. (Refer to Chapter 7, paragraph 7-2 for instructions.)

A6 PCB Configuration

☐ Verify the jumper configuration of the A6 PCB per table below.

541XXA Model	PCB Jumpers		Jumpers		
	J5	J6	J7	J8	J9
54117A	2 & 3 (bottom)	2 & 3 (bottom)	1 & 2*	2 & 3	1 & 2
54147A	2 & 3 (bottom)	1 & 2 (top)	1 & 2*	2 & 3	2 & 3
All Others	1 & 2 (top)	2 & 3 (bottom)	1 & 2*	2 & 3	either

*Use pins 2 & 3 if performing adjustment prior to Temperature Compensation procedure.

SYSTEM MENU
DISK UTILITIES
SYSTEM SETUP
DATA POINTS
RESET
CONFIGURE:
SOURCE
ANALYZER
PLOTTER
APPLICATIONS
GPIB MODE
USE ◆ THEN PRESS SELECT

RESET MENU
RESET IS CONFIGURED TO KEEP:
CAL DATA
MARKERS
LIMITS
RESET
RESET TO FACTORY DEFAULTS
USE ◆ THEN PRESS SELECT

Reference Voltage Adjustment

☐ If the ALC Pre-Adjustment procedure (paragraph 6-6) was performed during this session, proceed with the Power Output Adjustment procedure, below. Otherwise, perform Reference Voltage Adjustment in Steps 1 through 5 of the pre-adjustment procedure. Then proceed with the Power Output Adjustment procedure, below.

Power Output Adjustment

☐ The pre-adjustment and final adjustment procedures for power output adjustment are identical, except for certain measurement tolerances. Perform the procedure in paragraph 6-6 at this time as the final adjustment. If the pre-adjustment procedure was performed in a previous session, perform it again to verify the adjustments and to make necessary corrections. Then, proceed to the ALC Flatness Adjustment procedure, below.

NOTE

Pre-adjustment specification is ±0.5 dB, but at this point the specification is tightened to ±0.05 dB.

ALC Flatness Adjustment

Step 1. Press the System Menu key and select **RESET** from the displayed menu (top left) using the Menu up/down and Select keys.

Step 2. From the RESET MENU (bottom left) select **RESET TO FACTORY DEFAULTS.**

Step 3. Press the Frequency key to display the START/STOP menu.

- For all models, except 54117A and 54147A: Set START and **STOP** for the low- and high-end frequencies.
- *For 54117A and 54147A:* Set **START** for 2.0 GHz and **STOP** for the high-end frequency.

Step 4. Press Channel 2 Display On/Off key to off.

CHANNEL: 1
INPUT: A
TRANSMISSION
RETURN LOSS
SWR
POWER
DTF
VIEW CAL
SELECT INPUT
TRACE MEMORY
REF LINE
USE ◆ THEN
PRESS SELECT

Step 5. Press the Menu up/down and Select keys, configure the 541XXA for a power measurement using Input A, as follows:

- Choose **SELECT INPUT**, from the CHANNEL menu (top left)
- Then choose **NON-RATIO A**, from the SELECT INPUT menu (middle left).
- Select **POWER,** when you are returned to the CHANNEL menu.

Step 6. Press the Output Power key, and set to 5 dB below the Reset level.

Step 7. Press the Graticule On/Off key to on.

Step 8. Connect a suitable 560 or 5400 Series detector between the Input A and RF Output connectors.

CHANNEL: 1
SELECT INPUT
NON-RATIO
A
B
R
RATIO:
A/R
B/R
USE ◆ THEN
PRESS SELECT

Step 9. Press the Channel 1 AutoScale key.

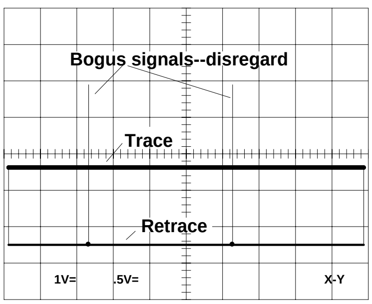
Step 10. Observe the Channel 1 trace on the 541XXA display.

Step 11. Adjust A6R90 (Figure 6-5, page 6-14) to obtain a flat trace per the output power flatness specifications shown in the table below.

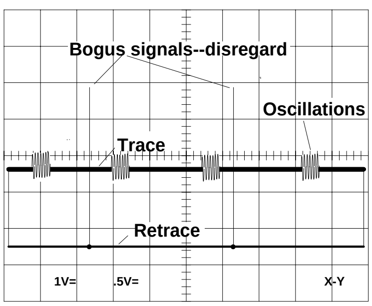
Model	Without Attenuator	With Attenuator
54117A, 54130A, 54137A	±0.5 dB	±1.0 dB
54119A, 54128A, 54131A	±0.4 dB	±0.9 dB
54136A	±1.0 dB	±2.5 dB
54147A	±0.75 dB	±1.0 dB

Step 12. If a flat trace can not be obtained, move jumper A6P2 to the other end of header J1 and repeat the adjustment of A6R90.

Model	Without Attenuator	With Attenuator
54117A	+12 dBm	+10 dBm
54119A – 54147A	+12 dBm	+9 dBm



Waveform at TP28, 54117–54136A



Waveform at TP28 with Oscillations

ALC Operating Point Adjustment

Step 1. Press Output Power and set the power level as shown in the table at top left.

Step 2. Set oscilloscope controls as follows:

- Horizontal Sweep: X-Y mode
- CH 1 vertical sensitivity: 1V/div
- CH 2 vertical sensitivity: 0.5V/div (with X10 probe)
- CH1 input: DC
- CH2 input: DC

Step 3. Connect a BNC-to-BNC cable between the 541XXA rear panel Horizontal Output connector and CH1 (X Input) on the oscilloscope.

Step 4. Adjust the position controls on the oscilloscope for a flat trace in the center of the screen.

Step 5. Connect the oscilloscope's CH2 probe to A6TP28 (Figure 6-5, page 6-14); connect the probe ground clip to the 541XXA chassis.

Step 6. Observe that the oscilloscope displays a waveform with a negative dc component (middle left).

Step 7. *For 54117A through 54136A:*

- Adjust A6R133 to move the oscilloscope trace more positive until the trace oscillates (bottom left). and/or the 541XXA Unleveled LED lights.
- Adjust A6R133 back two turns (trace more negative).

For 54137A and 54147A:

- Adjust A19R31 on the multiband controller (Figure 6-8, page 6-19) to move the oscilloscope trace more positive until the trace oscillates and/or the 541XXA Unleveled LED lights.
- Adjust A19R31 back two turns (trace more negative).

Model	Without Attenuator	With Attenuator
54117A	+12 dBm	+10 dBm
54119A – 54147A	+12 dBm	+9 dBm

Step 8. Reduce the RF power by 12 dB for all units except 54117A with attenuator. Reduce the RF power by 11dB for 54117A with attenuator.

Step 9. Observe the oscilloscope display and verify that there are no oscillations present. If oscillations are present, readjust A6R133 (A19R31 for 54137A/54147A) negative or positive until the oscillation stops. Continue the adjustment one turn past the point where oscillation stops.

Step 10. If potentiometer A6R133 (A19R31) was readjusted in step 9, again set the output power level as shown in the table at top left and confirm that no oscillations are present.

Step 11. For the 54117A and 54147A, go to paragraph 6-12 (page 6-50) to perform adjustments for the 0.01 to 2 GHz band. For all other models, go to paragraph 6-13 (page 6-57), Temperature Compensation Adjustments.

6-11 ALC/RF POWER ADJUSTMENT FOR MODELS 54154A – 54177A

Use this procedure to make final adjustments to the A24 ALC/Frequency Instruction PCB for models 54154A through 54177A.

This procedure is in four parts: Reference Voltage Adjustment, Power Output Adjustment, Minimum RF Power When Set to Maximum RF Power Check, and ALC Operating Point Adjustment. All variable resistors (Rx) and test points (TPx) referred to in this procedure are on the A24 ALC/Frequency Instruction PCB.

Required Test Equipment

- ☐ Power Meter, with suitable matching power sensor
- ☐ Digital Voltmeter, with 4-1/2 digits resolution
- ☐ Oscilloscope, dual channel with two X10 probes
- ☐ ANRITSU RF Detector to match 541XXA model

A24 PCB Configuration

- ☐ If the Temperature Compensation Adjustment (paragraph 6-14) is to be performed, install J7 jumper between pins 2 and 3. Otherwise, install J7 jumper between pins 1 and 2. (Pins 1 and 2, temperature compensation is on; pins 2 and 3, temperature compensation is off.)

SYSTEM MENU
DISK UTILITIES
SYSTEM SETUP
DATA POINTS
RESET
CONFIGURE:
SOURCE
ANALYZER
PLOTTER
APPLICATIONS
GPIB MODE
USE ◆ THEN PRESS SELECT

RESET MENU
RESET IS CONFIGURED TO KEEP:
CAL DATA
MARKERS
LIMITS
RESET
RESET TO FACTORY DEFAULTS
USE ◆ THEN PRESS SELECT

FREQUENCY MENU
START
02.000 GHz
STOP
XX.XXX GHz
PRESS SELECT FOR CENTER/WIDTH

Reference Voltage Adjustment

☐ If the ALC Pre-Adjustment procedure (paragraph 6-6) was performed during this session, proceed with the Power Output Adjustment procedure, below. Otherwise, perform Reference Voltage Adjustment in Steps 1 through 5 of the pre-adjustment procedure. Then proceed with the Power Output Adjustment procedure, below.

Power Output Adjustment

☐ The pre-adjustment and final adjustment procedures for power output adjustment are identical, except for certain measurement tolerances. Perform the procedure in paragraph 6-6 at this time as the final adjustment. If the pre-adjustment procedure was performed in a previous session, perform it again to verify the adjustments and to make necessary corrections. Then, proceed to the ALC Flatness Adjustment procedure, below.

NOTE

Pre-adjustment specification is ±0.5 dB, but at this point the specification is tightened to ±0.05 dB.

Minimum RF Output Power Check

☐ This procedure checks that the Source module's RF output power is 0.5 dBm greater the 541XXA specified output power level when the cursor is set to the maximum output power setting.

Step 1. Press the System Menu key and select **RESET** from the displayed menu (top left) using the Menu up/down and Select keys.

Step 2. From the RESET MENU (bottom left) select **RESET TO FACTORY DEFAULTS.**

Step 3. Press the Output Power key and rotate the Data Entry knob to maximum allowable power level (maximum over-range).

Step 4. Press the Frequency key to display the START/STOP menu (left).

- Set **START** for the 2.0 GHz.
- Set **STOP** for the high-end frequency.

Step 5. Press Channel 2 Display On/Off key to off.

Step 6. Connect the ANRITSU RF detector between the RF Output and the Input A connectors.

CHANNEL 1
MOVE CURSOR
TO
MAXIMUM
MINIMUM
NEXT MKR
dB SEARCH
X.XX dBr
SETUP
OPTIONS
SET CHAN 2
USE ♦ THEN
PRESS SELECT

CURSOR
1: XX.XXdB
2: XXXX GHz
1: XX.XXdBr
X.XXXX GHz

FREQUENCY
MENU
CENTER
XX.XXX GHz
WIDTH
0.500 GHz
PRESS SELECT
FOR
CENTER/WIDTH

Step 7. Press the Cursor On/Off key.

Step 8. Press the Select key.

Step 9. Choose **MINIMUM** from the displayed menu (top left); then press Select to return to the CURSOR menu.

Step 10. Record the frequency from the displayed Cursor menu (middle left).

Step 11. Press the Frequency key to display the CENTER/WIDTH menu.

Step 12. Set the **WIDTH** to 500 MHz, and set the **CENTER** frequency to the frequency recorded in Step 9.

Step 13. Repeat steps 6 through 9, above.

Step 14. Press the Frequency key to display the CENTER/WIDTH menu.

Step 15. Set the **CENTER** frequency to the frequency recorded from the actions performed in Step 12, above.

Step 16. Connect the power sensor to the power meter; calibrate the power meter and set the CAL FACTOR for the frequency set in Step 15, above.

Step 17. Connect the power sensor to the 541XXA RF Output connector.

Step 18. Read the power meter and ensure that the reading is ≥ 0.5 dBm above the guaranteed RF output power level.

Example: For 54169A with attenuator, ensure reading is ≥1.5 dBm.

FREQUENCY MENU
START
02.000 GHz
STOP
XX.XXX GHz
PRESS SELECT FOR CENTER/WIDTH

CHANNEL: 1 INPUT: A
TRANSMISSION
RETURN LOSS
SWR
POWER
DTF
VIEW CAL
SELECT INPUT
TRACE MEMORY
REF LINE
USE ◆ THEN PRESS SELECT

CHANNEL: 1 SELECT INPUT
NON-RATIO
A
B
R
RATIO:
A/R
B/R
USE ◆ THEN PRESS SELECT

ALC Flatness Adjustment

Step 1. Press the Frequency key to display the START/STOP menu (left).

- Set **START** for the 2.0 GHz.
- Set **STOP** for the high-end frequency.

Step 2. Press Channel 2 Display On/Off key to off.

Step 3. Press the Menu up/down and Select keys, configure the 541XXA for a power measurement using Input A, as follows:

- Choose **SELECT INPUT**, from the CHANNEL menu (top left)
- Then choose **NON-RATIO A**, from the SELECT INPUT menu (middle left).
- Select **POWER,** when you are returned to the CHANNEL menu.

Step 4. Press the Output Power key, and set to the power level 5 dB below Reset power, as shown in the table below.

Model	Without Attenuator	With Attenuator
54154A thru 54169A	–1 dBm	–4 dBm
54177A	–4 dBm	–7 dBm

Step 5. Press the Graticule On/Off key to on.

Step 6. Connect a suitable 560 or 5400 Series detector between the Input A and RF Output connectors.

Step 7. Press the Channel 1 AutoScale key.

Step 8. Observe the Channel 1 trace on the 541XXA display.

Step 9. Adjust A24R90 (Figure 6-6, page 6-14) to obtain a flat trace per the output power flatness specifications shown in the table below.

Model	Without Attenuator	With Attenuator
54154A thru 54169A	±1.0 dB	±2.0 dB
54177	±1.0 dB	±3.0 dB

Model	Without Attenuator	With Attenuator
54154A thru 54169A	–6 dBm	–9 dBm
54177A	–9 dBm	–12 dBm

Step 10. If a flat trace can not be obtained, move jumper A24P2 to the other end of header J1 and repeat the adjustment of A24R90.

ALC Operating Point Adjustment

Step 1. Press Output Power and set the power level to the value shown in the table shown at top left.

Step 2. Set oscilloscope controls as follows:

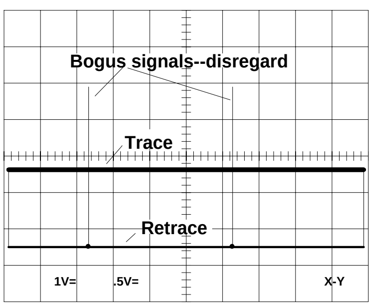
- Horizontal Sweep: X-Y mode
- CH 1 vertical sensitivity: 1V/div
- CH 2 vertical sensitivity: 0.5V/div (with X10 probe)
- CH1 input: DC
- CH2 input: DC

Step 3. Connect a BNC-to-BNC cable between the 541XXA rear panel Horizontal Output connector and CH1 (X Input) on the oscilloscope.

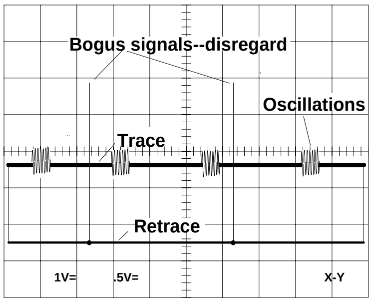
Step 4. Adjust the position controls on the oscilloscope for a flat trace in the center of the screen.

Step 5. Connect the oscilloscope's CH2 probe to A24TP28 (Figure 6-9, page 6-20); connect the probe ground clip to the 541XXA chassis.

Step 6. Observe that the oscilloscope displays a waveform with a negative dc component (bottom left).



Waveform at TP28



Waveform at TP28 with Oscillations

Step 7. *For 54154A through 54169A:*

- Adjust A23R31 (Figure 6-9, page 6-20) to move the oscilloscope trace more negative until the trace oscillates. and/or the 541XXA Unleveled LED lights.

- Adjust A23R31 back two turns (trace more positive).

For 54177A:

- Adjust A23R31 on the multi-band controller to move the front part of the oscilloscope trace more negative until the trace oscillates and or the unit becomes unlevelled. (Some units may not become unlevelled or oscillate.) Now, readjust A23R31 two turns to make the oscilloscope trace more positive.

NOTE

Only the front part of the scope trace will move when A23R31 is adjusted.

- Adjust A24R93 on the ALC PCB as A23R31 was adjusted to set the end part of the trace to the correct level (that is, two turns more positive from the unleveled and/or oscillation point).

  If the end part of the scope trace is more negative than the front part of the trace, adjust A24R93 to align both parts of the scope trace.

  If it is more positive leave the adjustment of A24R93 as is.

Step 8. *For 54154A through 54169A:*

- Increase the power output level by 10 dB.

- Observe the oscilloscope display and verify that there are no oscillations present. If oscillations are present, readjust A23R31 to made the front part of the trace more negative until the oscillation stops.

- Now, readjust A23R31 one more turn to make the trace more negative.

For 54177A:

- Increase the power output level by 10 dB.
- Observe the oscilloscope display and verify that there are no oscillations present. If oscillations are present, readjust A23R31 to made the front part of the trace more negative until the oscillation stops.
- Now, readjust A23R31 one more turn to make the trace more negative.
- If the end part of the trace is oscillating, readjust A24R93 in concert with A23R31 to set the end part of the trace to the correct level.

Step 9. *For the 54161A, 54169A, and 54177A, go to paragraph **6-12** to perform adjustments for the **0.01** to 2 GHz band.*

6-12 ALC/RF POWER ADJUSTMENT FOR RF BAND MODELS

Use this procedure to make (final) adjustments to the ALC/Frequency Instruction PCB for models 54107A through 54111A and for the RF (heterodyne) band of models 54117A, 54147A, 54161A, 54169A, and 54177A.

This procedure is in three parts: Reference Voltage Adjustment , Power Output Adjustment Procedure, and ALC Operating Point Adjustment Procedure. Unless otherwise noted, all variable resistors (Rx) and test points (TPx) referred to in this procedure are on the ALC/ Frequency Instruction PCB. For the 54154A–54177A, this is A24; for all others, it is A6.

Required Test Equipment

☐ Digital Voltmeter, with 4-1/2 digits resolution

☐ Oscilloscope, dual channel with two X10 probes

☐ ANRITSU RF Detector

Preliminary

☐ Remove the 541XXA top cover. (Refer to Chapter 7, paragraph 7-2 for instructions.)

☐ Set up test equipment as shown in Figure 6-20.

A6 PCB Configuration

☐ For 54107A, 54109A, and 54111A, verify the jumper configuration of the ALC/Frequency Instructions PCB per table below. (For 54117A, 54147A, 54161A, 54163A, 54169A, and 54177A, jumpers were set in paragraphs 6-10 and 6-11.)

PCB Jumpers		D35429-3 PCB Jumpers		
J5	J6	J7	J8	J9
1 & 2 (top)	2 & 3 (bottom)	1 & 2*	1 & 2	2 & 3

*Use pins 2 & 3 if performing adjustment prior to Temperature Compensation procedure.

SYSTEM MENU
DISK UTILITIES
SYSTEM SETUP
DATA POINTS
RESET
CONFIGURE:
SOURCE
ANALYZER
PLOTTER
APPLICATIONS
GPIB MODE
USE ◆ THEN PRESS SELECT

RESET MENU
RESET IS CONFIGURED TO KEEP:
CAL DATA
MARKERS
LIMITS
RESET
RESET TO FACTORY DEFAULTS
USE ◆ THEN PRESS SELECT

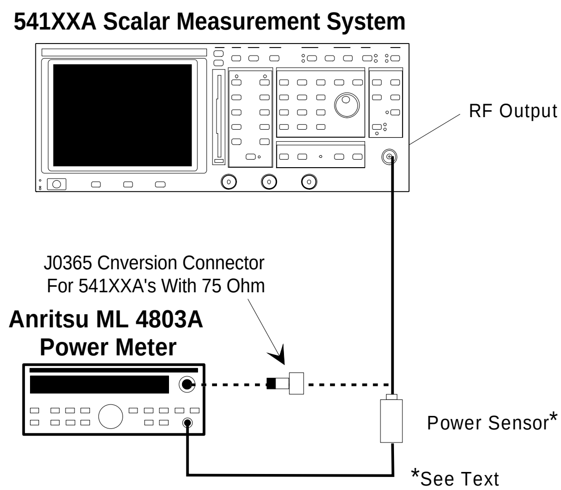


Figure 6-20. *Equipment Setup for ALC Pre-Adjustment Procedure*

Power Output Adjustment

☐ The pre-adjustment and final adjustment procedures for power output adjustment are identical. Perform the Power Output Adjustment procedure for RF models in paragraph 6-7 at this time as the final adjustment. If the pre-adjustment procedure was performed in a previous session, perform it again to verify the adjustments and to make necessary corrections.

NOTE

Pre-adjustment specification is ±0.5 dB, but is changed to ±0.05 dB for this step.

ALC Flatness Adjustment

Step 1. Press the System Menu key and select **RESET** from the displayed menu (top left) using the Menu up/down and Select keys.

Step 2. From the RESET MENU (bottom left) select **RESET TO FACTORY DEFAULTS.**

Step 3. Press the Frequency key to display the START/STOP menu .

- For 54107A–54111A: Set **START** and **STOP** for the low- and high-end frequencies.
- *For 54117A, 54147A, 54161A, 54169A, 54177A:* Set **START** for 0.01 GHz and **STOP** for 2.0 GHz.

Step 4. Press Channel 2 Display On/Off key to off.

CHANNEL: 1 INPUT: A
TRANSMISSION
RETURN LOSS
SWR
POWER
DTF
VIEW CAL
SELECT INPUT
TRACE MEMORY
REF LINE
USE ◆ THEN PRESS SELECT

CHANNEL: 1 SELECT INPUT
NON-RATIO
A
B
R
RATIO:
A/R
B/R
USE ◆ THEN PRESS SELECT

Step 5. Press the Menu up/down and Select keys, configure the 541XXA for a power measurement using Input A, as follows:

- Choose **SELECT INPUT**, from the CHANNEL menu (top left)
- Then choose **NON-RATIO A**, from the SELECT INPUT menu (middle left).
- Select **POWER,** when you are returned to the CHANNEL menu.

Step 6. Press the Output Power key, and set output power to 5 dB below the Reset level.

Step 7. Press the Graticule On/Off key to on.

Step 8. Connect a suitable 560 or 5400 Series detector between the Input A and RF Output connectors on the 541XXA front panel.

Step 9. Press the Channel 1 AutoScale key

Step 10. *For the 54107A through 54111A*, observe the Channel 1 trace and adjust R91 (Figure 6-5 or 6-6, Page 6-14) to obtain a flat trace.

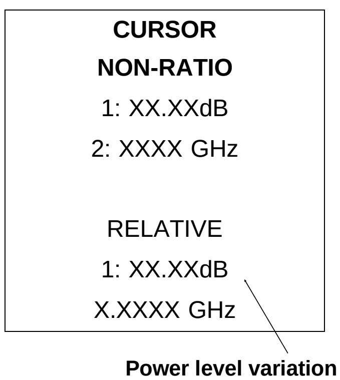
- Press the Auto Scale key to increase the display resolution, as necessary.
- If the requisite flatness, per the table below, can not be obtained, move jumper P4 the other end of header J4 and repeat the adjustment of R91.

Model	Output Impedance	Without Attenuator	With Attenuator
54107A	50 Ohms 75 Ohms	±0.3 dB ±0.5 dB	±1.0 dB ±1.2 dB
54109A	50 Ohms 75 Ohms	±0.4 dB ±0.6 dB	±1.1 dB ±1.3 dB
54111A	50 Ohms 75 Ohms	±0.6 dB ±0.8 dB	±1.3 dB ±1.5 dB

Step 11. *For 54117A, 54147A, 54161A, 54169A, 54177A equipped with an internal attenuator:*

- Go to the ALC Operating Point Adjustment.

Model	Power Level
54117A, 54147A	+10 dBm
54161A, 54169A	+4 dBm
54177A	+1 dBm



For 54117A, 54147A, 54161A, 54169A, 54177A without an attenuator:

- Press the Frequency key to display the START/STOP menu.
- Set **STOP** to the high-end frequency.
- Set the power output level to the reset power level shown in the table at top left.
- Press the Channel 1 Auto Scale key.
- Press the Cursor On/Off key to display the CURSOR menu (left).
- Using the Data Entry knob, move the main cursor to the point on the 541XXA trace having the lowest amplitude.
- Press the Relative cursor key.
- Using the Data Entry knob, move the relative cursor to the point on the 541XXA trace having the highest amplitude.
- Verify that relative cursor readout is within ±1.0 dB. Readjust R90 or R91, as necessary.
- Reduce the power output level by 10 dB.
- Press the Channel 1 Auto Scale key.
- Repeat the power output variation measurement; re-adjust R90 or R91, as necessary.
- Again set the power output level to the reset value, as shown in the table at top left.
- Repeat the adjustment of R90 and R91 (last five bulleted steps) as necessary until no further adjustment is required.

Model	Without Attenuator	With Attenuator
54107, 54109, 54111 50Ω output	+14 dBm	+12 dBm
54107, 54109, 54111 75Ω output	+12 dBm	+10 dBm
54117A	+12 dBm	+10 dBm
54147A	+12 dBm	+9 dBm
54161A, 54169A	–6 dBm	–9 dBm
54177A	–9 dBm	–12 dBm

Step 12. *For models 54107A, 54109A, and 54111A:*

- Set the power output level as shown in the table at left.
- Press the Channel 1 Auto Scale key .
- Adjust A6R112 (Figure 6-5, Page 6-14) fully clockwise.
- If oscillations are present on the trace, adjust A6R183 until the oscillations stop.
- Go to the ALC Operating Point Adjustment.

ALC Operating Point Adjustment

Step 1. Press Output Power and set the power level as shown in the table at top left.

Step 2. Set oscilloscope controls as follows:

- Horizontal Sweep: X-Y mode
- CH 1 vertical sensitivity: 1V/div
- CH 2 vertical sensitivity: 0.5V/div (with X10 probe)
- CH1 input: DC
- CH2 input: DC

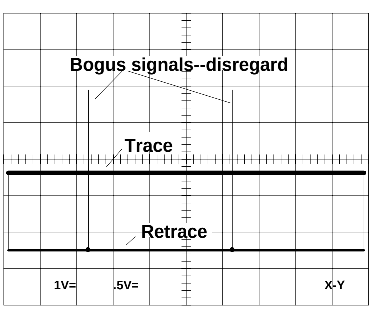
Step 3. Connect a BNC-to-BNC cable between the 541XXA rear panel HORIZONTAL OUTPUT connector and CH1 (X Input) on the oscilloscope.

- Adjust the position controls on the oscilloscope for a flat trace in the center of the screen.

Step 4. Set the oscilloscope's Channel 2 trace to center screen.

Step 5. Connect the oscilloscope's CH2 probe to A6TP28 (Figure 6-5, Page 6-14); connect the probe ground clip to the 541XXA chassis.

Step 6. Observe that the oscilloscope displays a waveform with a negative dc component (bottom left).



Waveform at TP28, 54117–54136A

Step 7. *For models 54107A, 54109A, and 54111A:*

- Adjust A6R183 until the waveform dc component value is –3.5V ±0.5V, as indicated by the oscilloscope trace.
- Note that this value is nominally 2.5V below the –1V “Upper Trip” value shown in Figure 6-21. This difference value is labeled “A” in Figure 6-21.

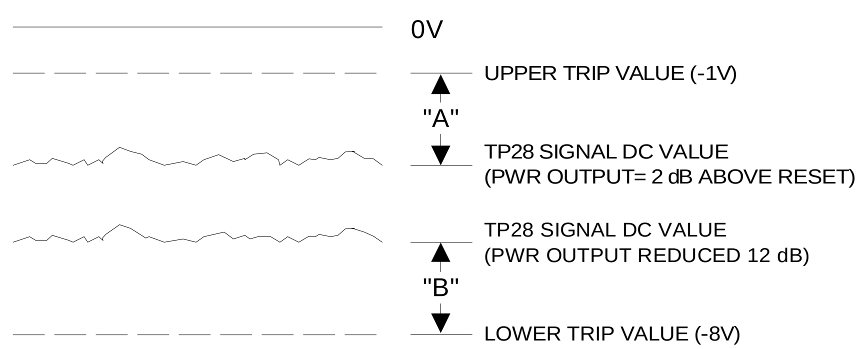


Figure 6-21. *RF Models ALC Operating Point Adjustment Point Diagram*

- Verify that there are no oscillations present on the trace.
- Reduce the power output level 12 dB and measure the waveform dc component.
- It should be –5.5V ±0.5V (that is, it is nominally 2.5V above the –8V “Lower Trip” value). If so, the adjustment is complete.
- If trip value is incorrect, note the difference between the measured dc component value and the lower trip value (labeled “B” in figure).
- Adjust A6R183 so that difference value “A” is within ±0.5V of difference value “B.”

Step 8. *For models 54117A, 54147A, 54161A, 54169A, 54177A :*

- Verify that there are no oscillations present on the oscilloscope trace and that the 541XXA Unleveled LED does not light.

- If either condition is present:
  For 54117A: adjust A6R133 (Figure 6-5, page 6-14) to move the oscilloscope trace slightly more negative until the oscillation and or unleveled conditions stops.

  For 54147A: adjust A19R31 (Figure 6-8, page 6-19) to move the oscilloscope trace slightly more negative until the oscillation and or unleveled conditions stops.

  For 54161A, 54169A, 54177A: adjust A23R31 (Figure 6-9, page 6-20) to move the trace more positive until the oscillation start.

- Reduce the power output level as follows:
  For 54117A, reduce by 11 dB.

  For 54147A, reduce by 12 dB.

  For 54161A, 54169A, 54177A, increase by 10 dB.

- Verify that no oscillation or unleveled condition is present. If either condition is present, readjust A6R133 (54117A), A19R31 (54147A), or A23R31 (54161A, 54169A, 54177A) to move the oscilloscope trace slightly more negative until the oscillation and or unleveled conditions stops..

Model	Without Attenuator	With Attenuator
54107, 54109, 54111 50Ω output	+14 dBm	+12 dBm
54107, 54109, 54111 75Ω output	+12 dBm	+10 dBm
54117A, 54147A	+12 dBm	+9 dBm
54161A, 54169A	–1 dBm	–4 dBm
54177A	+1 dBm	–2 dBm

Step 9. *For all models:*

- Remove the detector from the RF Output connector and verify that the Unleveled LED remains off.

- Again, set the power output level as shown in table at left. Verify that the Unleveled LED remains off.

6-13 TEMPERATURE COMPENSATION ADJUSTMENT

This procedure ensures that the ALC PCB circuits temperature compensation adjustments are properly set. *Perform this procedure only if the ALC PCB has been replaced, or if the Down Converter or Directional Coupler on the RF deck have been replaced.*

The Temperature Compensation Adjustments are organized by model groups, as shown below:

- ☐ 54117A/54147A/54161A/54169A/54177A Procedure (this page)
- ☐ 54107A/54109A/54111A Procedure (page 6-63)
- ☐ 54119A–54137A, 54154A, 54163A Procedure (page 6-69)

The procedure for each model group is complete and provides all of the steps necessary to perform the adjustments.

SYSTEM MENU

DISK UTILITIES
SYSTEM SETUP
DATA POINTS
RESET
CONFIGURE:
SOURCE
ANALYZER
PLOTTER
APPLICATIONS
GPIB MODE
USE ◆ THEN PRESS SELECT

RESET MENU

RESET IS CONFIGURED TO KEEP:
CAL DATA
MARKERS
LIMITS
RESET
RESET TO FACTORY DEFAULTS
USE ◆ THEN PRESS SELECT

Required Test Equipment

- ☐ Dummy Down Converter Thermistor — ANRITSU T38300, or equivalent (see Appendix C).
- ☐ Dummy Directional Coupler Thermistor — ANRITSU T38301, or equivalent (see Appendix C).
- ☐ Power Meter — with suitable matching power sensor (Table 1-2)
- ☐ ANRITSU RF Detector — to match 541XXA model (Table 1-2)

Preliminary

- ☐ Remove 541XXA top and side covers, then set back loosely in place. Refer to Chapter 7 for instructions.

NOTE

Throughout the below procedures, you will be directed to remove the covers, perform an action, and replace the covers several times. Do as directed. It is important that the covers remain in place so as to provide a consistent, normal temperature within the unit.

- ☐ Remove the ALC/Frequency Instruction PCB and place jumper J7 on pins 2 and 3 of P7; replace the PCB. (This PCB is shown in Figure 6-5 or 6-6, page 6-14).

54117A/54147A/54161A/54169A/54177A Procedure:

Step 1. Press the System Menu key and select **RESET** from the displayed menu (top left) using the Menu up/down and Select keys.

CHANNEL: 1
INPUT: A
TRANSMISSION
RETURN LOSS
SWR
POWER
DTF
VIEW CAL
SELECT INPUT
TRACE MEMORY
REF LINE
USE ◆ THEN
PRESS SELECT

CHANNEL: 1
SELECT INPUT
NON-RATIO
A
B
R
RATIO:
A/R
B/R
USE ◆ THEN
PRESS SELECT

Model	Without Attenuator	With Attenuator
54117A	+5 dBm	+4 dBm
54147A	+5 dBm	+2 dBm
54161A, 54169A	+1 dBm	–2 dBm
54177A	–4 dBm	–7 dBm

Step 2. From the RESET MENU (bottom left or previous page) select **RESET TO FACTORY DEFAULTS.**

Step 3. Press the Frequency and Select keys to display the CENTER/WIDTH menu.

Step 4. Set **CENTER** for 2.0 GHz and **WIDTH** for 0.1 GHz.

Step 5. Press Channel 2 Display On/Off key to off.

Step 6. Press the Menu up/down and Select keys, configure the 541XXA for a power measurement using Input A , as follows:

- Choose **SELECT INPUT**, from the CHANNEL menu middle left)
- Then choose **NON-RATIO A**, from the SELECT INPUT menu (bottom left).
- Select **POWER,** when you are returned to the CHANNEL menu.

Step 7. Press the Output Power key and set the power level to 5 dB below the reset power level, as shown in the table at bottom left.

Step 8. Press the Markers key.

Step 9. Set **M1** to 1.975 GHz (below).

MARKERS 1-4
M1: 01.950
1:
M2: 02.025
1:
M3: -OFF-
M4: -OFF-
MARKERS 5-8
PRESS SELECT
FOR ON/OFF

USE ◆ THEN
PRESS SELECT

MARKERS 1-4
M1: 01.950
1:
M2: 02.025
1:
M3: -OFF-
M4: -OFF-
MARKERS 5-8
PRESS SELECT
FOR ON/OFF

USE ◆ THEN
PRESS SELECT

Step 10. Set **M2** to 2.025 GHz.

Step 11. Press the Power On/Off key to off .

Step 12. Remove the top cover.

Step 13. Disconnect the Down Converter cable at connector J4 of the A4 Motherboard PCB.

Step 14. Connect one end of the Dummy Down Converter Thermistor, T38300, to the end of the cable, and connect the other end of T38300 to connector J4. (It is necessary to remove the A5 and A6 or A24 PCB's to perform this operation.)

Step 15. Set the T38300 jumper to the NORM position.

Step 16. Replace the top cover.

Step 17. Connect a suitable 560 or 5400 Series detector between the RF Output and Input A connectors.

Step 18. Press the Power On/Off key to on; allow the 541XXA to warm up for 30 minutes.

Step 19. Press the Markers key and note the **M1** and **M2** marker readings that appear on the displayed menu (left).

Step 20. Press the Power On/Off key to off.

Step 21. Remove the top cover.

Step 22. Remove the ALC PCB, and move jumper J7 to pins 1 and 2 of P7; replace the PCB.

Step 23. Replace the top cover.

Step 24. Press the Power On/Off key to on; allow the 541XXA to warm up for 10 minutes.

Step 25. Remove the top cover.

Step 26. Set the T38300 jumper to the CAL position.

Step 27. Adjust R81, on the ALC PCB (Figure 6-5 or 6-6, page 6-14), so that the RF band marker (M1) is per table at left.

Temperature Calibration Offset, Het Band

Model	Volts
54117A, 54147A	0.75
54161A, 54169A	0.90
54177A	1.25

Step 28. Remove the left side-cover (your right, as you face the unit.)

Step 29. Disconnect the black wire from the thermistor output of the Directional Coupler on the RF deck (see Chapter 7, Figure 7-12 (54117A), 7-17 (54147A), 7-18 (54161A, 54169A, or 7-19 (54177A) for location).

Step 30. Connect the Dummy Directional Coupler Thermistor, T38301, between the black wire and the 54XXA chassis (ground).

Temperature Calibration Offset, Microwave Band

Model	Volts
54117A, 54147A	0.35
54161A, 54169A	0.15
54177A	1.35

Step 31. Adjust R104, on ALC/Frequency Instruction PCB (Figure 6-5 or 6-6, page 6-14) so that marker M2 is per the table at left.

Step 32. Press the Power On/Off key to off.

Step 33. Remove the T38300 and T38301 fixtures.

Step 34. Reconnect the black wire to the thermistor output terminal of the directional coupler and the down converter cable to connector A4J4.

FREQUENCY MENU
CENTER
02.000 GHz
WIDTH
00.000 GHz
PRESS SELECT FOR START/STOP

Step 35. Replace the top and right-side covers.

Step 36. Press the Power On/Off key to on; allow the 541XXA to warm up for 10 minutes.

Step 37. Press the Frequency and Select keys to display the CENTER/WIDTH menu .

Step 38. Set **WIDTH** for 0.0 GHz.

Step 39. Set power as per table bottom left.

Step 40. Press Channel 1 Display On/Off key to off to place the 541XXA in a CW mode.

Step 41. Connect the power meter to the RF Output connector, as shown in Figure 6-22 (page 6-64).

Model	Without Attenuator	With Attenuator
54117A	+12 dBm	+10 dBm
54147A	+12 dBm	+9 dBm
54161A, 54169A	+4 dBm	+1 dBm
54177A	+1 dBm	–2 dBm

Step 42. Verify that the power meter reading is within the specifications listed in Table 6-2 (page 6-64).

Step 43. If necessary, adjust the RF output power level using A6or A24R62.

Step 44. Press the Output Power key, and reduce the power output level by 10 dB.

FREQUENCY MENU
START
00.010 GHz
STOP
XX.XXX GHz
PRESS SELECT FOR CENTER/WIDTH

Model	Without Attenuator	With Attenuator
54117A	+12 dBm	+10 dBm
54147A	+12 dBm	+9 dBm
54161A, 54169A	+4 dBm	+1 dBm
54177A	+1 dBm	–2 dBm

Model	Without Attenuator	With Attenuator
54117A	+0 dBm	–1 dBm
54147A	+0 dBm	–3 dBm
54161A, 54169A	–6 dBm	–9 dBm
54177A	–9 dBm	–12 dBm

Step 45. Verify that the power meter reading is within the specifications listed in Table 6-2 for minimum ALC level.

Step 46. If necessary, adjust the RF output power level using A6 or A24R196.

Step 47. Increase the output power by 10 dB, and repeat Steps 39 through 45 as necessary so that the power level values are correct for Steps 41 and 44.

Step 48. Press the Frequency key to display the START/STOP menu.

Step 49. Press the Frequency key.

Step 50. Set **START** to be 10 MHz and **STOP** to be the model's high-end frequency.

Step 51. Press the Output Power key, and set the power level as shown in the table at middle left.

Step 52. Connect a suitable 560 or 5400 Series RF detector between the RF Output and Input A connectors.

Step 53. Press the Auto Scale key and confirm that the Unleveled LED in not lit.

Step 54. Press the Output Power key, and set the power level as shown in the table at bottom left.

Step 55. Press the Auto Scale key and confirm that the Unleveled LED is not lit.

This completes the temperature compensation adjustments for the 54117A, 54147A, 54161A, 54169A, and 54177A.

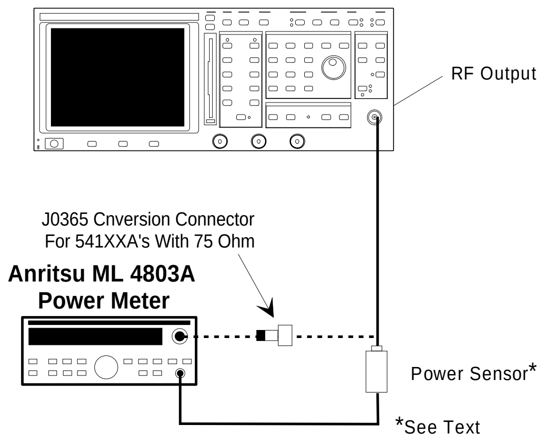


Figure 6-22. *Equipment Setup for ALC Pre-Adjustment Procedure*

Table 6-2. *Output Power Level Specifications*

Model	Without Attenuator	Specification (dB)	With Attenuator	Specification (dB)
54107A, 54109A *50Ω Output*	+12 dBm to +2 dBm	±1.0	+10 dBm to –1 dBm	±2.0
54111A *50Ω Output*	+12 dBm to +2 dBm	±1.0	+10 dBm to –1 dBm	±2.5
54107A, 54109A *75Ω Output*	+10 dBm to +0 dBm	±1.2	+10 dBm to –1 dBm	±2.4
54111A *75Ω Output*	+10 dBm to +0 dBm	±1.0	+10 dBm to –1 dBm	±2.9
54117A	+10 dBm to +0 dBm	±1.2	+10 dBm to –1 dBm	±2.5
54119A, 54128A, 54130A, 54131A	+10 dBm to +0 dBm	±1.0	+7 dBm to –3 dBm	±2.5
54136A	+7 dBm to –3 dBm	±1.0	+4 dBm to –6 dBm	±4.0
54137A, 54147A	+10 dBm to +0 dBm	±1.0	+7 dBm to –3 dBm	±2.9
54154A, 54161A, 54163A, 54169A	+6 dBm to –4 dBm	±1.0	+3 dBm to –7 dBm	±4.0
54177A	+1 dBm to –9 dBm	±1.0	–2 dBm to –12 dBm	±5.0

SYSTEM MENU
DISK UTILITIES
SYSTEM SETUP
DATA POINTS
RESET
CONFIGURE:
SOURCE
ANALYZER
PLOTTER
APPLICATIONS
GPIB MODE
USE ◆ THEN PRESS SELECT

RESET MENU
RESET IS CONFIGURED TO KEEP:
CAL DATA
MARKERS
LIMITS
RESET
RESET TO FACTORY DEFAULTS
USE ◆ THEN PRESS SELECT

FREQUENCY MENU
CENTER
02.000 GHz
WIDTH
00.000 GHz
PRESS SELECT FOR START/STOP

54107A/54109A/54111A Procedure:

Step 1. Press the System Menu key and select **RESET** from the displayed menu (top left) using the Menu up/down and Select keys.

Step 2. From the RESET MENU (bottom left) select **RESET TO FACTORY DEFAULTS.**

Step 3. Press the Frequency and Select keys to display the CENTER/WIDTH menu .

Step 4. Set **WIDTH** for 0.0 GHz, and set **CENTER** for the applicable frequency shown below.

Step 5. Press the Menu up/down and Select keys, configure the 541XXA for a power measurement using Input A , as follows:

Model	Frequency
54107A	750 MHz
54109A	1100 MHz
54111A	1500 MHz

- Choose **SELECT INPUT**, from the CHANNEL menu (below).
- Then choose **NON-RATIO A**, from the SELECT INPUT menu (below).

CHANNEL: 1 INPUT: A
TRANSMISSION
RETURN LOSS
SWR
POWER
DTF
VIEW CAL
SELECT INPUT
TRACE MEMORY
REF LINE
USE ◆ THEN PRESS SELECT

CHANNEL: 1 SELECT INPUT
NON-RATIO
A
B
R
RATIO:
A/R
B/R
USE ◆ THEN PRESS SELECT

Model	Without Attenuator	With Attenuator
54107A, 54109A, 54111A; 50Ω output	+7 dBm	+5 dBm
54107A, 54109A, 54111A; 75Ω output	+5 dBm	+3 dBm

■ Select **POWER,** when you are returned to the CHANNEL menu.

Step 6. Press the Output Power key.

Step 7. Set the power level as shown in the table at left.

Step 8. Connect a suitable 560 or 5400 Series RF detector between the 541XXA Input A and RF Output connectors.

Step 9. Press the Channel 1 Auto Scale key.

Step 10. Press the Output Power key to off.

Step 11. Remove the top cover and left side covers (your right, as you face the unit).

Step 12. Disconnect the Down Converter cable at connector J4 of the A4 Motherboard PCB.

Step 13. Connect one end of the Dummy Down Converter Thermistor, T38300, to the end of the cable.

Step 14. Set the T38300 jumper to the NORM position.

Step 15. Connect the other end of T38300 to connector J4. (It is necessary to remove the A5 and A6 PCB's to perform this operation.)

Step 16. Replace the covers.

Step 17. Press the Power On/Off key to on; allow the 541XXA to warm up for 30 minutes.

CURSOR
1: XX.XX dB

XX.XXXX GHz
RELATIVE (Δ)
1: XX.XX dB

XX.XXXX GHz

Step 18. Press the Cursor key and note cursor reading from the displayed menu (left).

Step 19. Press the Power On/Off key to off.

Step 20. Remove the top cover.

Step 21. Remove the A6 PCB, and move jumper J7 to pins 1 and 2 of P7; replace the PCB.

Step 22. Set the T38300 jumper to the CAL position.

Step 23. Replace the top cover.

Step 24. Press the Power On/Off key to on and allow it to warm up for 10 minutes.

Step 25. Remove the top cover.

Step 26. Adjust A6R81 so that the cursor reading is 0.55 ±0.05 dB less than the value noted in Step 18.

Step 27. Press the Power On/Off key to off.

Step 28. Remove the T38300 fixtures.

Step 29. Replace the top cover.

Step 30. Press the Power On/Off key to on.

Step 31. Press the Frequency and Select keys to display the CENTER/WIDTH menu .

Step 32. Set **WIDTH** for 0.0 GHz, and set **CENTER** to a value that is 0.75 times the high-end frequency (Example: 2250 MHz for 54111A—0.75X3000=2250).

Step 33. Verify that the power meter reading is within specification per Table 6-2 (page 6-62).

Step 34. If necessary, adjust the reset RF output power level (A6R56), or the minimum ALC power level (A6R190).

Step 35. Press the Frequency and Select keys to display the START/STOP menu .

Step 36. Set **START** for 1 MHz, and set **STOP** for the high-end frequency.

Step 37. Press the Output Power key, and set the power level 2 dB above the Reset value, as shown in the table at left.

Model	Without Attenuator	With Attenuator
54107A, 54109A, 54111A; 50Ω output	+14 dBm	+12 dBm
54107A, 54109A, 54111A; 75Ω output	+12 dBm	+10 dBm

Step 38. Connect a suitable 560 Series RF detector between the RF Output and Input A connectors.

Step 39. Press the Auto Scale key and confirm that the Unleveled LED in not lit.

This completes the temperature compensation adjustments for the 54107A, 54109A, and 54111A.

SYSTEM MENU
DISK UTILITIES
SYSTEM SETUP
DATA POINTS
RESET
CONFIGURE:
SOURCE
ANALYZER
PLOTTER
APPLICATIONS
GPIB MODE
USE ◆ THEN PRESS SELECT

RESET MENU
RESET IS CONFIGURED TO KEEP:
CAL DATA
MARKERS
LIMITS
RESET
RESET TO FACTORY DEFAULTS
USE ◆ THEN PRESS SELECT

FREQUENCY MENU
CENTER
02.000 GHz
WIDTH
00.000 GHz
PRESS SELECT FOR START/STOP

54119A through 54137A and 54154A, 54163A Procedure:

Step 1. Press the System Menu key and select **RESET** from the displayed menu (top left) using the Menu up/down and Select keys.

Step 2. From the RESET MENU (bottom left) select **RESET TO FACTORY DEFAULTS.**

Step 3. Press the Frequency and Select keys to display the CENTER/WIDTH menu .

Step 4. Set **WIDTH** for 0.0 GHz, and set **CENTER** for the applicable frequency shown below.

Model	Frequency (GHz)	Model	Frequency (GHz)
54119A	5.2	54136A	21.8
54128A	10.2	54137A	10.0
54130A	16.2	54154A	16
54131A	13.0	54163A	20

Step 5. Press the Menu up/down and Select keys, configure the 541XXA for a power measurement using Input A , as follows:

- Choose **SELECT INPUT**, from the CHANNEL menu (below).
- Then choose **NON-RATIO A**, from the SELECT INPUT menu (below).

CHANNEL: 1 INPUT: A
TRANSMISSION
RETURN LOSS
SWR
POWER
DTF
VIEW CAL
SELECT INPUT
TRACE MEMORY
REF LINE
USE ◆ THEN PRESS SELECT

CHANNEL: 1 SELECT INPUT
NON-RATIO
A
B
R
RATIO:
A/R
B/R
USE ◆ THEN PRESS SELECT

Model	Without Attenuator	With Attenuator
54119A, 54128A, 54130A, 54131A, 54136A 54137A	+5 dBm	+2 dBm
54154A, 54163A	–1 dBm	–4 dBm

CURSOR
1: XX.XX dB

XX.XXXX GHz
RELATIVE (Δ)
1: XX.XX dB

XX.XXXX GHz

FREQUENCY MENU
CENTER
0.000 GHz
WIDTH
XX.XXXGHz
PRESS SELECT FOR START/STOP

- Select **POWER,** when you are returned to the CHANNEL menu.

Step 6. Press the Output Power key.

Step 7. Set the power level as shown in the table at top left.

Step 8. Connect a suitable 560 or 5400 Series RF detector between the 541XXA Input A and RF Output connectors.

Step 9. Press the Channel 1 Auto Scale key.

Step 10. Allow the 541XXA to warm up for 30 minutes.

Step 11. Press the Cursor key and note cursor reading from the displayed menu (middle left).

Step 12. Press the Power On/Off key to off.

Step 13. Remove the top and left side covers (your right as you face the unit).

Step 14. Remove the ALC/Frequency Instruction PCB (A6 or A24, based on model), and move jumper J7 to Pin 1 and 2 of P7. Replace the PCB.

Step 15. Disconnect the black wire from the thermistor output of the Directional Coupler on the RF deck.

Step 16. Connect the Dummy Directional Coupler Thermistor, T38301, between the black wire and the 54XXA chassis (ground).

Step 17. Replace the covers.

Step 18. Press the Power On/Off key to on; allow the 541XXA to warm up for 10 minutes.

Step 19. Adjust R104 (Figure 6-5 or 6-6, page 6-14) so that the cursor reading is 0.35, ±0.05 dB less than the value noted in Step 11 for 54119A, 54128A, 54130A, 54131A, and 54136A. It should be 0.15 dB less for 54154A and 54163A.

Step 20. Press Power On/Off key to off.

Step 21. Remove the T38301 fixture, and reconnect the black wire to the thermistor output.

Step 22. Press the Frequency and Select keys to display the CENTER/WIDTH menu .

FREQUENCY MENU

START
XX.XXX GHz

STOP
XX.XXX GHz

PRESS SELECT FOR CENTER/WIDTH

Model	Without Attenuator	With Attenuator
54119A, 54128A, 54130A, 54131A, 54136A 54137A	0 dBm	–3 dBm
54154A, 54163A	–6 dBm	–9 dBm

Model	Without Attenuator	With Attenuator
54119A, 54128A, 54130A, 54131A, 54136A 54137A	12 dBm	9 dBm
54154A, 54163A	+4 dBm	+1 dBm

Step 23. Set **WIDTH** for 0.0 GHz, and set **CENTER** for the model's low-end frequency.

Step 24. Press Channel 1 Display On/Off key to off to place the 541XXA in a CW mode.

Step 25. Connect the power meter to the RF Output connector, as shown in Figure 6-22 (page 6-62). Press the output power key and set the power to 10dB above the value listed in the table at middle left.

Step 26. Verify that the power meter reading is within the specifications listed in Table 6-2 (page 6-62).

Step 27. If necessary, adjust the RF output power level using R62 on the ALC/Frequency Instruction PCB.

Step 28. Press the Output Power key, and reduce the power output level by 10 dB, as shown in the table at middle left.

Step 29. Verify that the power meter reading is within the specifications listed in Table 6-2 for minimum ALC level.

Step 30. If necessary, adjust the RF output power level using R196, on the ALC/Frequency Instruction PCB.

Step 31. Increase the output power by 10 dB, and repeat Steps 26 through 30 as necessary to obtain correct power level values in steps 26 and 29.

Step 32. Press the Frequency and Select keys to display the START/STOP menu .

Step 33. Set **START** for the model's low-end frequency, and set **STOP** for the high-end frequency.

Step 34. Press the Output Power key, and set the power level as shown in the table at middle left.

Step 35. Connect a suitable RF detector between the RF Output and Input A connectors.

Step 36. Press the Channel 1 Auto Scale key and confirm that the Unleveled LED in not lit.

Step 37. Reduce the RF power by 12 dB for 54119A through 54137A and 10 dB for 54154A and 54163A.

Step 38. Press Channel 1Auto Scale key and confirm that the Unleveled LED is not lit.

6-14 BAND SWITCH-POINT ADJUSTMENT

This procedure ensures that the power difference at the 2.0 GHz band switch point of models 54117A, 54147A, 54161A, 54169A, and 54177A is reduced to a minimum.

Required Test Equipment

☐ Oscilloscope, dual channel with two X10 probes

SYSTEM MENU
DISK UTILITIES
SYSTEM SETUP
DATA POINTS
RESET
CONFIGURE:
SOURCE
ANALYZER
PLOTTER
APPLICATIONS
GPIB MODE
USE ◆ THEN PRESS SELECT

Preliminary

☐ Remove the 541XXA top cover. (Refer to Chapter 7, paragraph 7-2 for instructions.)

Procedure

Step 1. Press the System Menu key and select **RESET** from the displayed menu (top left) using the Menu up/down and Select keys.

Step 2. From the RESET MENU (bottom left) select **RESET TO FACTORY DEFAULTS.**

Step 3. Press the Frequency key to display the START/STOP menu

RESET MENU
RESET IS CONFIGURED TO KEEP:
CAL DATA
MARKERS
LIMITS
RESET
RESET TO FACTORY DEFAULTS
USE ◆ THEN PRESS SELECT

FREQUENCY MENU
START XX.XXX GHz
STOP
XX.XXX GHz
PRESS SELECT FOR CENTER/WIDTH

Step 4. Set **START** for 1.950 GHz and **STOP** for 2.050 GHz.

Step 5. Press Channel 2 Display On/Off key to off.

CHANNEL: 1
INPUT: A
TRANSMISSION
RETURN LOSS
SWR
POWER
DTF
VIEW CAL
SELECT INPUT
TRACE MEMORY
REF LINE
USE ◆ THEN PRESS SELECT

CHANNEL: 1
SELECT INPUT
NON-RATIO
A
B
R
RATIO:
A/R
B/R
USE ◆ THEN PRESS SELECT

Step 6. Press the Menu up/down and Select keys, configure the 541XXA for a power measurement using Input A , as follows:

- Choose **SELECT INPUT**, from the CHANNEL menu (top left)
- Then choose **NON-RATIO A**, from the SELECT INPUT menu (middle left).
- Select **POWER,** when you are returned to the CHANNEL menu.

Step 7. Press the Graticule On/Off key to on.

Step 8. Connect a suitable 560 or 5400 Series detector between the Input A and RF Output connectors on the 541XXA front panel.

Step 9. Press the Output Power key, and reduce the output power 2 dB below the Reset value.

Step 10. Press the Channel 1 AutoScale key

NOTE

In the following steps, the adjustments R56 and R190 are on the ALC/Frequency Instruction PCB. This PCB is A6 for 54117A and 54147A; it is A24 for 54161A, 54169A, and 54177A. Both are shown on page 6-14.

Step 11. Adjust R56 until there is no visible step at the 2.0 GHz switch point.

Step 12. Reduce the power output level by 7 dB.

Step 13. Press the Channel 1 Auto Scale key.

Step 14. Adjust R190 until there is no visible step at the 2.0 GHz switch point.

Step 15. Press the power key, and increase the output power level by 7 dB.

Step 16. Repeat steps 11 through 14 until no further adjustment is required.

Step 17. Set the power output level to 2 dB below the reset value. Verify that the RF power difference between the heterodyne band (<2.0 GHz) and the microwave band (>2.0 GHz) does not exceed 1 dB.

Step 18. Repeat Step 18 at 4 dB, 6 dB, and 8 dB below the reset power level.

6-15 CRT MONITOR ADJUSTMENTS

These procedures are used to adjust the CRT monitor brightness, contrast, and horizontal size. Perform this procedure whenever a new CRT monitor assembly or Graphics Processor PCB has been installed (see Chapter 7). All other CRT monitor adjustments should be performed by qualified service personnel only.

WARNING

Hazardous voltages are present inside the instrument when ac line power is connected. These procedures should only be performed by service personnel who are fully aware of the potential hazards associated with high voltage.

Required Equipment

- ☐ Adjustment of the CRT horizontal size requires the use of a plastic or nylon hex alignment tool. Do not use metal tools to adjust CRT monitor settings.

Preliminary

- ☐ Remove the 541XXA top and left side covers, then set them back loosely in place. Refer to Chapter 7 for instructions.

NOTE

For this procedure, it is important that a consistent temperature be maintained within the unit. These adjustments must be made with the instrument at normal operating temperature.

Brightness and Contrast Adjustment

Step 1. Refer to the locator drawing on the CRT Monitor assembly top cover and locate the brightness and contrast trim pots, accessible through the side opening (Figure 6-23).

Step 2. Reset the instrument.

Step 3. Using the front panel INTENSITY control, set the display to intensity level 9 (refer to Chapter 3 of the *541XXA Operation Manual*).

Step 4. Carefully adjust the brightness and contrast trim pots until the display just starts to “bloom” or distort.

Step 5. Set the display intensity to level 1.

Step 6. Adjust, if required, the brightness and contrast to achieve a level that is just visible.

Step 7. Repeat steps 2 through 6 until the desired intensity levels at 1 and 9 are achieved.

Step 8. Replace the 541XXA top and left side covers.

Step 9. Verify that the adjustment remains as desired throughout the operating temperature range of the instrument.

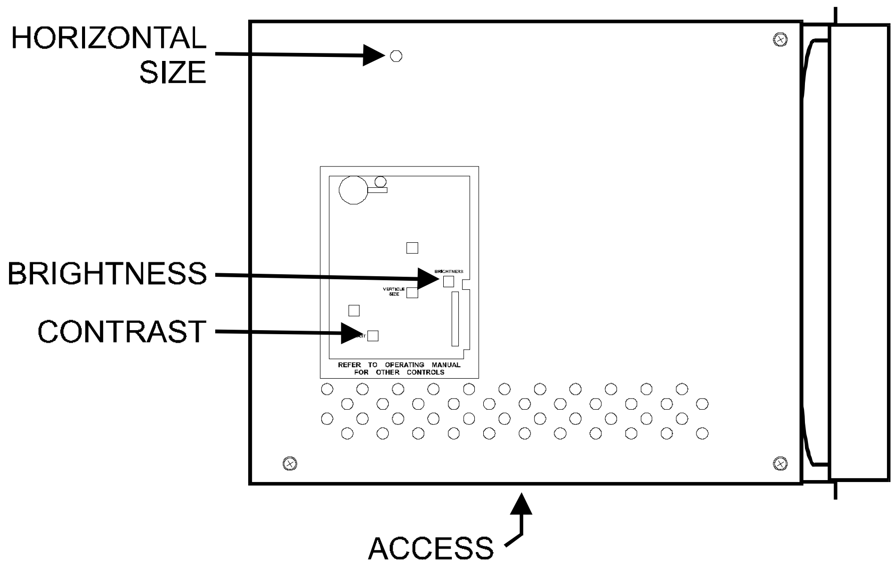


Figure 6-23. *CRT Monitor Adjustments*

Horizontal Size Adjustment

Step 1. Remove the 541XXA top cover.

Step 2. Insert a plastic or nylon hex alignment tool through the access hole (see Figure 6-23) and carefully adjust the horizontal size coil until the display is centered on the CRT.

Step 3. Replace the 541XXA top and side covers.

Step 4. Verify that the adjustment remains as desired throughout the operating temperature range of the instrument.

Chapter 7
Removal and
Replacement Procedures

Table of Contents

Chapter 7
Removal and Replacement Procedures

7-1 INTRODUCTION

The disassembly procedures presented in this chapter describe how to gain access to the major 541XXA assemblies and parts for troubleshooting or replacement.

WARNING

Hazardous voltages are present inside the instrument when ac line power is connected. Turn off the instrument and remove the line cord before removing any covers or panels. Trouble shooting or repair procedures should only be performed by service personnel who are fully aware of the potential hazards.

CAUTION

Many assemblies in the 541XXA contain static-sensitive components. Improper handling of these assemblies may result in damage to the assemblies. ***Always*** observe the static-sensitive component handling precautions described in Chapter 1, Figure 1-2.

7-2 REMOVE AND REPLACE 541XXA COVERS

Adjustment and troubleshooting operations require removal of the top cover. Replacement of some 541XXA assemblies and parts require removal of all covers. The following procedures describe this process. The replacement process is the reverse of the removal process.

Preliminary

☐ Disconnect the power cord from the unit.

Procedure

Step 1. To remove the top cover:

- Place the 541XXA on its bottom (top-side up).
- Remove the feet from the two top corners at the rear of the 541XXA (Figure 7-1).
- Remove the center screw from rear of the top cover.
- Lift and slide the top cover away from the 541XXA.

Step 2. To remove the bottom cover:

- Place the 541XXA on its top (bottom-side up).
- Remove the feet from the two bottom corners at the rear of the 541XXA.
- Remove the center screw from rear of the bottom cover.
- Lift and slide the top cover away from the 541XXA.

Step 3. To remove the left cover:

- Place the 541XXA on its right side (left-side up).
- Remove the feet from the two left-side corners at the rear of the 541XXA.
- Remove the center screw from rear of the left side cover.
- Lift and slide the side cover away from the 541XXA.

Step 4. To remove the right cover:

- Place the 541XXA its left side (right-side up).
- Remove the feet from the two right-side corners at the rear of the 541XXA.

- Remove the center screw from rear of the right side cover.
- Peel back the rubber sheathing at either end of the handle assembly, and remove the screws from underneath. Pull the handle straight away, and set it aside.
- Lift and slide the side cover away from the 541XXA.

CAUTION

The green headed screws have Metric threads.

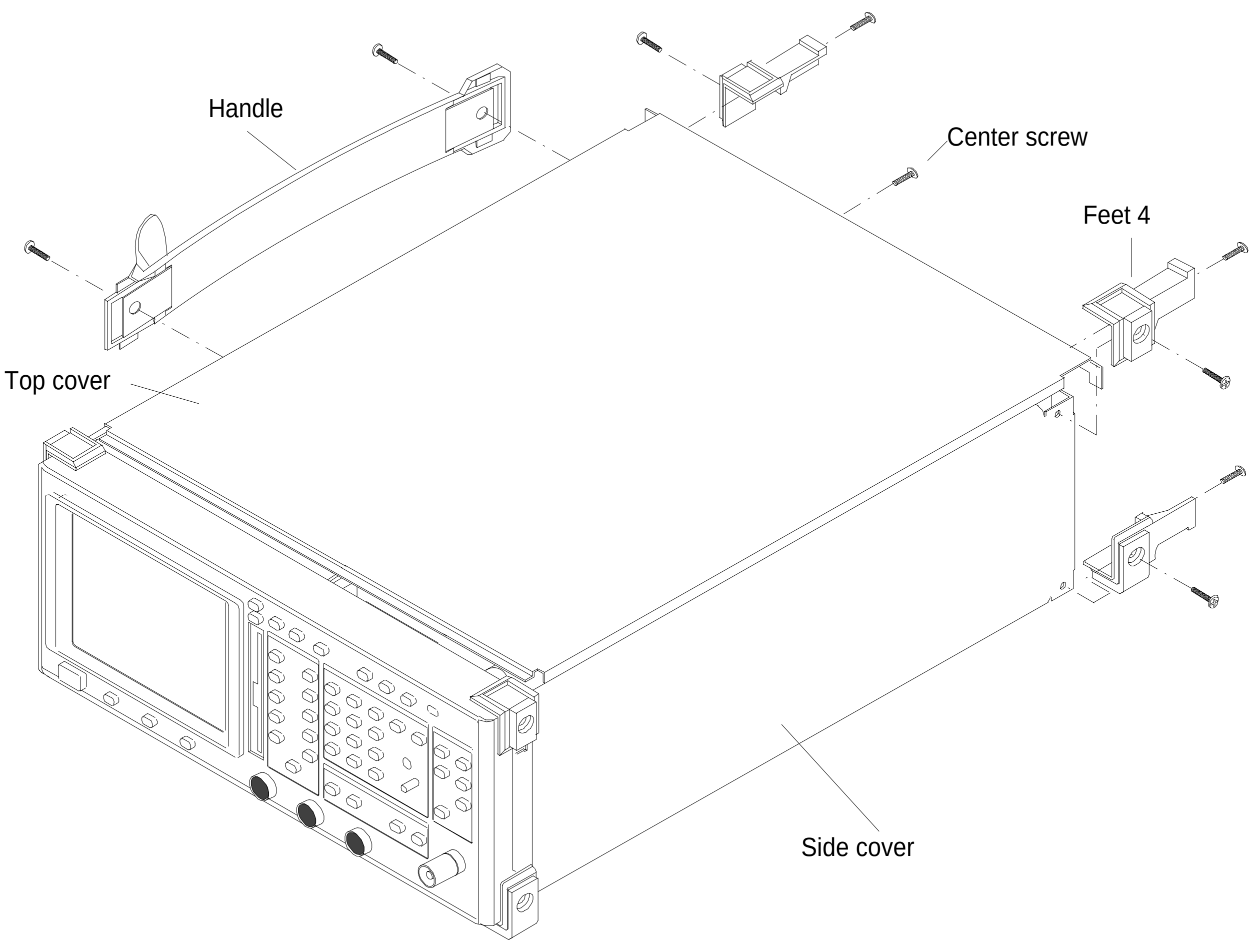


Figure 7-1. *Exploded View of Chassis Covers*

7-3 REMOVE AND REPLACE THE A5, A6, A7 AND A8 PCBs

This paragraph provides instructions for removing and replacing the A5, A6, A7 and A8 PCB's, which are located underneath the cover of the card cage. The replacement process is the reverse of the removal process.

Preliminary

☐ Remove the top cover (paragraph 7-2).

Procedure

Step 1. Place the 541XXA on its bottom (top-side up).

Step 2. Loosen the four captive screws on the card-cage cover (Figure 7-2).

Step 3. Remove card-cage cover and set aside.

Step 4. Lift up on the edge tabs of the selected PCB(s) and lift straight way. (Note that locations of A5, A6, A7 and A8 PCB's are shown on top of card cage cover.)

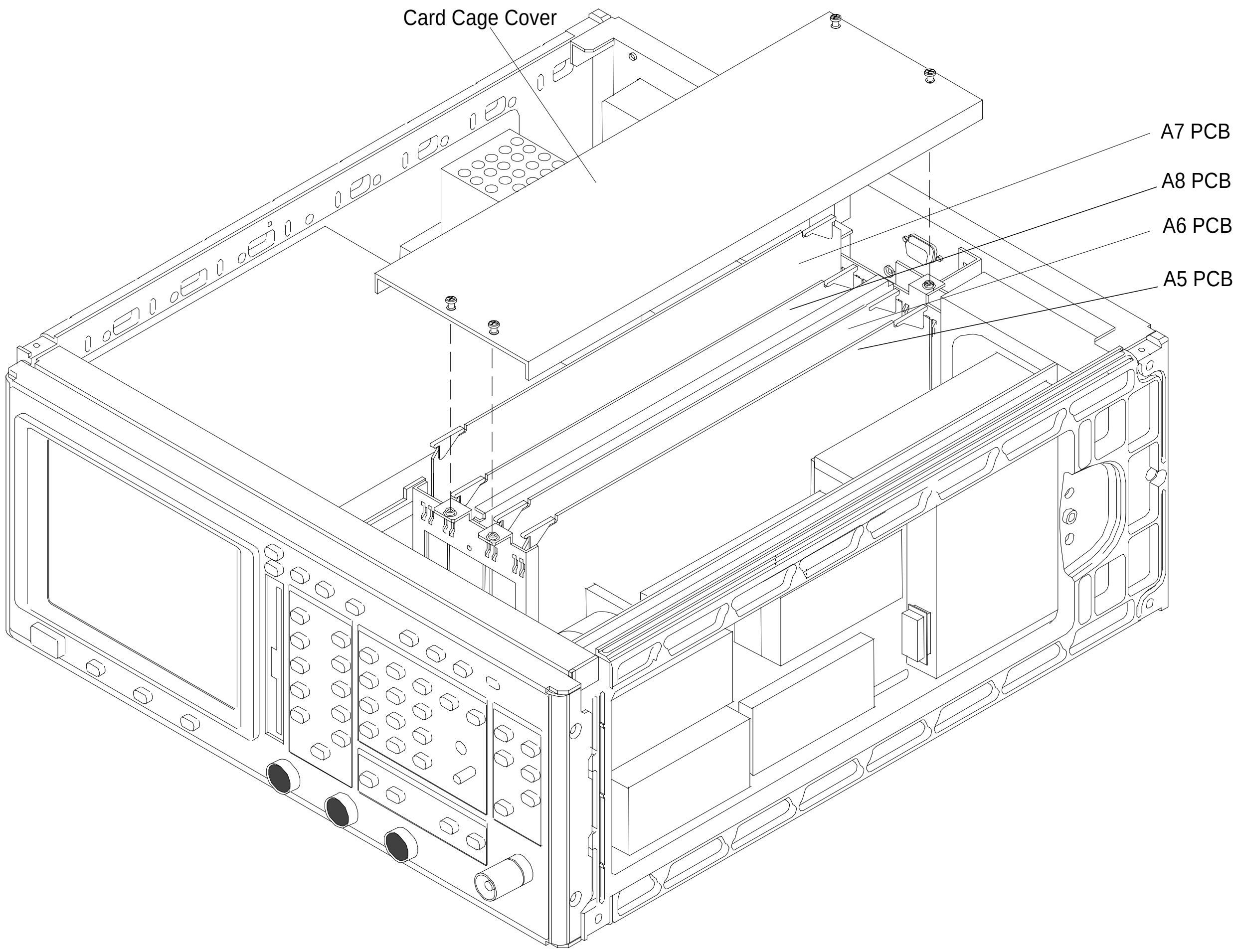


Figure 7-2. *Exploded View of A5, A6, A7 and A8 PCBs*

7-4 REMOVE AND REPLACE THE FRONT PANEL ASSEMBLY

This paragraph provides instructions for removing and replacing the front panel assembly of the 541XXA. The replacement process is the reverse of the removal process.

Preliminary:

☐ Remove the top, bottom, and side covers (paragraph 7-2).

Procedure:

Step 1. Orient the 541XXA as appropriate to remove the four corner brackets and tilt bail from the front of the 541XXA (Figure 7-3).

Step 2. Slide the surrounding bezel straight away from the front panel, and set it aside.

Step 3. Place the 541XXA on its bottom (top-side up).

Step 4. Using the blade of a small screwdriver as a pry, loosen the holding collar and disconnect the ribbon cable from the rear of the floppy disk drive (Detail A).

NOTE

Removing the A7 PCB will make it easier to loosen the connector collar.

Step 5. Remove the screw that secures the card cage to the disk drive.

Step 6. Disconnect the ribbon cable from the A2 PCB connector by pulling it straight away.

Step 7. Place the 541XXA on its right side (left-side up).

Step 8. Remove the two nuts shown in Figure 7-3, Detail B, from the backside of the front panel, using a 1/4 inch nut driver.

Step 9. Place the 541XXA on its top (bottom-side up).

Step 10. Remove four screws from the bottom of the front panel.

CAUTION

Use care to avoid damaging the Power On/Off switch and cable, which is now hanging free.

Step 11. Place the 541XXA on its bottom (top-side up).

Step 12. Remove the four side screws.

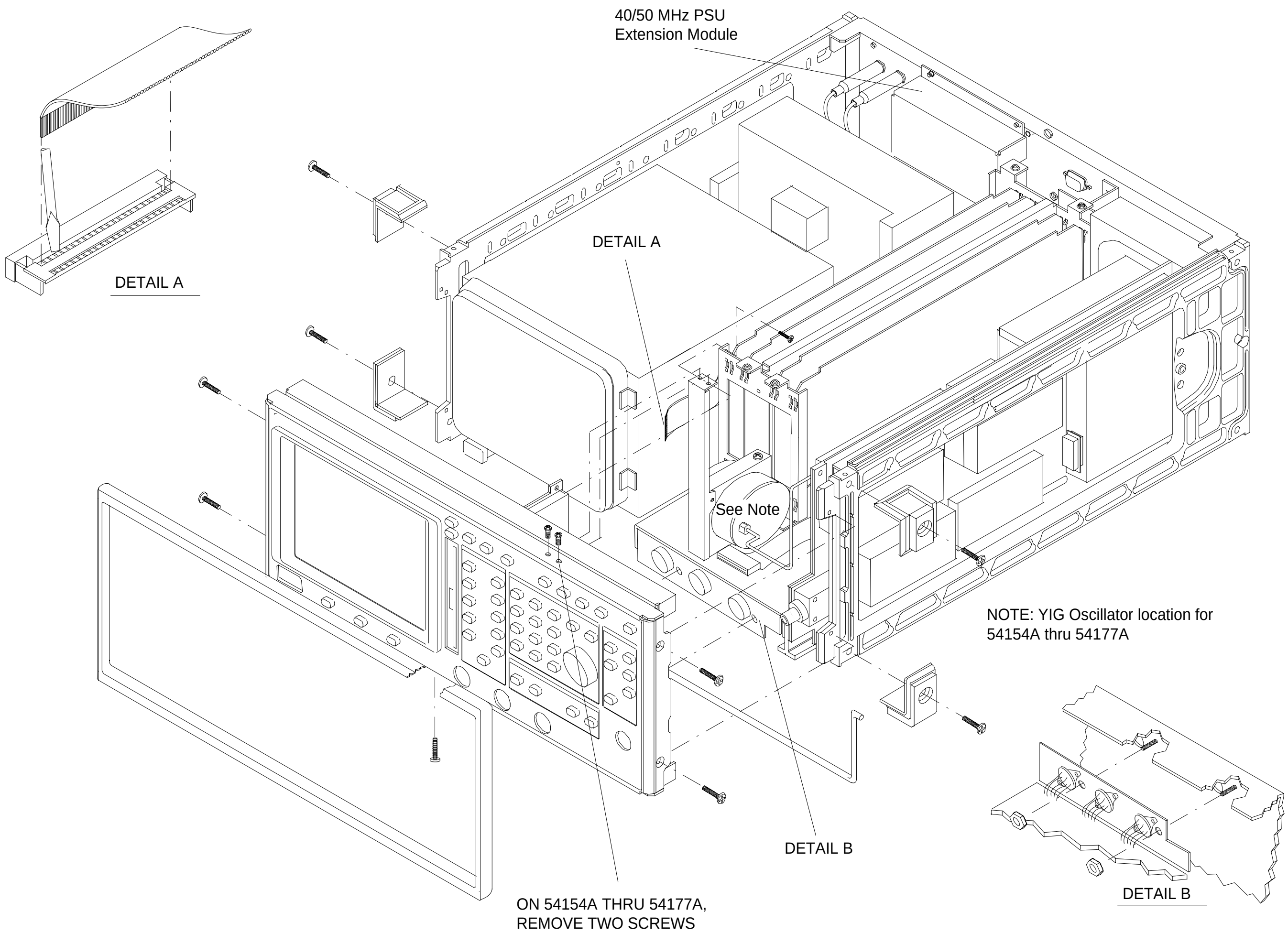


Figure 7-3. *Exploded View of Front Panel Assembly*

Step 13. Gently pull front panel assembly forward until it is clear of the RF output connector, and lay it flat on the work surface.

7-5 REMOVE AND REPLACE THE A1/A2 PCB's

This paragraph provides instructions for removing and replacing the A1 Front Panel PCB and A2 Front Panel Interface PCB. The replacement process is the reverse of the removal process.

Preliminary:

☐ Remove the top, bottom, and side covers (paragraph 7-2)

☐ Remove the front panel assembly (paragraph 7-4).

Procedure:

Step 1. With the front panel assembly laying face up on the work surface (Figure 7-4), disconnect the cables at connectors A2J2 and A2J3 .

Step 2. Remove eight screws.

Step 3. Remove the A1/A2 PCB assembly by lifting it straight away.

Step 4. Separate the A1 and A2 PCBs by carefully working them apart. They are held together by the mating of connectors A1P1 and A2XA1.

7-6 REMOVE AND REPLACE THE FRONT PANEL KEY SWITCH MEMBRANE

This paragraph provides instructions for removing and replacing the front panel keys switch membrane. The replacement process is the reverse of the removal process.

Preliminary:

☐ Remove the top, bottom, and side covers (paragraph 7-2)

☐ Remove the front panel assembly (paragraph 7-4).

☐ Remove the A1/A2 PCB assembly (paragraph 7-5).

Procedure

Step 1. With the key-switch membrane exposed, carefully peel it away from the inside of the front panel backplate (Figure 7-4, Detail A).

CAUTION

Avoid touching the black switch contacts in the membrane. They can be damaged or destroyed by the oils in human skin.

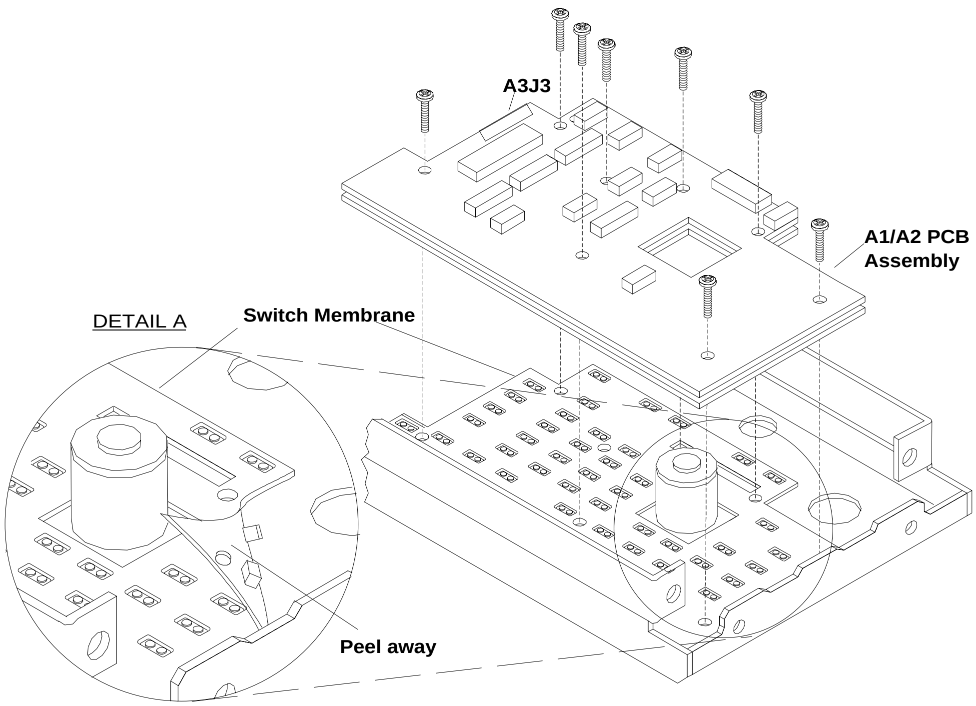


Figure 7-4. *Exploded View of A2, A1, and A10 PCBs*

7-7 REMOVE AND REPLACE THE A10 PCB

This paragraph provides instructions for removing and replacing the A10 Menu PCB. The replacement process is the reverse of the removal process.

Preliminary:

☐ Remove the top, bottom, and side covers (paragraph 7-2).

☐ Remove the front panel assembly of the unit (paragraph 7-4).

Procedure

Step 1. With the front panel assembly laying face up on the work surface, disconnect the cable at connectors A2J3 (Figure 7-4).

Step 2. Open the soft-metal cable clamps, and free the cable assembly.

Step 3. Remove two screws, and lift the A10 PCB and attaching cable assembly straight away.

7-8 REMOVE AND REPLACE THE A3 PCB

This paragraph provides instructions for removing and replacing the A3 Signal Channel PCB, which is located immediately behind the front panel input connectors. Use this procedure also for gaining access to the Input A, Input B, and (optional) Input R connectors for replacement. The replacement process is the reverse of the removal process.

Preliminary

☐ Remove the top, bottom, and side covers (paragraph 7-2).

☐ Remove the A5 and A6 PCBs (paragraph 7-3), to gain access to motherboard connector A4J16.

Procedure

Step 1. With the 541XXA top-side up on, disconnect the cable from A4J16 (on the motherboard).

Step 2. Place 541XXA on its top (bottom-side up).

Step 3. Disconnect the white grounding wire (Figure 7-5), and dress it away from the PCB.

Step 4. Disconnect the ribbon cable connector at the rear of the A3 PCB.

Step 5. Remove the five screws and flat washers.

Step 6. Remove the two nuts that fasten the front panel to the chassis.

Step 7. Remove the A3 PCB by lifting its rear edge and pulling it toward the rear of the 541XXA.

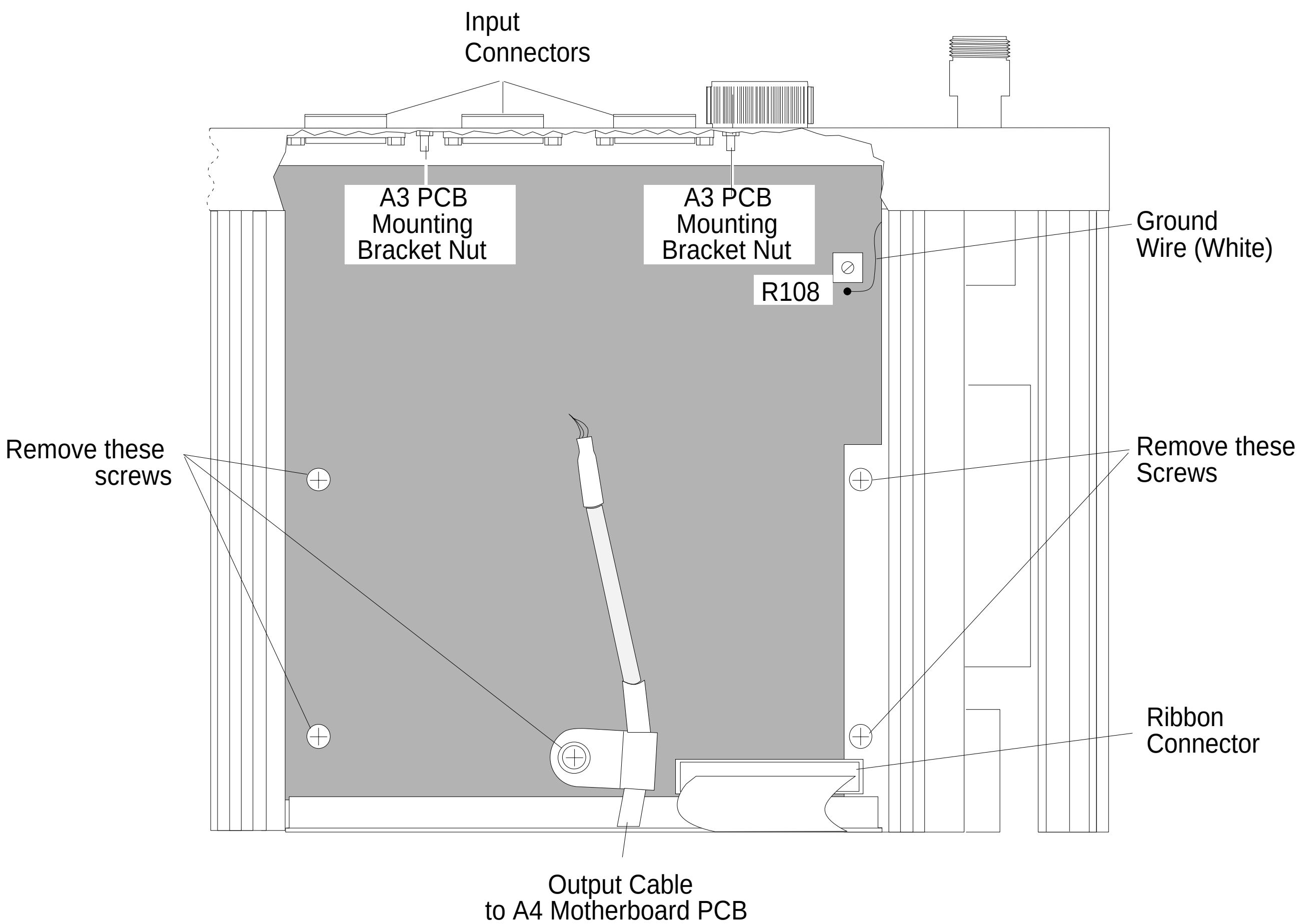


Figure 7-5. *Removing the A3 Signal Channel PCB and Front Panel Input Connectors*

7-9 REMOVE AND REPLACE THE POWER SUPPLY ASSEMBLY

This paragraph provides instructions for removing and replacing the Power Supply Assembly, which consists of the A9 Power Supply Motherboard PCB and the A16 Power Supply Converter PCB. The power supply assembly is removed/replaced as a complete unit. The replacement process is the reverse of the removal process.

Preliminary:

☐ Remove the top, bottom, and side covers (paragraph 7-2).

☐ Remove the A9 PCB from the card cage.

Procedure:

Step 1. Place 541XXA on its left side (right-side up).

Step 2. Remove the two screws that fasten the Power On/Off switch mounting bracket to the chassis (Figure 7-6, top).

Step 3. Slide the surrounding bezel straight away from the front panel, and set it aside.

Step 4. Remove the two screws that fasten the power supply assembly bottom bracket to the chassis center rail.

Step 5. Place the 541XXA on its bottom (top-side up).

Step 6. Disconnect the cable from the Line Voltage Selector Module at connector J1 of the Power Supply Motherboard.

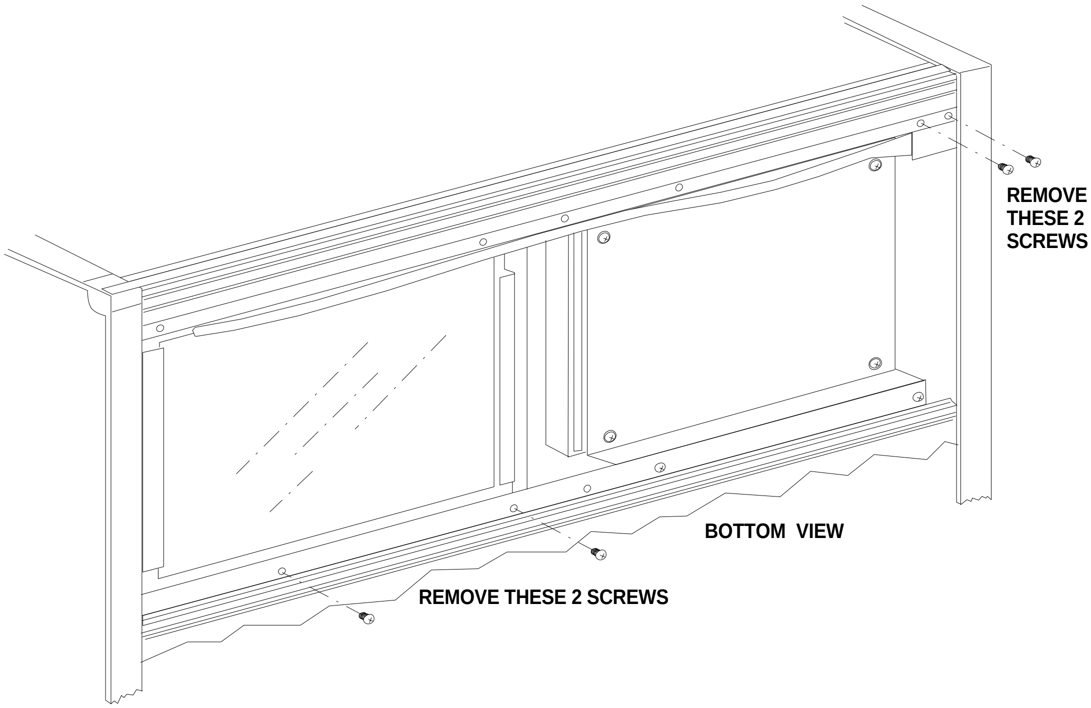
Step 7. Similarly, disconnect the fan cable at connector J3.

Step 8. Disconnect the cable at connector J2 (at the front edge of the Power Supply Motherboard).

Step 9. From the rear panel, remove two screws from the LineVoltage Selector Module, and slide the module rearward to allow clearance for removing the power supply.

Step 10. Remove the three screws that fasten the power supply assembly to the chassis side rail (Figure 7-3, bottom).

Step 11. Lift the power supply assembly up and forward to remove from unit.



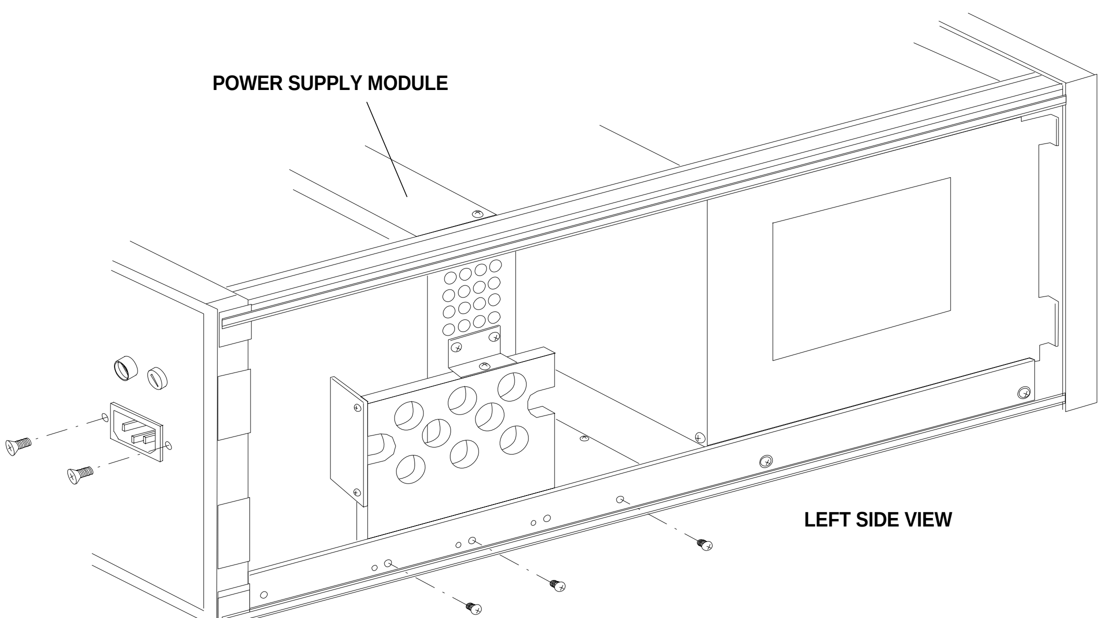


Figure 7-6. *Removing the Power Supply Assembly*

7-10 REMOVE AND REPLACE THE CRT MONITOR ASSEMBLY

This paragraph provides instructions for removing and replacing the CRT Monitor Assembly, which consists of the CRT monitor unit and mounting bracket. The CRT Monitor Assembly is removed/ replaced as a complete unit. The replacement process is the reverse of the removal process.

Preliminary:

☐ Remove the top, bottom, and side covers (paragraph 7-2).

☐ Remove the A5 and A6 PCBs (paragraph 7-3).

Procedure:

Step 1. Place the 541XXA on its left side (right-side up).

Step 2. Remove four screws, flat, and lock washers (Figure 7-7).

Step 3. While supporting the CRT monitor assembly, place the 541XXA on its bottom side (top-side up).

Step 4. Disconnect the CRT monitor assembly cable at connector J15 of the A4 Motherboard PCB (A5J15).

Step 5. Move the assembly to the rear and lift from unit.

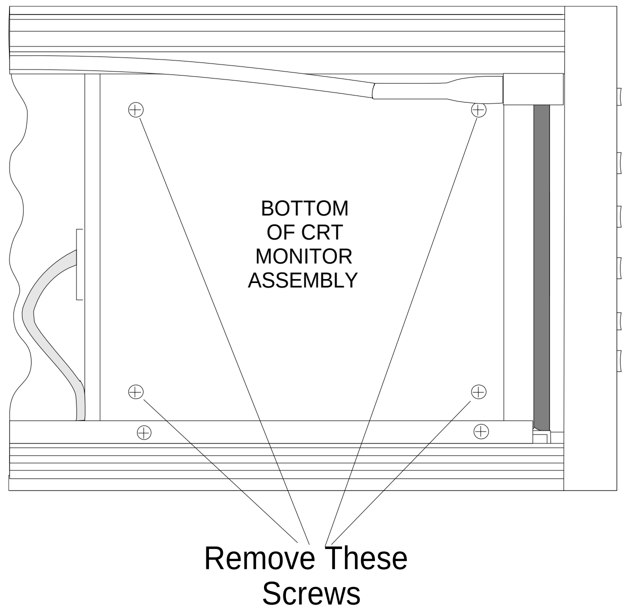


Figure 7-7. *CRT Monitor Assembly Removal (Bottom)*

7-11 REMOVE AND REPLACE THE REAR PANEL ASSEMBLY

This paragraph provides instructions for removing and replacing the Rear Panel Assembly. This panel must be removed to replace the fan and rear panel connectors. The replacement process is the reverse of the removal process.

Preliminary:

☐ Remove the top, bottom, and side covers (paragraph 7-2).

Procedure:

Step 1. Orient the 541XXA as appropriate to remove two screws from the bottom of the rear panel and one screw from the middle of either side of the rear panel (Figure 7-8).

Step 2. Remove the fan connection from J3 on the A9 Power Supply PCB (A9J3).

Step 3. Remove the Line Voltage Module connection from A9J1.

Step 4. Remove the EXTERNAL MONITOR connection from J17 on the A4 Motherboard (A4J17).

Step 5. Remove two screws (located between the fan and the connector bank) from the rear panel.

Step 6. Work the rear panel away from the frame to remove.

NOTE

All rear panel parts are assessable; it is not necessary to disconnect any other cables.

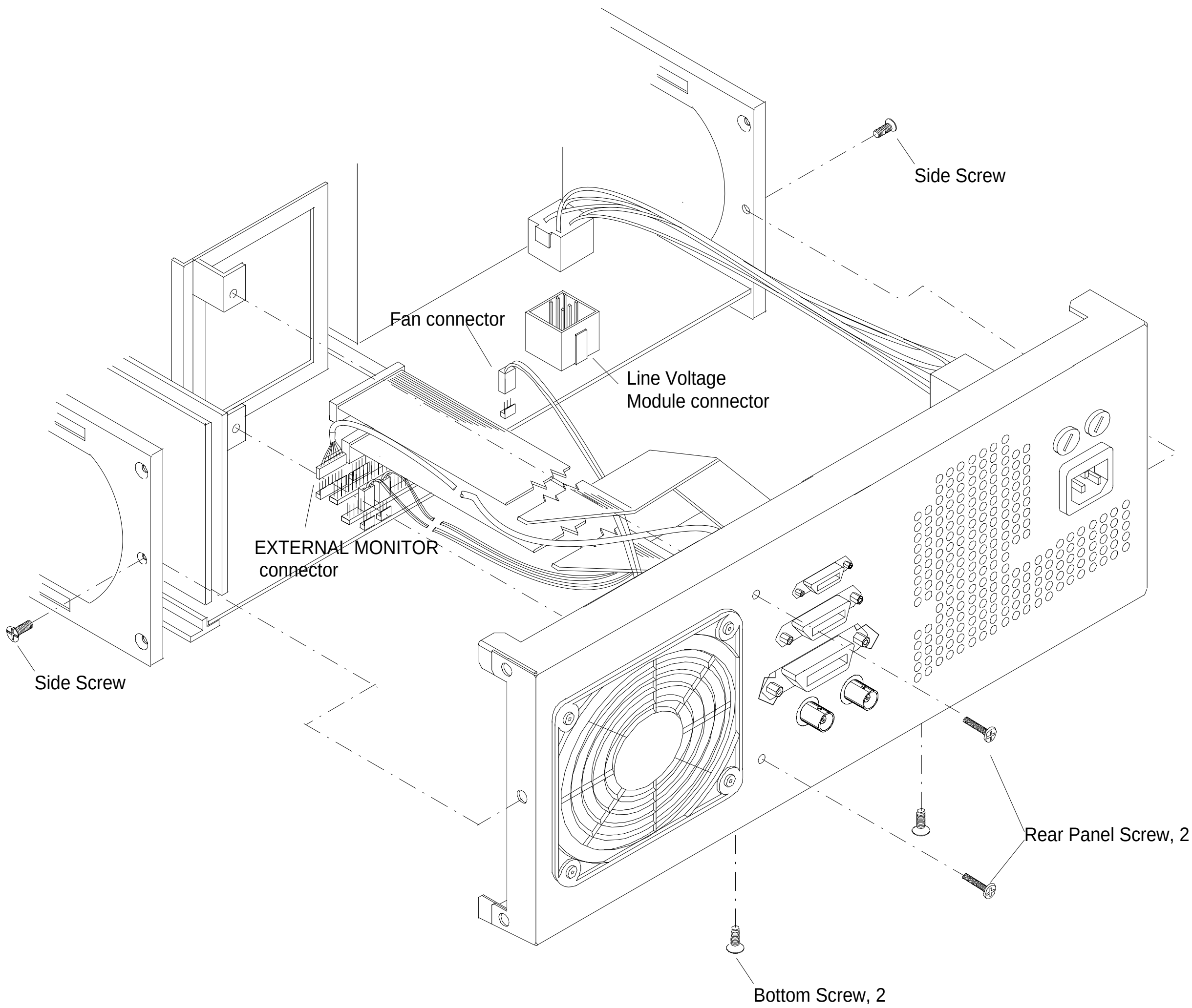


Figure 7-8. *Exploded View of Rear Panel Assembly*

7-12 REMOVE AND REPLACE THE FAN ASSEMBLY

This paragraph provides instructions for removing and replacing the rear panel cooling fan assembly. The replacement process is the reverse of the removal process.

Preliminary:

☐ Remove the top, bottom, and side covers (paragraph 7-2).

Procedure:

Step 1. Disconnect the fan power cable from the motherboard connector.

Step 2. While supporting the fan from the backside, remove four corner screws and pull the fan screen straight away.

Step 3. Lift the rear panel away from the fan and fan space bracket.

NOTES

The fan filter should be cleaned at this time, if necessary.

7-13 RF DECK COMPONENTS, OVERVIEW

The 541XXA series uses four basic RF deck configurations: 54107A/ 54109A/ 54111A, 54117A/54119A, 54128A, 54130A, 54131A, 54136A, and 54137A/54147A. Remove and Replace procedures for the RF and microwave components located on these assemblies are organized and presented for each assembly.

7-14 REMOVE AND REPLACE THE RF DECK ASSEMBLY

This paragraph provides instructions for removing and replacing the RF deck assembly, which is located on the left side of the chassis.

NOTES

- Normally, it is not necessary to remove the RF Deck from Models 54107A, 54109A, and 54111A. Almost all troubleshooting and repair operations can be performed with the RF Deck in place.
- Also, most of the side-mounted components on the remaining models can be accessed without having to remove the RF deck. If deck removal is necessary, it will be so stated within the procedure.

Preliminary:

☐ Remove the top, bottom, and side covers (paragraph 7-2).

☐ Remove the front panel assembly (paragraph 7-4).

Procedure:

Step 1. Disconnect all cable connections between the RF deck and the A4 Motherboard.

Step 2. Place the 541XXA on its right side (left-side up).

Step 3. Remove the one screw from the middle-rear of the bracket; remove two screws from the top of the bracket (Figure 7-10).

Step 4. Remove three hex screws from the RF deck, and lift the RF deck straight away to remove.

Step 5. To replace the RF deck, reverse the removal process.

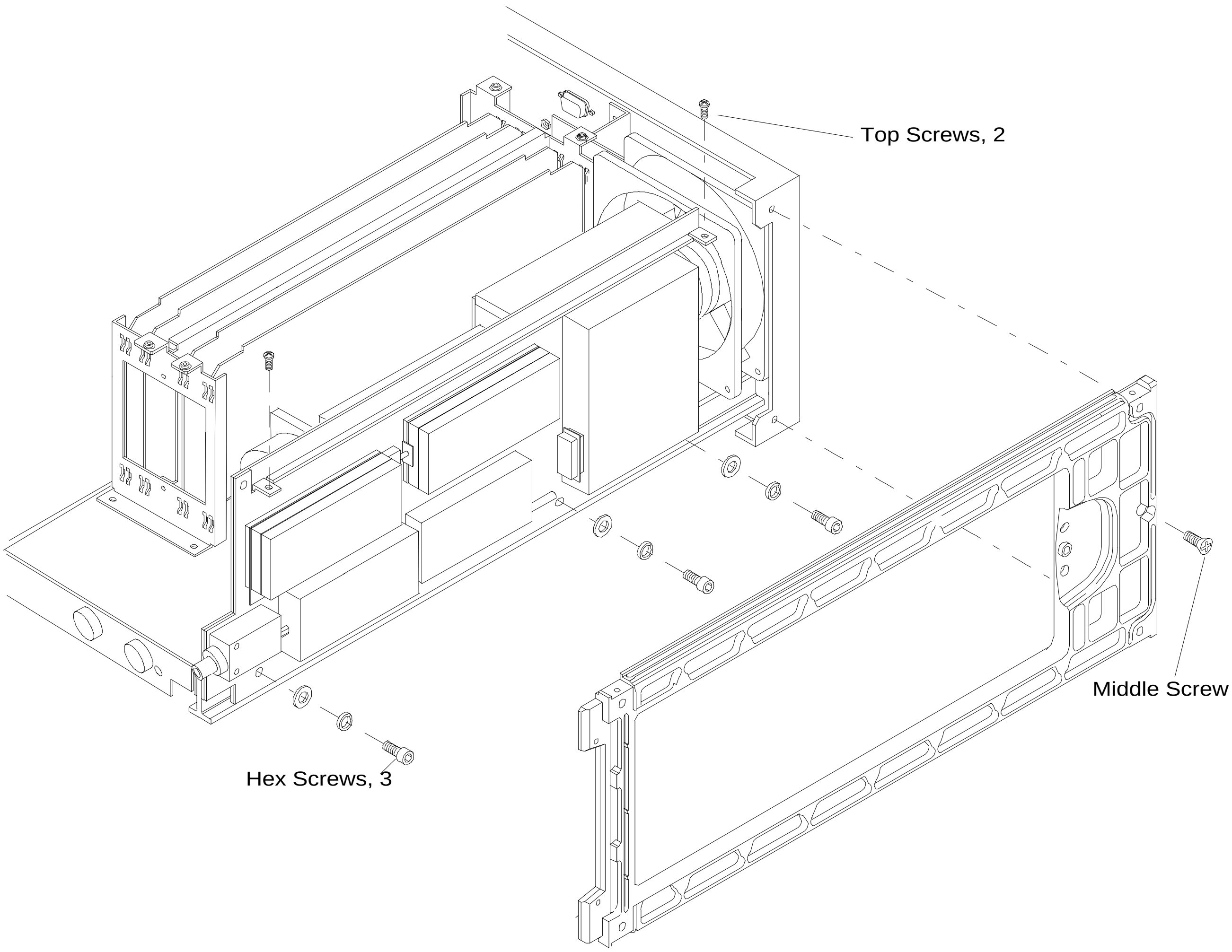


Figure 7-10. *RF Deck Removal/Replacement*

7-15 REMOVE AND REPLACE 54107A, 54109A, 54111A RF COMPONENTS

This paragraph provides instructions for removing and replacing the RF components on the 54107A, 54109A, and 54111A RF decks. Procedures are organized by component. Refer to Figure 7-11 for component locations. In all cases, the replacement procedure is the reverse of the removal procedure.

Preliminary

☐ Remove the top, bottom, and left-side covers (paragraph 7-2).

☐ Place the 541XXA on its right side (left-side up).

25/75 Marker Generator Procedure

Step 1. Remove the marker generator connection from motherboard connector A4J18.

Step 2. Remove one RF connector.

Step 3. Remove four screws, and lift the marker generator straight away.

Down Converter Procedure

Step 1. Remove the RF Deck (paragraph 7-14).

Step 2. Remove three RF connectors and one control connector.

Step 3. Remove four screws from the inward-facing side (not shown), and lift the down converter straight away.

Isolator Procedure

Remove two RF connectors, and remove the isolator.

Step Attenuator Procedure

Step 1. Remove the step attenuator connection from motherboard connector A4J6.

Step 2. Remove two RF connectors.

Step 3. Remove four screws, and lift the step attenuator straight away.

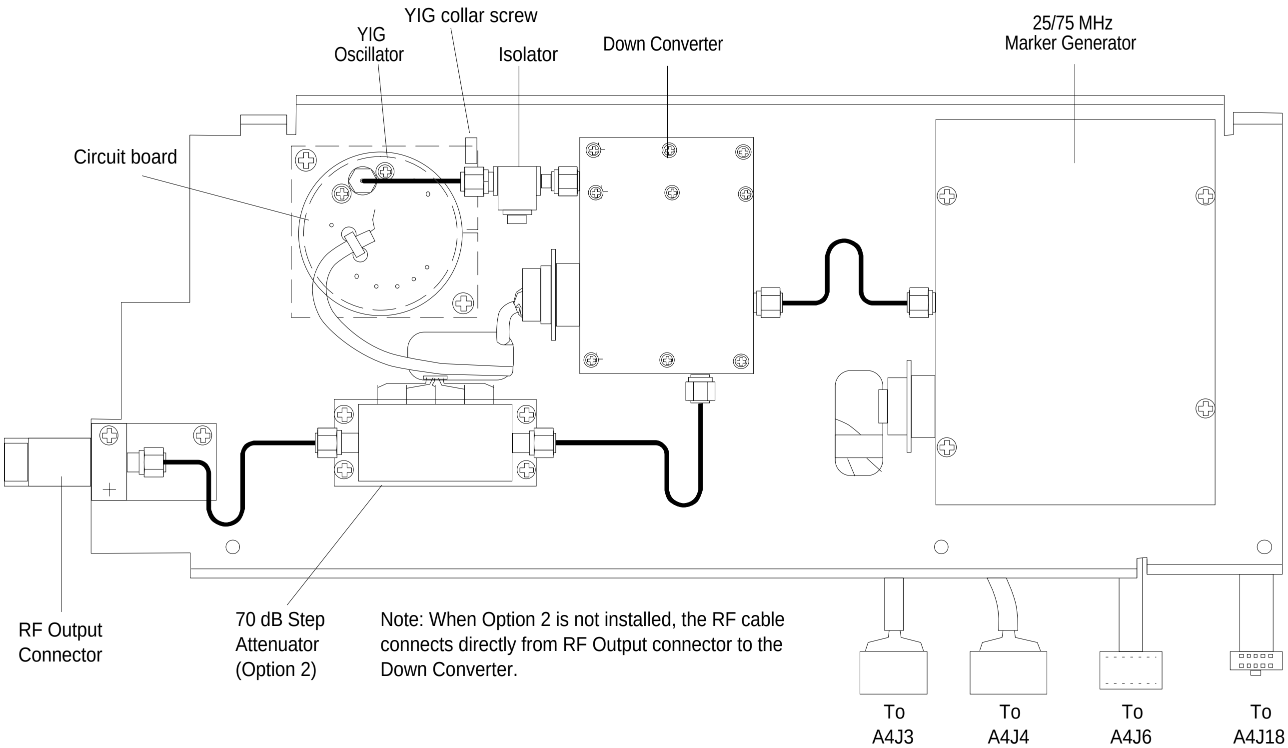


Figure 7-11. *Models 54107A, 54109A, and 54111A RF Deck Parts Location*

RF Output Connector Procedure

Step 1. Remove one RF connector.

Step 2. Remove the two screws shown, and a third screw from the opposite side; slide the connector to the rear to remove.

YIG Oscillator Procedure

Step 1. Remove the YIG oscillator connection from motherboard connector A4J3.

Step 2. Remove one RF connector.

Step 3. Remove two screws from the YIG circuit board.

Step 4. From the side opposite that shown, loosen the YIG collar-screw and slide the YIG out and away.

7-16 REMOVE AND REPLACE 54117A, 54119A MICROWAVE COMPONENTS

This paragraph provides instructions for removing and replacing the microwave components on the 54117A and 54119A RF decks. Procedures are organized by component. Refer to Figures 7-12 and 7-13 for component locations. In all cases, the replacement procedure is the reverse of the removal procedure.

Preliminary

☐ Remove the top, bottom, and left-side covers (paragraph 7-2).

☐ Place the 541XXA on its right side (left-side up).

25 MHz Marker Module Procedure

Step 1. Unsolder four wires and disconnect one wire.

Step 2. Remove two press-on RF connectors.

Step 3. Remove six screws from the outer cover; remove the cover and set it aside.

Step 4. Remove four screws, and lift the marker module straight away.

500 MHz Marker Module Procedure

Step 1. Remove the marker connection from A17J4 on the RF Distribution PCB (Figure 7-13).

Step 2. Remove two RF connectors.

Step 3. Remove six screws from the outer cover; remove the cover and set it aside.

Step 4. Unsolder four wires from 25 MHz Marker Module.

Step 5. Remove four screws, and lift the marker module straight away.

500 MHz VCO/Power Amplifier/Divider Module Procedure

Step 1. Remove the connection from A17J2 on the RF Distribution PCB (Figure 7-13).

Step 2. Remove one RF connector.

Step 3. Remove nine screws from the outer cover; remove the cover and set it aside.

Step 4. Remove six screws, and lift the module straight away.

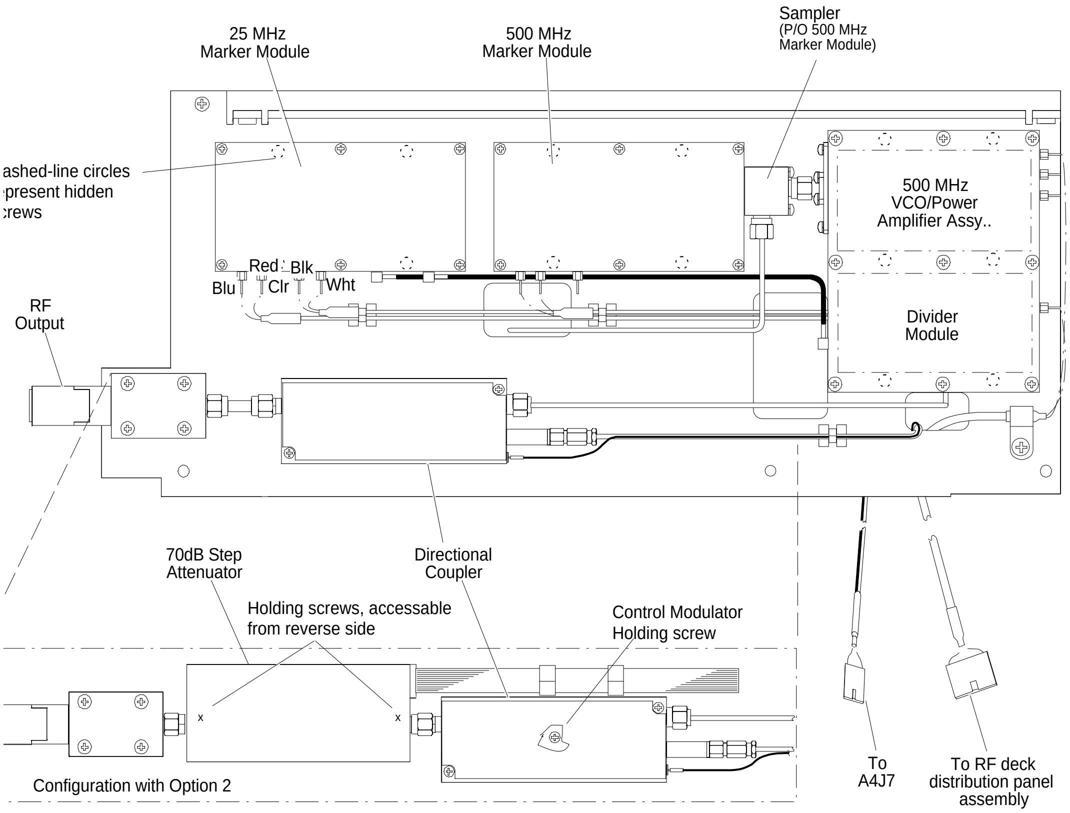


Figure 7-12. *Models 54117A and 54119A RF Deck Parts Location (External Side Detail)*

Directional Coupler Procedure

Step 1. Remove the connection from A4J7 on the motherboard.

Step 2. Remove two screws first, then remove the two connections on the right side.

Step 3. Remove two RF connectors from the rear of the Directional Coupler.

Step 4. Slide the Directional Coupler back while unscrewing the last RF connector, then lift the module straight away.

Step Attenuator and RF Output Procedure

Step 1. Remove the Directional Coupler (see above procedure).

Step 2. Remove the D25432 Marker Package (See Figure 7-13 and procedure on next page).

Step 3. Remove two screws from the attenuator package ("X" in Figure 7-12); disconnect the remaining connector and lift the attenuator straight away.

Step 4. Remove four screws from the RF Output assembly; slide assembly to the rear and out.

NOTE

For the procedures on this page, starting with the D25432 Marker Package, the RF deck (paragraph 7-14) has to be removed.

D25432 Marker Package Procedure

Step 1. Remove one RF connectors and one control connector (Figure 7-13).

Step 2. Remove four screws and lift the marker package straight away.

YIG Oscillator Procedure

Step 1. Remove the YIG oscillator connection from motherboard connector A4J3.

Step 2. Remove one RF connector.

Step 3. Remove two screws from the YIG circuit board.

Step 4. Loosen the YIG collar screw and slide the YIG out and away.

Down Converter Procedure

Step 1. Remove three RF connectors and one control connector.

Step 2. Remove four screw, and lift the down converter straight away.

A17 RF Deck Distribution Panel Procedure

Step 1. Remove the panel connection from motherboard connector A4J4.

Step 2. Remove two control connectors.

Step 3. Remove four screw, and lift the panel straight away.

Control Modulator Procedure

Step 1. Remove four screw-on and two press-on RF connectors.

Step 2. Remove the directional coupler from the opposite side (see procedure on page 7-24).

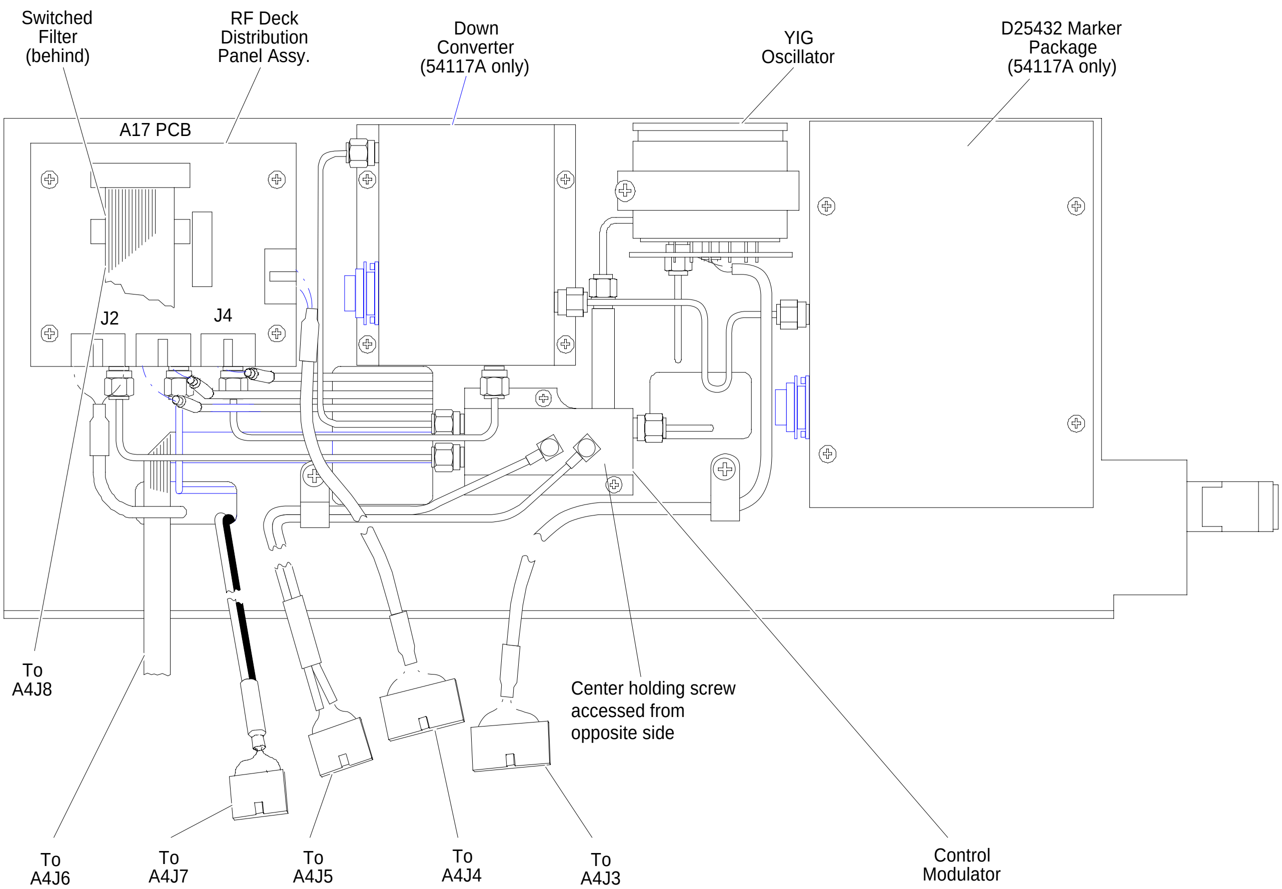


Figure 7-13. *Models 54117A and 54119A RF Deck Parts Location (Internal Side Detail)*

Step 3. Remove the center holding screw for the control modulator.

Step 4. Lift the control modulator straight away to remove.

7-17 REMOVE AND REPLACE 54128A, 54130A, 54131A, 54136A MICROWAVE COMPONENTS

This paragraph provides instructions for removing and replacing the microwave components on the 54128A, 54130A, 54130A, 54131A, and 54136A RF decks. Procedures are organized by component. Refer to Figures 7-14 and 7-15 for component locations. In all cases, the replacement procedure is the reverse of the removal procedure.

Preliminary

☐ Remove the top, bottom, and left-side covers (paragraph 7-2).

☐ Place the 541XXA on its right side (left-side up).

25 MHz Marker Module Procedure

Step 1. Unsolder four wires and disconnect one wire.

Step 2. Remove two press-on RF connectors.

Step 3. Remove six screws from the outer cover; remove the cover and set it aside.

Step 4. Remove four screws, and lift the marker module straight away.

500 MHz Marker Module Procedure

Step 1. Remove the marker connection from A17J4 on the RF Distribution PCB (Figure 7-13).

Step 2. Remove two RF connectors.

Step 3. Unsolder four wires from 25 MHz Marker Module.

Step 4. Remove six screws from the outer cover; remove the cover and set it aside.

Step 5. Remove four screws, and lift the marker module straight away.

500 MHz VCO/Power Amplifier/Divider Module Procedure

Step 1. Remove the connection from A17J2 on the RF Distribution PCB (Figure 7-13).

Step 2. Remove one RF connector.

Step 3. Remove nine screws from the outer cover; remove the cover and set it aside.

Step 4. Remove six screws, and lift the module straight away.

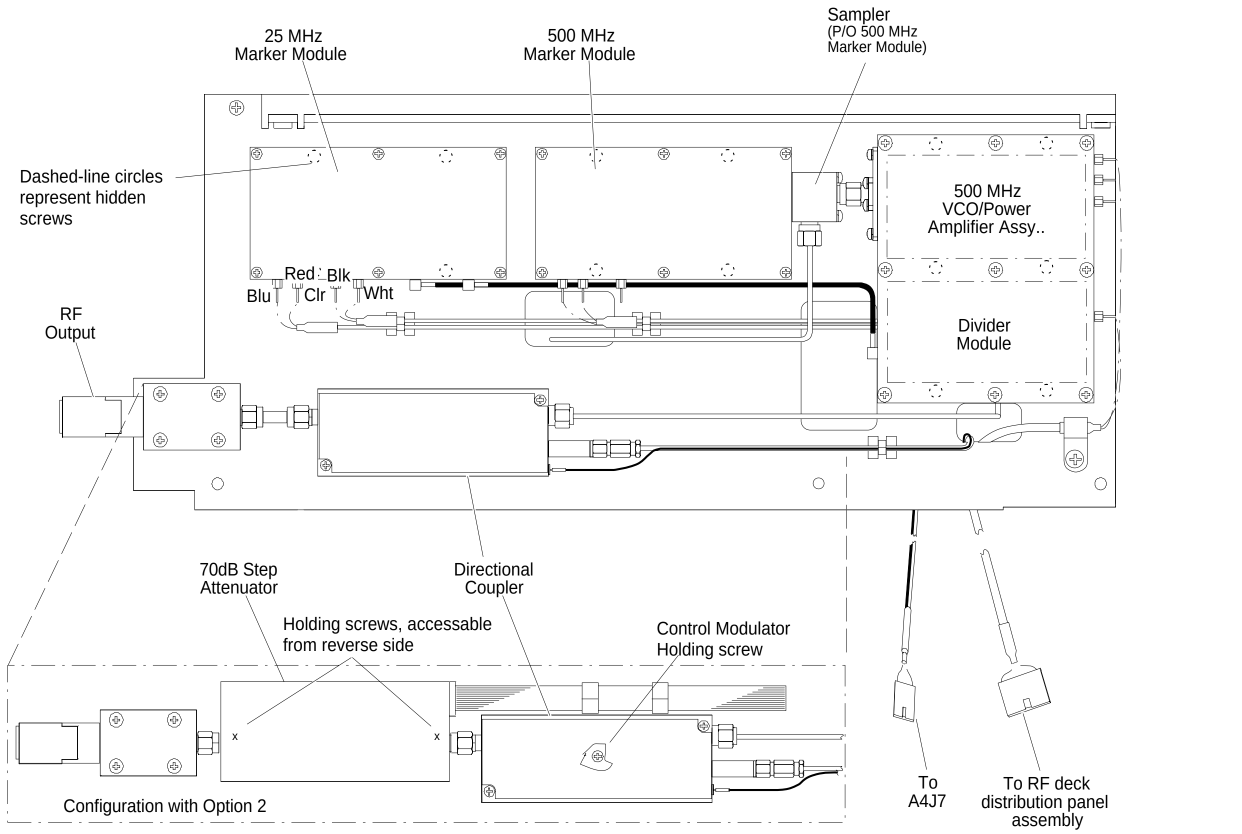


Figure 7-14. *Models 54128A, 54130A, 54131A, and 54136A RF Deck Parts Location (External Side Detail)*

Directional Coupler Procedure

Step 1. Remove the connection from A4J7 on the motherboard.

Step 2. Remove two screws first, then remove the two connections on the right side.

Step 3. Remove two RF connectors from the rear of the Directional Coupler.

Step 4. Slide the Directional Coupler back while unscrewing the last RF connector, then lift the module straight away.

Step Attenuator and RF Output Procedure

Step 1. Remove the Directional Coupler (see above procedure).

YIG Oscillator Procedure

NOTE

For all of the procedures on this page, the RF deck (paragraph 7-14) has to be removed.

Step 1. Remove the YIG oscillator connection from motherboard connector A4J3.

Step 2. Remove one RF connector.

Step 3. Remove two screws from the YIG circuit board.

Step 4. Loosen the YIG collar screw and slide the YIG out and away.

A17 RF Deck Distribution Panel Procedure

Step 1. Remove the panel connection from motherboard connector A4J4.

Step 2. Remove two control connectors.

Step 3. Remove four screw, and lift the panel straight away.

Control Modulator Procedure

Step 1. Remove four screw-on and two press-on RF connectors.

Step 2. Remove the directional coupler from the opposite side (see procedure on page 7-24), if step attenuator is installed.

Step 3. Remove the center holding screw for the control modulator.

Step 4. Lift the control modulator straight away to remove.

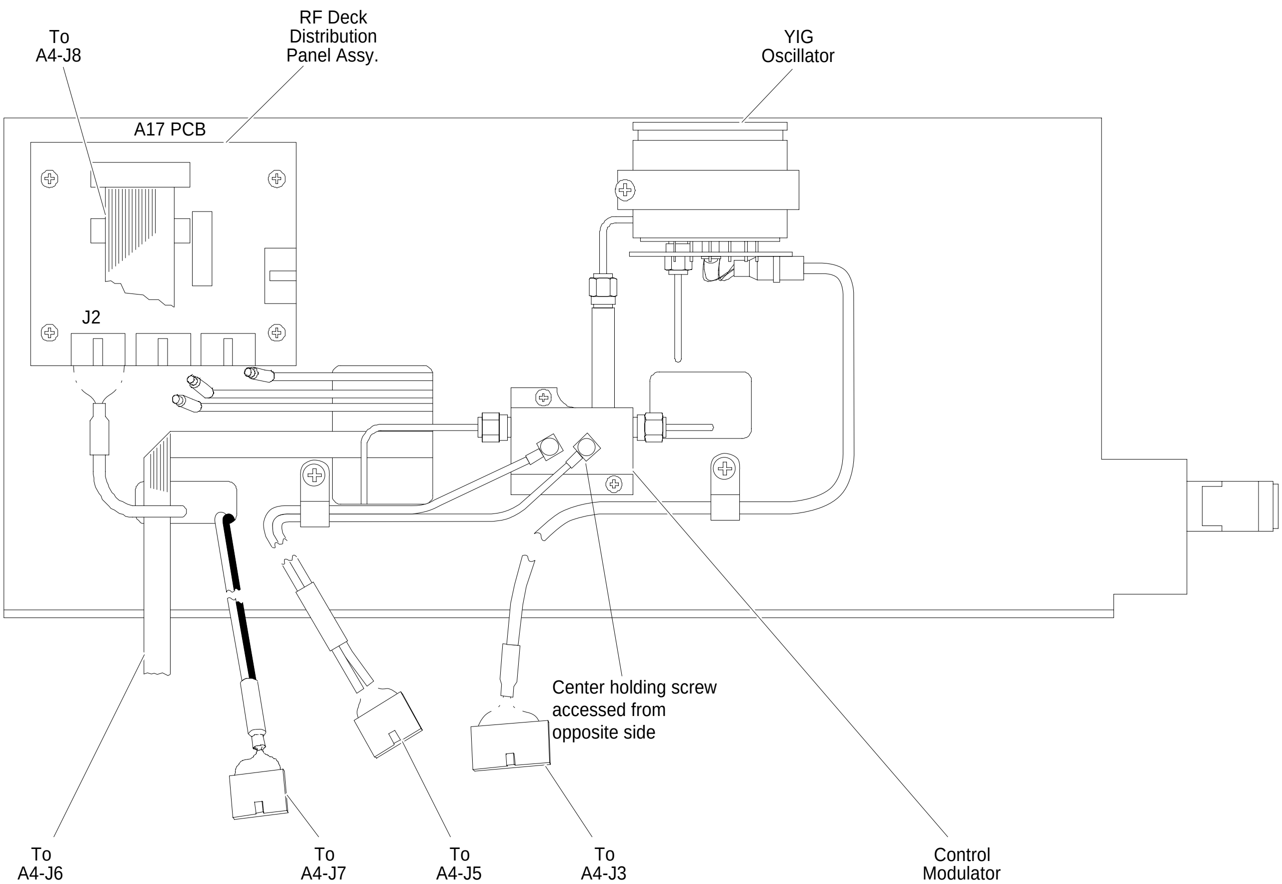


Figure 7-15. *Models 54128A, 54130A, 54131A, and 54136A RF Deck Parts Location (Internal Side Detail)*

7-18 REMOVE AND REPLACE 54137A, 54147A MICROWAVE COMPONENTS

This paragraph provides instructions for removing and replacing the microwave components on the 54137A and 54147A RF decks. Procedures are organized by component. Refer to Figures 7-16 and 7-17 for component locations. In all cases, the replacement procedure is the reverse of the removal procedure.

Preliminary

- ☐ Remove the top, bottom, and left-side covers (paragraph 7-2).
- ☐ Place the 541XXA on its right side (left-side up).

25 MHz/500 MHz Marker Modules Procedure

Step 1. Remove the marker connection from A19J5 on the Multiband Controller PCB (Figure 7-17).

Step 2. Remove six screws from the outer cover; remove the cover and set it aside. Remove two additional screws, and expose the bottom assembly.

Step 3. Remove four screws on the bottom assembly.

Step 4. Remove two RF connectors.

Step 5. Lift the two marker modules straight away.

500 MHz VCO/Power Amplifier/Divider Modules Procedure

Step 1. Remove the connection from A19J4 on the Multiband Controller PCB (Figure 7-17).

Step 2. Remove one RF connector.

Step 3. Remove the MCX connector from the 25MHz output.

Step 4. Remove six screws from the outer cover; remove the cover and set it aside. Remove two additional screws, and expose the bottom assembly.

Step 5. Remove four screws, and lift the modules straight away.

Directional Coupler Procedure

Step 1. Remove the connection from A4J7 on the motherboard.

Step 2. Remove two screws first, then remove the two connections on the right side.

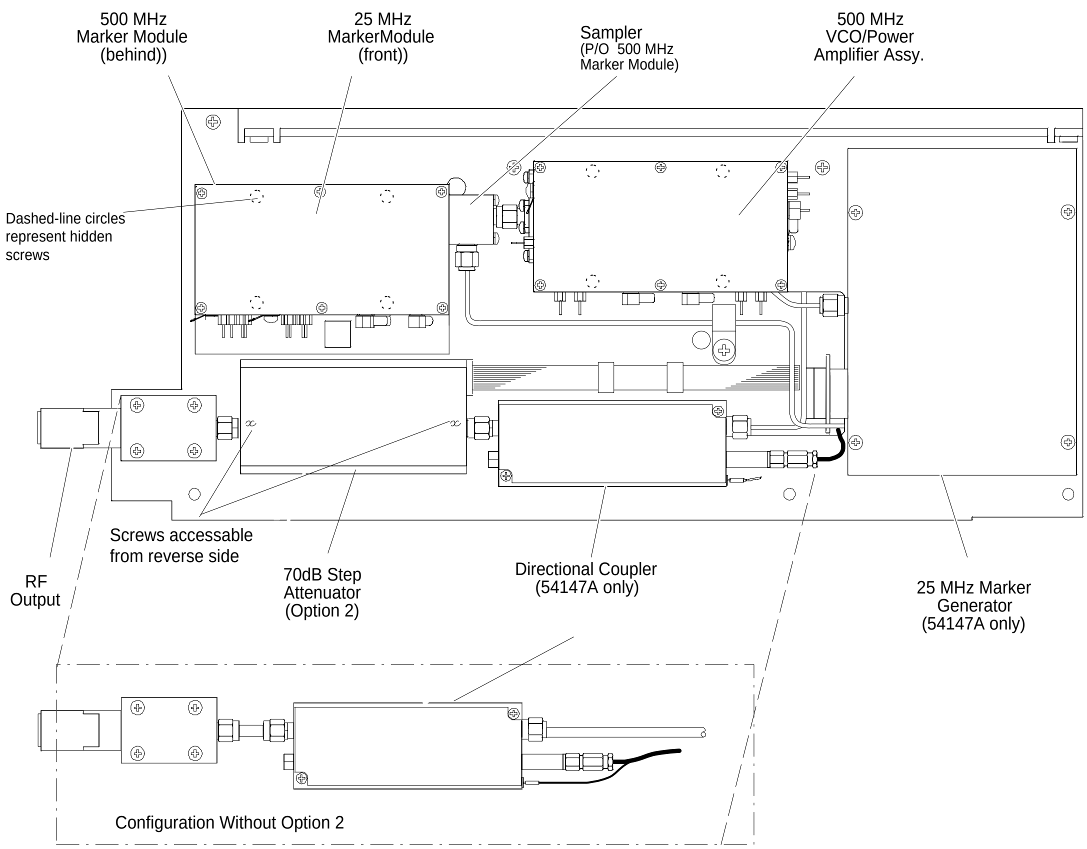


Figure 7-16. *Models 54137A and 54147A RF Deck Parts Location (External Side Detail)*

Step 3. Remove two RF connectors from the rear of the Directional Coupler..

Step 4. Slide the Directional Coupler back while unscrewing the last RF connector, then lift the module straight away

Step Attenuator and RF Output Procedure

Step 1. Remove the Directional Coupler (see above procedure).

Step 2. Remove the Switched Filter (See Figure 7-17 and procedure on next page).

Step 3. Remove two screws from attenuator package ("X" in Figure 7-16), disconnect the remaining RF connector, and lift the attenuator straight away.

Step 4. Remove four screws from the RF Output assembly; slide assembly to the rear and out.

D25432 Marker Package Procedure

Step 1. Remove one RF connectors and one control connector (Figure 7-13).

Step 2. Remove four screws and lift the marker package straight away.

NOTE

For the procedures on this page, starting with the YIG oscillator procedure, the RF deck (paragraph 7-14) has to be removed.

YIG Oscillator Procedure

Step 1. Remove the YIG oscillator connection from motherboard connector A4J3.

Step 2. Remove one RF connector.

Step 3. Remove two screws from the YIG circuit board.

Step 4. Loosen the YIG collar screw and slide the YIG out and away.

Multiband Controller PCB Procedure

Step 1. Remove the panel connections from motherboard connectors A4J11 and A4J8.

Step 2. Remove five control connectors.

Step 3. Remove five screws, and lift the panel straight away.

Down Converter Procedure

Step 1. Remove Multiband Controller PCB.

Step 2. Remove three RF connectors and one control connector.

Step 3. Remove four screw, and lift the down converter straight away.

Switched Filter Procedure

Step 1. Remove all RF cables connected to the assembly.

Step 2. Remove the control cable.

Step 3. Remove four screws.

Step 4. Lift the Switched Filter Assembly straight away to remove.

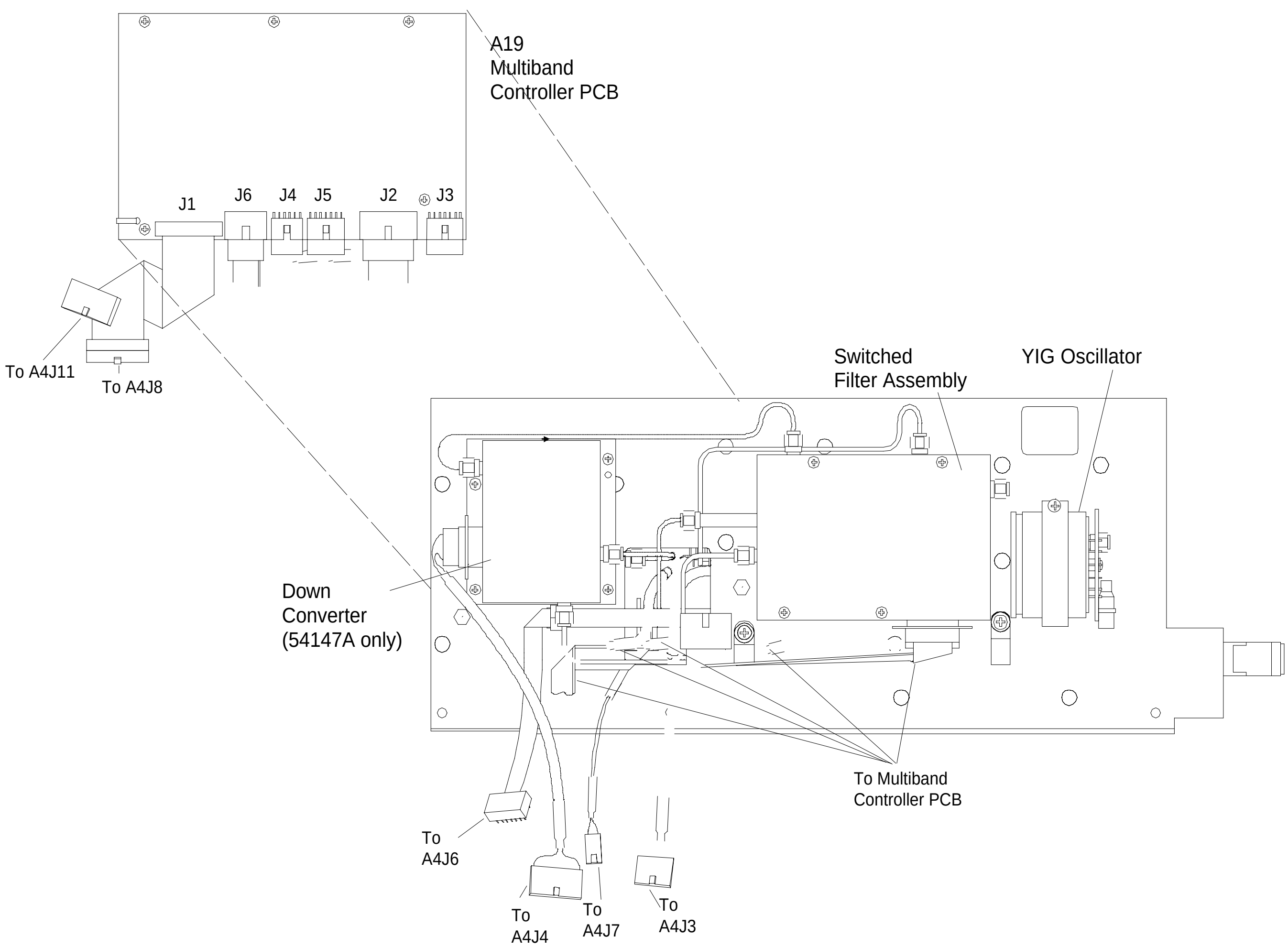


Figure 7-17. *Models 54137A and 54147A RF Deck Parts Location (Internal Side Detail)*

7-19 REMOVE AND REPLACE 54154A THROUGH 54169A MICROWAVE COMPONENTS

This paragraph provides instructions for removing and replacing the microwave components on the 54154A through 54169A RF decks. Procedures are organized by component. Refer to Figures 7-18 and 7-19 for component locations. In all cases, the replacement procedure is the reverse of the removal procedure.

Preliminary

☐ Remove the top, bottom, and left-side covers (paragraph 7-2).

☐ Place the 541XXA on its right side (left-side up).

25 MHz/500 MHz Marker Modules Procedure

Step 1. Remove the marker connection from A23J5 on the Multiband Controller PCB (Figure 7-19).

Step 2. Remove six screws from the outer cover; remove the cover and set it aside. Remove two additional screws, and expose the bottom assembly.

Step 3. Remove four screws on the bottom assembly.

Step 4. Remove two RF connectors.

Step 5. Lift the two marker modules straight away.

500 MHz VCO/Power Amplifier/Divider Modules Procedure

Step 1. Remove the connection from A23J4 on the Multiband Controller PCB (Figure 7-19).

Step 2. Remove one RF connector.

Step 3. Remove the MCX connector from the 25MHz output.

Step 4. Remove six screws from the outer cover; remove the cover and set it aside. Remove two additional screws, and expose the bottom assembly.

Step 5. Remove four screws, and lift the modules straight away.

Directional Coupler Procedure

Step 1. Remove the connection from A4J7 on the motherboard.

Step 2. Remove two screws first, then remove the two connections on the right side.

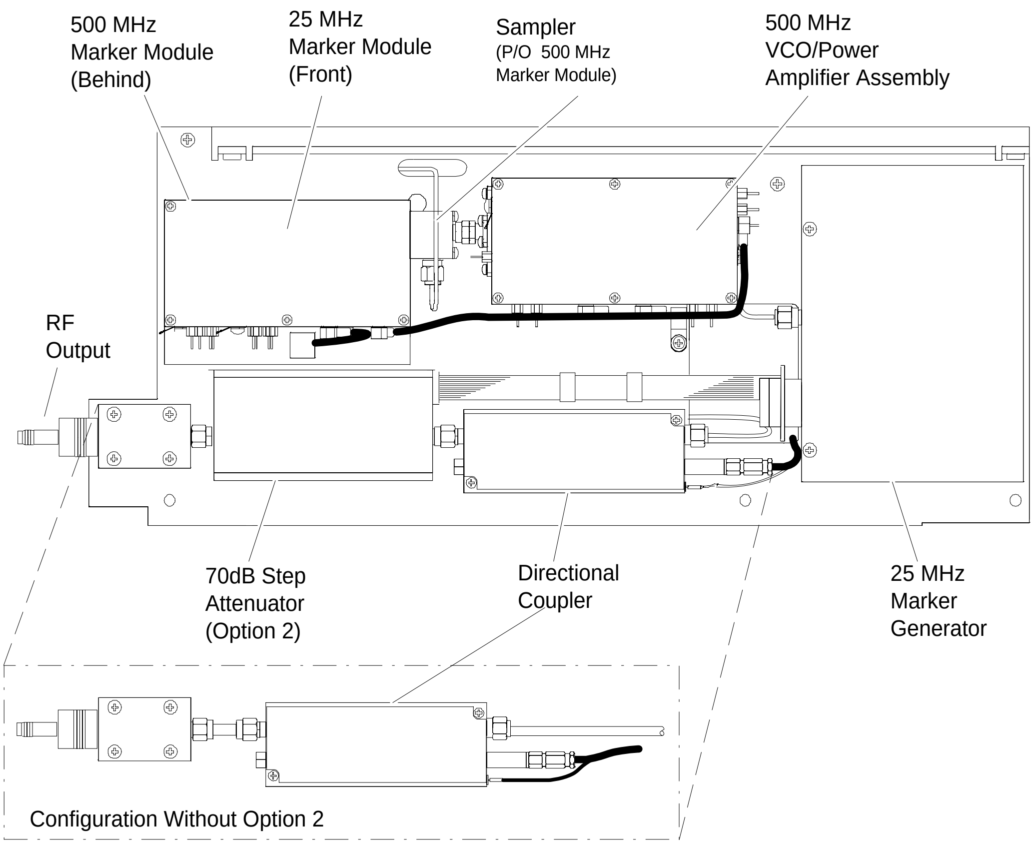


Figure 7-18. *Models 54154A through 54169A RF Deck Parts Location (External Side Detail)*

Step 3. Remove two RF connectors from the rear of the Directional Coupler.

Step 4. Slide the Directional Coupler back while unscrewing the last RF connector, then lift the module straight away

Step Attenuator and RF Output Procedure

Step 1. Remove the Directional Coupler (see above procedure).

Step 2. Remove the Switched Filter (See Figure 7-19 and procedure on next page).

Step 3. Remove two screws from attenuator package ("X" in Figure 7-18), disconnect the remaining RF connector, and lift the attenuator straight away.

Step 4. Remove four screws from the RF Output assembly; slide assembly to the rear and out.

D25432 Marker Package Procedure

Step 1. Remove one RF connectors and one control connector (Figure 7-13).

Step 2. Remove four screws and lift the marker package straight away.

YIG Oscillator Procedure

Step 1. Remove the YIG oscillator connection from motherboard connector A4J3.

Step 2. Remove one RF connector.

Step 3. Remove two screws from the YIG circuit board.

Step 4. Loosen the YIG collar screw and slide the YIG out and away.

Multiband Controller PCB Procedure

Step 1. Remove the panel connections from motherboard connectors A4J11 and A4J8.

Step 2. Remove five control connectors.

Step 3. Remove five screws, and lift the panel straight away.

Down Converter Procedure

Step 1. Remove Multiband Controller PCB.

Step 2. Remove three RF connectors and one control connector.

Step 3. Remove four screw, and lift the down converter straight away.

Switched Filter Procedure

Step 1. Remove all RF cables connected to the assembly.

Step 2. Remove the control cable.

Step 3. Remove four screws.

Step 4. Lift the Switched Filter Assembly straight away to remove.

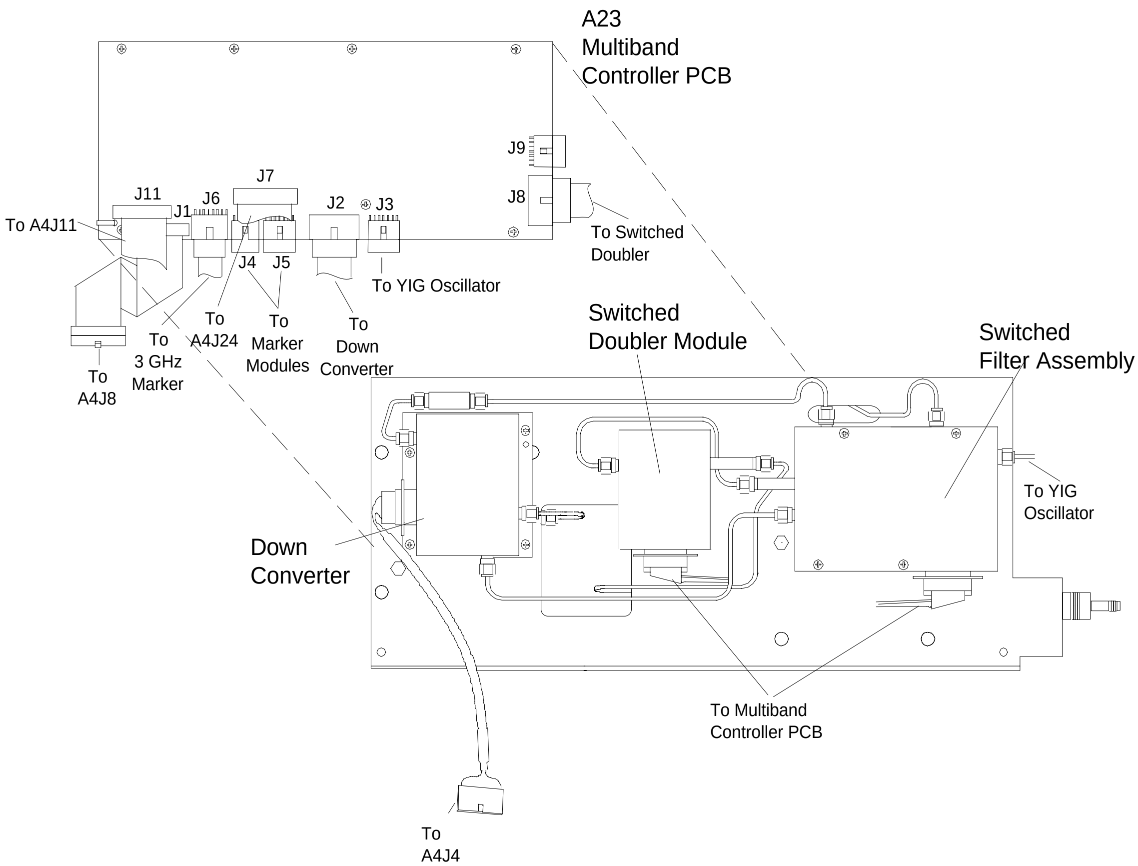


Figure 7-19. *Models 54154A through 54169A RF Deck Parts Location (Internal Side Detail)*

Switched Doubler Procedure

Step 1. Remove the multiband controller assembly (see above).

Step 2. Remove all RF cables connected to the assembly.

Step 3. Remove the control cable.

Step 4. Remove the VCO/PA Divider module to allow access to the four screws which mount the Switched Doubler.

Step 5. Remove four screws.

Step 6. Lift the Switched Doubler Assembly straight away to remove.

7-20 REMOVE AND REPLACE 54177A MICROWAVE COMPONENTS

This paragraph provides instructions for removing and replacing the microwave components on the 54177A RF deck. Procedures are organized by component. Refer to Figures 7-20 and 7-21 for component locations. In all cases, the replacement procedure is the reverse of the removal procedure.

Preliminary

☐ Remove the top, bottom, and left-side covers (paragraph 7-2).

☐ Place the 541XXA on its right side (left-side up).

25 MHz/500 MHz Marker Modules Procedure

Step 1. Remove the marker connection from A23J5 on the Multiband Controller PCB (Figure 7-21).

Step 2. Remove six screws from the outer cover; remove the cover and set it aside. Remove two additional screws, and expose the bottom assembly.

Step 3. Remove four screws on the bottom assembly.

Step 4. Remove two RF connectors.

Step 5. Lift the two marker modules straight away.

500 MHz VCO/Power Amplifier/Divider Modules Procedure

Step 1. Remove the connection from A23J4 on the Multiband Controller PCB (Figure 7-21).

Step 2. Remove one RF connector.

Step 3. Remove the MCX connector from the 25MHz output.

Step 4. Remove six screws from the outer cover; remove the cover and set it aside. Remove two additional screws, and expose the bottom assembly.

Step 5. Remove four screws, and lift the modules straight away.

Directional Coupler Procedure

Step 1. Remove the connection from A4J7 on the motherboard.

Step 2. Remove two screws first, then remove the two connections on the right side.

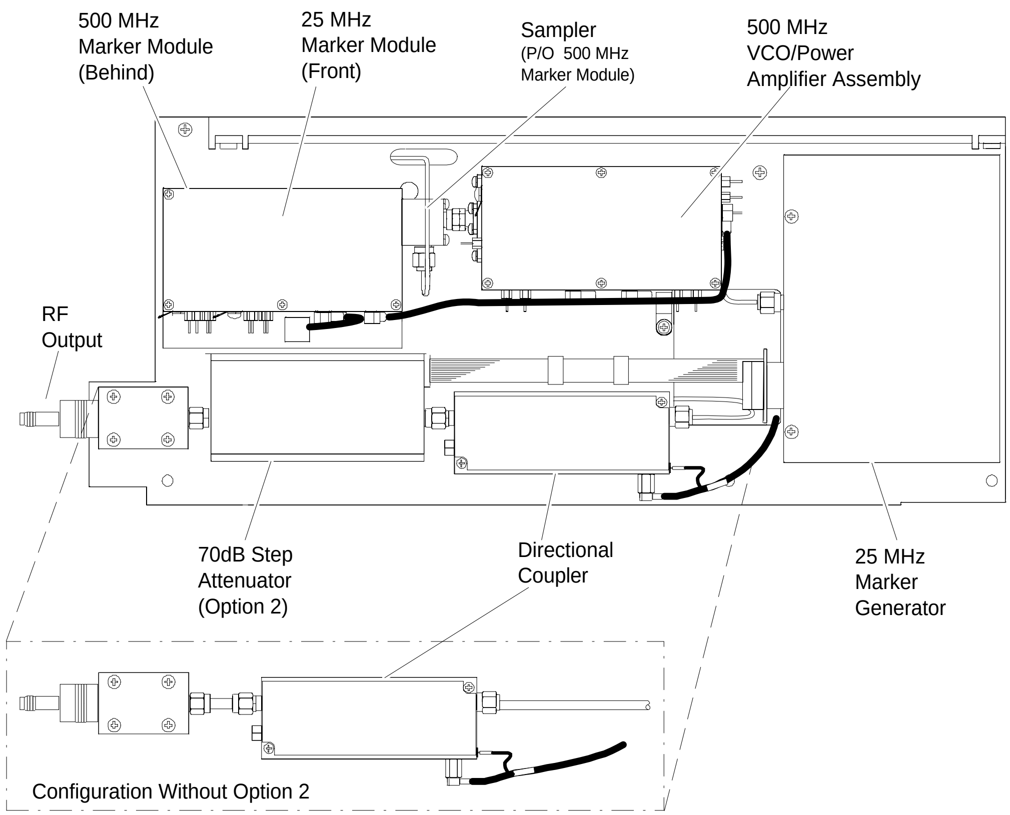


Figure 7-20. *Models 54177A RF Deck Parts Location (External Side Detail)*

Step 3. Remove two RF connectors from the rear of the Directional Coupler.

Step 4. Slide the Directional Coupler back while unscrewing the last RF connector, then lift the module straight away

Step Attenuator and RF Output Procedure

Step 1. Remove the Directional Coupler (see above procedure).

Step 2. Remove the Switched Filter (See Figure 7-21 and procedure on next page).

Step 3. Remove two screws from attenuator package ("X" in Figure 7-20), disconnect the remaining RF connector, and lift the attenuator straight away.

Step 4. Remove four screws from the RF Output assembly; slide assembly to the rear and out.

D25432 Marker Package Procedure

Step 1. Remove one RF connectors and one control connector (Figure 7-13).

Step 2. Remove four screws and lift the marker package straight away.

YIG Oscillator Procedure

Step 1. Remove the YIG oscillator connection from motherboard connector A4J3.

Step 2. Remove one RF connector.

Step 3. Remove two screws from the YIG circuit board.

Step 4. Loosen the YIG collar screw and slide the YIG out and away.

Multiband Controller PCB Procedure

Step 1. Remove the panel connections from motherboard connectors A4J11 and A4J8.

Step 2. Remove five control connectors.

Step 3. Remove five screws, and lift the panel straight away.

Down Converter Procedure

Step 1. Remove Multiband Controller PCB.

Step 2. Remove three RF connectors and one control connector.

Step 3. Remove four screw, and lift the down converter straight away.

Switched Filter Procedure

Step 1. Remove all RF cables connected to the assembly.

Step 2. Remove the control cable.

Step 3. Remove four screws.

Step 4. Lift the Switched Filter Assembly straight away to remove.

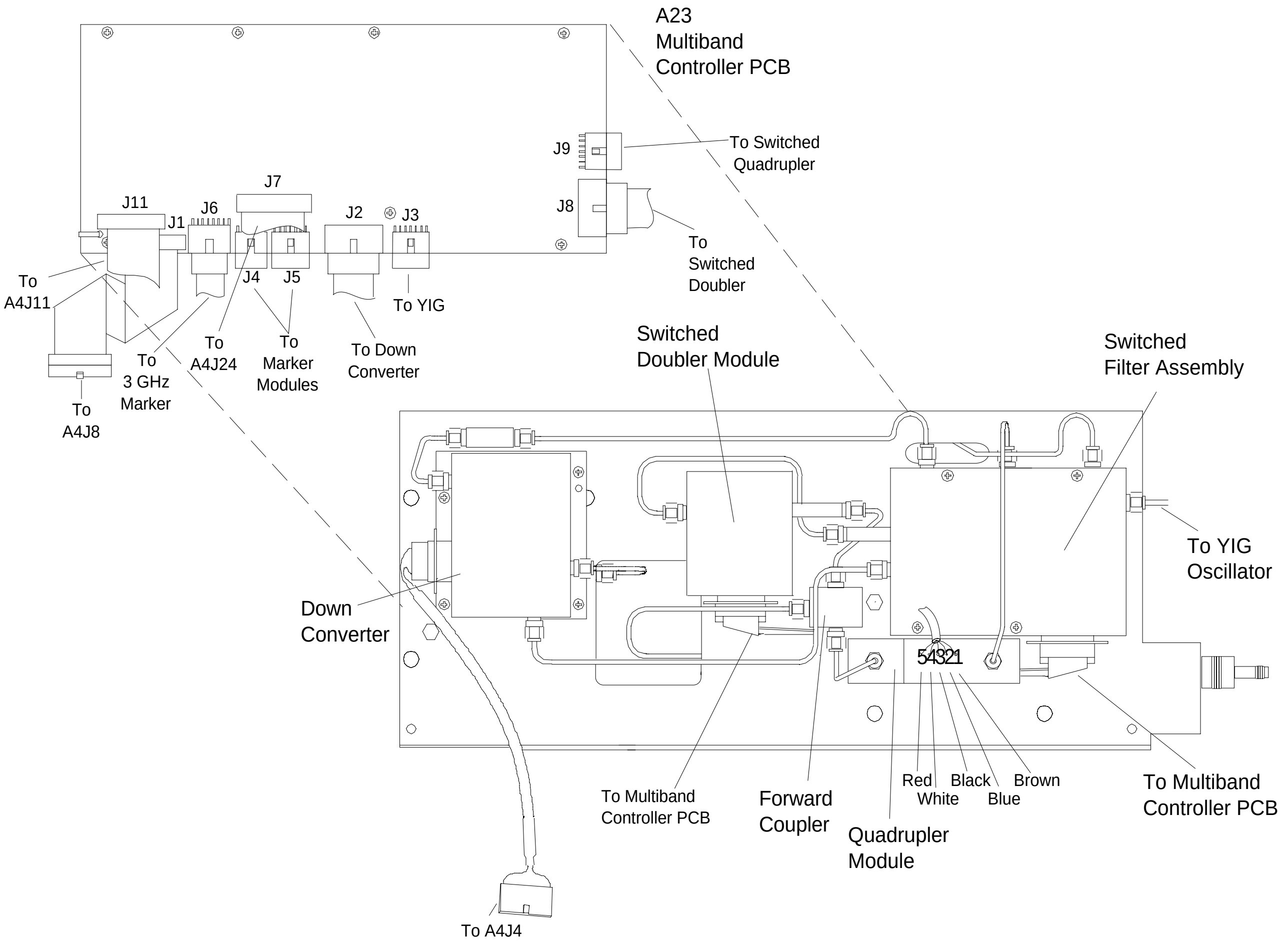


Figure 7-21. *Models 54177A RF Deck Parts Location (Internal Side Detail)*

Quadrupler Module Procedure

Step 1. Remove all RF cables connected to the assembly.

Step 2. Remove all the microwave cables from the Quadrupler.

Step 3. Remove the two screws which secure the plate the Quadrupler is mounted on.

Step 4. Remove the Quadrupler from the RF deck.

Appendix A
RF Detector Diode Replacement Procedures

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Appendix A
RF Detector Diode Replacement Procedures

A-1 RF DETECTOR DIODE REPLACEMENT PROCEDURES

Series 5400-71XXX RF Detectors and series 560-7XXX RF Detectors are used with 54XXA systems. Paragraph A-2 contains the procedure for replacing defective detector diodes in model 5400-71B75 RF Detectors, and paragraph A-2 contains the procedure for replacing detector diode modules in series 560-7XXX RF Detectors.

NOTE

Models 5400-71N50 and 5400-71N75 RF Detectors do not have field-replaceable detector diodes. Series 5400-6NXXX Autotesters also do not.

Required Adjustments

Whenever the detector diode (or diode module) of these RF Detectors is replaced, the two potentiometers that are part of the RF detector PCB subassembly (Figures A-1 and A-4) must be readjusted. The potentiometer readjustment is done after the defective diode is removed, but before the replacement diode is installed.

Test Equipment Required

The procedure in this appendix require a digital multimeter (DMM) that has a display resolution of at least 3-1/2 digits. (John Fluke Model 8840A, or equivalent).

A-2 REPLACEMENT OF DETECTOR DIODE FOR MODEL 5400-71B75 RF DETECTOR

The model 5400-71B75 RF Detector is equipped with a field-replaceable detector diode. To replace, proceed as follows:

Step 1 Unfasten the four detector housing top cover retaining screws. Remove the top cover.

Step 2 Unplug the defective diode (Figure A-1) from the PCB subassembly and remove.

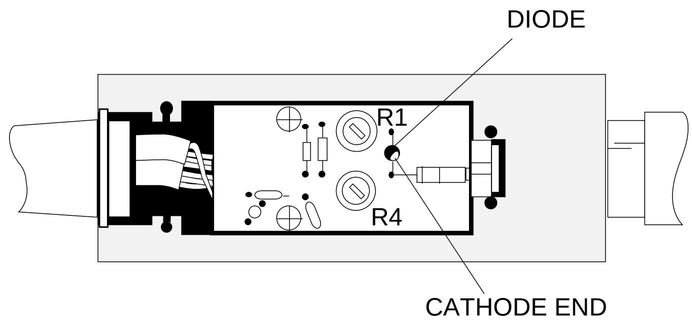

Figure A-1. *Model 5400-71B75 RF Detector Housing Layout Diagram*

Step 3 Set potentiometer R1 fully clockwise (maximum resistance).

Step 4 Connect the DMM leads between pins 1 and 2 of the rf detector cable connector (Figure A-2). Measure the resistance value, which is the maximum resistance of R1 (approximately 40.5 kΩ is typical). Record this value; it will hereafter be referred to as "R_T".

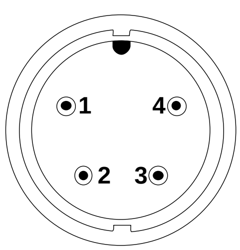

Figure A-2. *RF Detector Cable Connector Pin Orientation*

Step 5 Obtain the "K" value from the replacement diode container label (Figure A-3).

Step 6 Compute the set value for R1 as follows:

$$R1_{set} = K \times R_T$$

Step 7 Adjust R1 counterclockwise until the DMM indicates the $R1_{set}$ value calculated in step 6.

Step 8 Connect the DMM leads between pin 3 of the rf detector cable connector and the cable shield.

Step 9 Obtain the "R_0" value from the replacement diode container label.

Step 10 Adjust R4 until the DMM indicates the "R_0" value. Disconnect the DMM.

Step 11 Orient the cathode end (white dot) of the replacement diode as shown in Figure A-1 (white dot toward centerline of the detector PCB subassembly). Insert the diode into the socket of the PCB subassembly.

Step 12 Reinstall the top cover, securing it with the four retaining screws. This completes replacement of detector diode.

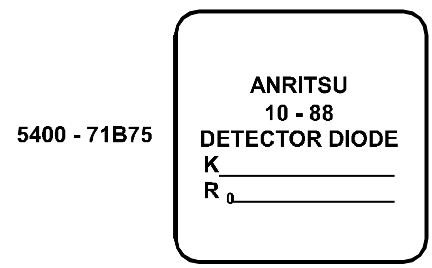

Figure A-3. *Replacement Diode Container Label*

A-3 REPLACEMENT OF DIODE MODULES FOR SERIES 560-7XXX RF DETECTORS

Series 560-7XXX RF Detectors are equipped with a field-replaceable diode module that contains (in addition to the detector diode) a thermistor, a resistor, and two capacitors. To replace, proceed as follows:

Step 1 Unfasten the four detector housing top cover retaining screws. Remove the top cover.

Step 2 Unfasten the two retaining screws that hold down the RF detector PCB subassembly (Figure A-4).

Step 3 Slide the cable retainer out of the rf detector housing assembly. When the cable retainer clears the housing, disconnect the PCB subassembly from the diode module. Remove spring washer.

Step 4 Remove fiberglass module retainer from detector housing. This retainer can be removed by prying it out using a small screwdriver, or by pulling it out using short, round nose pliers.

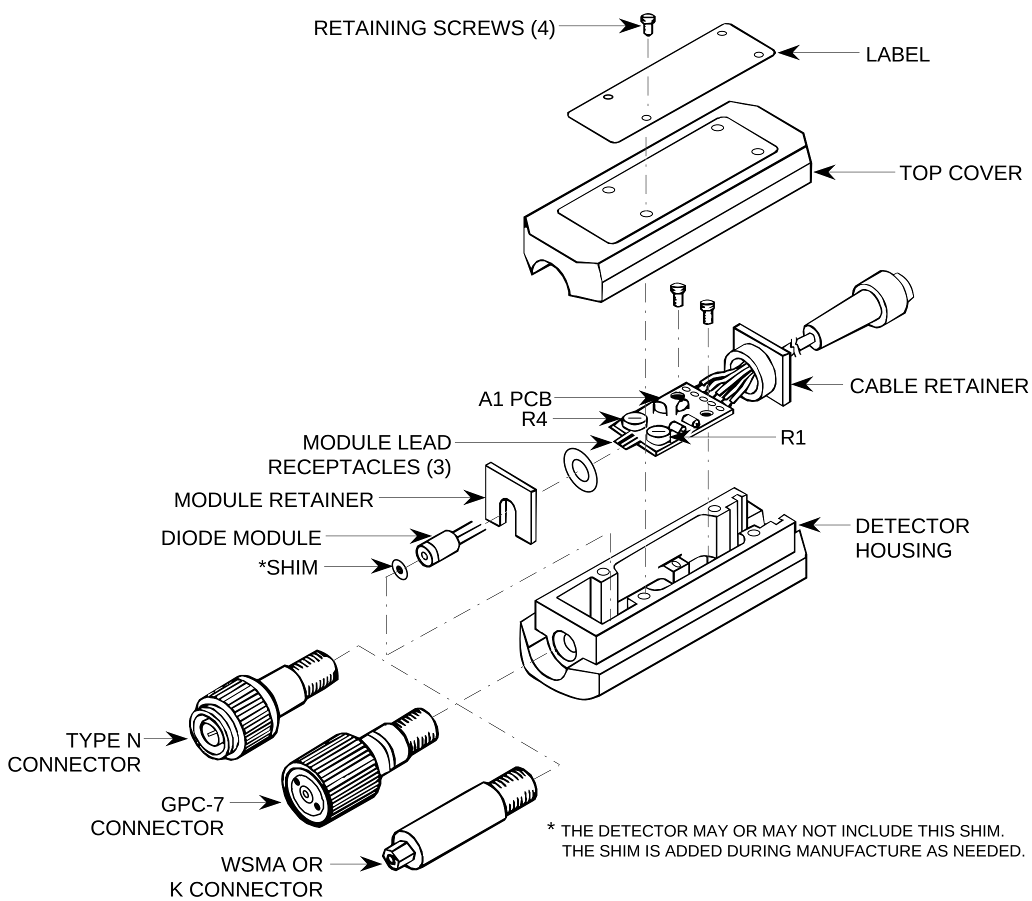

Figure A-4. *Series 560-7XXX RF Detectors, Exploded View*

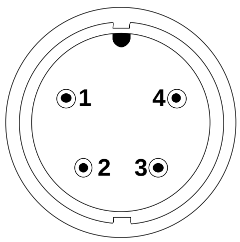

Figure A-5. RF Detector Cable Connector Pin Orientation

Step 5 Remove diode module from rear of connector body by pulling it straight out.

Step 6 Connect the DMM leads between pins 1 and 2 of the rf detector cable connector (Figure A-5). Measure the resistance value, which is the maximum resistance of R1 (approximately 40.5 kΩ is typical). Record this value; it will hereafter be referred to as "R_T".

Step 7 Obtain the "K" value from the replacement diode container label (Figure A-6).

Step 8 Compute the set value for R1 as follows:

$$R1_{set} = K \times R_T$$

Step 9 Adjust R1 counterclockwise until the DMM indicates the $R1_{set}$ value calculated in step 8.

Step 10 Connect the DMM leads between pin 3 of the rf detector cable connector and the cable shield.

Step 11 Obtain the "R_0" value from the replacement diode container label and adjust R4 until the DMM indicates this value. Disconnect the DMM.

Step 12 Orient detector housing normally (Figure A-4). Insert replacement diode module into rear of connector body so that center lead *is on top*.

Step 13 Orient spring washer so that the two curved flanges point toward the rear of the detector housing and are positioned horizontally (i.e., 3 o'clock and 9 o'clock positions).

Step 14 Insert fiberglass module retainer between the replacement diode module and spring washer. Push down on retainer until fully seated.

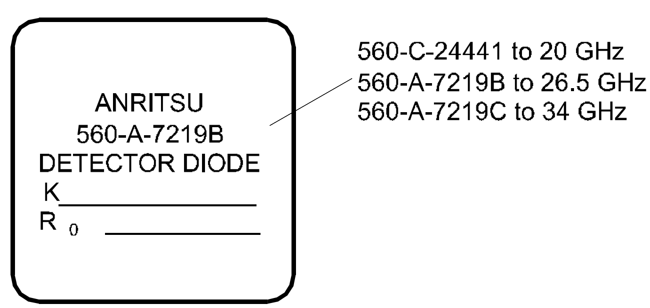

Figure A-6. Replacement Diode Module Container Label

Step 15 Orient PCB subassembly normally as shown in Figure A-4 and insert into detector housing so that leads from replacement diode module mate with connectors on PCB subassembly.

Step 16 Insert cable retainer into slot in detector housing.

Step 17 Fasten PCB subassembly into detector housing using two retaining screws.

Step 18 Reinstall the top cover, securing it with the four retaining screws. This completes replacement of detector diode module.

Appendix B Fabrication of RF Detector Simulator

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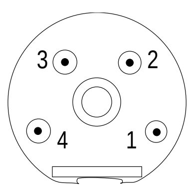
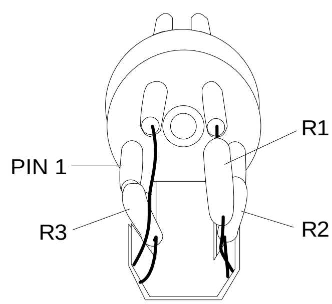
Appendix B
Fabrication of RF Detector Simulator

B-1 RF DETECTOR SIMULATOR

The RF detector simulator (T1492) is a special test aid that is used in the adjustments procedure for the series 541XXA Network Analyzers (refer to Chapter 6, paragraph 6-2). The T1492 may be fabricated as illustrated in Figure B-1, below. Or, it may be purchased from ANRITSU as a special order item. Contact your ANRITSU sales office for further details.



FRONT VIEW



REAR VIEW

Reference Designator	Description	ANRITSU Part Number
R1, R2	Resistor, Metal Film, 1 MΩ, 0.1%	110-1M-0.1
R3	Resistor, Metal Film, 5.11 kΩ, 1%	110-5.11K-1
–	Connector Plug, Switchcraft, inc., 09CL4M	551-271

To fabricate the detector simulator, refer to figures above and proceed as follows:

1. Remove screw that secures connector shell to connector assembly.
2. Remove connector assembly from connector shell and note pin numbers located on front of connector.
3. Solder one end of resistor R1 to pin 3.
4. Solder other end of resistor R1 to the shield post.
5. Solder one end of resistor R2 to pin 4.

Figure B-1. *Fabrication of T1492 Detector Simulator (1 of 2)*

6. Solder other end of resistor R2 to the shield post.
7. Solder one end of resistor R3 to pin 1.
8. Solder other end of resistor R3 to the shield post. Return wire from shield post back to pin 2 and solder.
9. Insert connector assembly into connector shell and refasten screw.

Figure B-1. *Fabrication of T1492 Detector Simulator (2 of 2)*

Appendix C
Fabrication of Dummy Thermistor Test Aids

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Appendix C
Fabrication of Dummy Thermistor Test Aids

C-1 T38300 DUMMY THERMISTOR TEST AID

The T38300 Dummy Down Converter Thermistor is a special test aid that is used in the Temperature Compensation Adjustment Procedure (Chapter 6, paragraph 6-10). This test aid may be fabricated as shown below; or, it may be purchased from ANRITSU as a special order item. Contact your ANRITSU sales office for further details.

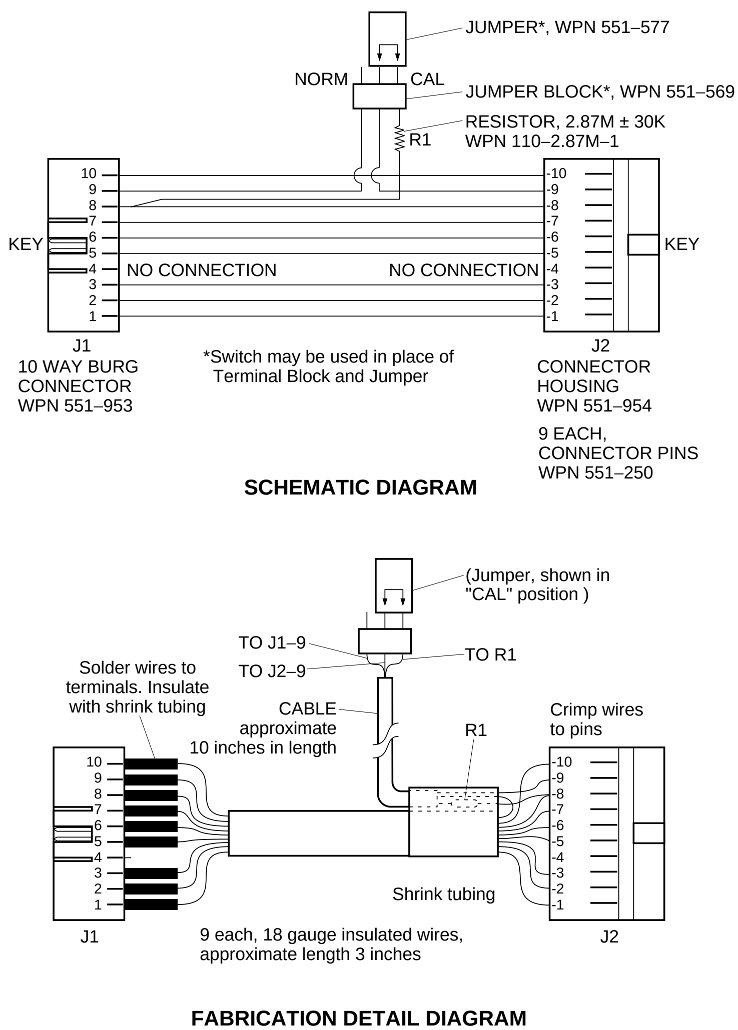

Figure C-1. *Fabrication of T38300 Dummy Down Converter Thermistor*

C-2 T38301 DUMMY THERMISTOR TEST AID

The T38301 Dummy Directional Coupler Thermistor is a special test aid that is used in the Temperature Compensation Adjustment Procedure for series 541XXA Network Analyzers (Chapter 6, paragraph 6-10). This test aid may be fabricated as shown below; or, it may be purchased from ANRITSU as a special order item. Contact your ANRITSU sales office for further details.

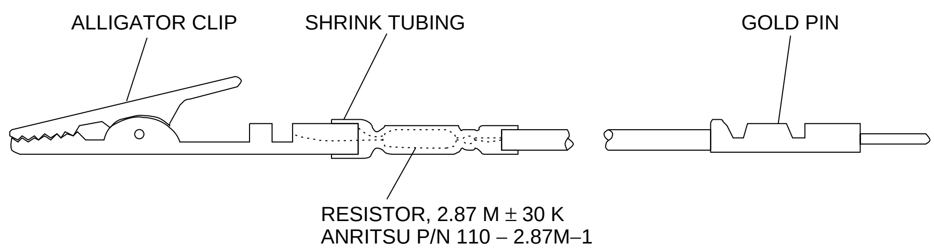

Figure C-2. *Fabrication of T38301 Dummy Directional Coupler Thermistor*

Appendix D
Performance Specifications

This appendix contains the 54100A Series Network Analyzer Technical Data Sheet. This data sheet provides performance specifications and other technical data that will aid you in performing maintenance on the 541XXA.

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