Product Introduction

Verifying Effectiveness of Proprietary and Standard FEC in 40G/43G Networks

MP1595A
40G SDH/SONET Analyzer
Verifying Effectiveness of Proprietary and Standard FEC in 40G/43G Networks

MP1595A Proprietary Random Error Insertion Technique Provides Unique Standards-Based Solution For All FEC Performance Testing
Unique Verification of 40G/43G FEC Efficiency

Background

- 40G/43G networks require sophisticated Forward Error Correction (FEC) to achieve acceptable performance
  - ITU-T G.709 specifies the standard FEC process
  - Many equipment vendors are also developing proprietary enhanced FEC methods

- ITU-T O.182 defines required test methods for verifying FEC performance
  - Based on generating an error pattern having a Poisson distribution of randomness
  - Must be applied to both standard and proprietary FEC solutions
Implementing Unique FEC Verification

- **Step 1**
  - Network equipment with vendor-unique FEC encoding transmits OTU-3 (43 Gbps) OTN frames to MP1595A

- **Step 2**
  - MP1595A loops back the OTU-3 data frames using Transparent Through Mode
  - Anritsu proprietary technique inserts random frame errors in the vendor-unique FEC transmissions
Implementing Unique FEC Verification

- **Step 3**
  - Network equipment with unique FEC monitors frame errors received on its DUT Rx input

- **Basis of Anritsu’s ideal FEC performance testing**
  - Ability to insert OTU-3 frame errors using Transparent Through Mode
  - Proprietary FEC error generation technique
    - Operates with network equipment standard or unique FEC
    - Randomness complies with ITU-T O.182 requirements
Importance of Random Error Insertion

- ITU-T O.182 requires random error insertion based on a Poisson distribution
- Improper error generation results in tests that do not correctly model actual 40G/43G network behavior
- Anritsu MP1595A uses patented process to generate errors correctly matching Poisson distribution of randomness
  - The industry’s only solution for correct and accurate 40G/43G FEC performance verification
Measured vs. Theoretical Bit Error Rates

- Using correctly randomized error insertion is the only way to properly evaluate an FEC decoder under test.
Next Steps

- Download the ITU-T O.182 FEC testing standard:
  - www.itu.int/rec/T-REC-O.182/en
- Review the Anritsu white papers about FEC testing and the ITU-T standards:
  - “FEC Efficiency New Test Method”
  - “Technologies for Verifying Poisson Error Generator Performance”
- Get MP1595A 40G SDH/SONET Analyzer literature:
  - Data sheet
  - Product introduction
- See an MP1595A demonstration so you can evaluate its performance and ease of use
Unique Verification of 40G/43G FEC Efficiency

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